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Brief 70-10370

NASA TECH BRIEF

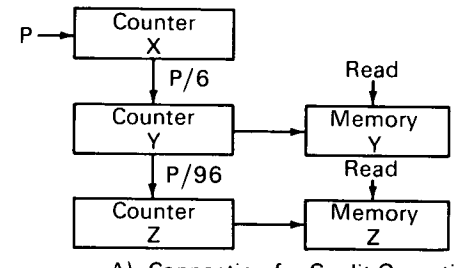
Pulse-Rate Averaging Circuit

A pulse-rate averaging circuit has been designed to provide a secondary control signal during inoperative periods of an intermittent primary control system. The circuit was originally developed for use in a solar-array orientation control system, to enable the array to continue accurate tracking during dark periods, when the solar reference was hidden. It may also be applied wherever it is desired to obtain an average pulse rate over a fixed time interval, such as in a digital frequency meter. With an analog-to-digital converter, the averaging circuit may be used to determine the average value of an analog signal. It may also be programmed to provide pulse frequency division by any integer within its design range, and hence may be used as a variable-rate pulse generator capable of very low pulse rates.

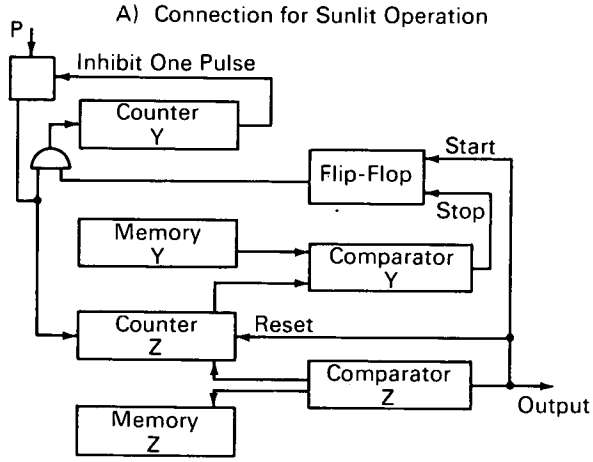
The averaging circuit operates in two modes, one during sunlight, the other during darkness. The illustration shows a block diagram of the circuit in each mode.

In sunlight (see Figure 1A), the circuit is configured as a serial array of three counters (X, Y, and Z), the most significant two of which (Y and Z) are connected in parallel to two memory units. Input pulses (P) from the primary control system are counted, and periodically the contents of counters Y and Z are accumulated in memory. The division ratios of the three counters are set so that the most significant count (in Z) represents an integral number of command pulses to the array orientation control, and the second most significant count (in Y) represents a fractional part of a command, to the nearest 1/16.

In darkness, the averaging circuit is logically reconfigured into the output mode shown in Figure 1B. The two most significant counters and their associated



A) Connection for Sunlit Operation



B) Connection for Dark Period Operation

Block Diagrams of Pulse-Rate Averaging Circuit

memories are connected to two comparator circuits. The counters are initially set to zero and input pulses are transmitted simultaneously to both counters. Increments to counter Y are stopped when comparator Y senses equality between the contents of counter Z and memory Y. Increments to counter Z continue until its contents equal those of memory Z, at which point comparator Z produces an output command pulse, resets counter Z to zero, and restarts counter Y.

(continued overleaf)

Counting continues in this manner until counter Y reaches its full count (15) and resets to zero. The reset pulse is used to inhibit the next input pulse, causing the increase of counter Z, and hence the next output command pulse, to be delayed by one count. Thus, over one full cycle of operation the number of input pulses per command pulse is fixed at the average integer-and-fraction value stored in memories Y and Z. At the resumption of sunlight operation, the circuit is reconfigured into its input mode, the counters and memories are reset to zero, and another average is accumulated.

Note:

No additional documentation is available. Specific questions, however, may be directed to:

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No patent action is contemplated by NASA.

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