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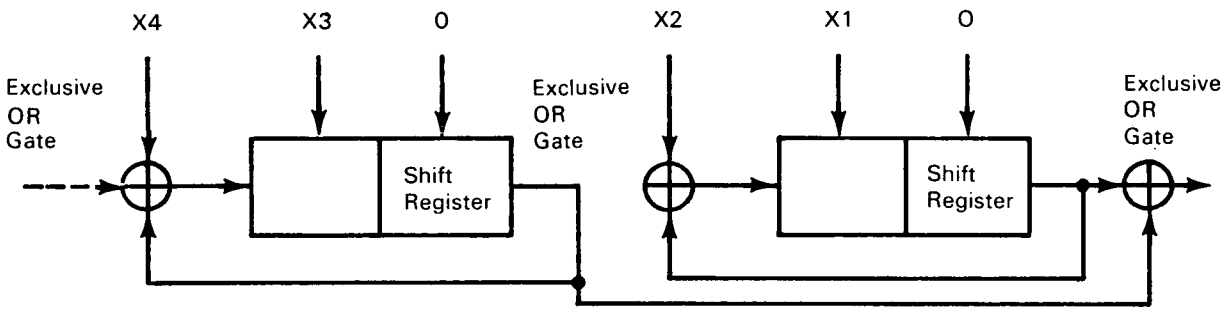
NASA TECH BRIEF

Block Encoders for Reed-Muller Codes



Block Diagram Logic Circuit
for Reed-Muller Code Scheme.

The problem:

To increase error-free reception by a high-rate telemetry channel under extremely adverse signal-noise with minimal use of additional hardware. The format of the transmitted data is a block-encoded, 6-bit orthogonal code-word.

The solution:

Encoding algorithms were developed for generating a 32 × 64-bit matrix Reed-Muller code from the 6-bit orthogonal code; the larger matrix increases the probability of error-free reception. Variations of logic circuits were designed to implement the block encoding schemes.

How it's done:

The Reed-Muller code is constructed as follows:

$$A = \begin{bmatrix} +1 & +1 \\ +1 & 1 \end{bmatrix}; \quad B = \begin{bmatrix} A & A \\ A & \bar{A} \end{bmatrix}; \quad N = \begin{bmatrix} (N\text{-}1) & (N\text{-}1) \\ (N\text{-}1) & \overline{(N\text{-}1)} \end{bmatrix}$$

An orthogonal matrix of a simple two-variable code dictionary is formed by adding the complement of the code in the lower right, i. e.,

1	1	1	1
1	-1	1	-1
1	1	-1	-1
1	-1	-1	1

Two-variable

From the Reed-Muller code structure it may be deduced that each code symbol is a mod-2 function between a certain set of the original information bits; the selection of these sets of the original information bits is a simple mapping between the original information bits and the binary sequence. In the application, the mod-2 function is equivalent to a parity function which indicates whether the number of "ones" in a vector (i.e., in a row or column of the matrix) is odd or even.

The criteria for the design of a logic circuit which implements the code scheme, shown in the figure, are based on the mod-2 algebraic expressions:

(continued overleaf)

$X \oplus 0 = X$

$X \oplus X = 0$

$X \oplus X \oplus X = X$

$X \oplus X \oplus X \oplus X = 0$, etc.

Odd number of X equals X, even number X equals 0. If a set of variables in the shift register is continually shifted around and entered through the mod-2 function between the output register and another variable (every other cycle), and each variable in the register will be mod-2 added with the entry variable and every other time not. A mod-2 mapping between the entry variables and the binary sequence is obtained by several modules connected together by two-term mod-2 functions. For a large number of variables, identical modules can be added as required and each new module is clocked once every other cycle of the preceding one.

Note:

Requests for further information may be directed to:

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Patent status:

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