September 1970

#### Brief 70-10051

# NASA TECH BRIEF



NASA Tech Briefs announce new technology derived from the U.S. space program. They are issued to encourage commercial application. Tech Briefs are available on a subscription basis from the Clearinghouse for Federal Scientific and Technical Information, Springfield, Virginia 22151. Requests for individual copies or questions relating to the Tech Brief program may be directed to the Technology Utilization Division, NASA, Code UT, Washington, D.C. 20546.

## **Block Encoders for Reed-Muller Codes**



Block Diagram Logic Circuit for Reed-Muller Code Scheme.

#### The problem:

To increase error-free reception by a high-rate telemetry channel under extremely adverse signalnoise with minimal use of additional hardware. The format of the transmitted data is a block-encoded, 6-bit orthogonal code-word.

#### The solution:

Encoding algorithms were developed for generating a  $32 \times 64$ -bit matrix Reed-Muller code from the 6-bit orthogonal code; the larger matrix increases the probability of error-free reception. Variations of logic circuits were designed to implement the block encoding schemes.

#### How it's done:

The Reed-Muller code is constructed as follows:



An orthogonal matrix of a simple two-variable code

dictionary is formed by adding the complement of the code in the lower right, i. e.,



From the Reed-Muller code structure it may be deduced that each code symbol is a mod-2 function between a certain set of the original information bits; the selection of these sets of the original information bits and the binary sequence. In the application, the mod-2 function is equivalent to a parity function which indicates whether the number of "ones" in a vector (i.e., in a row or column of the matrix) is odd or even.

The criteria for the design of a logic circuit which implements the code scheme, shown in the figure, are based on the mod-2 algebraic expressions:

(continued overleaf)

This document was prepared under the sponsorship of the National Aeronautics and Space Administration. Neither the United States Government nor any person acting on behalf of the United States Government assumes any liability resulting from the use of the information contained in this document, or warrants that such use will be free from privately owned rights.  $\begin{array}{rcl} X \oplus 0 &= X \\ X \oplus X &= 0 \\ X \oplus X \oplus X \oplus X &= X \\ X \oplus X \oplus X \oplus X \oplus X &= 0, \ \text{etc.} \end{array}$ 

Odd number of X equals X, even number X equals 0. If a set of variables in the shift register is continually shifted around and entered through the mod-2 function between the output register and another variable (every other cycle), and each variable in the register will be mod-2 added with the entry variable and every other time not. A mod-2 mapping between the entry variables and the binary sequence is obtained by several modules connected together by two-term mod-2 functions. For a`large number of variables, identical modules can be added as required and each new module is clocked once every other cycle of the preceding one.

### Note:

Requests for further information may be directed to:

Technology Utilization Officer NASA Pasadena Office 4800 Oak Grove Drive Pasadena, California 91103 Reference: B70-10051

## Patent status:

This invention is owned by NASA, and a patent application has been filed. Royalty-free, nonexclusive licenses for its commercial use will be granted by NASA. Inquiries concerning license rights should be made to NASA, Code GP, Washington, D.C. 20546.

Source: Tage O. Anderson of Caltech/JPL under contract to NASA Pasadena Office (NPO-10629 and NPO-10636)