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Buck-Boost DC Voltage Regulator

A circuit has been developed to provide buck-boost voltage regulation through a wide range of operating frequencies without the intervals of high power dissipation which occur in similar circuits using

bases of Q_1 and Q_2 and the slave outputs to the bases of Q_3 and Q_4 . The regulator operates in a phase-retarded mode, and gives maximum boost to the output voltage with minimum phase shift in

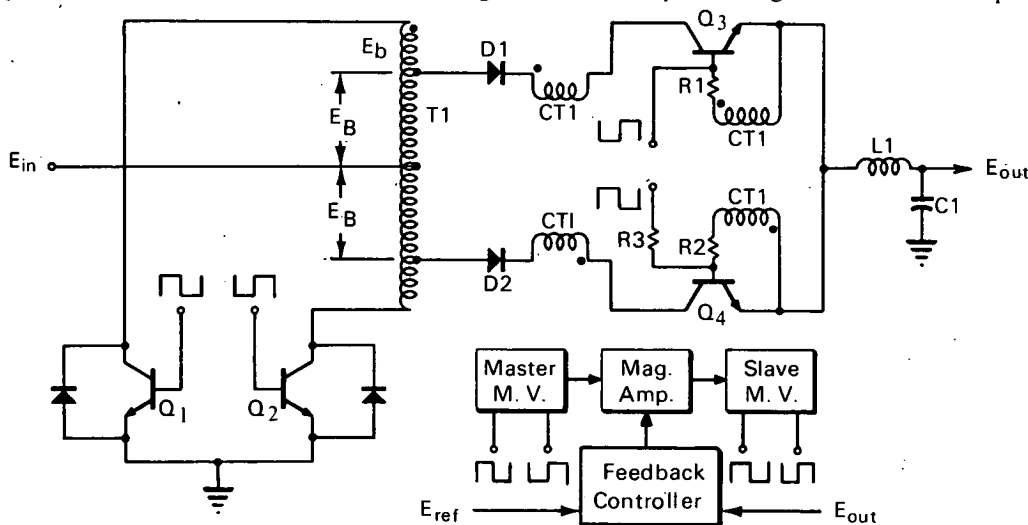


Figure 1. Buck-Boost Voltage Regulator

silicon controlled rectifiers. This improved regulator should be of interest throughout the electronics industry.

As illustrated in Figure 1, the regulator is composed of the following functional circuit elements: a master multivibrator (M.V.), a magnetic amplifier, a slave M.V., a feedback controller, an inverter, a chopper, and an output filter. One output from the master M.V. is coupled through the variable-phase delay magnetic amplifier to drive the slave M.V. Twin, phase-inverted square wave outputs are taken from the master, and similar outputs, delayed by a phase shift β , are taken from the slave. The master outputs are normally connected to the

the magnetic amplifier. The regulator is described assuming this mode of operation. However, with equal facility, the connections of master and slave may be reversed, to operate the regulator in a phase-advanced mode and give maximum boost with maximum phase shift.

The feedback controller compares a divided portion of the output voltage E_{out} with a zener reference voltage E_{ref} , to produce an error signal, which is amplified and used to control the phase shift of the magnetic amplifier.

The principle of operation of the regulator involves combining a dc voltage source to be regulated with an ac voltage source in a chopper circuit.

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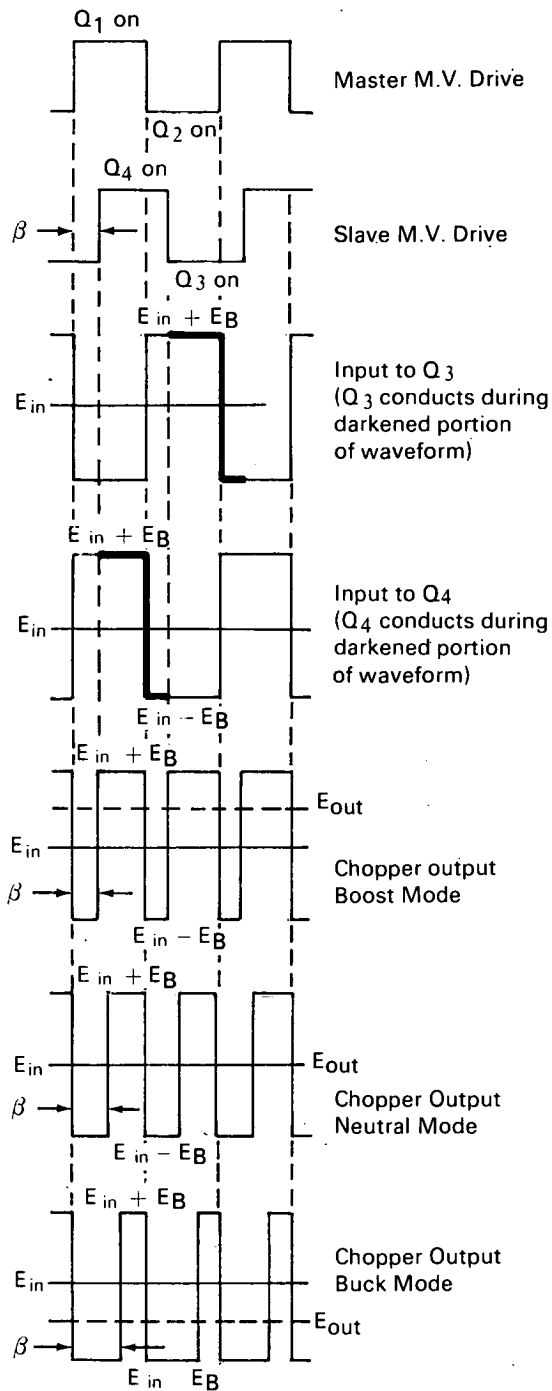


Figure 2. Ideal Waveforms

Operation of the chopper circuit is adjustably phase displaced from that of the inverter to permit an additive or subtractive component of voltage to be impressed upon the dc input voltage as required for output voltage regulation.

The inverter switching is controlled by the outputs of the master M.V. Conduction of either of the

inverter transistors Q_1 or Q_2 allows the dc input, E_{in} , to appear across the primary windings of autotransformer T1. This input voltage is coupled to the transformer secondary and provides an ac voltage, E_B , which is combined with the input and then applied to the chopper circuit. The switching of the chopper circuit transistors, Q_3 and Q_4 , is controlled by outputs from the slave M.V., and hence are phase delayed from the switching of the inverter transistors. This phase displacement, β , is variable and results in the required switching of the power chopper transistors between conducting and nonconducting states to cause the impressed voltage from the inverter to be either additive or subtractive. By varying the relative time duration of the buck (subtractive) interval to the boost (additive) interval, the output level can be regulated.

The subtractive mode of operation is achieved by maintaining one of the power chopper transistors Q_3 and Q_4 in conduction (by means of an inductive load L1 and current transformer CT1) during the time when the subtractive half cycle of the impressed ac voltage is present at the active secondary winding of the autotransformer.

The output from the chopper circuit is applied to an averaging filter L1-C1, which smooths the pulsating dc to the desired output level. The resultant dc output, E_{out} , can thus be controlled at a value less than, equal to, or greater than E_{in} . Figure 2 is a graphic representation of the ideal waveforms of the circuit operating in either buck, boost, or neutral modes.

Note:

Requests for further information may be directed to:

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Patent status:

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