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March 4, 1969 JAMES E. WEBB 3,431,559
ADMINISTRATOR OF THE NATIONAL AERONAUTICS
AND SPACE ADMINISTRATION
TELEMETRY WORD FORMING UNIT
Filed May 17, 1967 Sheet 1 of 5

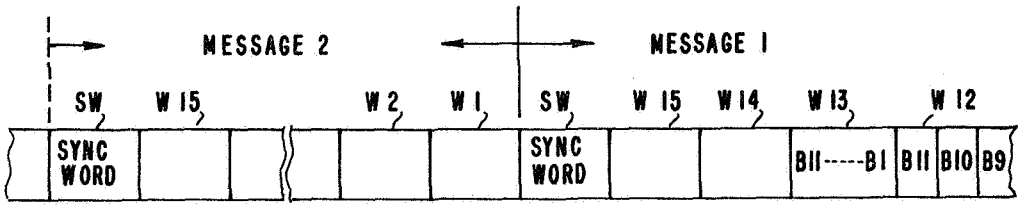
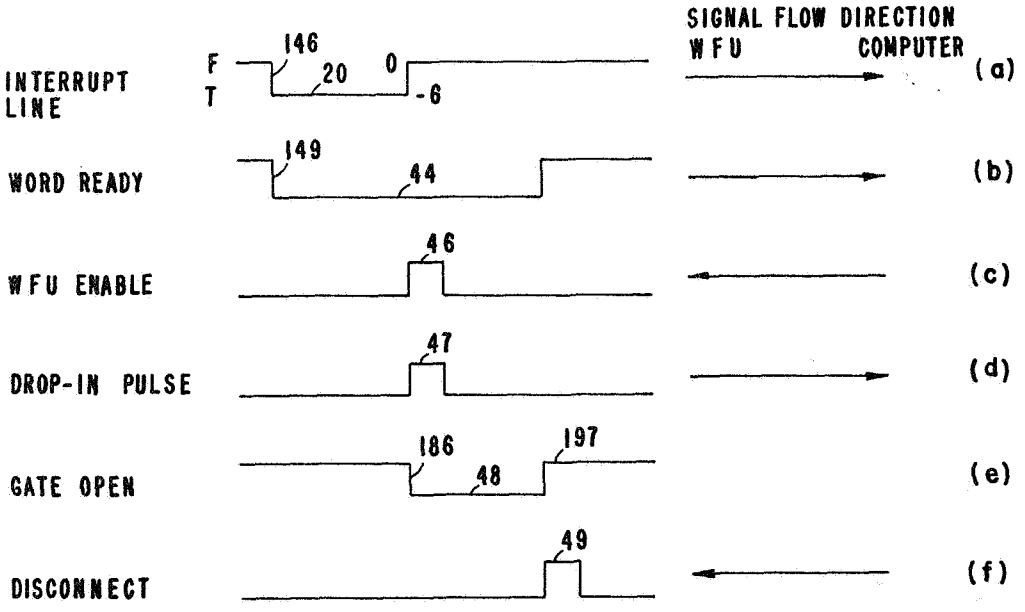


FIG. 1

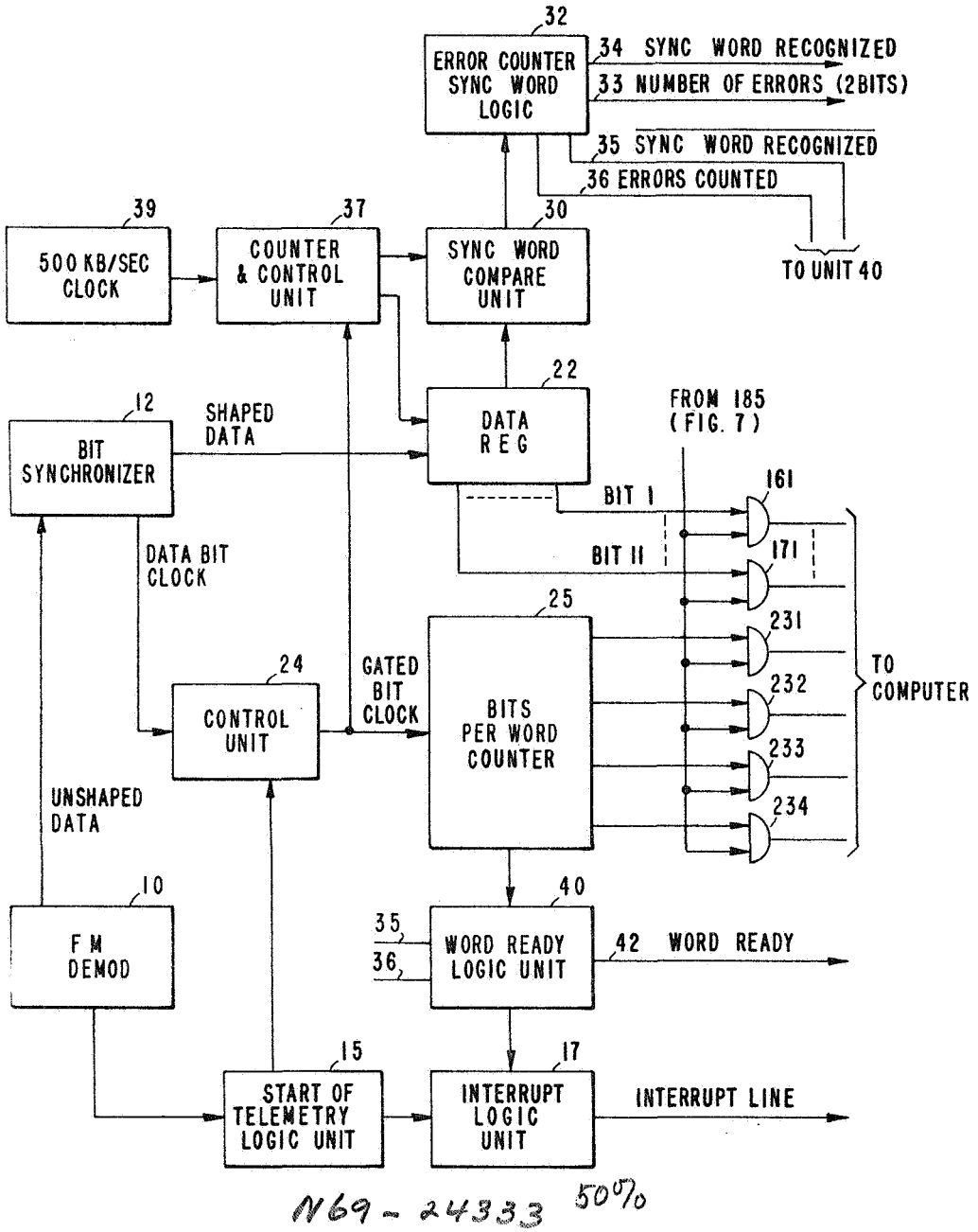
FIG. 3



INVENTOR
HOYT HOLMES NELSON
BY D E Leslie
Fish & Cox
ATTORNEYS

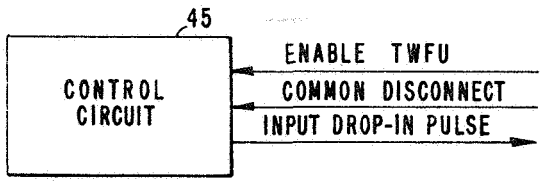
N69-24333

March 4, 1969 JAMES E. WEBB 3,431,559
ADMINISTRATOR OF THE NATIONAL AERONAUTICS
AND SPACE ADMINISTRATION
TELEMETRY WORD FORMING UNIT
Filed May 17, 1967 Sheet 2 of 5



N69-24333 50%

FIG. 2



INVENTOR
HOYT HOLMES NELSON
BY D E Leslie
Adams & Cox
ATTORNEYS

54

March 4, 1969 JAMES E. WEBB 3,431,559
ADMINISTRATOR OF THE NATIONAL AERONAUTICS
AND SPACE ADMINISTRATION
TELEMETRY WORD FORMING UNIT
Filed May 17, 1967 Sheet 3 of 5

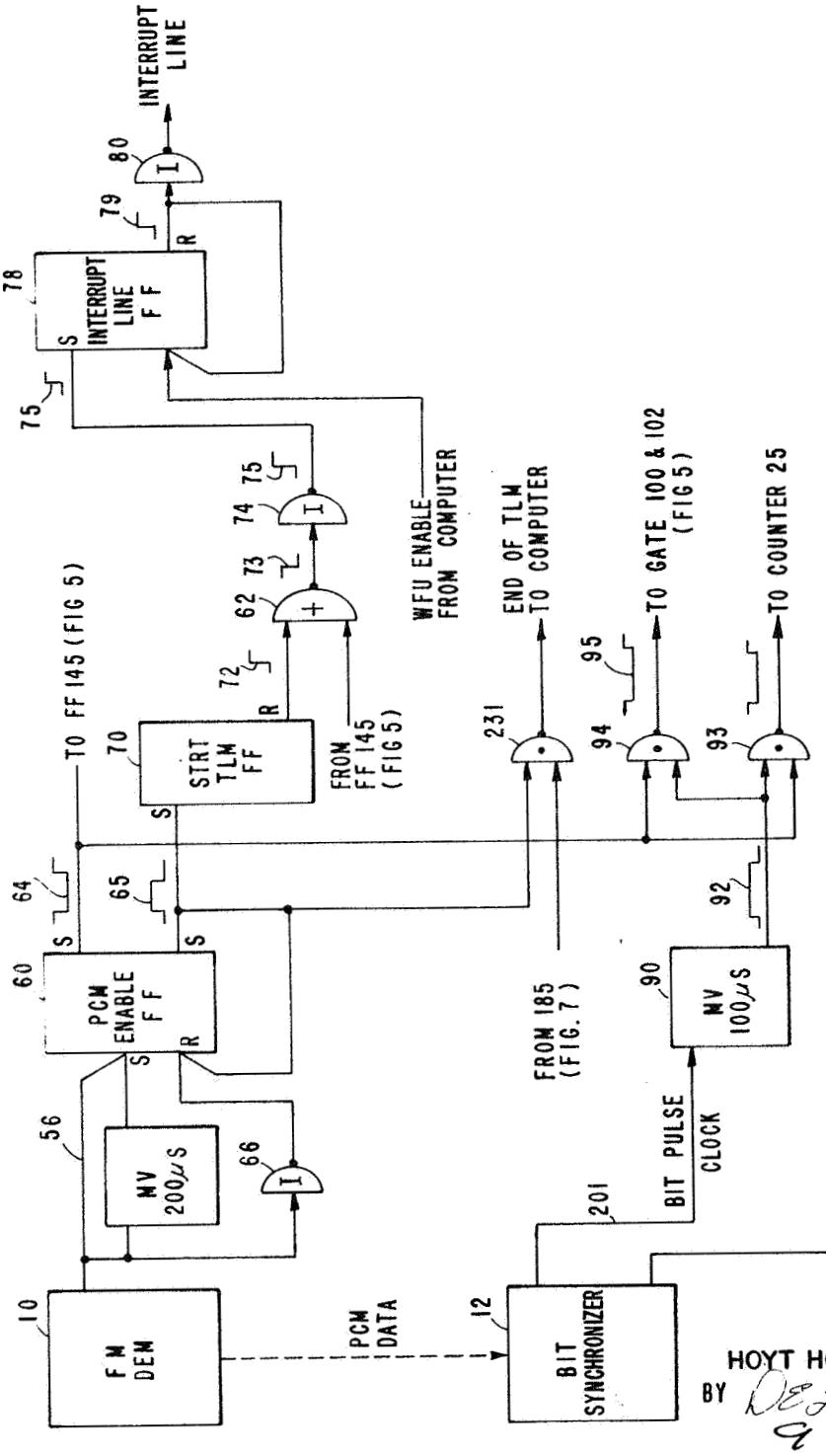


FIG. 4

INVENTOR
HOYT HOLMES NELSON
BY D. E. Leslie
Fowler & McCoy
ATTORNEYS

March 4, 1969 JAMES E. WEBB 3,431,559
ADMINISTRATOR OF THE NATIONAL AERONAUTICS
AND SPACE ADMINISTRATION
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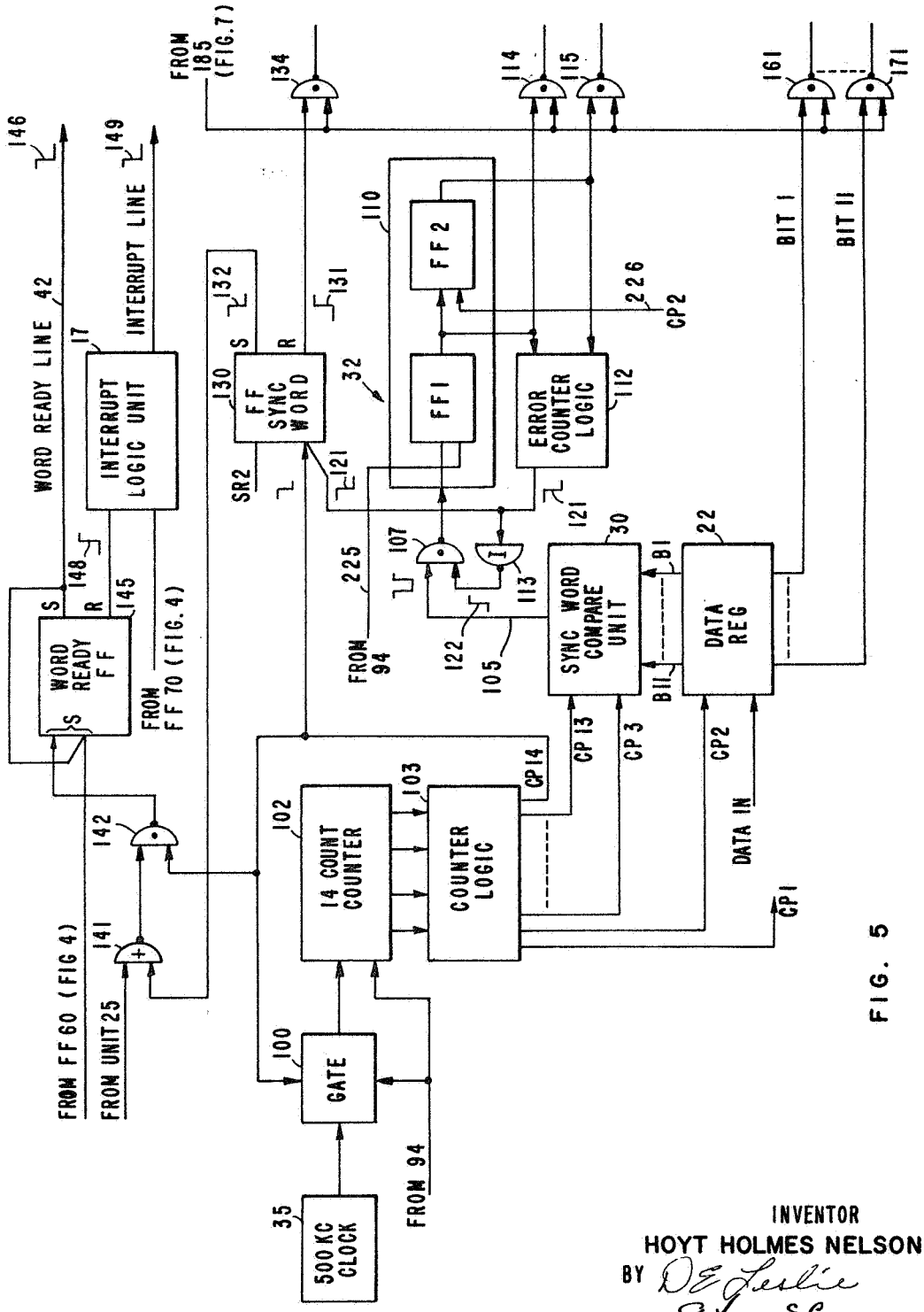

FIG. 5

INVENTOR
HOYT HOLMES NELSON
BY D E Leslie
Fraser & Co
ATTORNEYS

March 4, 1969 JAMES E. WEBB 3,431,559
ADMINISTRATOR OF THE NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
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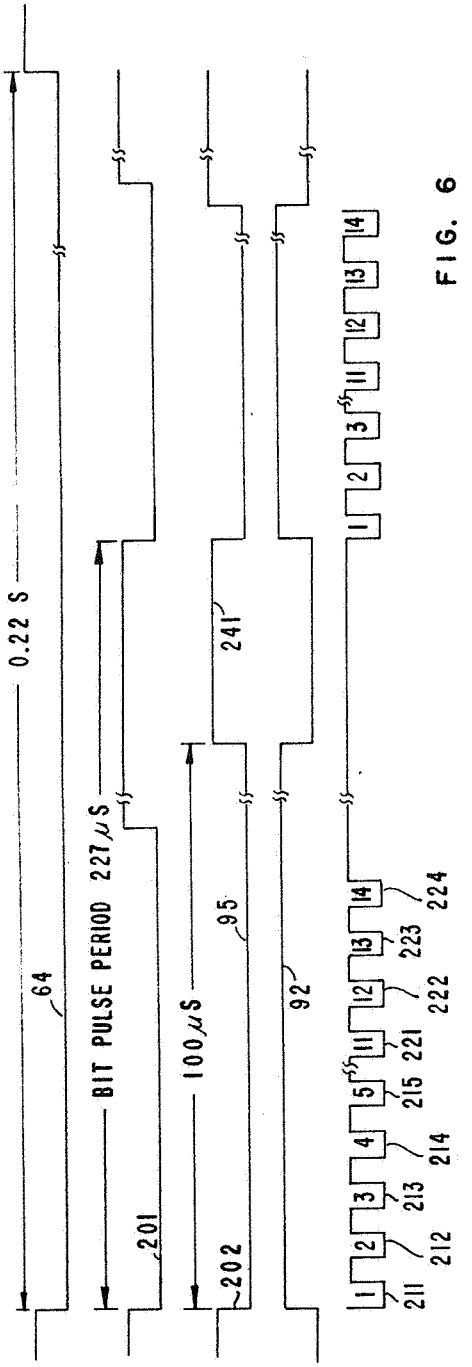

FIG. 6

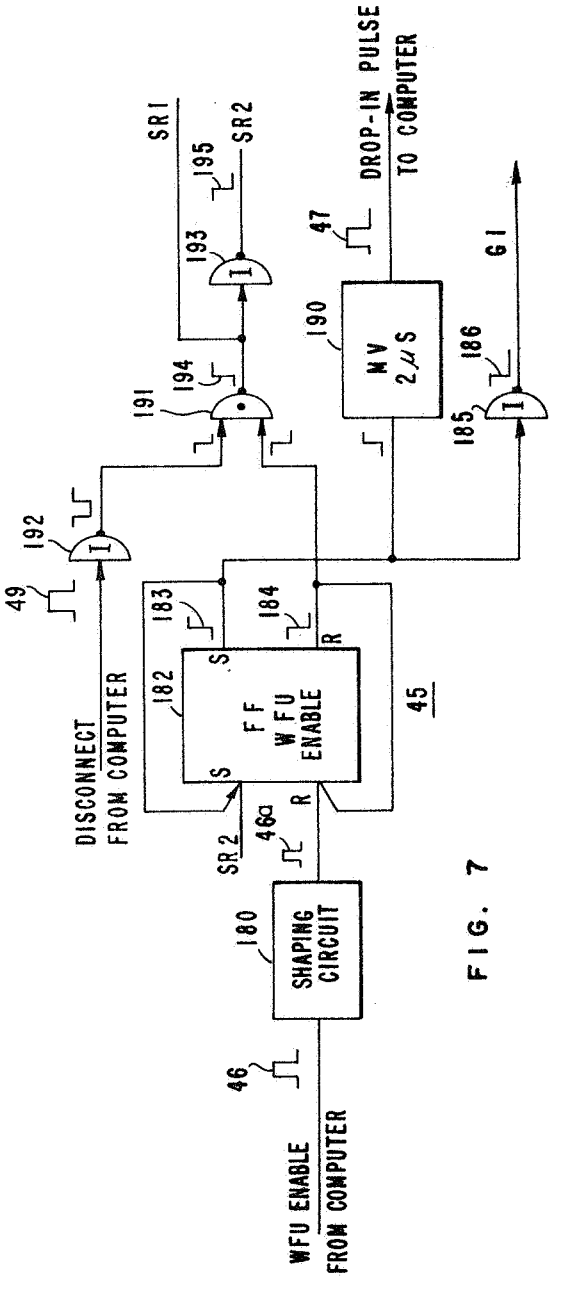

FIG. 7

INVENTOR
HOYT HOLMES NELSON
BY
ATTORNEYS

United States Patent Office 3,431,559 Patented Mar. 4, 1969

3,431,559

TELEMETRY WORD FORMING UNIT

James E. Webb, Administrator of the National Aeronautics and Space Administration, with respect to an invention by Hoyt Holmes Nelson, Palo Alto, Calif.

Filed May 17, 1967, Ser. No. 640,785
U.S. Cl. 340—172.5 10 Claims
Int. Cl. G11b 13/00

The invention described herein was made in the performance of work under a NASA contract and is subject to the provisions of Section 305 of the National Aeronautics and Space Act of 1958, Public Law 85–568 (72 Stat. 435; 42 USC 2457).

BACKGROUND OF THE INVENTION

Field of the invention

This invention generally relates to telemetry decoding circuitry, and, more particularly, to a unit for forming words of telemetry information to be supplied to a computer.

Description of the prior art

In telemetry applications, as well as in other data communication systems, communicated messages consist of a plurality of words, each comprising a plurality of binary signals or bits. Generally, and in telemetry applications in particular, each message includes a frame synchronization word, hereafter referred to as a SYNC word which consists of a known sequence of bits or code. The purpose of the SYNC word with the known code is to form a reference for the receiving system, and therefrom relate which of the previously received bits form discrete words of the transmitted message. Generally, in telemetry applications, the received data is first supplied to a frequency modulation (FM) demodulator, wherein the beginning of the meaningful data is detected. Also, the demodulator generally supplies to a data recovery bit synchronizer, the bits which are demodulated from the carrier frequency which are then shaped and used to generate a bit rate clock signal output along with the re-shaped bits.

The received data is generally transferred to a general purpose computer wherein the data is processed in accordance with programs determined by the user. Since general purpose computers are capable of operating at speeds much higher than the rate at which bits may be received, thereto, it is generally desirable to include a decoding and buffer network between the computer and the FM demodulator and bit synchronizer which receives the data. The function of such a unit is generally to organize the received data in conjunction with a detected SYNC word into discrete words and prepare them for transfer to the computer, rather than perform all of these operations in the computer itself. Also, since a general purpose computer is capable of performing many functions while data is being received, it is generally desirable to be able to communicate with the computer and inform the latter only when data is ready to be transferred thereto, so that during the remainder of the time, the computer may communicate with other devices and/or process other programs. The unit then acts as a data time compressor and buffer as well as a data interpreter. It is towards such a unit that the present invention is directed.

Some of the problems encountered in prior art decoding type units are difficulties in sensing or detecting the SYNC word under adverse signal-to-noise (S/N) conditions, or due to irregular clock pulses supplied to the unit when the system is forced to re-synchronize every few seconds when a new telemetry burst is received. Many times, this problem is not dealt with effectively when telemetry data is transmitted continuously rather than in short bursts since the sensing of every SYNC word is not so important.

OBJECTS AND SUMMARY OF THE INVENTION

Accordingly, it is a primary object of the present invention to provide a new improved word forming unit for receiving telemetry data sent in short bursts and forming it for use by a computer with which the unit is associated.

Another object of the present invention is to provide and improve a word forming unit in which the criteria for detecting a SYNC word are adjustable to compensate for varying signal-to-noise conditions.

And a further object of the present invention is to provide an improved word forming unit which is protected from irregularly supplied clock pulses, so as to prevent the units and the computer associated therewith from misinterpreting data supplied thereto, and filling available storage space in the computer with useless information.

A further object of the present invention is to provide a word forming unit in which data is protected even under computer temporary hang-up causing a delay in the transfer of the data to the computer.

Still a further object of the present invention is to provide a new word forming unit utilizing standard commercial logic modules, capable of forming words from telemetry data received thereby, and transferring it to a computer, which is capable of operating in simultaneous conjunction with the unit of the present invention, as well as, with other peripheral equipment associated therewith.

These and other objects of the invention are achieved by providing a unit capable of receiving a signal, indicating the beginning of a time interval during which data received in an FM demodulator is to be transferred to the unit through a bit synchronizer. The unit includes a plurality of subunits, each performing a different function. The function of one subunit is to provide an indication to the computer upon the start of the telemetry interval during which data is supplied to a data register of the unit from the bit synchronizer. A bits-per-word counter is utilized to indicate at all times the number of bits transferred to the data register since the last data transfer. The bits-per-word counter is reset each time, after reaching a count equal to the number of bits per word which are soon to be transmitted.

In addition, comparing circuitry is employed in the unit to sense, each time a new bit is transferred to the data register, whether the content of the data register represents a preselectable SYNC word which is used to properly divide a previously received stream of bits into appropriate separate words. The comparing circuit is associated with an error counting logic network, the function of which is to indicate to the computer whether a frame SYNC word has been recognized or whether an

error threshold level has been reached, indicating that the bits in the data register differ from the expected code of the frame SYNC by a selected adjustable given number of bits.

Signals are also supplied through the unit to indicate to the computer when the unit stores sufficient information which is meaningful to the computer. Thereafter, when the computer is ready (but before the next data bit is received) it addresses the unit, enabling a plurality of gates through which the content of the data register, the bits-per-word counter, the errors-per-word counter as well as an indication whether a SYNC word has been recognized, an indication of start or end of telemetry (when applicable) and an indication of correct word parity are transferred to the computer and stored therein. The comparison operation, as well as, the other operations in the subunits are performed in a multi-phase clock sequence which is controlled by a selected number of high frequency clock pulses, generated each time a new bit is transferred to the data register from the bit synchronizer.

The novel features that are considered characteristic of this invention are set forth with particularity in the appended claims. The invention will best be understood from the following description when read in connection with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGURE 1 is a simple diagram of a stream of bits, forming multiword messages, useful in explaining the present invention;

FIGURE 2 is an overall simplified block diagram of the present invention;

FIGURE 3 is a diagram of pulses useful in explaining the enabling pulses supplied between the unit of the present invention and a computer, with which the unit is assumed to communicate;

FIGURES 4 and 5 are partial block diagrams of the arrangements, shown in FIGURE 2;

FIGURE 6 is a waveform diagram of pulses generated in the unit of the present invention; and

FIGURE 7 is a simple block diagram of a control circuit shown in FIGURE 2.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

In order to simplify the following description of the present invention, reference is first made to FIGURE 1 which is a simplified diagram of a stream of bits of the type which may be received in a receiver of a telemetry system, after the removal of various carrier signals therefrom. It is appreciated by those familiar with the art, that when data is telemetered from a source, such as a spacecraft to a ground receiving station, the meaningful data, after the removal of various carrier signals, consists of messages, each comprising a plurality of multibit words. The number of bits in each word is usually fixed. Since in such receiving systems, the data bits received may not necessarily start with the beginning of a particular word in any of the messages, a frame SYNC word containing a predetermined multibit code is included in each message. Upon detecting such SYNC word, the previously received stream of bits may be divided into discrete words in order to properly interpret the received data. Once a SYNC word is detected, the number of bits received until the detection of a subsequent SYNC word is accurately monitored, to determine whether any meaningful data bits have been lost in the transmission process.

The present invention will be described in conjunction with data words, each consisting of eleven bits, with each message assumed to consist of sixteen words including a SYNC word. In FIGURE 1, only a portion of a message **1** is diagrammed, while a message **2** is completely diagrammed, shown including data words W1 through W15, followed by a SYNC word designated SW. It is appreciated, that if the beginning of the received data is in the middle of message such as, in the middle of data word

W12, the bits of words W13, W14 and W15 of message **1** cannot be properly divided into discrete words until the SYNC word SW of message **1** is detected. Once such a word is detected, the previously received data bits of message **1** can be divided into discrete groups of eleven bits to form the various data words of message **1**. It is the basic function of the present invention to provide the means necessary for receiving such a stream of bits and to operate thereon to detect the SYNC word in each message, as well as, provide the computer with which the unit is interlocked, necessary information, in order to properly interpret the bits transmitted thereto through the unit of the present invention.

FIGURE 2 which is a simpli-

the start of telemetry logic unit **15** is to provide a signal or interrupt line to the computer with which the unit is assumed to be associated, to indicate to the computer that the start of telemetry has been detected and that data is being transferred to the unit, so as to alert the computer to prepare itself for data transmission in the near future.

This signal on an interrupt line is designated by numeral **20** in line *a* of FIGURE 3 which is a diagram of waveforms of various signals which are either supplied by the word forming unit of the present invention to the computer or from the computer to the unit. The direction of the flow of the signals is indicated by the arrows on the right hand side of FIGURE 3. Arrows pointing to the right indicate signals supplied to the computer, while those pointing to the left indicate signals supplied by the computer to the word forming unit. In one actual reduction to practice, the various signals employed in the unit varied between 0 and −6 volts, the zero (0) indicating a false (F) state, while the −6 volt indicates at true (T) state. As is seen from line *a* of FIGURE 3, the signal on the interrupt line is supplied to the computer to indicate the sending of beginning of telemetry is a −6 volt or a T signal.

As the start of telemetry signal is supplied by the FM demodulator to actuate start-of-telemetry logic unit **15**, stripped bids of data are supplied by the demodulator to the bit synchronizer **12**, and therefrom to a data register **22**. Also, the bit synchronizer **12** supplies substantially in synchronism with each data bit, the data bit clock pulse, hereafter referred to as a bit pulse. Such bit pulses are often referred to by those familiar with the art of telemetry as PCM clock pulses. Each bit pulse is supplied through a control unit **24** to a bits-per-word counter **25**. The control unit **24** is controlled by the start of telemetry logic unit **15**, so that only after the sensing of the start of telemetry by unit **15** is control unit **24** enabled to supply the bit pulses to unit **25**, wherein the pulses are counted. The bits-per-word counter is operated to be reset to a count of 1 by the receipt of a new bit pulse each time the count herein reaches a number equal to the bits-per-word of the data received thereby.

Thus in the present example, since each word is assumed to consist of 11 bits, the bits per-word counter **25** is reset after the count therein reaches 11. Also, in one embodiment of the present invention, the data register **22** con-

sists of 11 bits thereby having a capability of storing a complete word therein. In another embodiment, as will be described hereafter, the data register is capable of storing an additional bit to prevent any bit loss, whenever the computer with which the unit is associated is hung up and is incapable of receiving the data from the data register upon an appropriate command by the unit.

As seen from FIGURE 2, the word forming unit of the present invention includes a SYNC word compare unit **30** which is connected to the data register **22**, as well as, to an error counter and SYNC word logic **32**. Also, the unit includes a clock **39** which provides clock pulses at a rate, much higher than the rate of the bit pulses supplied by the bit synchronizer. In one embodiment of the present invention, the period of each bit pulse from the synchronizer is at least 200 microseconds in which case the period of each clock pulse interval from clock **39** is chosen to be equal to 2 microseconds. Therefore, in FIGURE 2, clock **39** is designated as a 500 kb./sec. clock. The output of clock **39** is connected to a counter and control unit **37**, the output of which is connected to the SYNC word compare unit **30**, as well as, to the data register **22**. Unit **37** in turn is controlled by the output of control unit **24**.

After the sensing of the start of telemetry by logic unit **15**, the counter and control unit **37** (in response to each bit pulse from synchronizer **12** is supplied through control unit) are enabled to provide a string of high frequency pulses which are used to control the basic operation of the word forming unit of the present invention, in a manner that will be described hereinafter in greater detail. These pulses, for explanatory purposes, will be referred to as the control pulses.

In one embodiment of the invention, unit **37** is operated to provide a sequence of 14 control pulses in response to each bit pulse supplied to the bits-per-word counter **25**. Eleven of the fourteen control pulses are supplied to the SYNC word compare unit **30** to sequentially compare each bit, stored in the data register with a preselected binary state, representing the code of the known SYNC word to be detected and thereby compare the content of the eleven bits in the data register with the expected code of the SYNC word. Each bit in register **22** is compared to determine its binary state. If its state matches that of the state of the corresponding bit in the code, forming the SYNC word, the absence of an error signal is supplied to logic unit **32**. However, if the comparison is negative, an error signal is supplied to logic **32** wherein the errors are counted in an error counter which, with the logic associated therewith is adjusted to count up to a preselected maximum count. When this count is reached, a signal is provided on the number-of-errors lines **33** for subsequent transmittal to the computer. If however, after scanning or comparing each bit in the data register **22**, the maximum count is not reached in error counter **32**, thereby indicating that the bits in the data register **22** are in binary states corresponding to the code of the SYNC word, a signal is supplied on a SYNC-word-recognized line **34**, which may be thought of as comprising a second output line of logic **32**.

Logic **32** includes two additional output lines, designated by numerals **35** and **36**. Output line **34** provides a signal representing the absence of the recognition of the SYNC word, while output line **37** provides a signal indicating that all the bits in data register **22** have been compared and all the errors have been counted. The latter two output lines are supplied to a word-ready logic unit **40**, which is also supplied with a signal from the bits-per-word counter **25** whenever the count in the bits-per-word counter is a maximum, i.e. eleven (11) in the present example. Unit **40** has a word ready output line **42** on which a word ready signal is supplied to the computer whenever all the errors have been counted and the count in the bits-per-word counter **25** is 11 or a SYNC word has been recognized by logic **32**. The word ready signal is diagrammed in line *b* of FIGURE 3 and is designated by a true signal **44**. The interrupt line is also sent to the computer whenever the word ready signal is sent, except that the word ready signal by itself is sent for a start of telemetry indication to the computer.

Once the computer senses the signals on the interrupt line and word ready line, and is capable of interrupting any of the routines performed thereby, a word forming unit (WFU) enable signal is supplied by the computer to a control circuit **45** in the WFU of the present invention. The latter signal, is diagrammed on line *c* of FIGURE 3 and is designated by numeral **46**. Upon receiving signal **46** from the computer, control circuit **45** returns a drop-in pulse or signal **47** to the computer, to indicate that the enabling signal **46** has been received. At the same time, the control circuit **45** provides enabling signals to a plurality of gates to enable the transmission of the content of the data register **22**, the bits-per-word counter **25** and the signals on the SYNC word recognized line **34** and error lines **33** respectively to the computer. The signal generated by control circuit **45** to open the plurality of gates is diagrammed in FIGURE 3 line *e* and is designated by the true signal **48**. After the computer has received all the necessary information, a disconnect signal **49** is supplied by the computer to the WFU through control circuit **45**. This signal closes the gates, as well as, resets signal **44** representing the word ready signal to a zero (0) level, until a subsequent state in the word forming unit again provides a true signal on the word ready line.

For a more complete description of the word forming unit of the present invention, reference is made to FIGURES 4 and 5 which are more detailed block diagrams of circuits, shown in FIGURE 2. FIGURE 6 is a diagram of waveforms of signals which are useful in explaining the teachings disclosed herein. In FIGURE 4, the start of telemetry logic unit **15**, the interrupt logic unit **17** and the control unit **24** are diagrammed in more detail, while in FIGURE 5 the rest of the circuitry of FIGURE 2 is shown in greater detail. As previously explained, the FM demodulator **10** provides the unit with a signal, indicating that a telemetry burst containing a sequence of data bits is being received.

Assuming, that each telemetry burst consists of approximately five messages, each of sixteen words, with eleven bits per word, for a total of 880 bits and that the bit rate is 4.4 kilobits (kb./sec.) $\pm 10\%$, the unit of the present invention must be turned ON for a maximum of 0.22 second. A timer (not shown) in the FM demodulator **10** keeps a pulse code modulation (PCM) status line ON or true for this time. Because the PCM status line can have a tendency to jitter at the start of telemetry, many false start (and end) of telemetry signals might be sent to the computer which could conceivably fill up the computer's available storage space for data if it answered all these incorrect interrupts. To prevent this, the PCM status line is not directly used by the WFU but is delayed by 200 microseconds, before being sampled by the WFU. If the PCM status line is not still present 200 microseconds after its beginning, then the WFU will consider the signal a "jitter pulse" and ignore it. In FIGURE 4, numeral **56** represents the PCM status line and numeral **62** represents a 200 microsecond monostable multivibrator, both connected to the S input of PCM enable flip-flop **60**. When the PCM status line is true and remains so for 200 microseconds, FF **60** is set by the delayed pulse of unit **62** so that the S output thereof is true for 0.22 second, designated in FIGURE 4 by pulse **64**.

The complement of signal **64**, designated in FIGURE 4 by numeral **65** is present on the reset (R) output of flip-flop **60**. As long as the R output of flip-flop **60** is false, assumed to be represented by a "0" volt level, it indicates that telemetry is ON, i.e. meaningful data is being received. In addition, the output of the demodulator **10** is supplied through a gate **66** operating as an inverter, as indicated by the "I" therein. The output of inverter **66**,

as well as the R output of flip-flop **60** are supplied to a reset (R) input of **60**, so that at the end of 0.22 second the flip-flop is reset to indicate the end of telemetry.

The R output of FF **60** is connected to the S input of a start telemetry flip-flop **70**, the R output of which is connected to one input of an OR gate **62**. The positive leading edge of signal **65**, occurring at the start of telemetry delayed by 200 microseconds, sets flip-flop **70** so that the R output thereof switches from a negative to a positive level, i.e. from a true to a false level as indicated by a positive leading edge of a pulse **72**. When one of the inputs of gate **62** is false, i.e. its level is "0," the output of it is true as indicated by negative leading edge **73**. This in turn causes the outputs of gate **74**, operating as an inverter, to provide a false output represented by numeral **75** which is supplied to the S input of an interrupt line flip-flop **78**. When the S input of flip-flop **78** is false, i.e. its level goes through a positive-going transition, the R output thereof changes to false as indicated by leading edge pulse **79**. Pulse **79** is supplied to the input of an inverter **80**. Its output is therefore true or at —6 volt level which is supplied to the computer as signal **20** on the interrupt line. Signal **20** is diagrammed in line *a* of FIGURE 3.

Thus it is seen that upon the sensing of the start of telemetry, indicated by the positive going leading edge of pulse **65** at the R output of flip-flop **60**, a true or —6 volt interrupt line signal is supplied to the computer. The function of this signal is to alert the computer that telemetry has begun and that the computer should, as part of the general processing be prepared to receive data from the unit. As telemetry is sensed, the bit synchronizer **12** begins to supply a stream of data bits to the data register **22**, as well as, bit pulses. As previously indicated, the bit rate in the example herein described is assumed to be 4.4 kilobits per second (kb./sec.), so that the period of each bit pulse is about 227 microseconds. However, it is possible that sometimes at the start of telemetry the frequency of the bit pulses supplied by the bit synchronizer can be much higher than the desired rate, resulting in unwanted words being read into the data register **22** and therefrom to the computer, to the point where available computer storage space is exceeded before any useful data words arrive.

In order to prevent this from occurring, in accordance with the teachings of the present invention, a multivibrator **90** is supplied with each bit pulse from synchronizer **12**. In response thereto, the multivibrator **90** provides a pulse having a width of 100 microseconds and whose minimum off time is 80 microseconds for continuous operation. As a result, the maximum rate at which the clock may be supplied to the unit is limited to 5.5 kb./sec. However, when the bit rate of the bit pulses from the synchronizer **12** is less than 5.5 kb./sec., which under normal conditions is only 4.4 kb./sec., the multivibrator **90** provides response to each bit pulse a false signal, designated **92** of a duration of 100 microseconds. This pulse is supplied to one input terminal of each of NAND gates **93** and **94**, the other inputs of which are connected to the S output of flip-flop **60**. As a result, during the duration of each of the pulses from multivibrator **90** both inputs of each of NAND gates **93** and **94** are false, therefore providing a true or a —6 volt output.

Thus, under normal conditions, as each bit pulse is received from bit synchronizer **12**, a true pulse of a duration of 100 microseconds is provided by each of gates **93** and **94**. The true pulses from gate **93** are supplied to the bits-per-word counter **25** (FIGURE 2), so that in response to each data bit, received by register **22**, the count in the counter **25** is increased by 1. The true pulse from gate **94** is supplied, as seen from FIGURE 5, to a gate **100** which controls the supply of control pulses from the 500 kc. clock **35** to a 14-count counter **102**. The output of gate **94** is also supplied to the 14-count counter **102**, which together with the gate **100** and a counter logic **103** may be thought of as comprising the counter and control unit **37**, shown in FIGURE 2.

Briefly, the true output of gate **94** represented by pulse **95**, when supplied to gate **100** (FIGURE 5) enables the gate so that pulses from clock **35** may be supplied therethrough to the counter **102**. Also, the true level of pulse **95** is supplied to the counter **102** (FIGURE 5) to enable the flip-flops (not shown) therein to respond to the high frequency pulses supplied thereto from the clock **35**. The period of each square wave pulse from clock **35** is 2 microseconds. As the counter counts up the high frequency pulses supplied thereto, the state of each of the flip-flops of the counter is supplied to the counter logic **103** having **14** output lines. These are designated CP1 through CP14. When the count in counter **102** is one (1), a true (—6 volt) level is impressed on output line CP1, representing the first control pulse as hereinbefore defined. Similarly, a true or negative level is impressed on each of the output lines to form each of the other 13 control pulses.

The first control pulse, i.e. the true level on output line CP1 is not utilized at all. This time is used to allow data transients to settle. However, the second control pulse is utilized by connecting the output line CP2 to the data register, using the second control pulse to shift the data in the register as is done in a conventional shift register. Thus, the data supplied to the data register **22** from the bit synchronizer (FIGURE 2) is advanced or clocked into the register by means of the second control pulse supplied by the counter logic **103**. The next 11 control pulses on lines CP3 through CP13 are supplied to the SYNC word compare unit **30**, which as seen from FIGURE 5 is connected to each of the bits in the data register **22**, i.e. the unit **30** has 11 inputs connected to the 11 outputs of the 11 bits (B1–B11) in the register **22**.

The basic function of the SYNC word compare unit **30** is to compare the state of each bit during the period of each high frequency control pulse, supplied thereto, and determine whether the state of the particular bit corresponds to that expected thereof in accordance with the pre-selected code of the SYNC word. If the state of the particular bit compares with the expected state, an absence of an error signal is induced in the output line **105** of unit **30**. However, if the binary state of the bit does not compare with that expected thereof in accordance with code of the SYNC word, a true error signal is supplied via line **105** to a NAND gate **107** which forms part of the error counter and SYNC word recognized logic **32** (FIGURE 2). That is, during the period consisting of 11 control pulse intervals, from 0 to a maximum of 11 error pulses may be induced in line **105**, depending on the number of bits in the data register, whose binary states do not compare with those expected thereof in accordance with the code of the SYNC word to be recognized. The output of NAND gate **107** is connected to an error counter **110** which in FIGURE 5 is shown comprising of two flip-flops FF1 and FF2. The output of each flip-flop is connected to an error counter logic **112**, the output of which is connected through an inverter **113** to the other input of NAND gate **107**. The output of flip-flops FF1 and FF2 are also connected to NAND gates **114** and **115** respectively.

The error counter logic **112** is manually controlled so that when the count in counter **110** reaches a preselected count, the output of error counter logic **112** is a true level as indicated by the negative leading edge **121**, so that the output of inverter **113** to the NAND gate **107** is a false or positive leading edge **122** thereby causing the output of **107** to be a true or —6 volt level, irrespective of the true error signals supplied thereto via line **105** from unit **30**. As a result, the output of **107** continues to be a true or —6 volt output which inhibits the supply of pulses to counter **110**. Thus, the count therein remains fixed.

As seen from FIGURE 5, the output of error counter logic **112** is also connected to a SYNC word flip-flop **130**.

Also, the 14th control pulse via the output line CP14 of logic 103 is supplied to the same SYNC word flip-flop, as well as, to gate 100. The function of the 14th control pulse is to disable gate 100 to prevent the supply of additional high frequency clock pulses from being supplied to counter 102 from clock 35. Thus, when the 14th clock pulse is generated, the count in counter 102 remains at 14. Pulse CP14 is also used to reset FF130 when the level or output of logic 112 is false. However, when the output is true, as is the case when the number of errors has been exceeded, logic 112 inhibits CP14 from resetting FF130, so that its R output is false as indicated by 131 and its S output true, as indicated by 132. When the R output of flip-flop 130 is at a false or 0 volt level, it indicates the absence of the recognition of a SYNC word. This output is supplied to a NAND gate 134 which is enabled, as will be explained hereafter, to supply to the computer a signal indicating the absence of the recognition of a SYNC word.

Reference is again made to counter 110 and the error counter logic 112. Let it be assumed, that it is desired to supply the computer with the signal indicating that the SYNC word is recognized only when the 11 bits in the data register 22 are in binary states which correspond to those expected thereof in accordance with the code of the SYNC word. In such a case, the error counter logic 112 is adjusted to block any signals from being supplied to counter 110 through gate 107 once the count in counter 110 is one, i.e. one more than the expected 0 errors assumed. In such a case, if one of the bits in register 22 does not compare with the expected state thereof, i.e. the word in the register is not to be assumed as a SYNC word, an error signal is supplied via line 105 to 107 which advances the count in the counter 110 to 1. As a result, the output of logic 112 becomes true as indicated by numeral 121, blocking by means of inverter 113 the supply of any additional error signals to be counted in counter 110.

If all the bits in the data register 22 are in binary states in accordance with the code of the SYNC word, i.e. they comprise a SYNC word, no error signals are supplied via line 105 to gate 107. As a result, after the 13th control pulse, the count in counter 110 is 0, resulting in a false output of logic 112 which in turn allows flip-flop 130 to be reset by CP14 so that its R output is true. This when supplied via gate 134 to the computer indicates the recognition of a SYNC word in the data register 22. As previously stated, if the error count exceeds the predetermined limit, a —6 volt level will result on the reset level control of FF 130 (sig. 121) thereby preventing CP14 from resetting FF 130. Logic 112 may be controlled so that even when a preselected number of error signals are supplied via line 105 from unit 30, still the computer assumes that the bits in register 22 consists of a SYNC word. This is particularly desirable under severe signal-to-noise conditions when a danger exists that one or more of the bits may have inadvertently been reversed by the bit synchronizer so that it is desired to provide the computer with a SYNC word recognition signal even though one or more of the bits in register 22 do not correspond to the states expected thereof.

The S output of flip-flop 130 which is true in the absence of recognition of a SYNC word and false when a SYNC word is recognized, is supplied to one input of an OR gate 141 the other input of which is connected to the bits-per-word counter unit 25. Unit 25 provides a true or —6 volt level to gate 141 whenever the count in the bits-per-word counter 25 is other than 11. However, when the count therein is 11, i.e. a full count is reached therein, a zero volt or false signal is supplied to gate 141. Therefore, either the condition of 11th count or SYNC word recognized will result in a true (—6 volt) output at gate 141. The output of OR gate 141, as well as, the 14th control pulse CP14 are supplied to two inputs of a NAND gate 142, the output of which is connected to one of the set inputs of a word ready flip-flop 145. At the end of each error counting sequence, i.e. when the 14th control pulse arrives, this pulse opens the gate 142 allowing either the 11 bits or SYNC word recognized condition to pass through. The set or S output line of flip-flop 145 comprises the word ready line 42, assumed to be connected to the computer.

In operation, when the count in the bits-per-word counter 25 reaches 11, so that the input of 141 is 0 volts, the output thereof is true or —6 volts so that when the 14th control pulse is supplied to gate 142 by counter logic 103, both inputs to the NAND gate 142 are true, so that the output thereof is false. As a result, a false signal is supplied to flip-flop 45 and thereby setting it so that the level at the S output thereof on the word ready line 42 is true, as indicated by the negative leading edge 146. A similar logic operation occurs when instead of the 0 volt signal from unit 25, indicating that the bits-per-word counter stores the count of 11, the inputs to OR gate 141 from flip-flop 130 is false or 0 volts, a situation occurring when a SYNC word has been recognized by unit 30, as being stored in the data register 22.

Thus, the flip-flop 145 is said to provide a true output on the word ready line 42 whenever the count in the bits-per-word counter 25 reaches the count of 11 or when the 11 bits in the data register 22 are recognized to comprise a SYNC word. It should be pointed out, however, that the setting of the word ready line 42 to a true level occurs during the 14th control pulse, supplied by the counter logic 103 which enables the NAND gate 142. When the S output of flip-flop 145 is true, the R output thereof is set to a false or —0 volt level, as indicated by the positive leading edge 148, so that the output of unit 17 representing the interrupt line is true as indicated by the negative leading edge 149. Thus, except during the start of telemetry, when as hereinbefore described in conjunction with FIGURES 2 and 4 when the interrupt line only is set to true, thereafter each time the word ready flip-flop 145 is set to have a true output as indicated by numeral 146, the interrupt logic unit 17 is also set to have a true output. The negative leading edges 146 and 149 on the word ready line and the interrupt line respectively (FIGURE 5), are also designated in lines *a* and *b* respectively of FIGURE 3, in which numerals 20 and 44 represent true levels or pulses supplied to the computer from the word forming unit of the present invention.

As herebefore briefly explained, once the interrupt line and the ready line are true, when the computer is ready, a word forming unit (WFU) enable pulse 46 is supplied by the computer to the control circuit 45, shown in FIGURE 2 and in greater detail in FIGURE 7 to which reference is made herein. In response to the WFU enable pulse 46, the control unit generates a drop-in-pulse 47 which is returned to the computer to indicate that the enabling pulse 46 was received. Also, at the same time the interrupt line flip-flop 78 (FIGURE 4) is reset so that the level on the interrupt line is set from a true or —6 volts to a false level or 0 volts. Within control circuit 45, in response to the enabling pulse 46 a true pulse represented in line *e* of FIGURE 3 by numeral 48 is generated. The function of the true pulse 48 is to enable all the gates in the unit through which data or states of various elements therein are supplied to the computer. For example: pulse 48 is supplied to each of NAND gates 114, 115 and 134, shown in FIGURE 5 so that the computer may receive through gates 114 and 115 the states of flip-flops FF1 and FF2 respectively of the error counter 110, while gate 134 is used to indicate to the computer whether a SYNC word was recognized in the data register 22, or the absence of such recognition. Similarly, the unit of the present invention includes a plurality of gates through which the state of the 11 bits in the data register 22 are supplied to the computer. These are indicated in FIGURE 5 by numerals 161 through 171 respectively, gate 161 supplying to the computer the binary state of bit B1

in the register while gate **171** supplies to the computer the state of bit B11 in the register.

After the computer has received all the information necessary thereto, a disconnect pulse **49** is supplied by the computer to the control circuit **45**. The function of this disconnect pulse is to reset the word ready line to a false level, as well as, stop the reading operation. In response to pulse **49** the controlled circuit as will be explained herein after conjunction with FIGURE 7 provides stop read pulses hereafter deisgnated as SR1 and SR2 (FIGURE 7). These pulses are supplied to various circuits in the unit to reset them for subesquent operations when a second data bit and a corresponding bit pulse are received. It can be seen that SR1 and SR2 will occur only when FF **182** is enabled, i.e. when gate **191** is opened by a true level from the R of FF **182**. This prevents other common disconnects intended for other equipment from resetting useful information in the WFU.

As may be seen from FIGURE 7, the word forming unit (WFU) enable pulse **46** from the computer is suplied to a shaping circuit **180** in the control circuit **45**. The output of circuit **180** is a false output pulse **46***a* which is the same as the input pulse thereto. The output of circuit **180** is supplied to the R input of a WFU enable flip-flop **182**. When the false pulse **46***a* is applied to the R input, the set (S) output of flip-flop **182** is switched to a false level, as indicated by a positive leading edge **183**, while the reset or R output thereof is switched to a true level, as indicated by numeral **184**. The S output is supplied to an inverter **185**, so that when the flip-flop **182** is reset, the output of inverter **185** is true, as indicated by the negative leading edge **186**. It is this true level that is supplied to the various gates to enable the supply of the various signals and states to the computer. Also, the S output of flip-flop **182** is connected to the input of a two microsecond (μs) multivibrator **190** the output of which is the drop-in pulse **47** (see FIGURE 3) which is supplied to the computer to indicate that the enabling signal **46** has been received therefrom.

The R output of flip-flop **182** is supplied to one input of a NAND gate **191**, the other input of which is connected to the output of an inverter **192** the input of which is connected to the computer. When the computer has read out all the information necessary from the unit and is ready to service other units, the disconnect pulse **49** (see FIGURE 3) is supplied by the computer to inverter **192**. As a result both inputs to NAND gate **191** are true or −6 volt, resulting in a false output as indicated by numeral **194**. The output of NAND gate **194** represents a first stop-read signal, designated SR1. The output of the gate **194** is also supplied to an inverter **193**, the output of which is true as indicated by numeral **195**, to represent a second stop-read signal designated SR2. Thus, when disconnect pulse **49** is received, circuit **45** provides a false stop-read signal SR1, and true stop-read signal SR2. The latter signal is supplied to the S input of flip-flop **182** to set the flip-flop, so that its S output becomes true thereby causing inverter **185** to provide a false output which is represented by numeral **197** in line *e* of FIGURE 3. This false level closes or blocks all the gates in the unit from supplying the information to the computer until a subsequent enabling pulse such as **46** is received therefrom.

The teachings of the present invention may be summarized as follows: Upon receiving a start of telemetry indicating pulse from demodulator **10** (FIGURE 4), the unit of the present invention is enabled by means of flip-flop **60** (FIGURE 4) for a period long enough for all the bits in the particular burst of telemetry to be received. As hereinbefore assumed, each burst comprises of 880 bits, supplied at a rate of 4.4 kilobits per second. The unit is enabled for a period of at least .22 second by means of a timer in the FM demodulator and a pulse from the multivibrator **62** (FIGURE 4) which enables flip-flop **60** for a period of .22 second represented in FIGURE 6 by a true pulse **64** of a duration of 0.22 second. Pulse **64** is the same as the true output pulse **64** from the S output of flip-flop **60** as shown in FIGURE 4. Upon receiving from synchronizer **12** (FIGURE 4) the first bit pulse designated in FIGURE 6 by numeral **201** which is provided in coincidence with the first data bit supplied to data register **22**, the multivibrator **90** provides the false pulse **92** which is of a duration of 100 microseconds. When pulse **92** is provided by the multivibrator, the output of gate **94** is true providing the true pulse **95** (FIGURE 4) of the same duration, i.e., 100 microseconds.

The negative level of pulse **95**, designated in FIGURE 6 by numeral **202**, which is supplied to gate **100** (FIGURE 5) and counter **102**, opens gate **100** and enables counter **102** to count the high frequency pulses supplied thereto from clock **35**. The period of this clock is 2 microseconds while the actual duration or width of the pulse is only 1 microsecond. When the count in counter **102** reaches 14, the gate **100** is closed, inhibiting the counting of additional pulses therein. The 14 pulses counted by counter **102** are diagrammed in FIGURE 6 and are designated by numerals **211** through **224** respectively. Thus, the true level (**202**) of **95** enables the supply of the high frequency pulses to counter **102**. Also at the same time, the false pulse **92** from multivibrator **90** results in a true output of gate **93** (FIGURE 4) which is counted by the bits-per-word counter **95**. The leading edge **202** of pulse **95** is supplied through an inverter to flip-flop FF1 of error counter **110** via a line **225** (FIGURE 5) to reset the flip-flop to a "0" state.

When the count in counter **102** is 1, in response to the first pulse **211**, the output on line CP1 of logic **103** (FIGURE 5) is true. However, this output is not used for any control purposes, thereby enabling transients from the data transferred to the unit to settle down during the period of pulse **211**. When the count in counter **102** is 2 and the output line CP2 is true, it represents a 2nd control pulse used to shift the data in data register **22** (FIGURE 5). Also the 2nd control pulse is supplied via line **226** to reset flip-flop **2** in the error counter **110** (in case the previous resetting of FF1 had caused the setting of FF2). Thus, after the second control pulse the count in the counter **110** is "0". Control pulses on lines CP3 through CP13, i.e., the next 11 control pulses are used to sequentially compare the state of each of the 11 bits in the data register **22** with the expected binary state thereof in accordance with SYNC word code and provide an error signal on line **105** (FIGURE 5) whenever the state of a particular bit does not correspond with the expected state thereof in accordance with the code.

Error counter logic **112** is manually controllable to control the number of errors which can be tolerated and yet assume that the 11 bits in data register **22** correspond to the SYNC word, thereby providing SYNC word recognition under adverse signal-to-noise conditions. When the 14th pulse **224** is supplied to counter **102** and the count therein reaches 14, a true control pulse on CP14 is supplied by logic **103** which closes gate **100**, as well as, supplies control signals to flip-flop **130** and gate **142**, shown in FIGURE 5.

The signal to gate **142** is utilized to enable NAND gate **142** to set the word ready line **42** to true whenever the count in the bits-per-word counter **25** reaches 11, or when a SYNC word has been recognized, which is represented by the fact that the S output of flip-flop **130** is false, i.e., 0 volts. Once the word ready line **42** is set to true, the interrupt line representing the output of the interrupt logic unit **17** is also set to true, to indicate to the computer that the unit has gone through the necessary operations in response to the last received data bit and bit pulse **201**, and thereby alert the computer that the unit is ready to transmit the following information: the content of data register **22** via NAND gates **161** through **171**, the count in error counter **110** represented by the

states in flip-flop FF1 and FF2 in the counter via gates 114 and 115, the indication whether the SYNC word was recognized via NAND gate 134, the gates being shown in FIGURE 5, the count in the bits-per-word counter 25 (FIGURE 2) via NAND gates 231 through 234, an indication of end of telemetry (if applicable), a parity check on each word (not shown) and a data overflow bit (used only when the computer answers the WFU one bit period too late). The states of all these information bits as well as those of several control functions may be brought out for visual indication on a lamp panel supplied with the unit.

All this information is transferred to the computer only after the computer provides a word forming unit enable signal 46 (FIGURE 7) which results in a true output 186 from inverter 185, which enables the various gates through which the information is to be supplied to the computer. Referring again to FIGURE 6, at the end of the true pulse 95 of a duration of 100 microseconds, the false level thereof designated by numeral 241 causes counter 102 to be reset. This input is a DC, not an AC reset and requires 0 volts for the reset function. However, the gate 100 remains closed until a subsequent true level is supplied thereto from NAND gate 94. Since all the operations occur within the unit during the time that the 14 high frequency clock pulses are supplied by clock 35, a period of 28 microseconds, and since the bit pulse period is 227 microseconds (assuming a bit rate of 4.4 kilobits per second), after all the data has settled in the unit and the word ready line 42 has been set to true, the computer has 200 microseconds during which it can enable the unit to receive the data therefrom at its convenience.

The computer, upon receiving the data contained in the 11 bits of the data register 22, as well as, the count in the bits-per-word counter and the fact whether the SYNC word has been recognized or not, stores this information in the appropriate memory thereof. Then when a SYNC word is recognized such as the SYNC word of message 1 shown in FIGURE 1, depending on the count in the bits-per-word counter during such instance, the computer divides the previously received bits from the unit into the various words W12 through W15 of message 1, i.e. the computer divides the preceding bits received into discrete groups of 11 bits to form the words of message 1 which preceded the SYNC word. There are approximately five identical messages in 1 data burst, each containing a SYNC word.

For example, let us assume that the stream of bits from synchronizer 12 starts with the last 3 bits of W12 of message 1, then it is appreciated that the first 11 bits stored in register 22 will be B9, B10, B1 of W12 and B1 through B8 of W13. These will be transferred to the computer and stored therein. Then during the next three data transfers B9, B10, B11 of W13 and B1 through B8 of W14, B9, B10, B11 of W14 and B1 through B8 of W15, and B9, B10, B11 of W15 and B1 through B8 of SW will be transferred to the computer. Up to this point the computer cannot divide the bits into correct words. However, after the next three bit pulse intervals, i.e. after B9, B10 and B11 of SW are stored in register 22 the SYNC word SW will be recognized and the count in counter 25 will be 3. Thus, when the SW will be transferred to the computer and the count of 3 from 25, it indicates to the computer that the first three received bits belong to one word and thereafter each 11 bit group comprises a different word. Consequently the first three bits received by the computer are assigned to one word and the other 33 bits divided into three words such as W13, W14 and W15 of message 1.

Once a SYNC word is detected the bits-per-word counter is reset so that thereafter, when the next SYNC word such as SW of message 2 is detected the count in counter 25 should be 11. Any other count indicates a loss of a data bit in message 2 and thereby enables the computer to place any desired significance to message 2. The parity check performed by the WFU should indicate where the loss of bits occurred. However, to prevent any loss of data bits from occuring in the event that the computer is unable to accept the 11 bits in register 22 due to servicing other units, register 22 includes a storing capacity for an additional bit so that when the computer is ready it also receives the 1st bit of the previous word which it would normally lose. The count of 1 in the bits-per-word counter and the absence of a SYNC word recognized indication tells the computer that it waited 1 bit period too long before servicing the WFU.

Also the unit includes an additional NAND gate 231 (FIGURE 4) the output of which is true when the end of the telemetry burst is reached indicating that the computer can stop expecting data until the next data burst.

There has accordingly been shown and described herein a novel word forming unit for use with a data bit receiving system and a computer. It is appreciated that in light of the teaching disclosed herein, those familiar with the art may make modifications without departing from the spirit of the invention. Therefore, all such modifications are deemed to fall within the scope of the invention as defined in the appended claims.

What is claimed is:

1. In combination with a data receiving system, adapted to provide a stream of data bits, a data bit clock pulse associated with each data bit and a control signal of duration equal to the time required to provide said data bits, and a computer capable of receiving said data bits and arrange said bits into discrete multibit words, a word forming unit comprising:

A first control stage responsive to said control signal for defining a data transmission time interval which is at least equal to the time duration of said control signal;

a data register;

a bits-per-word counter;

means responsive to each data bit clock pulse during said data transmission time interval for advancing the count in said bits-per-word counter one count per data bit clock pulse, the maximum count in said bits-per-word counter being equal to the number of bits per word;

means responsive to each data bit clock pulse for providing a fixed sequence of control pulses in response thereto;

means for supplying each of said data bits to said data register, said register being responsive to one of the control pulses in said sequence for shifting the data bits therein;

comparing means coupled to said data register and responsive to a selected group of said control pulses in said sequence for providing error signals as a function of the comparisons of the data bits in said register with a selected multibit code representing a SNYC word;

error counting means coupled to said comparing means and including an error counter for counting up to a maximum preselected count said error signals;

SYNC word recognizing means coupled to said error counting means for providing a signal of a first level to indicate the presence of a SYNC word in said data register when the count in said error counter is less than said preselected count, said signal being of a second level indicating the absence of a SYNC word in said data register when the count in said error counter reaches said preselected number; and

output means coupled to said data register, the bits-per-word counter, the error counter and responsive to an enabling signal from said computer to supply said computer with the bits in said data register, the counts in said bits-per-word counter and in the error counter and the level of the signal from said

error counting means which indicates the absence or presence of a SYNC word in said data register.

2. The word forming unit as recited in claim 1 further including means providing a ready signal to the computer when the count in said bits-per-word counter is a maximum or when the signal from said SYNC word recognizing means if of said first level, indicating the presence of a SYNC word in said data register.

3. The word forming unit as recited in claim 2 wherein the number of bits storable in said data register is greater than the number of bits in each data word to prevent the loss of data bits when the computer does not respond to said ready signal before a subsequent data bit and an associated bit pulse are received by said unit.

4. The word forming unit as recited in claim 2 wherein the number of bits storable in said data register equals the number of bits in each data word.

5. The word forming unit as recited in claim 4 wherein said error counting includes controllable means for controlling the maximum preselected count, said count being equal to $X+1$, where X is equal to the maximum allowable number of errors in a word when compared with the true SYNC word.

6. The word forming unit as recited in claim 5 wherein said means responsive to each data bit clock pulse includes means for generating in response to each data bit clock pulse a corresponding clock pulse of a selected minimum time duration to limit the rate at which pulses are supplied to said bits-per-word counter.

7. In combination with a system providing a stream of data bits during each of a sequence of discrete transmission intervals, said bits defining data word each of n bits, said system further providing a bit clock pulse in conjunction with each bit, each stream of data bits including SYNC words comprising of n bits in selected binary states defining an n bit binary code, and a computer adapted to provide enabling and disabling control signals, a word forming unit comprising:

first means responsive to a signal from said system indicating the beginning of a transmission-interval-defining signal the duration of which is at least equal to said transmission interval during which said system provides a stream of data bits;

a shift register of at least $n+1$ bits;

a first counter of n bits;

second means responsive to each data bit clock pulse for providing a corresponding data bit control pulse of a minimum time duration;

third means for advancing the count in said first counter one count per data bit control pulse;

fourth means including a source of pulses for providing in response to each data bit control pulse a fixed number of control pulses arranged in a sequence;

fifth means for supplying each of said data bits provided by said system to said data register, said register being responsive to one of said control pulses in said sequence for shifting the data bits in said data register and entering each received data bit therein;

sixth means associated with said data register and responsive to a selected group of n control pulses in said sequence for sequentially comparing the binary state of each data bit in said register with a corresponding preselectable binary state of said code to provide an error signal when the binary state of the data bit in said register differs from the corresponding state in said code;

seventh means coupled to said sixth means for providing a SYNC-word-recognition signal when the number of error signals provided by said sixth means does not exceed a predetermined number x, an absence-of-SYNC-record-recognition signal and an error-indication signal when the number of error signals provided by said seventh means exceeds said number x;

eighth means coupled to said seventh means and said first counter and responsive to the last control pulse of said sequence for providing a word ready signal of said computer when either the count in said first counter is n or when said seventh means provides said SYNC-word-recognition signal; and

means for receiving a unit enabled signal from said computer to supply thereto, the data bits in said data register, the count in said first counter, and the signal provided by seventh means.

8. The word forming unit as recited in claim 7 wherein sequence of control pulses consists of $n+3$ control pulses and said data register shifts the data bits therein in response to the second control pulse of said sequence and wherein said sixth means is responsive to the 3rd through the $(n+z)$th control pulses for performing the sequential comparing therein.

9. The word forming unit as recited in claim 7 wherein said seventh means includes an error counter and controllable logic means for controlling the maximum number of error signals countable by said counter, said maximum number being $x+1$, where x is controllable to zero or an integer less than n.

10. The word forming unit as recited in claim 9 wherein sequence of control pulses consists of $n+3$ control pulses and said data register shifts the data bits therein in response to the second control pulse of said sequence and wherein said sixth means is responsive to the 3rd through the $(n+z)$th control pulses for performing the sequential comparing therein.

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GARETH D. SHAW, *Primary Examiner.*

66/255

AWARDS ABSTRACT

XNP-9225

Inventor: Hoyt Holmes Nelson
Contractor: Jet Propulsion Laboratory

~~JPL Case No. SC-192~~
NASA Case ~~No. 9225~~
December 29, 1966

TELEMETRY WORD FORMING UNIT

The primary object of the invention is to provide electronic circuitry to act as a buffer-like unit between a telemetry demodulator and a computer in order to simplify and reduce some of the tasks performed by the computer.

The unit includes a data register 22 (Figure 2), a bits-per-word counter 25 and a SYNC word compare unit 30. Basically, at start of telemetry each data bit is clocked into register 22 and the count of 25 incremented by one. With each clocked bit, the content of the register 22 is compared by unit 30 with a specific code comprising a SYNC word. When the count in the counter 25 is a maximum (11 in the example used), a ready signal is supplied to the computer to indicate that data, equal to a word length, is ready to be transferred thereto. Also, when the content of register 22 comprises the expected SYNC word, the ready signal is supplied to the computer. In addition, the count in counter 25 at such instant is also supplied to the computer. The latter count is used by the computer to reorganize previously received bits into discrete words.

The basic beneficial result is the use of a buffer-like unit capable of receiving data bits, transferring them to a computer as blocks of bits and detecting the location of SYNC words in a stream of bits from which the computer can divide the data bits between SYNC words into discrete data words. Thus the word forming task of the computer is greatly simplified, resulting in simpler programming and requiring less computer storage capacity.