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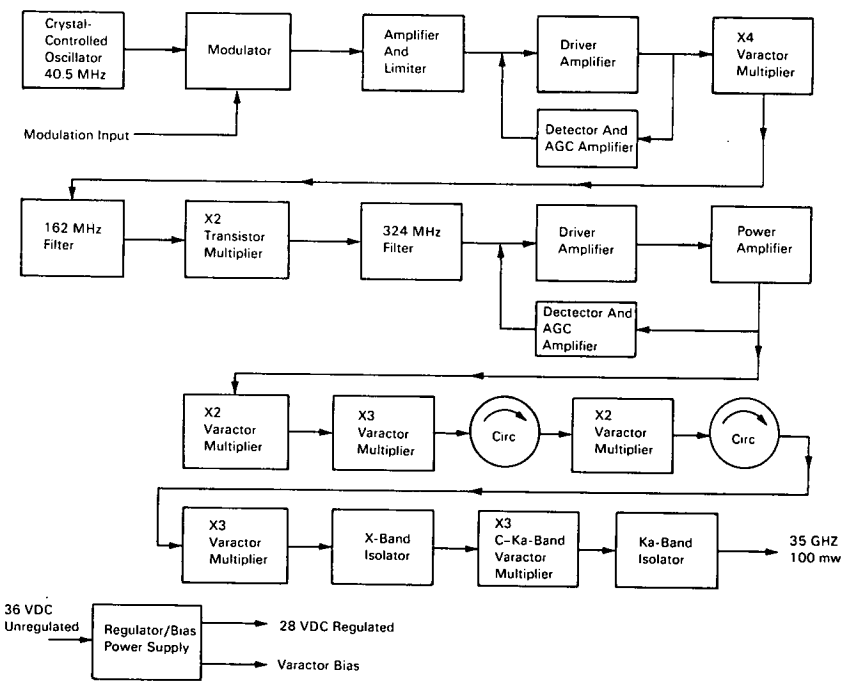
A 35 GHz Solid State Transmitter/Driver



A solid state transmitter/driver (multiplier) signal source has been designed and fabricated to produce a stable crystal-controlled CW power output of 100 mw at 35 GHz. The circuit requires 60 watts of dc input power and exhibits a signal/noise ratio of at least 30 dB below the carrier at 35 GHz. The signal source is contained in a package measuring 8×10×5.5 inches and weighing approximately 18 pounds.

It includes a series of semiconductor amplifiers and multipliers which produce a stable crystal-controlled drive power of approximately 18 watts at 325 MHz. This drive is then applied to a chain of varactor multipliers to a frequency of 35 GHz. The total frequency multiplication factor is 864. Printed-circuit, coaxial, stripline, and waveguide techniques are used for the various amplifiers and multipliers. A phase-modulation exciter is included in the source for telemetry signals.

As shown in the block diagram, the multiplier chain starts with a crystal-controlled oscillator operating at 40.5 MHz. A bandpass filter of 0.02% bandwidth is provided within the oscillator module to limit the noise bandwidth. Following the oscillator, a phase modulator is incorporated to allow frequency modulation of the output. The frequency response of the modulator is 400 Hz to 100 kHz, and it will produce

(continued overleaf)

a maximum deviation of ±215 kHz from 35 GHz output frequency. A limiter-amplifier follows the modulator to remove any amplitude modulation produced in the modulator. An AGC driver amplifier is then used to drive an X4 varactor multiplier to produce a stable 20 mw output at 162 MHz. An m-derived bandpass filter is then employed to suppress the third and fifth harmonics of 40.5 MHz created by the X4 multiplier. Adequate suppression of the spurious harmonics is especially important in the lower end of the chain, since amplification of these (spurious enhancement) is a function of the square of the multiplication factor of the multiplier chain. A transistor doubler is employed to multiply the frequency to 324 MHz and is followed by a 2-section bandpass filter for additional harmonic suppression. The resulting 324 MHz, 100 mw signal is then amplified to 18 watts by a linear driver and power amplifier string. An AGC loop around this amplifier insures a constant drive to the following multiplier regardless of temperature variations. Following the power amplifier, two lumped element varactor multipliers, a doubler and a tripler, are used to multiply the frequency to 1.95 GHz. A stripline circulator is used to isolate these multipliers from the following stripline S-C band doubler/circulator module. The output of this module is 3.9 GHz at 1.7 watts. A transition to Ku band waveguide is accomplished in the following C-X band tripler. The output of this unit is over 500 mw at 11.7 GHz. A waveguide isolator is used between this multiplier and the final multiplier in the chain. This final multiplication from 11.7 GHz to 35 GHz is accomplished by a cavity type tripler which provides 125 mw output power. With the inclusion of a final waveguide isolator and the output waveguide, a power output of 100 mw at 35 GHz is available at the output of the unit. Under normal operating conditions, the source will consume 60 watts of primary power from an unregulated 36 VDC supply in the booster. A regulator circuit has been incorporated in the unit to provide the stable 28 VDC power source required for operation of the multiplier chain.

Note:

Documentation is available from:

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No patent action is contemplated by NASA.

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