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Digital Filter Suppresses Effects of Nonstatistical Noise Bursts on Multichannel Scaler Digital Averaging Systems
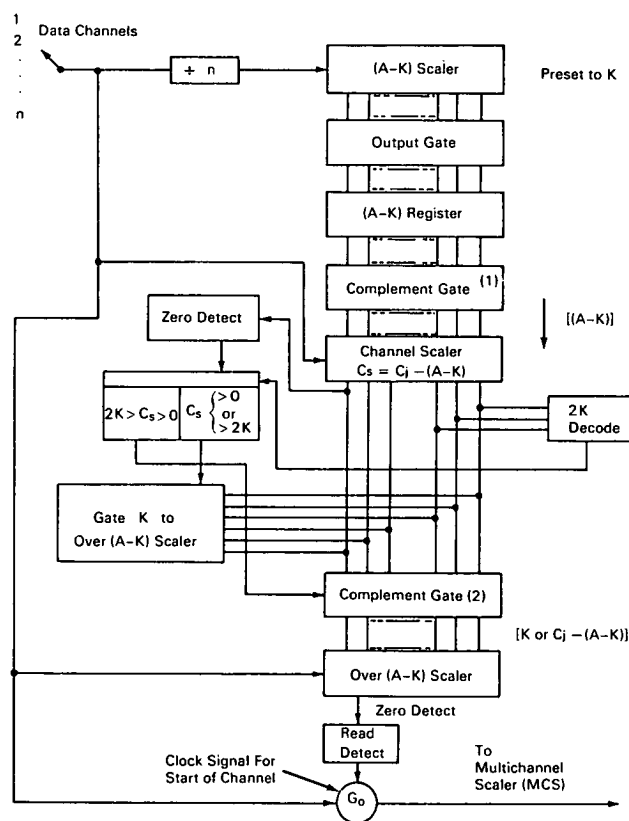
The problem:

To suppress the effects of large, nonstatistical noise bursts on data that have been averaged over many sweeps of a multichannel scaler. Digital data entering a multichannel scaler digital averaging system with a small signal-to-noise ratio will obscure or confuse data previously averaged by the system if the entering data pulse contains large, nonstatistical noise bursts. A means of filtering out such distorted pulse data is required.

The solution:

A digital noise filter, interposed between the sampled channels and the multichannel scaler digital averaging system, makes use of binary logic circuitry to compare the number of counts per channel (C_j) with the average number of counts per channel (A_m).

(continued overleaf)

If the channel count falls within $A_m \pm K$ ($\pm K$ = preset allowable count fluctuation), the channel count is accepted and passed to the multichannel scaler digital averaging system.

How it's done:

Before operating the digital filter (DF), a value K is chosen as the acceptable fluctuation limits about the average number of counts per channel A_m. The filter consists of four parallel paths: (1) a division scaler set to give one output count for every n input counts (n = number of channels being swept); (2) a channel scaler in which incoming counts for each channel j are accumulated; (3) the "OVER $(A-K)$" scaler which is used to output data to the multichannel scaler; and (4) a gate G_o to pass the output of the DF to the input of the multichannel scaler (MCS).

Before each sweep of the data channels, the $(A-K)$ scaler is preset to $\overline{K}$, the binary complement of K. At the end of the sweep, the content of this scaler is transferred by a parallel output gate to the $(A-K)$ register, and the $(A-K)$ scaler is cleared and reset to $\overline{K}$.

The DF reads each channel for a channel period of T_j during each sweep. At the start of each channel period T_j, the complement of $(A-K)$, $\overline{(A-K)}$, is non-destructively shifted by the complement gate (1) to the channel scaler. The channel scaler is thus preset to a value $-(A-K)$. The total counts in the channel scaler at the end of each period T_j will be $C_s = C_j - (A-K)$. The incoming counts for a data channel C_j fed to the channel scaler thus advance the scaler contents toward zero. If C_s reaches zero, then C_j exceeds the lower limit $(A-K)$. To determine whether or not C_j has exceeded the upper limit $(A+K)$, a $2K$ coincidence circuit monitors the channel scaler. If the channel scaler count C_s passes zero but does not pass $2K$, then C_j lies between the limits $(A+K)$ and $(A-K)$ and the channel information is acceptable. If the count C_s is less than zero or greater than $2K$, the allowable limits have been passed and the data are not acceptable. For $(A-K)<C_j<(A+K)$, the binary complement of the contents of the channel scaler [effectively $C_j - (A-K)$] are passed by complement gate (2) into the "OVER $(A-K)$" scaler. For $(A+K)<C_j<(A-K)$, the complement $\overline{K}$ is shifted into the "OVER $(A-K)$" scaler.

At the start of the next channel period T_{j+1}, gate G_o is opened and remains so until the "OVER $(A-K)$" scaler is driven to zero. While G_o is open, either C_j

$-(A-K)$ or K (depending on the contents of the scaler) is transferred into channel $j+1$ of the MCS Thus channel data accumulated in T_j are stored in channel $j+1$.

During T_1, no previous channel information is available, so channel 1 is used to accumulate the sum of all $(A-K)_m$ for the whole run. Thus for T_1 only, circuitry not shown closes G_o, permitting the value $A-K$ to enter channel 1 of the MCS if $C_1>(A-K)$. A small error occurs in the accumulated sum of the $(A-K)_m$ whenever $C_1<(A-K)$.

Notes:

1. A signal strength of $S>K$ is recorded as K rather than $S+K$. In this case, either the DF is bypassed or K must be large relative to S.

2. For the DF described, C_j (counts accumulated for a given channel in each pass) is not signal plus background $s+b$, but the much smaller number $s+K$.

3. This DF has been constructed with 155 integrated circuit devices and has fluctuation limits from 8 to 768 about the average count (2 figure binary precision).

4. Additional details are contained in Review of Scientific Instruments, vol. 37, no. 6, June 1966, p. 769-771.

5. Inquiries concerning this innovation may be directed to:

Patent status: