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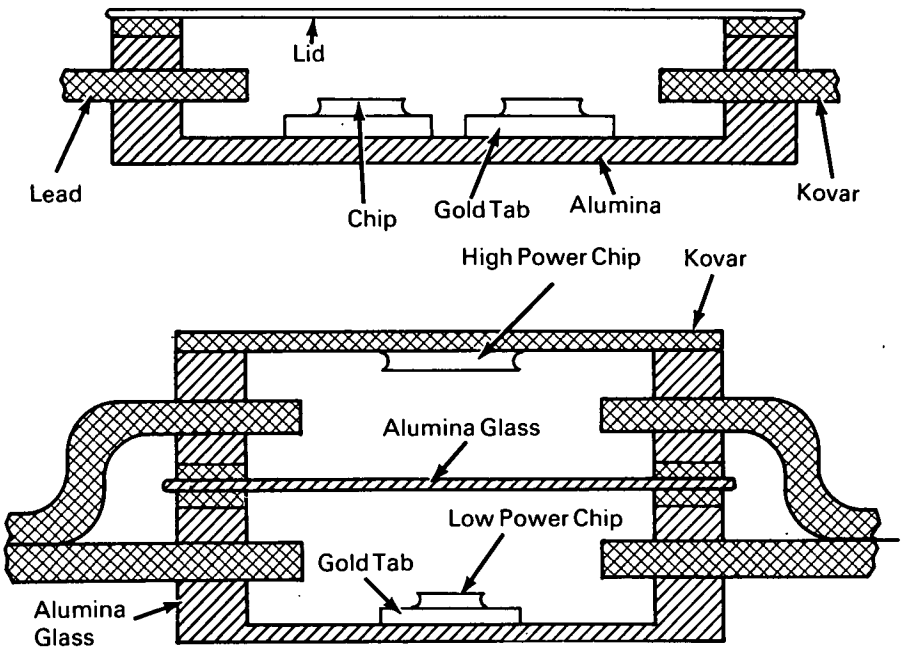
NASA TECH BRIEF

Multichip Packaging with Thermal Insulation



The problem:

In the emerging development of electronic chip usage, a significant advance is being made in space compression by high concentration of chips within a single package. However, thermal cross-coupling has been a limiting factor where low and high molecular power components have been combined in the same package.

The solution:

A thermal insulation technique that permits low and high molecular power components to operate in the same package without thermal cross-coupling.

How it's done:

The low power chip is mounted on a gold tab which is, in turn, mounted to the package on alumina glass, as shown in the lower sketch. The high power chip is mounted on a Kovar substrate and an alumina glass shield is interposed between the two chips. The alumina glass shield with a thermal conductivity of 0.043 tends to thermally isolate the chips while the Kovar substrate with a thermal conductivity of 0.193 acts as a heat sink to remove the heat from the high power chip.

The upper figure depicts a typical multichip molecular package with a resistor on one chip and a

(continued overleaf)

high current transistor on the other, with no thermal isolation. In tests, a power dissipation change of 250 mw in the transistor resulted in a 7.7% value change in the resistor. The same test, performed with the thermally isolated component depicted in the lower figure resulted in only a 0.15% value change in the resistor.

Note:

Inquiries concerning this innovation may be directed to:

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Reference: B68-10119

Patent status:

No patent action is contemplated by NASA.

Source: W. G. Mend and R. G. McInturff
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