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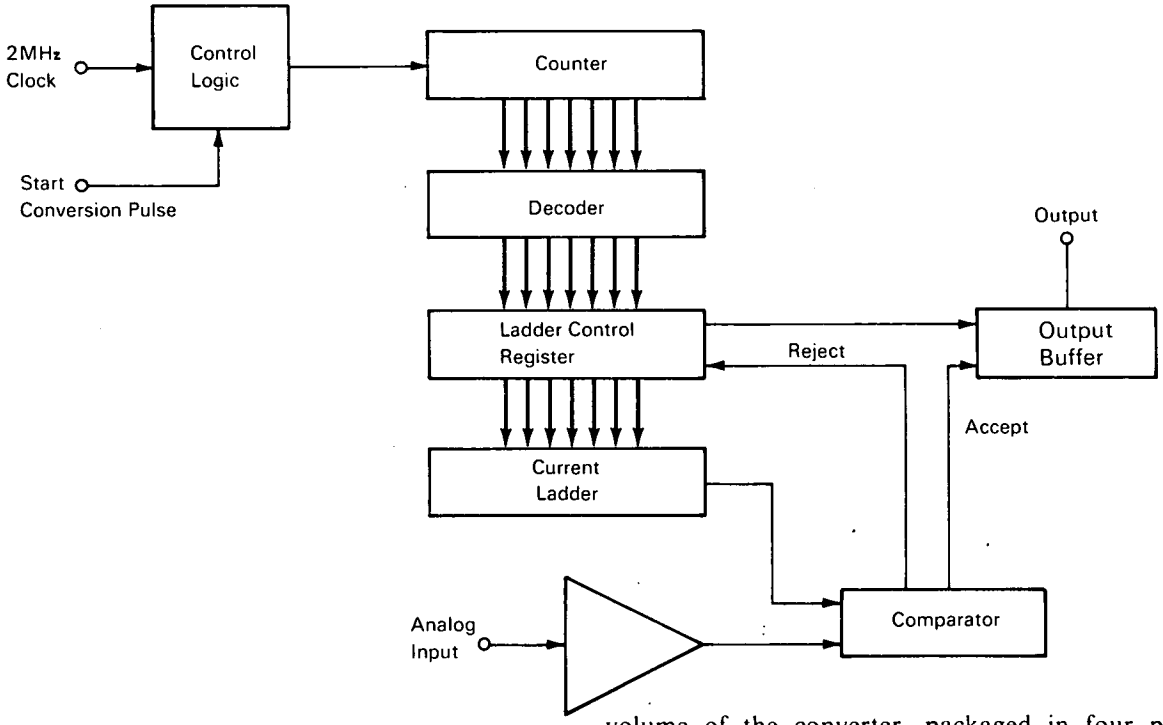
# NASA TECH BRIEF



## Small, Low Power Analog-to-Digital Converter




**The problem:**

To design a small, low-power, high-speed analog-to-digital converter that would be suitable for use in an airborne test data system.

**The solution:**

An 8-bit analog-to-digital converter using silicon chip integrated circuits. The output bit rate is 1 MHz and the maximum conversion rate is 125 kHz. The digital output quantum is 20 millivolts, and the maximum full scale output is 5.100 volts. Total power consumption is less than 840 milliwatts. The successive approximation method of analog-to-digital conversion is used to generate the digital output. Overall volume of the converter, packaged in four potted modules, is approximately 2 cubic inches.

Operation of the converter is summarized in conjunction with the block diagram. A start conversion pulse resets the control logic, counter, and ladder control register, which consists of 8 dc flip-flops and associated "dump" and reset logic. The most significant bit (bit 1) flip-flop in the ladder control register is set (by a specific output from the decoder) to switch the most significant current from the current ladder to the comparator summing line. At 750 nanoseconds after the end of the start conversion pulse, the bit 1 current is compared with the current derived from the analog input. If the summed ladder current

(continued overleaf)

is smaller than the analog current, the bit is retained; if it is larger, a dump pulse is generated to reset the appropriate control register flip-flop. When the flip-flop resets, it switches the corresponding ladder current off the summing line. At the end of the bit time (1 microsecond), the counter advances 1 count. This advance switches in the next smaller bit, the comparison is made after a 750 nanosecond settling time, and the bit is then either accepted or rejected. This procedure is repeated until all 8 bits have been compared. The control logic then resets register bits 2 through 8 and holds the counter in bit time zero until the next start conversion pulse is received. Simultaneously with each comparison, the output flip-flop is set if the bit is accepted and reset if the bit is rejected, generating the digital output.

**Notes:**

1. The converter can be used in any digital system in which it is necessary to convert an analog voltage into a serial digital signal and 8-bit accuracy is acceptable, such as in automated production or process control systems. With further development, the converter could be improved to operate at a higher speed and with greater accuracy.
2. Inquiries concerning this converter may be directed to:

   Technology Utilization Officer
   Marshall Space Flight Center
   Huntsville, Alabama 35812
   Reference: B68-10016

**Patent status:**

No patent action is contemplated by NASA.

Source: D. H. Fullerton and R. D. Dunn
of The Boeing Company
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