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Brief 68-10015

NASA TECH BRIEF

Input Gate Circuit Converted for Use as Linear Amplifier

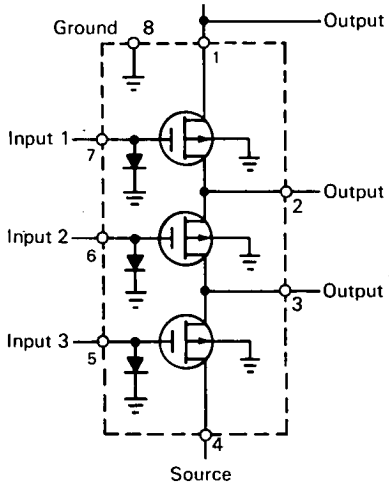

FIG. 1
MOS 3 INPUT GATE CIRCUIT

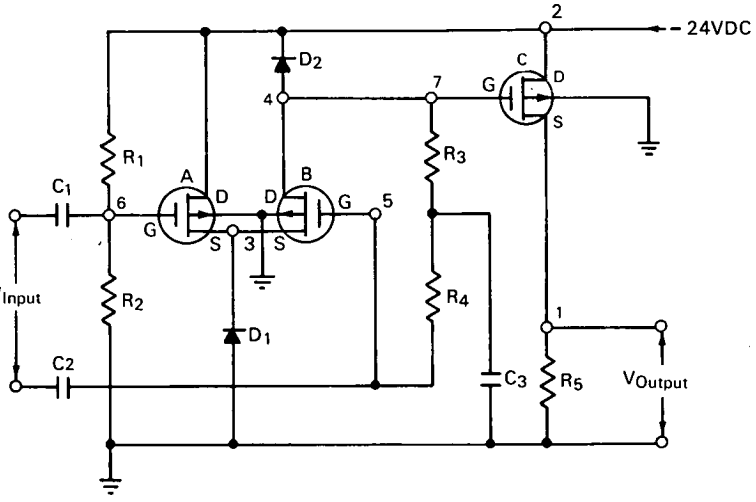

FIG. 2
LINEAR AMPLIFIER CONVERSION

The problem:

To design a linear amplifier in a microphone circuit that has high input impedance, low output impedance, low cost, and is small enough to fit on a standard printed circuit card. Existing techniques use several components and voltage feedback circuitry for impedance matching. These techniques usually require expensive and bulky components.

The solution:

Convert a commercially available integrated circuit that is marketed as a digital computer input gate circuit. This integrated circuit uses metal oxide semiconductor (MOS) devices, and is reconnected as a linear amplifier.

How it's done:

Figure 1 shows a commercially available integrated circuit, which is a P-channel enhancement type, three-input NAND gate circuit. The gate contains three MOS transistors in series. Figure 2 shows the same circuit biased and converted for linear operation. Because the source and drain of the MOS are interchangeable, the common connection may function as a source in one pair and a drain in another pair. By connecting pin 2 to the -24 vdc supply, pin 3 to source diode D_1, pin 4 to pin 7, and the remaining pins to suitable bias points, the circuit is converted. An ac input is coupled through capacitors C_1 and C_2 and is applied to the gate elements of MOS A and B. The MOS A and B circuit forms a differential amplifier controlling the gate of MOS C which controls the output signal across R_5.

Voltage dividers R_1 and R_2 provide dc bias for MOS A. Constant current diode D_1 supplies a constant 2-milliampere current to the source elements of MOS A and B. Thus a constant total drain current

(continued overleaf)

flows regardless of signal polarity. MOS A or B is enhanced whenever a negative voltage is applied to its gate. The electrostatic field produced by the gate voltage is applied to the source and drain junctions forming a continuous current path. The magnitude of the gate signal determines the degree of enhancement, which in turn determines conductivity.

Constant current diode D_2 supplies a constant 1-milliampere current with a high impedance load to the drain element of MOS B. The diode combination establishes circuit balance regardless of temperature effects to circuit parameters and overcomes the problem of transconductance mismatch. The values of voltage divider resistors R_1 and R_2 and resistors R_3 and R_4 are selected for balance of the high input impedance ratios which are necessary for MOS circuit operation. As MOS A and B vary in conduction, the amplified signal is applied to the gate elements of MOS C. As MOS C conducts, a low impedance output signal (3000 ohms) is developed across resistor R_5. Thus, an overall circuit impedance transformation from 10 megohms to 3 kilohms is provided.

The voltage gain of the circuit is linear over a frequency range of 4 Hz to 100 kHz. Above 100 kHz, the voltage gain decreases and is reduced by a half at approximately 180 kHz.

Note:

Inquiries concerning this circuit may be directed to:

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Reference: B68-10015

Patent status:

No patent action is contemplated by NASA.

Source: T. P. Harper
of IBM
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