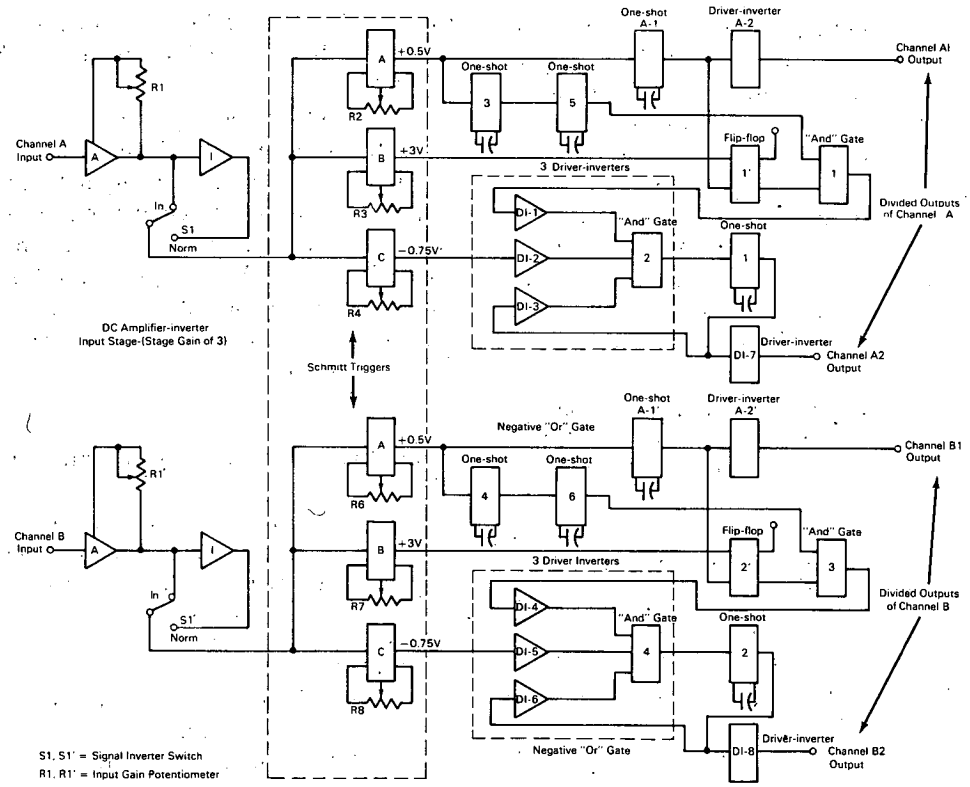
December 1967

Brief 67-10565

NASA TECH BRIEF

Logic Circuit Detects Both Present and Missing Negative Pulses in Superimposed Wavetrains



The problem:

To provide a device capable of detecting a negative polarity pulse in a signal containing superimposed negative and positive data pulse trains. Pulsed data, obtained as output from instrumentation such as flowmeters, is often formatted with positive data pulses from one channel added at twice their amplitude to negative data pulses from a second channel. Such data pulse trains are provided by an FM discriminator with low impedance output. A device is desired which can detect and separate negative polarity pulses and can also determine if a negative pulse is missing from its pulse train.

The solution:

A pulse divide and determination network, which provides a logical determination of pulse presence

(continued overleaf)

within a data train. The network uses digital logic circuitry to perform three functions: (a) to divide positive and negative pulses; (b) to shape the separated pulses; and (c) to determine, by means of coincidence logic, if negative pulses are missing from the pulse train.

How it's done:

The pulse divide and determination network (PD-DN) consists of two separate Schmitt trigger and logic networks for input Channels A and B. Each PD-DN channel consists of: (1) an input-inverter stage of gain 3 at optimum linearity; (2) three parallel Schmitt trigger circuits simultaneously driven by the input stage; and (3) associated one-shot, driver-inverter and digital logic circuitry driven by the Schmitt triggers to perform the required logical decisions and provide required four data-channel pulse outputs (A1, A2, B1, B2).

Assume a typical input pulse train, with Schmitt triggers A, B, and C set to trigger at +0.5 V, +3.0 V, and −0.75 V respectively, simultaneously applied to Channel A and B inputs. This waveform is amplified by Channel A and B amplifier inverter stages (A and I) and fed to the parallel configuration of Schmitt trigger circuits. The output of trigger circuit "A" (Channels A and B) is obtained for any input pulse exceeding a level of +0.5 V and is applied to one-shots A-1 (Channel A) and A-1' (Channel B). These one-shots feed driver-inverters A-2 and A-2' with a 600±50 μ-second pulse. The driver inverters invert the signals and provide low output impedance signals at Channel A1 and B1 outputs. The outputs at Channels A1 and B1 are thus 1-to-1 derivatives of Schmitt trigger circuit "A".

The output required of Channels A2 and B2 is a logical derivation composed of either Schmitt "C" or not Schmitt "B" during Schmitt "A" ON time (i.e., "C"+"A"·"B"). By inverting the inputs to AND gates 2 and 4 with two sets of three driver-inverters (DI-1, 2, 3, 4, 5, and 6), the AND gates are changed to negative OR gates. Schmitt trigger "C" triggers at −0.75 volt and provides a series of pulses which are inverted by DI-2 and 5 and become one input to the negative OR gates. The positive outputs from the OR gates trigger one-shots 1 and 2, which feed a 600±50 μ-second pulse to driver inverters DI-7 and 8. DI-7 and 8 produce Channel A2 and B2 outputs for the case of Schmitt "C" present during Schmitt "A" ON time.

In the event of coincident positive and negative input pulses, the condition where the resulting negative pulse amplitude is not great enough to trigger Schmitt "C" may exist. Schmitt "B" is adjusted so that, in this event, the positive pulse will not trigger Schmitt "B". Since "A" is adjusted to detect all positive pulses, the determination of "B" not having fired during "A" ON time, is as follows: The leading edges of Schmitt "A" output pulses also trigger delay one-shots 3 and 4 which in turn trigger one-shots 5 and 6. Schmitt "B" output pulses set flip-flops 1 and 2; the FALSE outputs of flip-flops 1 and 2 provide the second input to the negative OR gates. The FALSE outputs to the OR gates are actually true when the flip-flops are not set. The outputs of AND gates 1 and 3 (from flip-flops 1 and 2 and one-shots 5 and 6) form the desired logical product "A"·"B" which is inverted by DI-1 and 4 and fed to the AND gates 2 and 4.

To prevent double triggering of one-shots 1 and 2, the outputs of one-shots 1 and 2 are inverted by DI-3 and 6 and provide a third input to the AND gates. A positive transition, emanating from the negative OR gate, is thus inhibited during the period one-shots 1 and 2 are ON. Flip-flops 1 and 2 are reset by the trailing edge of Channels A1 and B1 output pulses to prepare the flip-flop for the next determination of a Schmitt "B" output.

Note:

Inquiries concerning this invention may be directed to:

Technology Utilization Officer
Marshall Space Flight Center
Huntsville, Alabama 35812
Reference: B67-10565

Patent status:

Inquiries about obtaining rights for the commercial use of this invention may be made to NASA, Code GP, Washington, D.C. 20546.

Source: Richard E. Rice,
Douglas Aircraft Company
under contract to
Marshall Space Flight Center
(MFS-12518)