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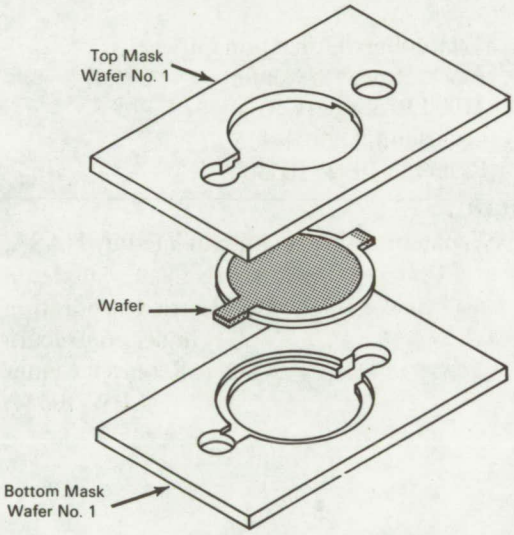
Brief 67-10550

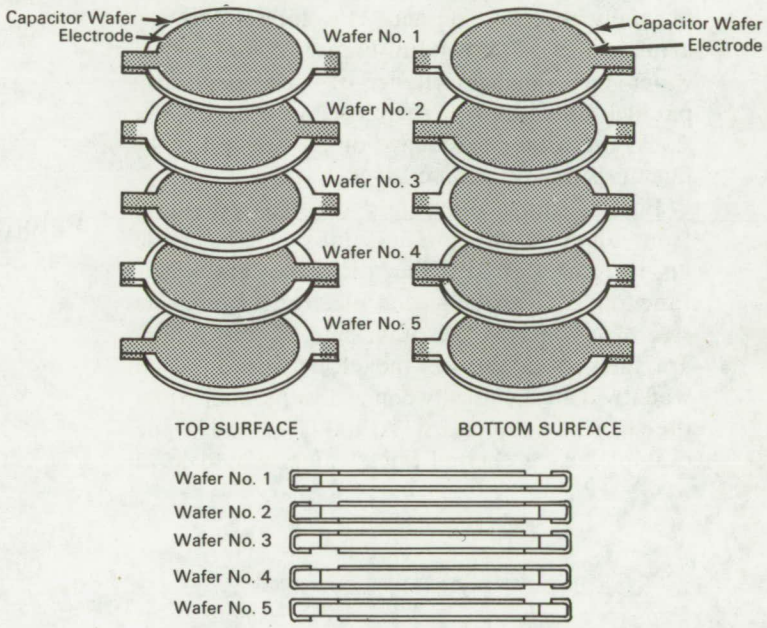
NASA TECH BRIEF

High-Temperature (1100°F) Capacitors Operate without Supplemental Cooling



MASKS USED FOR SPUTTERING ELECTRODES ON TABBED WAFERS

FIGURE I



PARALLEL INTERCONNECTION SCHEME

FIGURE 2

The problem:

To fabricate high-temperature capacitors which are compact, lightweight, and suitable for operation in a 800° to 1100°F temperature range without supplemental cooling.

The solution:

A multilayered capacitor fabricated with one-mil thick pyrolytic boron nitride and "wrap around" sputtered electrodes to achieve parallel electrical interconnections in a stacked configuration of 3 to 9 wafers.

How it's done:

Practically all fixed capacitors manufactured commercially (other than electrolytic types) are constructed by one of two general methods, stacking or rolling. The stacked approach was selected because of the characteristic brittleness of high-temperature dielectric materials.

The capacitor is fabricated as follows:

1. A one-inch square wafer of pyrolytic-boron nitride is sliced and lapped to a thickness of 1.0 mil.

(continued overleaf)

2. High purity platinum is sputtered on the pyrolytic boron nitride wafers. The electrodes are sputtered on both sides of the wafer at the same time to provide electrical continuity from the top and bottom electrodes around to the opposite side of each tab. Figure 1 shows a tabbed wafer positioned between the two masks. Proper mask to wafer registration is achieved by providing a countersunk depression in one of the masks conforming to the wafer outline. Coincident holes are drilled in the top and bottom masks to insure mask-to-mask registration.
3. The sputtered electrodes applied to each wafer are then connected so that the top electrode of wafer No. 1 is electrically connected to the bottom electrode of wafer No. 2. The bottom and top electrodes of wafers No. 1 and No. 2, respectively, are directly opposite each other and would normally come in contact. This interconnection arrangement is shown in Figure 2 for a five-wafer stack. The capacitance of each wafer is in parallel and additive; therefore, in a five-wafer stack, the total capacitance of the stack will be five times the capacitance of each wafer.

Figure 2 shows the wafers with tabs extending from opposite edges. These tabs will be made an integral part of the dielectric and their function is to extend each electrode from one side of a wafer to the other side. If the wafers are stacked as shown, the electrodes on each wafer will automatically connect in parallel when the stack is compressed. A 100-layer stack, for example, using one-mil thick wafers would have a compressed thickness only slightly in excess of 0.1 inch since the electrode thickness is negligible.

Notes:

1. The capacitors were tested in vacuum for electrical data (capacitance, dissipation factor, dc resistance) over the temperature range from room temperature to 1100°F. Measured values for this capacitor with a one-mil thick dielectric were:
   (a) Capacitance change from room temperature to 1100°F: 1.5%.
   (b) Dissipation factor at 1100°F: 0.009 (1kc/sec).
   (c) DC electric strength: room temperature—10,000 volts/mil; 1100°F—7,000 volts/mil.

   These test data indicated that the performance objectives for this capacitor could be exceeded by a substantial margin.
2. Inquiries concerning this invention may be directed to:

   Technology Utilization Officer
   Lewis Research Center
   21000 Brookpark Road
   Cleveland, Ohio 44135
   Reference: B67-10550

Patent status:

No patent action is contemplated by NASA.

Source: R. E. Stapleton
of Westinghouse Electric Corporation
under contract to
Lewis Research Center
(LEW-10324)