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Brief 67-10511

NASA TECH BRIEF

Logic Realization of Simple Majority Voting Connectives

x_1	x_2	x_3	x_1x_2	x_1x_3	x_2x_3	$x_1x_2 + x_1x_3 + x_2x_3$
0	0	0	0	0	0	0
0	0	1	0	0	0	0
0	1	0	0	0	0	0
0	1	1	0	0	1	1
1	0	0	0	0	0	0
1	0	1	0	1	0	1
1	1	0	1	0	0	1
1	1	1	1	1	1	1

Figure 1

Boolean Chart for 2-out-of-3 Majority

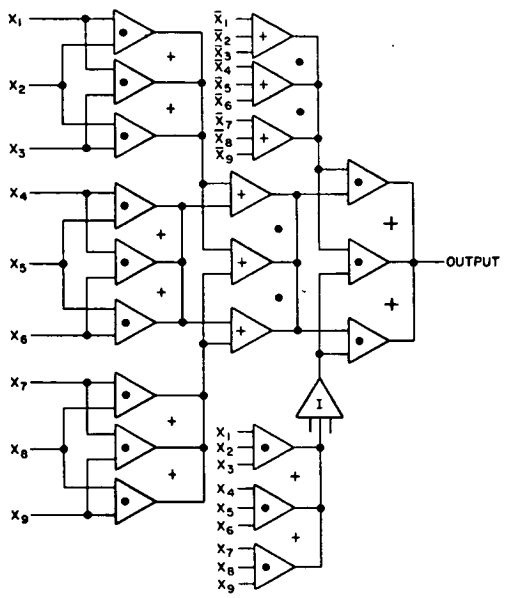

Figure 2

Detail Design of 5-out-of-9 Majority Circuit

In computer networks, an incorrect output is sometimes obtained due to a component failure, noise, or some other disturbance. To alleviate the situation, redundant circuitry is added to a network, thereby providing majority operation. In 2-out-of-3 majority circuitry, for example, any 1 of 3 circuits could give an incorrect output and yet the complete system would give the correct output.

The novelty of this approach lies in the simplicity of the circuitry used, inasmuch as only NAND gates are employed, and the modules used are among the most popular microelectronic or integrated circuits presently in use.

Figure 1 shows the simple case of 2-out-of-3 majority. The right-hand column corroborates the fact that a "true" output is obtained when at least two of the three inputs are "true".

Techniques have evolved which permit a minimum of circuits (combination of circuit elements), up to 5-out-of-9 using NAND elements, obtained through

(continued overleaf)

manipulation of the majority equations to fit the operation of the circuit elements. Minimum propagation delay through the network (elements in series) is stressed. Given nine inputs, an implementation has been devised which gives a "true" output when any five or more of the inputs are "true". Figure 2 shows a block diagram of 5-out-of-9 majority circuitry.

Note:

Inquiries concerning this invention may be directed to:

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Reference: B67-10511

Patent status:

Inquiries about obtaining rights for the commercial use of this invention may be made to NASA, Code GP, Washington, D.C. 20546.

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