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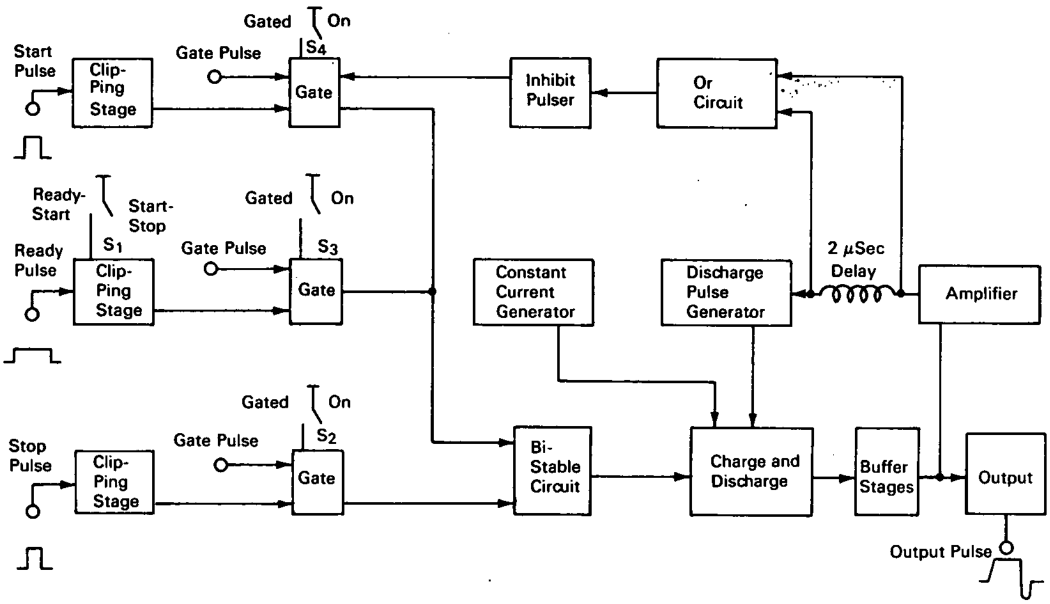
# AEC-NASA TECH BRIEF



## Solid-State Time-to-Pulse-Height Converter Developed




### The problem:

To design a circuit capable of producing an output pulse with an amplitude directly proportional to the time interval between two input pulses. A single circuit must be capable of operating under two separate and distinctly different input conditions. These conditions are:

1. Where it is desired to measure the time interval between two pulses which occur in very rapid succession. This time interval is generally of shorter duration than that of the pulse lengths themselves.
2. Where it is desired to measure the time interval between the starting point and the end point of a continuous "beam" type pulse. The circuit in this instance receives not two pulses, but one in the form of burst energy.

Commonly employed methods of obtaining time-to-pulse-height conversion require that separate circuits be used for each type of input condition.

### The solution:

A solid-state circuit which incorporates selected circuit options to achieve variable mode operation. A tunnel diode, used as a bistable element, controls the charging time of a capacitor in proportion to the time interval being measured. Time-to-pulse-height conversion is obtained for either randomly or periodically occurring pulses.

### How it's done:

The device achieves time-to-pulse-height conversion by controlling the "on" time of a bistable circuit which charges a capacitor. The voltage developed across the capacitor is thus proportional to the time

(continued overleaf)

interval. After a short time interval the capacitor is discharged so that the circuit is ready for a new conversion. The conversion is accomplished by five basic circuit functions: (1) wave shaping circuits and gates, (2) converter circuits, (3) capacitor discharge circuit, (4) start pulse inhibit circuit, and (5) isolating and output stages. The circuit permits two modes of operation: ready-start and start-stop.

The ready-start mode is used to measure the time interval between two pulses occurring at a random rate. By positioning $S_1$ in the ready-start position, the circuit turns on the bistable element whenever a start pulse appears in coincidence with a ready pulse. The ready pulse, whose duration is fixed by a delay cable, switches the bistable element off.

With $S_1$ in the start-stop position, a "ready current" is always present at the bistable circuit, and the bistable circuit is turned on by a start pulse. The circuit remains on until either stop pulse or a "negative" ready pulse is applied. This mode of operation is used for experiments where one pulse occurs at a periodic rate, i.e., pulsed beam experiments.

The wave shaping circuits and gates first shape the input pulses (start, ready, and stop) in size and duration. The start and stop pulses, which must be positive, are clipped to a duration of 7 microseconds. The ready pulse is clipped to a time longer than the true interval of interest. The start pulse is delayed so that for isochronous pulses the start pulse arrives later than the start of the ready pulse.

The capacitor discharge is controlled by the pulse generator and the charge and discharge circuitry. A normally cut off transistor amplifier is brought into conduction and discharges the capacitor after a 2 microsecond delay. The discharge current of the capacitor produces an output pulse of an amplitude directly proportional to the time interval between input pulses.

The "or" and inhibit pulser circuits close the gate to the start pulse regardless of the position of $S_4$. This is to ensure that a new start pulse will not enter when a cycle is in progress. A 2 microsecond delay line is included between the discharge pulse generator and the "or" circuit to provide a flat-topped pulse suitable for use with a multichannel pulse height analyzer.

The isolation and output section uses three cascaded emitter followers to present a very high impedance to the charging capacitor, thus minimizing capacitor leakage current and maintaining system accuracy.

## Notes:

1. Input pulses to the converter must have a rise time of less than 10 nanoseconds and an amplitude of at least 1.5 volts.
2. Ready pulses appearing at the input of the device must have a time duration greater than the time lag between the pulses under observation. This is to ensure that clipping of the ready pulse at the ready clipping line will not impair the complete coincidence condition which must occur between ready and start pulses.
3. If desired, all pulse inputs may be gated, thus reducing the duty cycle of the device. A positive pulse with an amplitude of 1.5 volts is required to open the gate.
4. Additional details contained in: *IEEE Transactions on Nuclear Science,* June 1964, pp. 399–405.
5. Inquiries concerning this innovation may be directed to:

   Office of Industrial Cooperation
   Argonne National Laboratory
   9700 South Cass Avenue
   Argonne, Illinois 60439
   Reference: B67-10053

Source: R. G. Roddick, Electronics Division, and R. J. Lynch, Physics Division
(ARG-170)

## Patent status:

Inquiries about obtaining rights for commercial use of this innovation may be made to:

Mr. George H. Lee, Chief
Chicago Patent Group
U.S. Atomic Energy Commission
Chicago Operations Office
9800 South Cass Avenue
Argonne, Illinois 60439