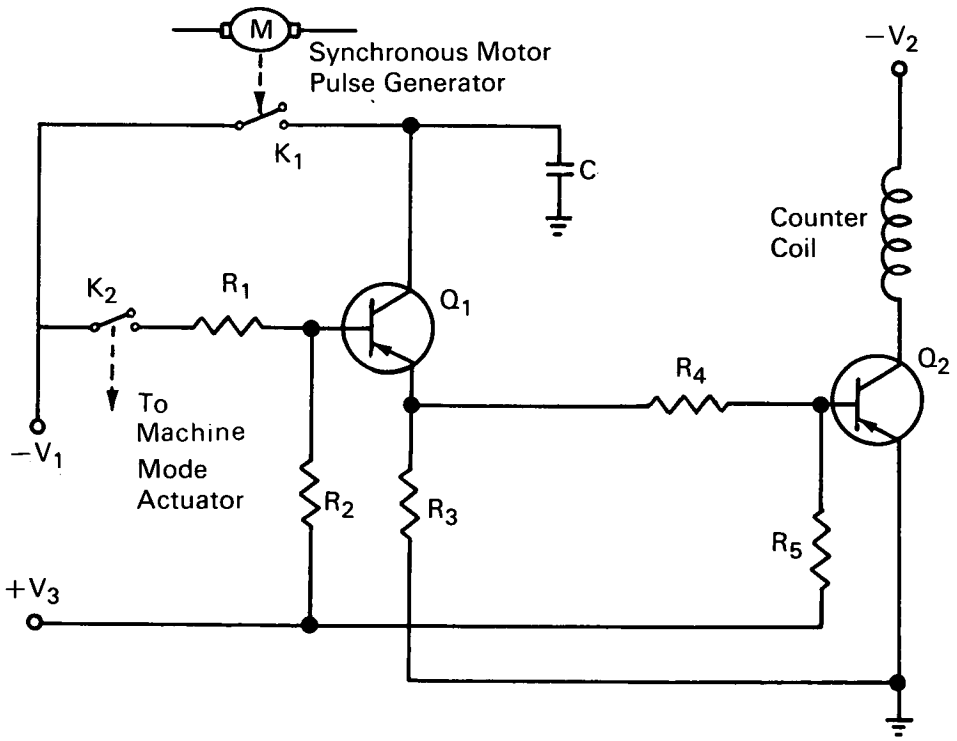
December 1966

Brief 66-10559

AEC-NASA TECH BRIEF

AEC-NASA Tech Briefs describe innovations resulting from the research and development program of the U.S. AEC or from AEC-NASA interagency efforts. They are issued to encourage commercial application. Tech Briefs are published by NASA and may be purchased, at 15 cents each, from the Clearinghouse for Federal Scientific and Technical Information, Springfield, Virginia 22151.

One-Count Memory Circuit Prevents Machine Mode Interaction



The problem:

To design an inexpensive one-count memory logic circuit to be used with electromechanical counter–printer machines which operate in either count or print mode. While the machine is in the print mode, it is desirable that the counter not be actuated to interfere with the printing process. Should a count pulse occur while the machine is in the print mode, the pulse must be stored and then transmitted as soon as the printing stops and the machine switches back to the count mode.

The solution:

A one-count memory logic circuit that advances the counter when the machine is in the count mode and provides storage for the count pulse when the machine is in the print mode. As soon as the printout is accomplished, the circuit releases the stored count pulse, and the counter advances.

How it's done:

Q_1 and Q_2 are initially biased in the nonconducting region by R_2 and R_5. The count pulse is generated by means of a synchronous motor-driven pulse generator

(continued overleaf)

which closes the contacts of K_1 for approximately 40 milliseconds once every minute. The contacts of K_2 are controlled by the mode of the machine.

When the machine is in the count mode, K_2 is closed. As K_1 closes, a count pulse of magnitude $-V_1$ turns Q_1 "on" driving the emitter negative. The negative emitter voltage of Q_1 saturates Q_2, allowing current to flow through the counter coil and to advance it one position.

When the machine is in the print-out mode, K_2 is open and Q_1 is biased "off". Should K_1 close while Q_1 is biased "off", the count pulse will charge the storage capacitor, C, to the value $-V_1$. As soon as the machine returns to the count mode, causing K_2 to close, Q_1 will turn "on" and C will discharge through Q_1, saturating Q_2 and advancing the counter one position.

Note:

Inquiries concerning this innovation may be directed to:

Office of Industrial Cooperation
Argonne National Laboratory
9700 S. Cass Avenue
Argonne, Illinois 60439
Reference: B66-10559

Patent status:

Inquiries about obtaining rights for commercial use of this innovation may be made to:

Mr. George H. Lee, Chief
Chicago Patent Group
U.S. Atomic Energy Commission
Chicago Operations Office
9800 S. Cass Avenue
Argonne, Illinois 60439

Source: B. De Forest,
Idaho Division
(ARG-90)