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NASA TECH BRIEF

Bipolar Current Driver for Memory Circuits

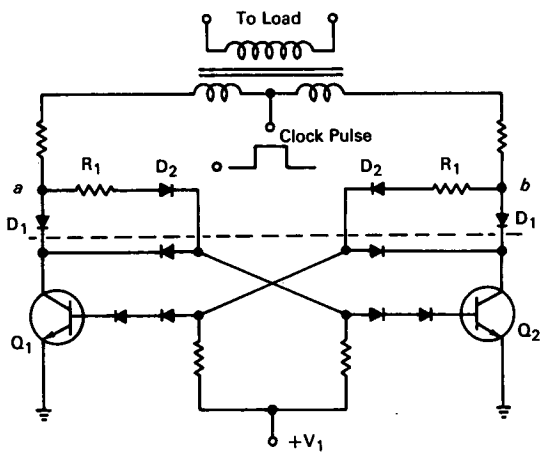

FIGURE 1

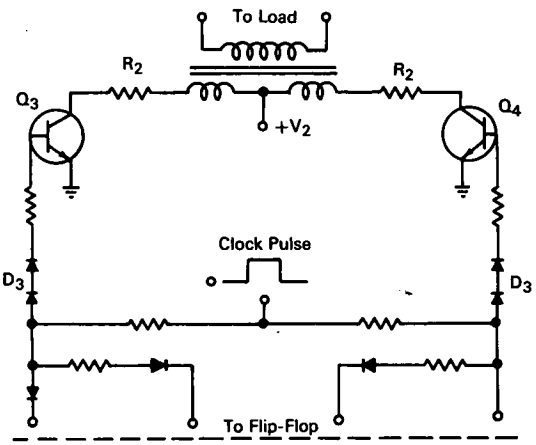

FIGURE 2

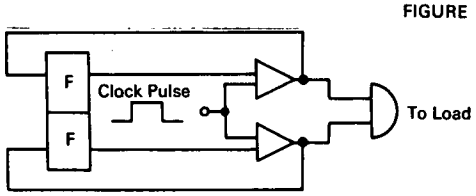

FIGURE 3

The problem:

To provide a bipolar driving current to a memory circuit, the polarity of which is determined by the state of a flip-flop. Ordinarily, the current flowing in the flip-flop is insufficient to act as a driving current since the logic circuit operates at a much lower level than is required for the driving circuit.

The solution:

A circuit which logically determines the state of a flip-flop and amplifies the current from a clock pulse flowing through the flip-flop by means of a feedback mechanism.

How it's done:

The circuit to be "read" is a standard low-current flip-flop, the portion below the dashed line in figure 1. Assume that Q_1 is conducting while Q_2 is nonconducting. With the clock pulse at ground potential, diodes D_1 and D_2 are back-biased and no current flows in the bit driver network (above the dashed line in figure 1). When a positive clock pulse is applied, the potential at node *b* increases far more than the potential at node *a* because transistor Q_1 remains in saturation. The potential at node *b* increases the forward bias of Q_1, allowing it to pass the additional current. Transistor Q_2 remains nonconducting since

(continued overleaf)

the small voltage at node *a* is insufficient to forward bias Q_2 in view of R_1 and the three diodes in the base connection. The current flowing from the clock pulse is transformer coupled to the load, and if Q_2 instead of Q_1 were conducting, a current of opposite polarity would be passed to the load. Thus the clock pulse supplies load current and steps up the operating level of the flip-flop. This circuit will provide sufficient driving current to the load if the clock pulse is of sufficient amplitude, and if the flip-flop is able to handle the additional current.

In cases in which the ratio of required load current to normal flip-flop current is very high (on the order of 10^4), a circuit such as that in figure 2 may be used. This circuit logically determines the state of the flip-flop as previously, but provides additional amplification through transistor Q_3 or Q_4. The resistors R_2 determine the collector current of the transistors, and diodes D_3 insure that either Q_3 or Q_4 will remain off.

Figure 3 illustrates the logic of operation of the circuits. The output of the "high" or "on" side of the flip-flop is amplified when the clock pulse is applied. Part of the amplified output is then fed back to the input of the flip-flop, thus increasing gain. The two outputs of the amplifiers are then appropriately connected to the load through transformer coupling.

Notes:

1. This principle may be applied to various memory driving circuits where power dissipation must be minimized.
2. One of the advantages of the type of driver illustrated in figure 1 is that fast rise times and short delays are obtained with ease because auxiliary amplifying components are not used.
3. Inquiries concerning this invention may be directed to:

   Technology Utilization Officer
   Goddard Space Flight Center
   Greenbelt, Maryland 20771
   Reference: B66-10469

Patent status:

Inquiries about obtaining rights for the commercial use of this invention may be made to NASA, Code GP, Washington, D.C. 20546.

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