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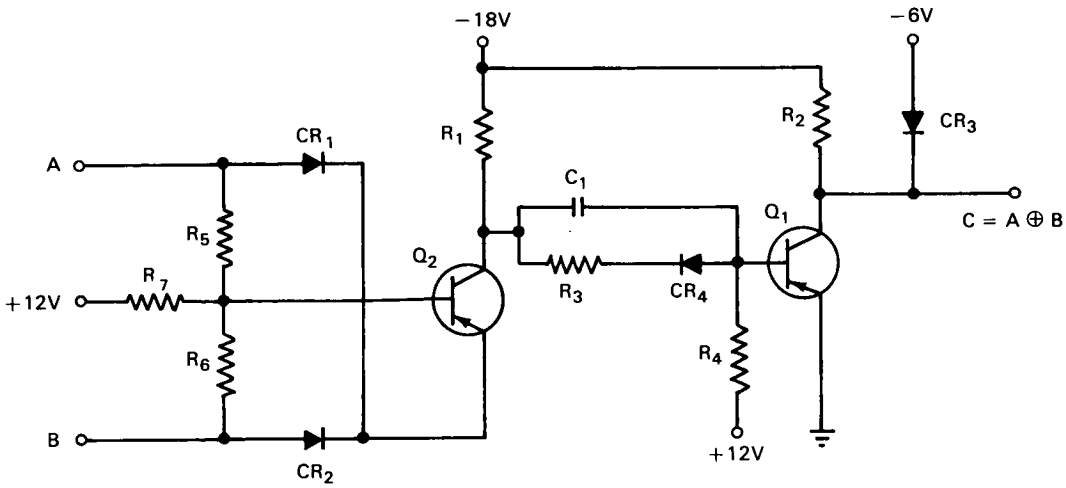
NASA TECH BRIEF

Exclusive-Or Logic Circuit Has Useful Properties



The problem:

A *Exclusive-Or* B, written A ⊕ B, is commonly implemented with conventional (*And/Or, Nor, Nand,* etc.) logic connectives. Such implementation, however, requires an excessively large number of connectives (normally five) to perform the one logic operation. Desired, therefore, is a single, simple *Exclusive-Or* connective; its proper use would substantially reduce total system hardware and number of interconnections between logic modules. The reduction is demonstrated in the familiar full adder where the sum bit S is commonly implemented with five multi-input conventional connectives; only two (two-input) *Exclusive-Or* connectives are required, however, since S can be expressed as S = A ⊕ B ⊕ C, where A, B, and C represent the augend, addend, and carry, respectively. Furthermore, the common implementation requires both assertion and negation inputs.

The solution:

The essential feature of the circuit is contained in the left portion of the figure, where CR_1, CR_2, R_5, R_6, and Q_2 are interconnected to perform the necessary switching for the *Exclusive-Or* operation. The right portion merely amplifies, restores, and inverts the signal.

How it's done:

Assume that the nominal voltages of −6 and 0 represent true and false, respectively. By examining the four input conditions, it is seen that CR_1, CR_2, R_5, R_6, and Q_2's base and emitter are interconnected so that Q_2 conducts *iff* (if and only if) either of the two inputs is true and the other is false (i.e., *iff* A ⊕ B). R_7 optimizes the input noise rejection by establishing the proper turn-on threshold of Q_2.

The relative values of R_1, R_3, and R_4 are such as to give maximum drive capability (four unit loads or

(continued overleaf)

9.6 ma) without exceeding one unit load (2.4 ma) at the input. In addition, the relative values of R_3 and R_4 are such that they maintain Q_2 in the off condition even in the presence of 2 volts noise.

Note:

Inquiries concerning this invention may be directed to:

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Langley Research Center
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Reference: B66-10272

Patent status:

Inquiries about obtaining rights for the commercial use of this invention may be made to NASA, Code GP, Washington, D.C. 20546.

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