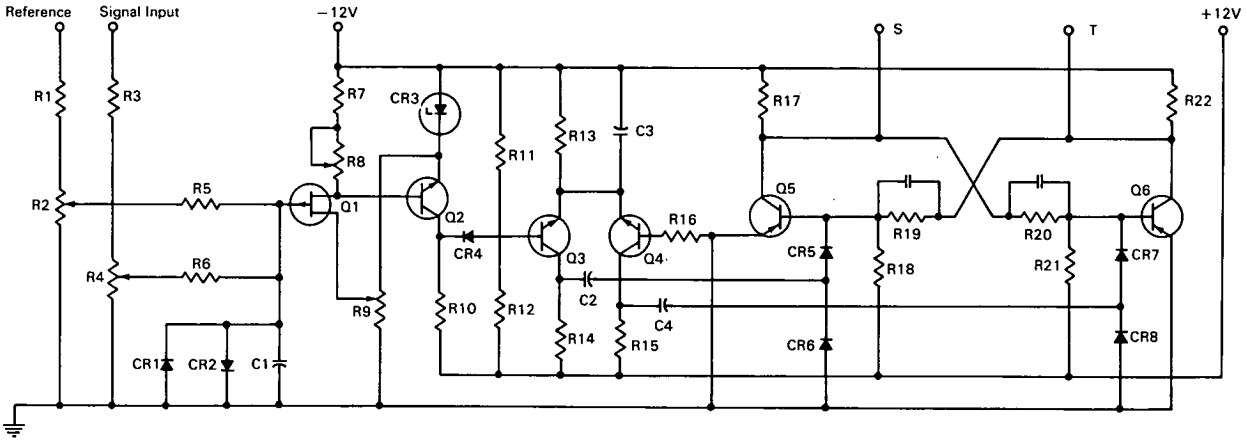
May 1966

Brief 66-10224

NASA TECH BRIEF

FET Comparator Detects Analog Signal Levels Without Loading Analog Device



The problem:

To design a voltage comparator circuit capable of detecting discrete analog computer output levels without excessively loading the output amplifier of the analog computer. The circuit must provide a digital output for analog voltages above or below a predetermined level. The cost and complexity of the circuitry must be lower than those of a conventional analog-to-digital converter.

The solution:

An FET (field effect transistor) common source amplifier to provide high input impedance and temperature stability, coupled by a differential amplifier to a bistable transistor flip-flop.

How it's done:

The circuit consists of four subsections: an input overload protection circuit (CR1 and CR2, with coupling isolation resistors, R1–R6); a high input-impedance amplifier (Q1 and Q2); a differential amplifier (Q3 and Q4); and, a bistable flip-flop (Q5 and Q6). The circuit is initially aligned by grounding the gate of Q1 and adjusting R9 until the drain of Q1 approaches −6.6 volts. Q1 is pinched off and Q2 is at cutoff. In this condition, CR4 is back biased, permitting Q3 to conduct through bias resistors R11 and R12. The voltage drop across R13 back biases Q4 and its collector goes to +12 volts. This positive-going signal is coupled through C4 and CR7 and to the base of the flip-flop transistor Q6. Q6 is turned off and Q5 is turned on. Thus the T output goes to −12 volts and the S output goes to −0.6 volt. This is the "logic 1" output condition.

The gate of Q1 sees the voltage difference between an applied reference voltage and the analog signal input. If the difference between the reference and the analog voltages is positive, Q1 remains pinched off, and the output condition of "logic 1" exists. If the difference between these voltages is negative, the

(continued overleaf)

gate voltage causes Q1 to conduct, thus allowing Q2 to become forward biased. CR4 is forward biased, driving the base of Q3 negative. Thus Q3 is cut off and Q4 is forward biased. When Q3 is cut off, its collector goes to +12 volts. A positive-going signal is coupled through C2 to CR5 and to the base of flip-flop transistor Q5. Q5 is cut off, and Q6 is turned on. Thus, output S goes to −12 volts and output T goes to −0.6 volt. This is the "logic 0" output condition.

Notes:

1. This circuit could be used to provide the initial circuits for a relay-controlled logic scheme. A group of these comparator circuits could be connected to provide a pulse-code-modulated system supplying a digital output for sinewave inputs in a binary ratio, thus forming a counter.
2. Inquiries concerning this invention may be directed to:

   Technology Utilization Officer
   Marshall Space Flight Center
   Huntsville, Alabama, 35812
   Reference: B66-10224

Patent status:

Inquiries about obtaining rights for the commercial use of this invention may be made to NASA, Code GP, Washington, D.C., 20546.

Source: H. L. Wallace
of General Electric Company
under contract to
Marshall Space Flight Center
(M-FS-503)