NASA TECH BRIEF

Simple Circuit Performs Binary Addition and Subtraction

Register A

Clock Pulses

"And" Gates

Register B
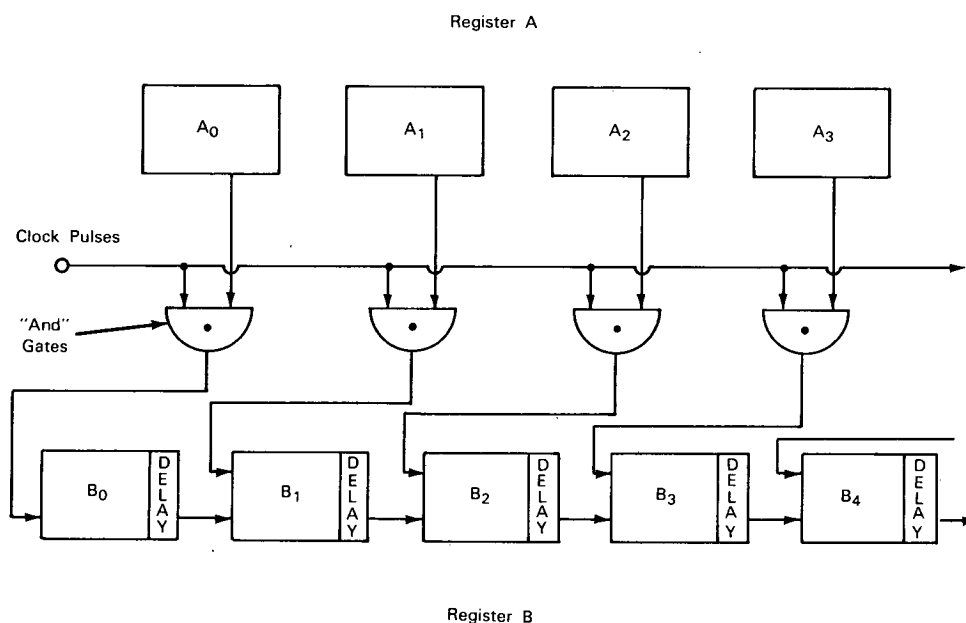
The problem: To reduce the number of logic circuits required to perform binary addition and subtraction. Previous methods have used separate units called adders or subtractors and have the disadvantages of excessive weight, circuit complexity, and high power drain.

The solution: A ripple adder that uses dual-input and delayed-output flip flops in one register. The contents of this register are summed with those of a standard register through conventional AND gates.

How it's done: The ripple adding circuit adds the contents of registers A and B and places the sum in register B. The flip flops that comprise register B

have been modified by the addition of a second input trigger and an output pulse delay.

With a binary "1" stored in a stage of register A, the clock pulse passes through the AND gate corresponding to that stage and triggers the input of the corresponding stage of register B. For addition, register B is designed to give an output pulse on the "1"-to-"0" transition. This output pulse is delayed from the input of the next stage to permit the contents of register A to be transferred before the ripple pulses travel through register B. For subtraction, register B is designed to produce an output pulse on the "0"-to-"1" transition, and the circuit subtracts the contents of register A from the contents of register B.

Notes:

1. This circuitry may be of interest to manufacturers of small computing equipment such as desk-top calculators.

2. Inquiries concerning this invention may be directed to:

> Technology Utilization Officer
> Goddard Space Flight Center
> Greenbelt, Maryland, 20771
> Reference: B65-10355

Patent status: NASA encourages the immediate commercial use of this invention. Inquiries about obtaining rights for its commercial use may be made to NASA, Code AGP, Washington, D.C., 20546.

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