November 1965

Brief 65-10334

NASA TECH BRIEF

Frequency Divider Is Free of Spurious Outputs

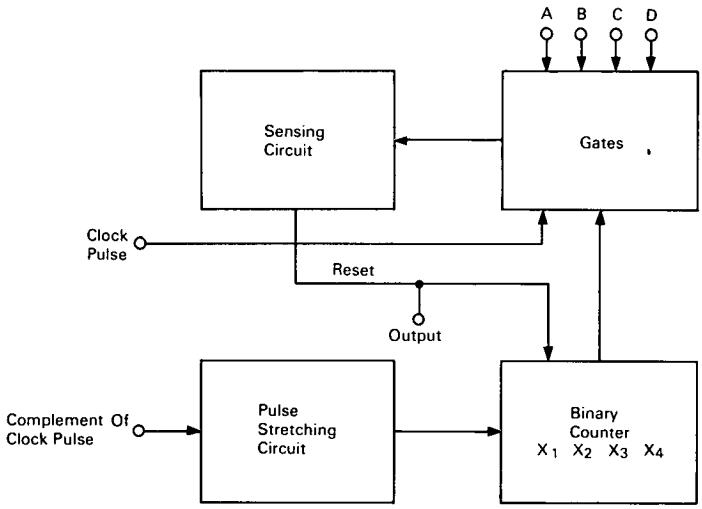

FIGURE 1

Input D C B A	No. Of States	Output $X_1 X_2 X_3 X_4$
1 1 1 1	1	0 0 0 0
1 1 1 0	2	0 0 0 1
1 1 0 1	3	0 0 1 0
1 1 0 0	4	0 0 1 1
1 0 1 1	5	0 1 0 0
1 0 1 0	6	0 1 0 1
1 0 0 1	7	0 1 1 0
1 0 0 0	8	0 1 1 1
0 1 1 1	9	1 0 0 0
0 1 1 0	10	1 0 0 1
0 1 0 1	11	1 0 1 0
0 1 0 0	12	1 0 1 1
0 0 1 1	13	1 1 0 0
0 0 1 0	14	1 1 0 1
0 0 0 1	15	1 1 1 0
0 0 0 0	16	1 1 1 1

FIGURE 2

The problem: To design a compact, stable frequency divider that will provide 16 output states from only 4 input circuits. The output must be free of spurious pulses related to triggering and resetting of the binaries.

The solution: A system of integrated circuits that count the number of input pulses and provide a positive-going output pulse for a selected number of inputs.

How it's done: The divider consists of 4 main circuits: a pulse stretching circuit, a counter, a set of gates, and a sensing circuit. The pulse stretching circuit makes the negative going transient of the complement of clock pulse occur at a later time than the positive going transient of the clock pulse. Thus the counter is reset to zero before the completion of a given number of states, determined by the amount of stretching of the complement of clock pulse. This prevents spurious pulses that might occur at the output of the binaries due to trying to trigger the binaries to the next state and reset them to zero at the same time. The counter functions as any binary counter and the gates combine any selected combination of binary outputs with the clock pulse to trigger the sensing circuit, which is essentially a one-shot monostable multivibrator. The sensing circuit delays application of the reset pulse until the negative going transient from the gate occurs and also extends the duration of the reset pulse a sufficient time to insure that all binaries are reset to zero. Figure 2 illustrates the mode of system operation. If the input is made 1111, X_1, X_2, X_3, and X_4 all remain at zero. If an input corresponding to a larger number of output states is selected, the output states will occur in order as illustrated. For example, if the input corresponding to 10 states is selected and the device set to zero, the output will proceed to 1001, reset to 0000 and then count to 1001 again. This will be repeated until the input is changed.

(continued overleaf)

Notes:

1. Only 4 inputs are required for a 16-state system instead of 7 as in previous devices.
2. The input is binary coded. When the unit is set to zero and allowed to count to a given output state, the output states also occur in ascending order in a binary code.
3. For any change of one in the input, the number of output states is only changed by one.
4. Inquiries concerning this invention may be directed to:

   Technology Utilization Officer
   Goddard Space Flight Center
   Greenbelt, Maryland, 20771
   Reference: B65-10334

Patent status: NASA encourages the immediate commercial use of this invention. Inquiries about obtaining rights for its commercial use may be made to NASA, Code AGP, Washington, D.C., 20546.

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