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# Transistorized Circuit Clamps Voltage With 0.1\% Error 



The problem: To apply two accurately clamped voltage levels ( +18 or 0 volts) to the input of a digital-to-analog resistive matrix that binarily develops a deflection staircase.
The solution: A transistorized clamping circuit that clamps either of two voltage levels ( +18 or 0 volts) with less than 0.1 percent voltage offset.
How it's done: When a positive 5.5 -volt level is applied to the base of transistor $\mathrm{Q}_{1}$ through resistor $\mathrm{R}_{1}$, transistor $\mathrm{Q}_{1}$ is driven into saturation. In this state, the collector-emitter voltage of transistor $Q_{1}$ is
approximately 30 millivolts and is relatively independent of temperature. The output of transistor $Q_{1}$ is applied directly to the digital matrix and to the base of transistor $\mathrm{Q}_{2}$ through resistor $\mathrm{R}_{3}$. This holds transistor $\mathrm{Q}_{2}$ at cutoff, which in turn keeps transistor $\mathrm{Q}_{3}$ (operating as an "inverted-mode" switch) biased off.

When a zero-volt level is applied to the base of transistor $\mathrm{Q}_{1}$ through resistor $\mathrm{R}_{1}$, transistor $\mathrm{Q}_{1}$ is biased off. Transistor $\mathrm{Q}_{2}$ is driven into saturation by current from the 24.5 -volt supply through resistors $\mathrm{R}_{2}$ and $\mathrm{R}_{3}$. The output of transistor $\mathrm{Q}_{2}$ turns transistor

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Q3 on and allows the 18 -volt supply to be applied through transistor Q3 to the digital matrix. The col-lector-emitter voltage in transistor $\mathrm{Q}_{3}$ is approximately 5 millivolts.

## Notes:

1. Whereas ideal output levels are 18.0 volts and 0.0 volt, actual performance obtainable is 18.005 volts $\pm 5 \mathrm{mv}$, and 0.030 volt $\pm 15 \mathrm{mv}$.
2. Although the speed of operation of this clamping circuit technique is limited by the charge storage in transistor $\mathrm{Q}_{1}$, it may be useful for analog, digital, and hybrid circuit applications.
3. Inquiries concerning this invention may be directed to:

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Patent status: NASA encourages the immediate commercial use of this invention. Inquiries about obtaining rights for its commercial use may be made to NASA, Code AGP, Washington, D.C., 20546.

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