

April 1965

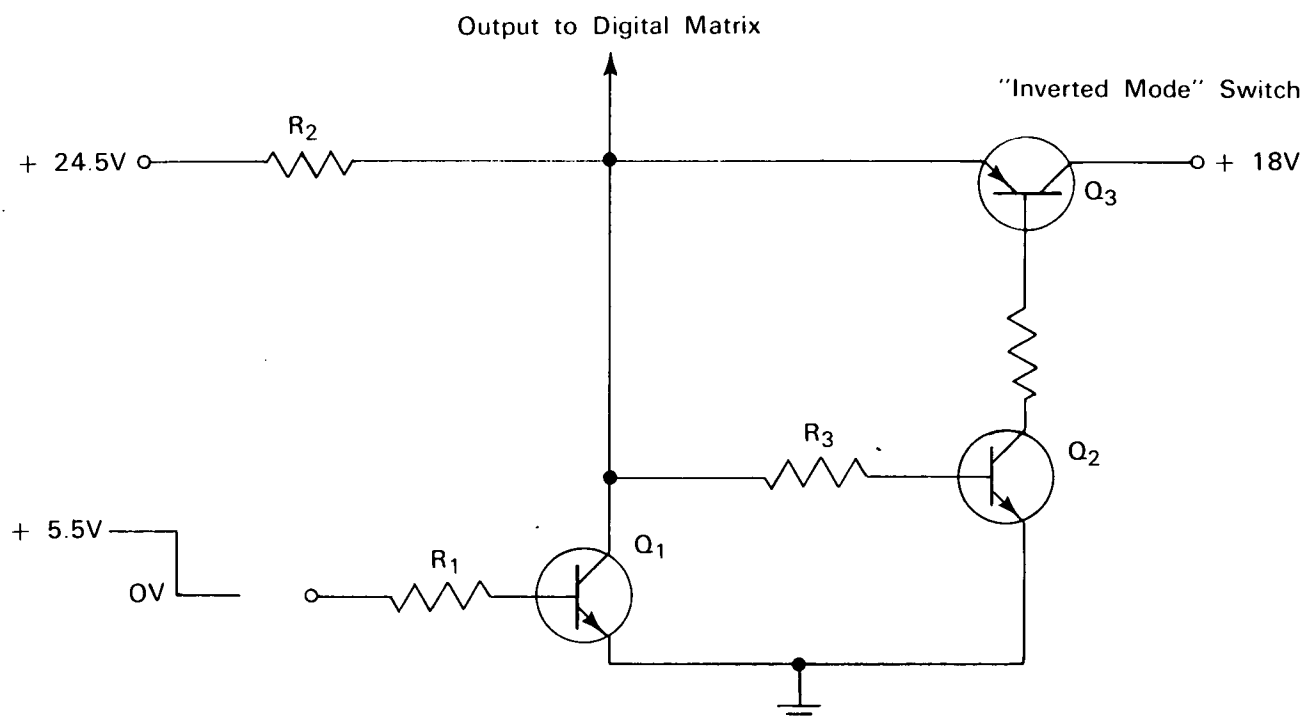
Brief 65-10118

NASA TECH BRIEF



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Transistorized Circuit Clamps Voltage With 0.1% Error



The problem: To apply two accurately clamped voltage levels (+18 or 0 volts) to the input of a digital-to-analog resistive matrix that binarily develops a deflection staircase.

The solution: A transistorized clamping circuit that clamps either of two voltage levels (+18 or 0 volts) with less than 0.1 percent voltage offset.

How it's done: When a positive 5.5-volt level is applied to the base of transistor Q₁ through resistor R₁, transistor Q₁ is driven into saturation. In this state, the collector-emitter voltage of transistor Q₁ is

approximately 30 millivolts and is relatively independent of temperature. The output of transistor Q₁ is applied directly to the digital matrix and to the base of transistor Q₂ through resistor R₃. This holds transistor Q₂ at cutoff, which in turn keeps transistor Q₃ (operating as an "inverted-mode" switch) biased off.

When a zero-volt level is applied to the base of transistor Q₁ through resistor R₁, transistor Q₁ is biased off. Transistor Q₂ is driven into saturation by current from the 24.5-volt supply through resistors R₂ and R₃. The output of transistor Q₂ turns transistor

(continued overleaf)

Q₃ on and allows the 18-volt supply to be applied through transistor Q₃ to the digital matrix. The collector-emitter voltage in transistor Q₃ is approximately 5 millivolts.

Notes:

1. Whereas ideal output levels are 18.0 volts and 0.0 volt, actual performance obtainable is 18.005 volts ± 5 mv, and 0.030 volt ± 15 mv.
2. Although the speed of operation of this clamping circuit technique is limited by the charge storage in transistor Q₁, it may be useful for analog, digital, and hybrid circuit applications.

3. Inquiries concerning this invention may be directed to:

Technology Utilization Officer
Goddard Space Flight Center
Greenbelt, Maryland, 20771
Reference: B65-10118

Patent status: NASA encourages the immediate commercial use of this invention. Inquiries about obtaining rights for its commercial use may be made to NASA, Code AGP, Washington, D.C., 20546.

Source: Radio Corporation of America,
under contract to Goddard Space Flight Center
(GSFC-196)