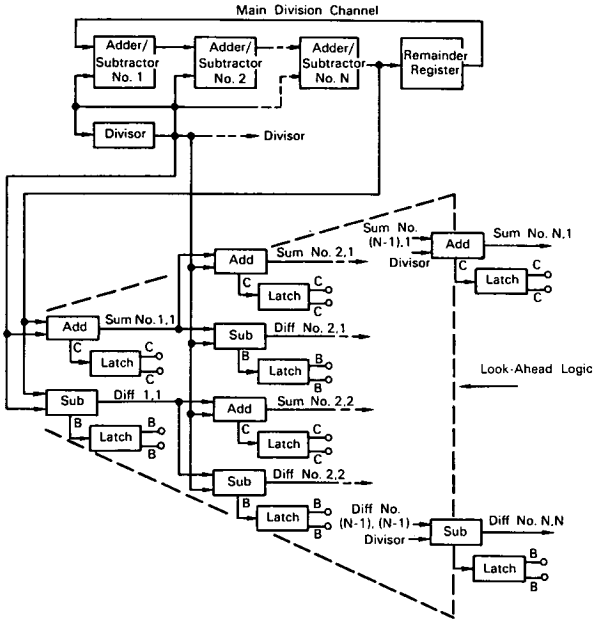
February 1965

Brief 65-10005

NASA TECH BRIEF

Computer Modification Reduces Time of Performing Iterative Division



The problem: Reducing the time required to perform iterative division. The division process is one of the most complex and time-consuming internal operations of a computer. In iterative division, successive additions or subtractions are performed between the divisor and dividend remainder, depending upon the sign relationship between the preceding remainder and divisor. Conventionally, this process requires one computer cycle per quotient bit because the sign of the remainder is the last item to be determined from the preceding iteration.

The solution: A serial-by-parallel divider employing a look-ahead feature that predetermines the sign relationships of several iterations before the computer cycle begins. Thus, several add/subtract decisions can be made and implemented in one computer cycle.

How it's done: The block diagram presents a serial-by-parallel divider with an N-iteration look-ahead logic configuration. Timing-signal lines, the quotient register, and the command control lines between the look-ahead logic section and the adder/subtractors are omitted for simplicity. The look-ahead logic section is a branching configuration of adders and subtractors. The divisor and the dividend remainder information bits pass through all the adders and subtractors with no delay or interim storage other than the inherent delay encountered in circuit components. Only the carry (C) and the borrow (B) conditions of the most significant bit are retained in latches at each branching level. These carry and borrow conditions at each level uniquely describe the sign relation between the divisor and the remainder

(continued overleaf)

for the associated iteration and are employed to preset the appropriate adder/subtractor in the main division channel.

Notes:

1. Any number of iterative divisions can be made in only one computer cycle using this method. However, the number of components required would be prohibitive for more than a three- or four-iteration look-ahead, because the branching increases geometrically for each decision level that is introduced.
2. This method can be employed in any data handling system in which high-speed division must be performed in a serial arithmetic unit.
3. Inquiries concerning this innovation may be directed to:

   Technology Utilization Officer
   Marshall Space Flight Center
   Huntsville, Alabama, 35812
   Reference: B65-10005

Patent status: NASA encourages commercial use of this innovation. No patent action is contemplated.

Source: International Business Machines Corp. under contract to Marshall Space Flight Center (M-FS-166)