A Simple and Effective Approach to Improve the Output Linearity of Switched-Current AMOLED Pixel Circuitry

Xiaojun Guo and S. R. P. Silva

***Abstract*—Switched-current (S-I)-type pixel circuits are widely studied for high-performance active-matrix organic light-emitting -diode displays but suffer significant sampling and hold (S/H) nonidealities. In this letter, a simple and effective capacitive compensation method is proposed to suppress the S/H nonidealities and, thus, to greatly improve the current-reproducing accuracy and the output linearity of the circuits. The analysis procedure clearly demonstrates the operation mechanism of the method, and the simulation results of Simulation Program with Integrated Circuit Emphasis prove its excellent applicability for S-I pixel circuits.**

***Index Terms*—Active-matrix, current-mode, organic light-emitting diode (OLED), sampling and hold, switched-current (SI), thin-film transistor (TFT).**

I. Introduction

With further advances of organic light-emitting-diode (OLED) display technologies toward even higher image quality, higher efficiency, lower power consumption, and larger size, the active-matrix architecture, which integrates OLEDs with thin-film-transistor (TFT) circuits in each display pixel, has become the technology of choice [1]. Compared with the voltage-mode driving methodology, the current-mode one has advantages such as improved display spatial uniformity, good environmental immunity, excellent linearity, and proven long-term stability [2], and thus, it is preferred for high-performance active-matrix OLEDs (AMOLEDs). To realize current-mode AM driving, the switched-current (S-I)-type pixel circuits were developed to control and drive the OLED elements [3], [4]. The long-time and signal-dependent settling problems in the S-I pixel circuits can be solved to meet the video bandwidth requirements by using current-scaling [5], [6], current-feedback [7], or hybrid driving approaches [2]. However, the S-I pixel circuits are based on the sampling and hold (S/H) operations and, thus, suffer the S/H nonidealities, which depend on the circuit's parameters and the input signal level [8]. The resultant signal-dependent S/H errors can deteriorate the current-reproducing accuracy and the output linearity of the circuits. In this letter, a simple and effective capacitive compensation method is proposed and analyzed to suppress the S/H nonidealities.

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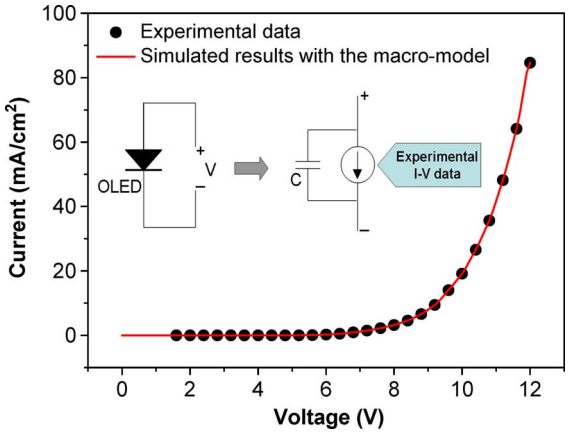

Fig. 1. OLED model current–voltage characteristics obtained via a macro-modeling approach [11] being fitted to the experimentally measured results of an inverted top-emitting OLED structure [10] used in this letter.

II. Simulation Setup

To analyze and verify the proposed design, Simulation Program with Integrated Circuit Emphasis (SPICE) circuit simulations with the commercial circuit simulator HSPICE vended by Synopsys are performed [9]. The electrical characteristics of an efficient inverted top-emitting OLED structure [10] are integrated into the SPICE simulations by using a macromodeling approach [11], which models the current–voltage characteristics by directly specifying the experimentally measured data points with the 1-D piecewise linear function in SPICE [9], as shown in Fig. 1. Because the experimental data are directly input into the model, the model can reproduce the real electrical characteristics of the device with no deviations.

The basic configuration of an n-type TFT S-I pixel circuit is shown in Fig. 2(a), which is designed for the inverted top-emitting OLED structures. Adopting top-emitting OLED structures removes limitations in the optical transparency of backplanes and the filling factor of traditional bottom-emitting OLED pixels. The inverted OLED structure technology is also somewhat preferred because for amorphous-silicon (a-Si) TFTs, which are often used in large-scale AMOLEDs where only n-type transistors are available, lower power can be achieved, while for polycrystalline silicon (poly-Si) TFTs, n-type TFTs usually have higher carrier mobility and, thus, lower operation voltage [12]. In the following, this n-type poly-Si TFT pixel circuit for the inverted OLED structure, as shown in Fig. 2(a), will be taken as an example for the analysis. Furthermore, due to similar operation mechanisms, the analysis procedure is also applicable for the a-Si TFT pixel

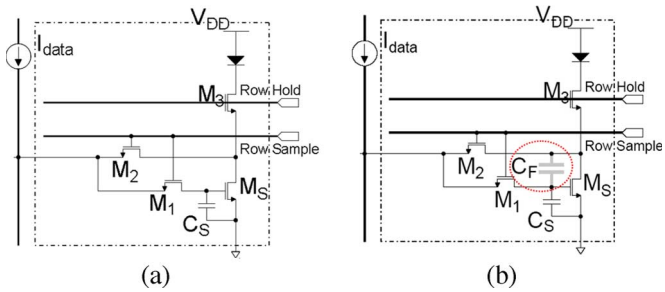

Fig. 2. (a) n-Type poly-Si TFT S-I pixel circuit for inverted top-emission OLED structures. (b) Circuit configuration showing the addition of the compensation capacitance C_F in the n-type TFT pixel circuit.

circuits, and also for the p-type TFT pixel circuits [13], which are designed for normal top-emitting OLED structures. The poly-Si TFT simulation model parameters are extracted based on the widely accepted Rensselaer Polytechnic Institute poly-Si TFT model [9] from the measurements. Values of the two main parameters—threshold voltage $(V_{\rm th})$ and effective carrier mobility $(\mu_{\rm eff})$—are the following: $V_{\rm th} = 1.25$ V and $\mu_{\rm eff} = 128\ {\rm cm}^2/{\rm V}\cdot{\rm s}$. The storage-capacitor value (C_S) is 0.2 pF. The channel width and length of the TFTs are the following: $(W/L)_{\rm MS} = 10\ \mu{\rm m}/15\ \mu{\rm m}$, $(W/L)_{M1,M2} = 20\ \mu{\rm m}/5\ \mu{\rm m}$, and $(W/L)_{M3} = 20\ \mu{\rm m}/10\ \mu{\rm m}$. The whole pixel area is $100 \times 300\ \mu{\rm m}$.

III. Analysis and Discussions

The operation of the SI pixel circuits can be divided into two phases: sampling and hold. For the circuit, as shown in Fig. 2(a), during the sampling phase, the video signal is converted to a current signal $I_{\rm data}$, then it is sampled into the current-sink transistor (M_S) during row selection; during the hold phase, M_S reproduces and holds the current signal to drive the lighting element. Theoretically, the modulated OLED current $I_{\rm OLED}$ is equal to the input data current. However, in a realistic case, the finally modulated emission current $I_{\rm OLED}$ is given by [8]

$$I_{\rm OLED} = \left(\sqrt{I_{\rm data}} - \sqrt{\beta_{M_S}}\cdot\Delta V_{\rm gs}^{M_S}\right)^2 + \lambda\cdot\Delta V_D^{M_S} \quad (1)$$

where β_{M_S} is the transconductance factor of M_S; $\Delta V_{\rm gs}^{M_S}$ and $\Delta V_D^{M_S}$ are, respectively, M_S's gate stored voltage and the drain voltage shift that occurs when the pixel operation changes from the sampling phase to the hold phase; and λ is a constant associated with the channel-length modulation and the kink effects of the poly-Si TFTs.

Equation (1) shows that the presence of $\Delta V_{\rm gs}^{M_S}$ and $\Delta V_D^{M_S}$ may cause deviation of $I_{\rm OLED}$ from $I_{\rm data}$. By using a long-channel TFT, λ can be minimized, and thus, the effects from $\Delta V_D^{M_S}$ may be suppressed. Moreover, the main problem for the pixel circuit that causes the deviation of $I_{\rm OLED}$ from $I_{\rm data}$ is $\Delta V_{\rm gs}^{M_S}$ due to charge injection and clock feed-through effects of M_1. In normal S/H circuit design, such switch effects are possible to be partially cancelled by using large storage capacitance (C_S), by adding a dummy transistor [14], or by using a CMOS transmission gate instead of the n-type TFT switch

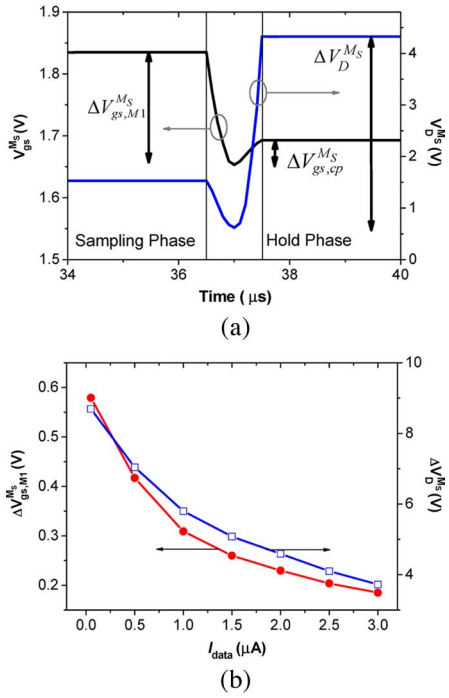

Fig. 3. (a) Variations of the M_S's gate-source voltage $V_{\rm gs}^{M_S}$ and drain-source voltage $V_D^{M_S}$ when the pixel circuit in Fig. 2(a) shifts from sampling phase to hold phase ($I_{\rm data} = 2.5\ \mu$A): $\Delta V_{{\rm gs},M_1}^{M_S}$ is the falling part due to the charge injection and clock feed-through effects on M_1, $\Delta V_{\rm gs,cp}^{M_S}$ is the rising part due to M_S's drain-to-gate coupling, and $\Delta V_D^{M_S}$ is M_S's drain-source voltage variation. (b) Similar variation trends of $\Delta V_{{\rm gs},M_1}^{M_S}$ and $\Delta V_D^{M_S}$ with an increase of $I_{\rm data}$ for the pixel circuit.

[15]. However, in the pixel circuit design, the dimension of C_S is limited by the pixel layout area, and large C_S may also slow the sampling operation. In addition, both the latter two methods increase the pixel complexity with the addition of a TFT and with the additional input pulse signals.

In this letter, a simple approach by adding a small compensation capacitance C_F between M_S's gate and drain is introduced to solve this problem, as shown in Fig. 2(b). The operation of this method is explained as follows.

As shown in Fig. 3(a), $\Delta V_{\rm gs}^{M_S}$ is composed of two parts: the falling part $\Delta V_{{\rm gs},M_1}^{M_S}$ due to the charge injection and clock feed-through effects on M_1 and the rising part $\Delta V_{\rm gs,cp}^{M_S}$ due to M_S's drain-to-gate capacitive coupling. When the pixel circuit operation changes from the sampling phase to the hold phase, the increase of $V_D^{M_S}$ will be coupled to the gate with the parasitic drain–gate capacitance $C_{\rm gd}$ and, thus, will cause an increase of $V_{\rm gs}^{M_S}$ with a certain amount of $\Delta V_{\rm gs,cp}^{M_S}$, which can be expressed as

$$\Delta V_{\rm gs,cp}^{M_S} = \frac{\Delta V_D^{M_S}\cdot C_{\rm gd}}{C_S + C_{\rm gd}} \quad (2)$$

where $C_{\rm gd}$ is the total capacitance between M_S's gate and drain.

Fig. 3(b) shows the signal dependence of both $\Delta V_D^{M_S}$ and $\Delta V_{{\rm gs},M_1}^{M_S}$ and also their similar change trends with the increase of input data current. Since $\Delta V_{\rm gs,cp}^{M_S}$ is proportional to $\Delta V_D^{M_S}$, if choosing a suitable $C_{\rm gd}$ with a given C_S, $\Delta V_{\rm gs,cp}^{M_S}$ can effectively counteract $\Delta V_{{\rm gs},M_1}^{M_S}$ over the whole range of $I_{\rm data}$.

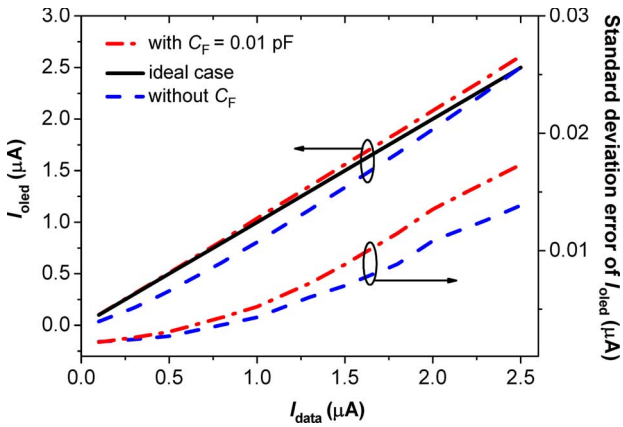

Fig. 4. Plots showing the greatly improved current-reproducing accuracy and output linearity of the S-I pixel circuit with the addition of a C_F of 0.01 pF between M_S's gate and drain. The obtained $I_{\rm OLED}$ standard-deviation error values of the pixel circuit with and without the addition of a C_F show the presence of C_F that does not cause much degradation of $I_{\rm OLED}$'s uniformity.

For the self-aligned TFT technology used in this letter, the gate-to-drain overlap capacitance is nearly zero. If we add a larger compensation capacitance C_F between the gate and the drain of M_S, then there will be $C_{\rm gd} \approx C_F$. Therefore, it is possible to control the value of $\Delta V_{\rm gs,cp}^{M_S}$ through modulating C_F, so that $\Delta V_{{\rm gs},M_1}^{M_S}$ might be effectively reduced over the whole range of $I_{\rm data}$.

The value of C_F is determined based on (2) and the ratio between the $\Delta V_D^{M_S}$ and the $\Delta V_{{\rm gs},M_1}^{M_S}$, as shown in Fig. 3(b). With $C_S = 0.2$ pF, a C_F of 0.01 pF is chosen to make $C_{\rm gd}/(C_S + C_{\rm gd}) \approx 1/20$; thus, $\Delta V_{\rm gs,cp}^{M_S}$ can roughly counteract $\Delta V_{{\rm gs},M_1}^{M_S}$ over the whole range of $I_{\rm data}$. Fig. 4 shows the simulated OLED current $I_{\rm OLED}$ as a function of the input data current $I_{\rm data}$ without C_F and with a C_F of 0.01 pF, respectively. Due to the signal-dependent S/H nonidealilities, the actual $I_{\rm OLED}$ versus $I_{\rm data}$ characteristics of the conventional S-I pixel circuit without adding a C_F present a significant linearity error compared to the ideal case.

By adding a C_F of 0.01 pF between M_S's gate and drain, the S/H nonidealilities are effectively suppressed, thus greatly improving the current-reproducing accuracy and the output linearity of the pixel circuit. C_F can be easily fabricated by using the gate and the drain of M_S as the two electrodes, and its value is much smaller than that of the C_S, which is 0.2 pF in this letter. Furthermore, this method does not need to use a large C_S to reduce the $\Delta V_{\rm gs}^{M_S}$, and the final overall area for capacitors can be smaller than that in conventional design. Therefore, the pixel aperture ratio and resolution will not be affected with the addition of a C_F. The ratio of C_F to C_S provides another adjustable parameter for optimizing the pixel circuit with given design specifications.

The effects of adding a C_F on the modulated OLED current $(I_{\rm OLED})$ uniformity of the S-I pixel circuit are also examined. To predict the $I_{\rm OLED}$'s uniformity influenced by the device process, Monte Carlo statistical circuit analysis was performed. In the analysis, Gaussian statistical distribution functions are adopted for modeling fluctuations of all related process and device parameters in the circuit [12]. Twenty percent of relative variations is assumed for the device physical model parameters including threshold voltage $(V_{\rm th})$ and effective carrier mobility $(\mu_{\rm eff})$. Ten percent of relative variations is assumed for the process-induced fluctuations including device length and width (W, L), gate oxide thickness $(t_{\rm ox})$, and capacitor values (C_S and C_F). Fig. 4 shows the standard deviation error of $I_{\rm OLED}$ obtained from the Monte Carlo analysis results. It can be seen that, although the presence of C_F contributes one more parameter influenced by the process variations, it does not cause much degradation of $I_{\rm OLED}$'s uniformity.

IV. Conclusion

A simple and effective method is introduced to suppress the S/H nonidealities in S-I pixel circuits by adding a small compensation capacitance for designing high-performance AMOLEDs. With this method, the pixel circuits do not need to use large-size storage capacitor and complicated circuit configurations. The simulation results show the current-copying accuracy, and the output linearity is greatly improved with little degradation of current uniformity via using such a method. The method is applicable for both n-TFT and p-TFT S-I pixel circuits for the inverted and normal top-emission OLED structures. Some other configurations of S-I AMOLED pixel circuits with S/H operations may also benefit from this method.

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