Improving Switching Performance of Thin-Film Transistors in Disordered Silicon

Xiaojun Guo, Tomoyuki Ishii, and S. R. P. Silva

***Abstract*—The silicon integrated electronics on glass or plastic substrates attracts wide interests. The design, however, depends critically on the switching performance of transistors, which is limited by the quality of silicon films due to the materials and substrate process constraints. Here, the ultrathin channel device structure is proposed to address this problem. In a previous work, the ultrathin channel transistor was demonstrated as an excellent candidate for ultralow power memory design. In this letter, theoretical analysis shows that, for an ultrathin channel transistor, as the channel becomes thinner, stronger quantum confinement can induce a marked reduction of OFF-state leakage current ($I_{\rm OFF}$), and the subthreshold swing (S) is also decreased due to stronger control of channel from the gate. Experimental results based on the fabricated nanocrystalline silicon thin-film transistors prove the theoretical analysis. For the 2.0-nm-thick channel devices, $I_{\rm ON}/I_{\rm OFF}$ ratio of more than 10^{11} can be achieved, which can never be obtained for normal thick channel transistors in disordered silicon.**

***Index Terms*—Leakage current, nanocrystalline silicon, subthreshold swing, thin-film transistor, ultrathin channel.**

I. Introduction

THERE IS a rapidly growing interest in building silicon integrated electronics on arbitrary substrates like glass or plastics to achieve seamless monolithic integration of human interface devices (displays or sensors) with the driving circuitry, signal processing integrated circuits, memories, and other related functional units [1]–[3]. Whether digital or analog, these integrated electronics depend critically on the current flowing in the basic elements—transistors, in normally off or subthreshold regime of operation. A low leakage current ($I_{\rm OFF}$) and a steep subthreshold swing (S) standing for high switching performance are required to achieve high transconductance, and these enable a low voltage swing to achieve the required on–off current ratio ($I_{\rm ON}/I_{\rm OFF}$) for high-speed and low power consumption [4]. However, the quality of the silicon films being achieved on these substrates is severely constrained by materials and substrate process limitations, resulting in amorphous and nano- or microcrystalline materials [5], [6]. The disorder in the material introduces a wide range of defects in the bandgap, which range from states caused by bond angle and bond length variations, coordination defects in amorphous materials, and grain boundary defects in microcrystalline materials [7], severely degrading the transistor's switching performance. First, carrier transport occurs via hopping or tunneling between states, leading to low effective mobility and, thus, low ON-state current [8]. Second, the presence of defects in the semiconductor layers leads to a decreasing effect of gate voltage on the surface potential, which in turn induces large S value [9]. Third, the trap states in the bandgap may assist the generation of carriers at the drain junction via thermionic emission or thermionic field emission of carriers, thus causing anomalous large leakage current [10]. In a previous work, the ultrathin channel transistor was demonstrated as an excellent candidate for ultralow power memory design [11]. In this letter, theoretical analysis and experimental results show that, for transistors in disordered silicon, using an ultrathin channel can contribute to steep S and exponentially decreased $I_{\rm OFF}$, potentially for high switching performance.

II. Basic Principles

As theoretically predicted and also experimentally observed [12]–[14], when the silicon film thickness ($t_{\rm Si}$) is reduced to a few nanometers, quantum confinement would result in modulation of the band structure, which gives rise to band-edge shifts in both the conduction- and valence-band minima relative to bulk silicon, thereby effectively increasing the bandgap (E_g). The increase of E_g can be derived as [15]

$$\Delta E_g = \Delta E_{C0} + \Delta E_{V0} = h^2/8m_e^* t_{\rm Si}^2 + h^2/8m_h^* t_{\rm Si}^2 \quad (1)$$

where ΔE_{C0} and ΔE_{V0} are the band-edge shifts in the conduction- and valence-band minima, respectively, h is the Planck constant, and m_e^* and m_h^* are the quantization effective masses of electron and hole, respectively.

Transistors in disordered silicon behave in a very similar fashion to crystalline device, and the energy barrier between the source and the channel governs charge transport in the inversion layer [9]. The height of the energy barrier $\Phi_{\rm SC}$ is given by

$$\Phi_{\rm SC} = \frac{E_g}{2} + \Phi_F - \Psi_S \quad (2)$$

where Φ_F is the Fermi level, and Ψ_S is the channel surface potential.

Below threshold, charge carriers have to traverse the barrier when diffusing from source to drain, as shown in Fig. 1. The

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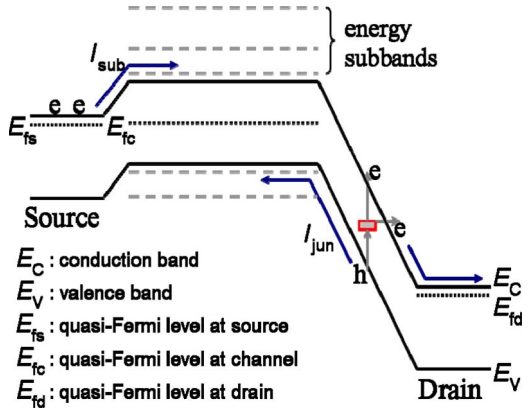

Fig. 1. Schematic band diagram of the thin-film transistor in disordered silicon, showing the discrete energy levels originating from carrier confinement in the thin channel, the subthreshold leakage current $(I_{\rm sub})$ generated by carriers traversing the barrier between the source and the channel, and the junction leakage $(I_{\rm jun})$ arising by electron–hole pairs generated via traps near the midgap at drain junction through thermal emission or thermionic field emission [10].

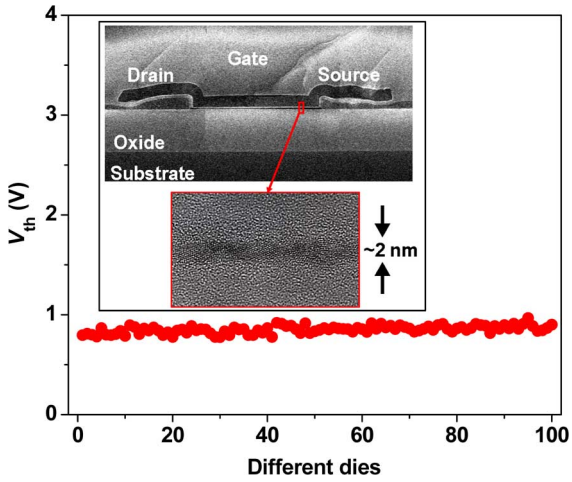

Fig. 2. Plot of the extracted threshold voltage $(V_{\rm th})$ values for the 2.0-nm-thick channel devices in 100 different dies on the same chip, showing very good uniformity. Inset: Cross-sectional scanning electron microscopy and TEM micrographs of the fabricated ultrathin channel nanocrystalline silicon thin-film transistors (the minimum channel thickness is 2.0 nm).

subthreshold current $(I_{\rm sub})$ can be expressed to first order as a function of $\Phi_{\rm SC}$ as follows:

$$I_{\rm sub} \propto \exp\left(-\frac{q}{kT}\cdot\Phi_{\rm SC}\right) \tag{3}$$

where k is the Boltzmann constant, T is the absolute temperature, and q is the electron charge.

Quantum confinement increases E_g and can thereby effectively reduce $I_{\rm sub}$. For transistors in disordered silicon, it has been found that the anomalously high leakage current arises by electron–hole pairs generated via traps near the midgap at drain junction through thermal emission or thermionic field emission [10], as shown in Fig. 1, and the junction leakage $(I_{\rm jun})$ can be given as $I_{\rm jun} \propto \exp(-(qE_g/2kT))$. Thus, the quantum confinement is also able to effectively reduce the junction leakage and, therefore, the total OFF-state leakage current $I_{\rm OFF}$ as

$$I_{\rm OFF} = I_{\rm sub} + I_{\rm jun} \propto \exp\left(-\frac{qE_g}{2kT}\right). \tag{4}$$

Whereas in the ON-state, the barrier height between the source and the channel diminishes because the increased $V_{\rm GS}$ brings high channel surface potential Ψ_S. The bandgap-widening effect becomes much less pronounced, and the ON-state current depends on the drift of majority carriers through the channel under the applied electric field. Therefore, as the channel becomes thinner, quantum confinement gets stronger, and higher $I_{\rm ON}/I_{\rm OFF}$ can be achieved.

Furthermore, when the channel becomes thinner, the effect of $V_{\rm GS}$ on Ψ_S increases, thus resulting in a steeper subthreshold swing (S), as follows [9]:

$$\frac{d\Psi_S}{dV_{\rm GS}} \approx \frac{C_{\rm ox}}{q\cdot d_c\cdot D_t} \tag{5}$$

$$S = \ln(10)\cdot\frac{kT}{q}\cdot\frac{1}{d\Psi_S/dV_{\rm GS}} \tag{6}$$

where $C_{\rm ox}$ is the gate dielectric capacitance per unit area, D_t is the density of localized trap states, d_c is the physical depth of the charged region in the channel, and when the channel becomes thin enough, d_c can be seen to be equal to $t_{\rm Si}$.

III. Results and Discussions

The devices used for this letter are nanocrystalline silicon thin-film transistors fabricated on p-type silicon substrate, which are composed of a thin layer of undoped nanocrystalline silicon, a gate insulator of 22.5-nm silicon oxide, and a 100-nm-thick layer of phosphorous-doped poly-Si as the gate electrode. The channel thickness varies from 8.0 to 2.0 nm. The precise channel thickness is achieved by controlling the chemical vapor deposition process at a very low deposition rate, and the average grain size of the channel is estimated from the planar transmission electron microscopy (TEM) micrographs about 10 nm. Details of the fabrication process can be referred to [11] and [16]. Micrographs of the final structure of fabricated devices are given in the inset in Fig. 2. The devices have good intrachip uniformity of electrical characteristics, even when the channel is as thin as 2.0 nm, as shown in Fig. 2, where the extracted threshold voltage $(V_{\rm th})$ values for the devices in different dies on the same chip are plotted.

The $I_{\rm DS}$–$V_{\rm GS}$ characteristics of the devices with different thick channels at a drain bias of 1.0 V are shown in Fig. 3(a). Since the devices exhibit extremely small leakage current, the data are obtained through converting the measurements for 500 parallel transistors to a per-transistor result. Fig. 3(b) shows the $I_{\rm OFF}$ reduction $(\eta_{\rm rat})$ and S as a function of $t_{\rm Si}$. $I_{\rm OFF}$ is extracted as the $I_{\rm DS}$ value at the bottom point of the $I_{\rm DS}$–$V_{\rm GS}$ curves in Fig. 3(a), which is corresponding to the lowest $I_{\rm OFF}$ value that the devices can reach after optimization of the voltage

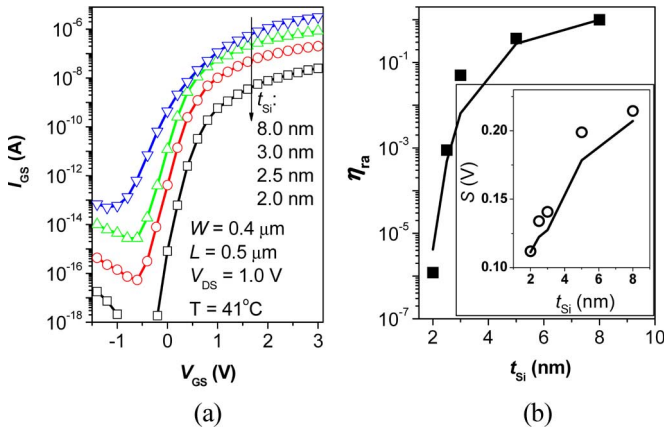

Fig. 3. (a) $I_{\rm DS}$–$V_{\rm GS}$ characteristics, which are measured at 41 °C, for the devices of different channel thicknesses ($t_{\rm Si}$) with a channel length of 0.5 μm and a channel width of 0.4 μm, at a drain bias of 1.0 V. (b) Leakage-current ($I_{\rm OFF}$) reduction ($\eta_{\rm rat}$) as a function of channel thickness ($t_{\rm Si}$) (■: Experimental results; —: Theoretical calculations). The $\eta_{\rm rat}$ for a device is the ratio of its $I_{\rm OFF}$ over the value for the device with an 8-nm-thick channel. Inset: Subthreshold swing (S) as a function of $t_{\rm Si}$ (○: Experimental results; —: Theoretical calculations).

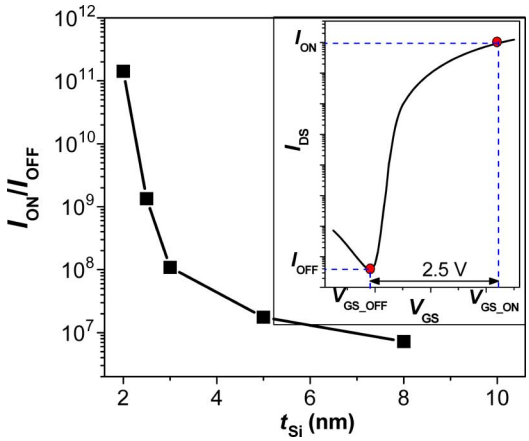

Fig. 4. $I_{\rm ON}/I_{\rm OFF}$ current ratio as a function of channel thickness ($t_{\rm Si}$). Inset: Definition of $I_{\rm ON}$ and $I_{\rm OFF}$–$I_{\rm OFF}$ is extracted as the $I_{\rm DS}$ value at the bottom point of the $I_{\rm DS}$–$V_{\rm GS}$ curves; $I_{\rm ON}$ is extracted as the $I_{\rm DS}$ at the $V_{\rm GS\_ON} = 2.5\ {\rm V} + V_{\rm GS\_OFF}$, where $V_{\rm GS\_OFF}$ is the gate voltage at the bottom point of the $I_{\rm DS}$–$V_{\rm GS}$ curves (the point where $I_{\rm OFF}$ is extracted).

bias. The $\eta_{\rm rat}$ for a device is the ratio of its $I_{\rm OFF}$ over the value for the device with an 8-nm-thick channel, and based on (4), it can be approximately expressed as

$$\eta_{\rm rat} = \frac{I_{\rm OFF}(t_{\rm Si})}{I_{\rm OFF}(t_{\rm Si} = 8\ {\rm nm})} \propto \exp\left(-\frac{q \cdot \Delta E_g(t_{\rm Si})}{2kT}\right) \qquad (7)$$

where $\Delta E_g(t_{\rm Si})$ is the bandgap widening relative to the bandgap for the 8-nm-thick channel devices.

Although we used 500 parallel transistors to make the small current observable, $I_{\rm OFF}$ values of the 2.0-nm-thick channel devices were still too small to be measured and were roughly estimated from the measurable parts in the $I_{\rm DS}$–$V_{\rm GS}$ curves. Applying this method to the thicker channel devices, we observed that although the obtained results are not exactly equal to the measured ones, they are well in the same order. Thus, this estimation will not have influence on the conclusion to be made in this letter. From Fig. 3(b), it can be seen that $I_{\rm OFF}$ decreases dramatically as $t_{\rm Si}$ is reduced. By assuming an electron effective mass of 0.19 m_e (electron mass) and a hole effective mass of 0.49 m_e, the bandgap widening for devices with different thick channels is calculated based on (1), and thereafter, $\eta_{\rm rat}$ values are obtained through (7), which can be seen to fit well with the experimental results, as shown in Fig. 3(b).

This proves that the marked reduction of $I_{\rm OFF}$ in thinner channel devices is due to stronger quantum confinement.

Fig. 3(b) also shows a steeper S in the devices with a thinner channel, just as predicted by (5) and (6). The S values were extracted by using the conventional definition as the inverse slope of the $\log(I_{\rm DS})$–$V_{\rm GS}$ curves in the subthreshold regime. The 2.0-nm-thick channel device has an S value of about 100 mV/dec. Based on (2), the effect of $V_{\rm GS}$ on the surface potential $d\Psi_S/dV_{GS}$ in the subthreshold regime can be derived as the negative value of the slope of $\Phi_{\rm SC}$ versus $V_{\rm GS}$, which were obtained through the Arrhenius plot of the drain current versus the inverse of the absolute temperature in the temperature range of 30 °C−120 °C in this letter. Then, based on (6), S values for devices with different thick channels were calculated and compared with the measured results in Fig. 3(b), showing good agreement. A steeper S in the thinner channel devices will allow a smaller $V_{\rm GS}$ swing to achieve the required $I_{\rm ON}/I_{\rm OFF}$ ratio.

At a given gate voltage swing, the decreased $I_{\rm OFF}$ and the improved subthreshold slope result in higher $I_{\rm ON}/I_{\rm OFF}$ ratio for the thinner channel devices, as shown in Fig. 4. To extract the $I_{\rm ON}$ values of devices with different channel thicknesses, for comparison, we fix the gate voltage swing at 2.5 V, and $I_{\rm ON}$ is extracted as the $I_{\rm DS}$ at the $V_{\rm GS\_ON} = 2.5\ {\rm V} + V_{\rm GS\_OFF}$, where $V_{\rm GS\_OFF}$ is the gate voltage at the bottom point of the $I_{\rm DS}$–$V_{\rm GS}$ curves (also the point where $I_{\rm OFF}$ is extracted), as shown in the inset in Fig. 4. For the 2.0-nm-thick channel devices, $I_{\rm ON}/I_{\rm OFF}$ ratio of more than 10^{11} was achieved, which can never be obtained for normal thick channel transistors in disordered silicon.

IV. Conclusion

By theoretical analysis and experimental results, it is proved that using an ultrathin channel effectively improves the switching performance of thin-film transistors in disordered silicon. When the channel becomes thinner, the OFF-state current $I_{\rm OFF}$ decreases significantly, which is attributed to the stronger quantum confinement along the channel thickness direction, and the subthreshold swing (S) also becomes steeper because the effect of $V_{\rm GS}$ on the channel surface potential Ψ_S increases. The low $I_{\rm OFF}$ and the steep S result in high $I_{\rm ON}/I_{\rm OFF}$ ratio, which exceeds 10^{11} for the devices with a 2.0-nm-thick channel at a given gate voltage swing of 2.5 V. The high $I_{\rm ON}/I_{\rm OFF}$ will enable to design integrated electronics on arbitrary substrates for applications where low power and fast access times are demanded.

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