High tolerance to gate misalignment in low voltage gate-underlap double gate MOSFETs


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Abstract—In this letter, we demonstrate for the first time that gate misalignment is not a critical limiting factor for low voltage operation in gate-underlap double gate (DG) devices. Our results show that underlap architecture significantly extends the tolerable limit of gate misalignment in 25 nm devices. DG MOSFETs with high degree of gate misalignment and optimal gate-underlap design can perform comparably or even better than self-aligned nonunderlap devices. Results show that spacer-to-stragggle \( (s/\sigma) \) ratio, a key design parameter for underlap devices, should be within the range of 2.3–3.0 to accommodate back gate misalignment. These results are very significant as the stringent process control requirements for achieving self-alignment in nanoscale planar DG MOSFETs are considerably relaxed without compromising the performance.

Index Terms—Cut-off frequency, double gate (DG) MOSFETs, gate capacitances, gate misalignment, intrinsic voltage gain, ultra-low-voltage (ULV) analog/RF applications, underlap design.

I. INTRODUCTION

DOUBLE GATE (DG) MOSFET has received considerable attention in recent years owing to the inherent suppression of short channel effects (SCEs), volume-inversion effect and excellent scalability [1], [2]. DG MOSFETs fabricated with channel in the plane of the wafer (standard configuration) [3], pose the difficult problem of how to fabricate a bottom gate underneath the FET body and align it to the top gate. The alignment of the dual gates is crucial to high performance because a misalignment will cause extra gate to source/drain overlap capacitance as well as loss of current drive.

In this letter, we use the concept of gate-underlap design [4]–[7] and for the first time propose a design methodology to alleviate the critical issue of gate misalignment in ultra-low-voltage DG devices. A design criterion to select underlap region parameters is proposed for minimizing the impact of gate misalignment on device performance for low voltage applications.

II. SIMULATIONS

The undoped DG devices [Fig. 1(a)] analyzed have been simulated using the 2-D simulator, ATLAS [8], with gate

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Fig. 1. (a) Schematic diagram of a DG MOSFET with back gate misaligned by a factor \( m = -0.5 \ L_g \). Negative (positive) \( m/L_g \) values represent back gate misaligned toward the source (drain). (b) Variation of SDE profile along the channel for \( \sigma = 12.5 \times 10^{-10} \) and 10 nm \((\square—\square)\) with \( d = 5 \ \text{nm/dec} \). Please note that only half of the device structure has been shown in (b).

III. RESULTS AND DISCUSSIONS

Fig. 2 shows the dependence of cutoff frequency \( (f_T) \) and intrinsic voltage gain \( (A_{VO}) \) on \( m/L_g \), along with the results of DG devices with nonunderlap (abrupt) SDE regions. Please note that the degradation will be nearly symmetric with respect to \( \pm m/L_g \) because analog FOMs were extracted in the subthreshold region at current density of 10 \( \mu A/\mu m \). An increase in gate misalignment \( (m) \) leads to a severe degradation in analog/RF FOMs in DG devices with nonunderlap design. Results for gate-underlap design show a high tolerance to gate misalignment (no change in \( f_T \) and \( A_{VO} \)) up to \( m/L_g \approx 0.25 \). Poorly aligned \( (m/L_g > 0.25) \) SDE devices achieve higher \( f_T \) and \( A_{VO} \) as compared to precisely aligned abrupt SDE devices, e.g., if \( m/L_g = 0.5 \), and \( \sigma \) is increased from 10 to 12.5 nm, the relative improvement in \( f_T \) increases from 1.1 to 1.5 and
in $A_{VO}$ (in decibels), from 1.2 to 1.7. In a more extreme case where $m/L_g = 0.75$ and $\sigma = 12.5$ nm, $f_T$ is comparable to that of abrupt SDE devices, but still a relative improvement of 1.5 is obtained in $A_{VO}$. The self-aligned devices will always perform better than the misaligned for the same SDE profile. Back gate misalignment can be tolerated without compromising the performance if the SDE region profile is designed with $\sigma = m/2$. These results are very significant as the stringent process control requirements to achieve a self alignment between the dual gates in a planar DG MOSFET are relaxed and a high degree of misalignment ($m/L_g \geq 0.5$) between top and bottom gates can be tolerated at nanoscale regimes.

The results of $f_T$ and $A_{VO}$ can also be understood in terms of spacer-to-straggle ratio ($s/\sigma$), an important technological parameter for the design and optimization of gate-underlap devices [7]. Misaligned DG MOSFETs designed with $s/\sigma = 2.3$ (with $\sigma = 10$ nm, $d = 5$ nm/dec, $s/L_g = 0.9$) achieve higher $f_T$ and $A_{VO}$ values as compared to those designed with abrupt SDE regions for $m/L_g = 0.5$. In order to accommodate higher gate misalignment ($m/L_g = 0.75$), $s/\sigma$ should be increased to 2.9 ($\sigma = 12.5$ nm, $d = 5$ nm/dec, $s/L_g = 1.4$). These results suggest that spacer width ($s$) should be approximately $3\sigma$, i.e., the spacer should be wide enough to ensure that all of the underlap profile is across the spacer and not under the gate. In an optimal design, it is more appropriate to increase $s$ to achieve higher $\sigma$ values as $d$ depends on thermal budget and diffusivity of dopants and very small values ($< 3$ nm/dec) may be difficult to achieve.

To further analyze the usefulness of the underlap design, we evaluate important analog parameters, such as transconductance-to-current ratio ($g_m/I_{ds}$), Early voltage ($V_{EA}$), transconductance ($g_m$) and total input capacitance ($C_{gg}$). As shown in Fig. 3(a) and (b), underlap devices with $m/L_g = 0.5$ for $\sigma \geq 10$ nm and $m/L_g = 0.75$ for $\sigma \geq 12.5$ nm, achieve higher ($g_m/I_{ds}$)peak values than self-aligned nonunderlap DG devices. An increase in $\sigma$ shifts the SDE doping away from the gate edge which minimizes SCE and improves gate controllability. This results in higher values in weak inversion region of $g_m/I_{ds}$ ($\sim 36$ V$^{-1}$) as compared to $\sim 30$ V$^{-1}$ (non-underlap SDE regions). Underlap architecture is particularly advantageous in the weak/moderate inversion regions, as the current flow is mainly due to diffusion of carriers and large straggles values ($\sim 12.5$ nm) do not degrade the performance. In strong inversion region ($\sim 5$ V$^{-1}$), large $\sigma$ values and wider spacers introduce additional parasitic resistance, which results in current ratio $I_{ds}/I_{Underlap}$/*Nonunderlap* < 1, i.e., degradation of $g_m$ at higher $I_{ds}$.

As shown in Fig. 4(a), $g_m$ initially increases up until $\sigma = 10$ nm and remains constant thereafter in DG devices with $m/L_g \leq 0.5$. An increase in $\sigma$ at a given $d$ results in longer effective channel length thereby suppressing SCE [6], [7] and improving $g_m$. DG devices designed with $m/L_g = 0.5$ achieve nearly the same or marginally higher $g_m$ values over the range of $\sigma$ values. In particular, $g_m$ is insensitive to $m/L_g$ values in the range 0 to 0.75 for $\sigma = 12.5$ nm and a minimum $A_{VO}$ of 22 dB is achievable for $\sigma$ lying between 10–12.5 nm.

Fig. 4(b) shows the variation of total gate capacitance ($C_{gg}$) and Early voltage ($V_{EA}$) ($I_{ds}/I_{ds}$, where $I_{ds}$ is the output conductance) with $\sigma$. An increase in $\sigma$ shifts the source/drain doping away from the gate edge, resulting in a significant reduction in parasitic fringing capacitance that leads to the decrease in $C_{gg}$. The underlap architecture results in the relative reduction of $C_{gg}$ (at $\sigma = 12.5$ nm) by 25% for $m/L_g = 0.5$ and 10% for $m/L_g = 0.75$. Underlap devices designed with $\sigma \leq 10$ nm and $m/L_g < 0.5$ achieve higher $C_{gg}$ as compared to self-aligned nonunderlap DG devices. The reduction in $C_{gg}$ along with an improvement in $g_m$ translates into higher $f_T$ values in misaligned gate-underlap DG devices. Even more significant aspect of underlap design is the substantial improvement in $V_{EA}$ due to the reduction of peak electric field (at the gate edge) with increase in $\sigma$. The improvement in $V_{EA}$ is nearly 1.8 times at
σ = 10 nm and four times at σ = 12.5 nm with m/Lg = 0.5. The increase in $V_{EA}$ coupled with an improvement in $g_m/I_{ds}$ at low $I_{ds}$ results in an improvement in $A_{VO} (= g_m/I_{ds} \times V_{EA})$.

Gate-underlap DG devices operated at low current levels are particularly useful for ULV analog/RF applications as both gain and speed of devices can be significantly improved in misaligned structures and stringent process control requirements to achieve a perfect-alignment can be considerably relaxed.

REFERENCES


