GRAPHENE NANOTECHNOLOGY FOR THE NEXT GENERATION LOGIC, MEMORY, AND 3D INTEGRATED CIRCUITS

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By

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Kansas City, Missouri

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Graphene Nanotechnology for the Next Generation Logic, Memory, and 3D Integrated Circuits

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Abstract

Floating gate transistor is the basic building block of non-volatile flash memory, which is one of the most widely used memory gadgets in modern micro and nano electronic applications. Recently there has been a surge of interest to introduce a new generation of memory devices using graphene nanotechnology. In this paper we present a new floating gate transistor (FGT) design based on multilayer graphene nanoribbon (MLGNR) and carbon nanotube (CNT). In the proposed graphene based floating gate transistor (GFGT) a multilayer structure of graphene nanoribbon (GNR) would be used as the channel of the field effect transistor (FET) and a layer of CNTs would be used as the floating gate. We have performed an analysis of the charge accumulation mechanism in the floating gate and its dependence on the applied terminal voltages. Based on our analysis we have observed that proposed graphene based floating gate transistor could be operated at a reduced voltage compared to conventional silicon based floating gate devices. We have presented detail analysis of the operation and the programming and erasing processes of the proposed FGT, dependency of the programming and erasing current density on different parameters, impact of scaling the thicknesses of the control and tunneling oxides. These analyses are done based on the equivalent capacitance model of the device.

We have analyze the programming and erasing by the tunneling current mechanism in the proposed graphene-CNT floating gate transistor. In this paper, we have investigated the mechanism of programming current and the factors that would influence this current and the behavior of the proposed floating gate transistor. The analysis reveals that programming is a strong function of the high field induced by the control gate, and the thicknesses of the control oxide and the tunnel oxide.

With the growing demand for nonvolatile flash memory devices and increasing limitations of silicon technologies, there has been a growing interest to develop emerging flash memory by using alternative nanotechnology. The proposed FGT device for nonvolatile flash memory contains an MLGNR channel and a CNT floating gate with SiO_2 as the tunnel oxide. In this paper, we have presented detail analysis of the electrical properties and performance characteristics of the proposed FGT device. We have focused on the following aspects: current-voltage (I-V) characteristics, threshold voltage variation (ΔV_{TH}), programming, erasing and reading power consumptions compared to the existing FGTs, and layer-by-layer current-voltage characteristics comparison of the proposed GFGT device. To realize graphene field effect transistor (GFET), a general model is developed, validated and analyzed. This model is also used to estimate graphene channel behavior of the proposed GFGT.

Reliability is the major concern of the Flash memory technology. We have analyzed retention characteristics of the proposed GFGT. We also have developed a radiation harness test model for the Si-FGT by using V_{TH} variation principle due to the radiation exposure. Flash memory experiences adverse effects due to radiation. These effects can be raised in terms of doping, feature size, supply voltages, layout, shielding. The operating point shift of the device forced to enter the logically-undefined region and cause upset and data errors under radiation

exposure. In this research, the threshold voltage shift of the floating gate transistor (FGT) is analyzed by a mathematical model.

Molybdenum disulfide (MoS2) based field effect transistor is considered as one of the promising future logic devices. Many other nanoelectronic devices based on MoS2 are currently under investigation. However, the challenge of providing reliable and efficient contact between 2D materials like MoS2 and the metal is still unresolved. The contact resistance between metal and MoS2 limits the application of MoS2 in current semiconductor technologies. In this paper, a detail analysis of metal-MoS2 contact has been presented. Specific contributions of this work are:investigation of the physical, material and electrical parameters that would determine the contact properties, analysis of the combined impact of the top and back gates for the first time, modeling of the crucial metal-MoS2 contact parameters, such as, sheet resistance (R_{Sh}), contact resistivity (ρ_c), contact resistance (R_C) and transfer length (L_T), investigation of the ways to incorporate the developed contact model into the electronic design automation (EDA) tools and investigation of different contact materials for the metal-MoS2 contact.

The three dimensional integrated circuit (3D- IC) is expected to extend Moore's law. To reduce interconnects and time delay, semiconductor industry is shifting 2D-IC to 2.5D-IC and 3D-IC. 3D-IC is the ultimate goal of the semiconductor industry, where 2.5D-IC is an intermediate state. It is important to realize CAD design challenges of the 2.5D-IC/3D-IC when minimum spacing interconnects are used. The major contributions of this research work are as follows. Previously, for the small scale experimental purpose, small numbers (10-20) of TSVs, interconnects, bumps are fabricated together by hand calculation. However in the real 3D-IC design, thousands of TSVs, interconnects, bumps are reuired. Therefore, an automated CAD

solution is required to provide precise physical design and verification. Therefore, a solid CAD solution is provided here. Compatible with 40nm-technology design, which enables the Silicon Interposer to integrate with the digital, analog and RF dies together. Dimensions and spacing of the TSV and Bump are optimized by the 3D EM full wave field solver. To our best knowledge, at the interposer level, this design reports the most dense and well-defined RDL, TSV and micro-bump co-design on Silicon Interposer, which will be used for 2.5D-IC.

Approval Page

The faculty listed below, appointed by the Dean of the School of Graduate Studies, have examined a dissertation titled “Graphene Nanotechnology the Next Generation Logic, Memory and 3D Integrated Circuits,” presented by Md Nahid Hossain, candidate for the Doctor of Philosophy degree, and hereby certify that in their opinion it is worthy of acceptance.

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Chapter 1 : Introduction and Background

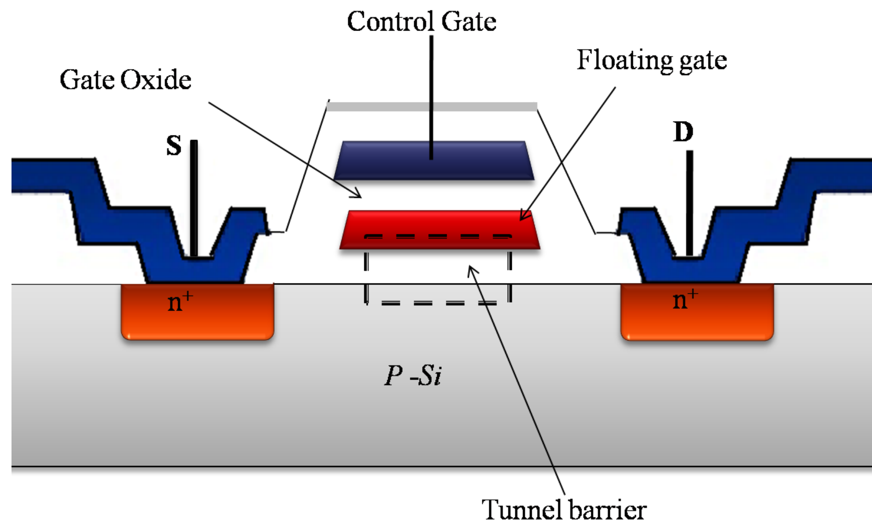
1.1. Introduction

Non-volatile flash memory that utilizes floating gate transistors (FGTs) has become the most widely used memory technology in numerous electronic applications. Due to continuous scaling and physical and material limits of conventional MOSFET technologies, silicon based floating gate transistors will no longer be able to meet the reliability, cost and efficiency requirements in future. Graphene that has extraordinary characteristics (very high carrier mobility, thermal conductivity, mechanical flexibility and strength, and optical transparency) is a highly promising material for future nonvolatile memory and other nanoelectronic devices [1]-[2]. The high carrier mobility of the MLGNR leads to the low latency and fast response. The intrinsic thermal conductivity protects the device from overheating. The mechanical flexibility inspires flexible memory, which is future of electronics design. In this paper we present the design of a new floating gate transistor using multilayer graphene nanoribbon (MLGNR) and carbon nanotube (CNT). The preliminary concept has been presented in our recent conference paper [50].

1.2. Conventional Si FGT Operation

The primary difference between a floating gate transistor and the standard MOSFET is the addition of a new gate, called the floating gate, between the original gate and the channel as shown in Figure 1-1:a. The original gate (topmost) is now called the control gate. A floating gate is basically a polysilicon gate surrounded by insulator and it has no electrical connection with other layers [6].To program or write floating gate transistor (Figure 1-1:b), a positive control gate voltage is applied. This positive voltage accumulates electrons from the channel

through the tunnel oxide (insulating layer) into the floating gate. The accumulated charges in the floating gate, is protected by the tunnel oxide and control oxide insulating layer. Therefore, the stored data is retained for years. To erase the data, a high negative voltage is applied at the control gate (Figure 1-1:c). This negative voltage depletes the accumulated electrons out of the floating gate [6]-[8].



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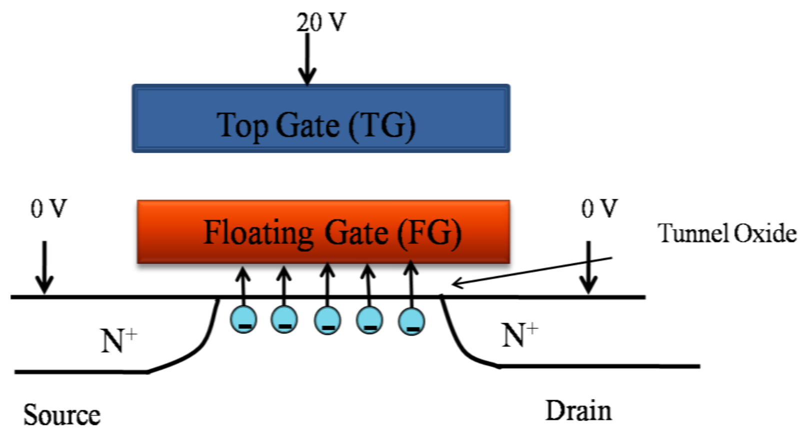

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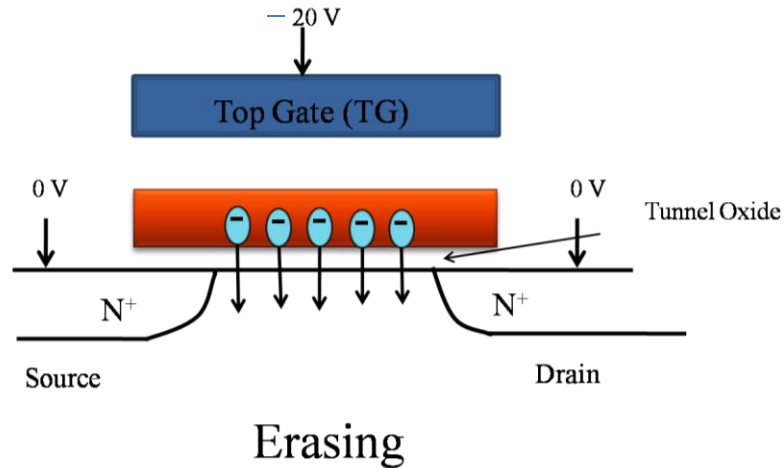


(c)

Figure 1-1: (a) Schematic diagram of a floating gate transistor. (b) Programming of the floating gate transistor, and (c) erasing of the floating gate transistor.

The working principle of the floating gate transistor is almost same as conventional MOSFET, where the source-drain current is monitored and controlled by the control gate voltage. The floating gate voltage or in other words the stored charge on the floating gate can control the channel between the drain and the source. The thickness of the dielectric layer is around 10nm or less [8]. Thinner insulation layer is required to facilitate tunneling between the channel and the floating gate. The detail working principle of a floating gate transistor can be found in any relevant textbook. Interested reader can also refer to [6]-[8] and our recent conference paper [50] for further details.

1.3. Literature Review

The nonvolatile flash memory utilizes floating gate transistor (FGT), which has become

the most widely used memory technology in numerous electronic applications. Due to the continuous scaling and physical and material limits of the conventional CMOS technology, silicon based FGTs will no longer be able to meet the reliability, cost and efficiency requirements in future. Many radical device and material alternatives are being explored for the flash memory technology in the nanometer range. Nanoscale single-bit floating gate transistors and ZnO nanoparticle based floating gate transistor on the low cost glass and plastic substrate for transparent electronics and memory devices are few examples [12]-[51]. The floating gate transistor using gold nanoparticle and multiple-bits floating gate transistor have been reported in [3]. Graphene is another material that is getting widespread attention from diverse groups of engineers and scientists. The memory window of graphene based memory cell is expected to be greater than that of silicon [4]. Several graphene based memory cells have been under investigation. A FGT device with MLGNR as the floating gate and molybdenum disulfide (MoS_2) as the channel materials has been proposed in [10]. Graphene and MoS_2 are utilized as the channel and charge trapping layer (floating gate) interchangeably with hexagonal boron nitride (hBN) as the tunnel barrier in [11]. Graphene oxide thin film based flexible nonvolatile resistive memory has also been explored in [5]. Graphene and graphene oxide have been explored as the channel, charge trapping layer and electrode in [14]-[19]. Large hysteresis, which arises due to the trapping of charges by the oxide layer, in the gate characteristics of graphene FETs can be utilized for nonvolatile memory application [20]-[21].

1.4. Emerging Trends of Flash Memory Device

The Field effect transistor (FET) is used for the logic application i.e. Microprocessor, ALU, and Volatile Memories i.e. SRAM, DRAM. Currently, different forms of Si-FET like MOSFET, FinFET are used for the logic operation. Figure 1-2 shows that graphene FET is an emerging logic device, which will replace the conventional Si-FET.

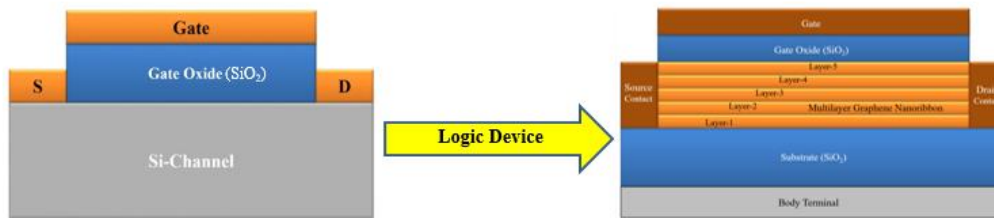


Figure 1-2: Emerging trend at the logic device (FET).

The floating gate transistor (FGT) is used for the nonvolatile memory application i.e. NAND Flash memory, NOR Flash memory, Solid state drive (SSD). Currently, different forms of Si-FGT like 2D FGT, 3D FGT are used for the nonvolatile flash memory operation. Figure 1-3 shows that graphene FGT is an emerging flash memory device, which will replace the conventional Si-FGT.

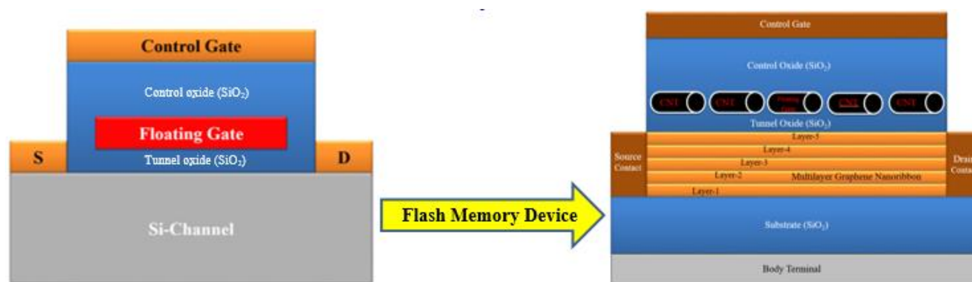


Figure 1-3: Emerging trend at the nonvolatile flash memory device (FGT).

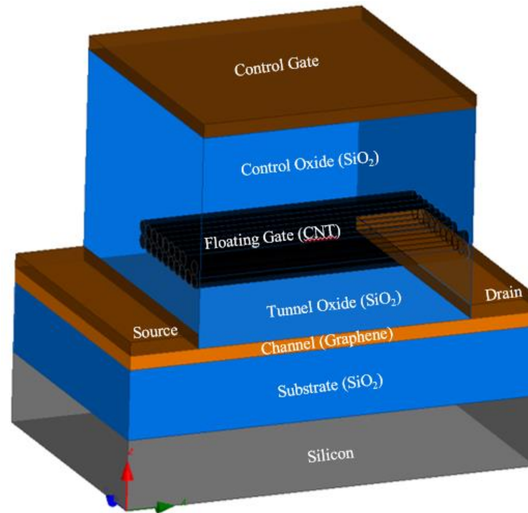
Chapter 2 : Proposed Graphene Based Flash Memory

2.1. Proposed Design

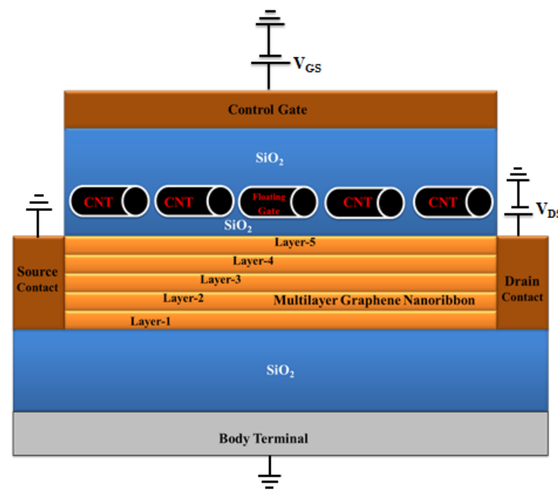
The proposed floating gate transistor is based on two forms of carbon/graphene nanostructures, metal contacts and SiO_2 insulator. Here MLGNR would be used as the channel and CNTs would be used as the charge trapping layer or the floating gate. The schematic of the proposed FGT is shown in Figure 2-1. The proposed FGT device is a single level cell (SLC) memory, because it can store one bit of data ('1'/'0').

We propose to use SiO_2 as the insulator around the CNT layer to isolate the external control gate, the floating gate (CNTs) and the channel (MLGNR). The control oxide (the SiO_2 layer between the floating and the external gate) blocks the stored charge in the CNTs and prevents data loss resulting from charge leakage into the control gate. Better and thicker control oxide effectively inhibits not only charge loss from the CNT charge storage layer, but also blocks charge-injection from the metal control gate. This results in a higher trapping efficiency and relieves the problem caused by the thin charge storage layer. However, thicker control oxide leads to higher operating voltage requirements. The tunnel oxide (the SiO_2 layer between the floating and the channel) must be thinner than the control oxide to allow electrons to smoothly tunnel to and from the channel and the floating gate during the programming and erasing operation. Under normal operating condition the tunnel oxide has the same function of the control oxide to prevent charge flow in and out of the floating gate. Therefore, the dielectric and physical properties of the oxides around the gates are very critical for the performance and reliability of the proposed floating gate transistor. In our future designs, we will explore

different insulators as the control and tunnel oxides to ensure higher reliability and low-power operation. The external control gate (top gate) and the body contact would be made of metal. A layer of SiO_2 dielectric is grown between the MLGNR channel and the body contact to provide substrate for graphene and electrical isolation. The body contact can also be configured as the back gate for better control.



(a) 3D view



(b) 2D view

Figure 2-1: Proposed CNT and MLGNR based floating gate transistor (a) 3D view, (b) Cross-section of the FGT with required electrical connection for its operation.

Layers of SiO_2 are grown around the CNT layer to isolate the external control gate, the floating gate (CNTs) and the channel (MLGNR). The control oxide (the SiO_2 layer between the floating and the control gates) blocks the stored charge in the CNTs and prevents data loss resulting from charge leakage into the control gate electrode. Adoption of the control oxide effectively inhibits not only charge loss from the CNT charge-storage layer, but also blocks charge-injection from the metal control gate. This results in a higher trapping efficiency and relieves the problem caused by the thin charge storage layer. The tunnel oxide (the SiO_2 layer between the floating and the channel) must be thinner than the control oxide to allow electrons to smoothly tunnel to and from the channel and floating gate during the programming and erasing operation. Under normal operating condition the tunnel oxide has the same function as the control oxide to prevent charge flow in and out of the floating gate. Therefore, the dielectric and physical properties of the oxides around the gates are very critical for the performance and reliability of the proposed floating gate transistor. The external control gate (top gate) and the body contact would be made of metal, polysilicon or any other suitable conducting material.

2.2. Why MLGNR Channel?

Graphene and CNT that have extraordinary characteristics (very high carrier mobility and thermal conductivity, extremely high flexibility and tensile strength, and optical transparency) are very promising nanomaterial for the emerging nonvolatile memory and other nanoelectronic devices [1]-[2]. The high carrier mobility in the MLGNR leads to low latency and fast response. The intrinsic thermal conductivity protects the device from overheating. The mechanical flexibility inspires flexible memory, which is the future of electronics design.

MLGNR is used as the channel material in the proposed design. Single layer nano-

patterned graphene FET is very noisy, while the nano-patterned few layer graphene FET shows reduced noise [37]-[38]. Although multiple layers of graphene is more efficient for gaining small sheet resistance, beyond a certain number, multi-layer GNRs would convert into graphite [39]. As the number of GNR layers increases, effective resistance saturates, which suggests that additional GNR layers will no longer improve resistance [40]. Therefore, the optimum number of layers in the MLGNR structure would depend on the performance requirements. Our future work will focus on the optimization of the proposed structure for the best possible performance. However, multiple GNRs would be required to provide strong conduction path and override noise.

Graphene channel offers several major advantages: (i) chemically doped graphene can be used as the channel material, (ii) graphene can be nano-patterned into any dimension because of its 2D sheet structure [46], (iii) the magnitude of the graphene bandgap is inversely proportional to the ribbon width (W): $E_{gap}= \alpha /(W-W^{*})$(nm), (W is the width of the transistor, W^{*}=16 nm and α=0.2–1.5 eV) thus the band gap becomes a lithographically designable parameter [46], and (iv) graphene based devices is fabricated on the existing SiO_2 substrate, which is grown on the Silicon wafer [49].

The ambipolar behavior of GNR channel device allows both N-type and P-type behavior in the same device by changing its back gate voltage both in the positive and negative regions [59]. The ambipolar effect is also observed in the top gated graphene device [58]. The ambipolar devices have some extraordinary advantages in realizing complementary circuits that offer low power consumption, wide noise margins and better stability [56]-[57]. The benefit of an ambipolar device is that it can be operated in two different regions. Any of the operating regions can be chosen by applying appropriate voltage. The 1/0 level can be set by

the program/erase voltage. A drain-source voltage (V_{DS}) is applied to start the conduction in the MLGNR channel. A positive control gate voltage (V_{GS}) is applied to program the transistor. Equally distributed voltage is assumed across each GNR layer in the MLGNR channel. Usually, graphene is doped by the atmospheric particles, photoresist deposit, metal etchants and Al_2O_3. Single layer graphene (SLG) is inherently p-type. On the other hand MLGNR is less responsive to the charge doping affects because the extra layers will reduce the impacts of these extra charges [23]-[25].

2.3.Why CNT Floating Gate?

CNT is used as the floating gate material in the proposed FGT. A significant hysteresis amid successive forward and backward C-V characteristics is observed in a FGT device, where CNTs are used as the floating gate [44]. CNTs have many exceptional properties such as adjustable band gap, high thermal stability, chemical inertness, flawless sidewall structure and close to zero surface states [41]-[43]. Excellent retention characteristic is also observed in CNT due to its exceptional structure and electrical characteristics [41]. These properties make CNTs very suitable for any charge storage node in memory devices. The structure of SWCNT is one dimensional because it transports the charge carriers only along one direction [42]-[43]. As a result, the trapped charges in the SWCNTs would be strongly confined and hard to tunnel out [41], which is good for charge retention. SWCNT's almost flawless surface feature compared to Si, Ge and other conventional device materials is another important property [42]. SWCNT (compared to Si and Ge nanocrystals that are previously used as the floating gate materials) has nearly no dangling bonds on its surface. The surface dangling bonds of Si plays a crucial role in the charge loss mechanism [45]. Therefore, CNT based

floating gate would not lose charge as in Poly-Si based floating gate.

2.4.Fabrication Process

The potential fabrication process of the MLGNR/CNT FGT would include the following steps. First, a 300 nm thick SiO_2 layer is thermally grown on a silicon wafer, which is the standard for the graphene based device. Second, MLGNR channel can be grown by the Chemical Vapor Deposition (CVD) method, followed by an etching process to obtain a rectangular shape MLGNR with a uniform channel length and width. Third, SiO_2-CNT-SiO_2 sandwich are grown on the MLGNR sheet. Fourth, Ti/Au metal contact pairs can be grown for the source, drain and control gate contact. Usually, graphene is doped by atmospheric molecules, photoresist residue, metal etchants and Al_2O_3. Single layer graphene (SLG) is inherently p-type. On the other hand MLGNR is less sensitive to charge doping effects because the additional layers will lessen the effects of these charges [23]-[25].

2.5.Methodology

In terms of design verification and validation for the proposed FGT, there are three major tasks: (i) graphene channel realization, (ii) CNT floating gate realization, and (iii) the development of the complete capacitance model to investigate the dynamic behavior of the proposed FGT device. One of the key issues in this regard is the estimation of graphene channel resistance. The theoretical modelling of graphene channel resistance is done based on the established simulation results and experiemntal data published by two teams from IBM [60] and UT-Austin & Texas Instruments [61] for graphene channel based field effect transistor (GFET). The carrier concentration formulas are taken from the GFET research of Philip Kim

of Harvard University and Kenneth L. Shepard of Columbia University [62]. The floating gate material must have better charge retention characteristics. The charge retention characteristics of CNT is investigated in [41] through some experimentation. We have used the data from [41] to justify using CNT as the charge retention layer or floating gate in our proposed design. In our future research, we will investigate how to optimize the floating gate design and CNT charge retention capacity based on the types, direction and fabrication process of the CNTs. For the complete current-voltage (I-V) characterization and dynamic behavior analysis, we need to investigate several I-V relations for the proposed device. To analyze the effect of the back gate we have derived I_{DS}-V_{BG} curve. Similarly, we have derived I_{DS}-V_{TG} and I_{DS}-V_{FG} curves to understand the effect of the top gate and the floating gate voltages on the performance of the proposed FGT. In deriving the I-V characteristics we have used experimental result of GFET [60] by the IBM team.

2.6.Contribution

The contribution of my research paper is discussed below separately. In [50], the primary concept of the proposed device is discussed. We did not provide any analysis and modeling of the operation, physical and electrical behaviors, and the impacts of different parameters. In [52], we provided detail description of the design and the underlying scientific explanation behind the concept. We have performed analysis of the electrical behaviors and dynamic characteristics of the device. We have also derived the capacitive model of the device and performed analysis of the impact of scaling oxide thickness on performance. Through our modeling and analysis we have identified some critical electrical, physical, and geometrical parameters that would influence the operation and performance of the device.

In [53], the control oxide and tunnel oxide scaling effects of the proposed FGT is illustrated. In [54], we have investigated the mechanism of programming current and the factors that would influence this current and the behavior of the proposed FGT. The analysis reveals that programming is a strong function of the high field induced by the control gate, and the thicknesses of the control and the tunnel oxides. In a separate project, we are investigating the impacts of radiation on the performance and reliability of this type graphene based memory device for defense and space applications [55].

2.7.Control and Tunnel Oxide Tradeoffs

The simplified equation of GCR is shown in (1). The term in the parenthesis of equation (1) determines the GCR.

$$\mathrm{GCR} = \frac{C_{FG}}{C_T}$$

$$= \frac{C_{FG}}{C_{FG} + C_{FS}}$$

$$= \frac{A\varepsilon 0(\frac{\varepsilon_{CO.}}{X_{CO}})}{A\varepsilon 0\left(\frac{\varepsilon_{CO.}}{X_{CO}}\right) + A\varepsilon 0(\frac{\varepsilon_{TO.}}{X_{TO}})}$$

$$= \frac{(\frac{\varepsilon_{CO.}}{X_{CO}})}{\left(\frac{\varepsilon_{CO.}}{X_{CO}}\right) + (\frac{\varepsilon_{TO.}}{X_{TO}})}$$

$$= \frac{1}{\frac{\left(\frac{\varepsilon_{CO.}}{X_{CO}}\right) + (\frac{\varepsilon_{TO.}}{X_{TO}})}{(\frac{\varepsilon_{CO.}}{X_{CO}})}}$$

$$= \frac{1}{1 + \frac{(\frac{\varepsilon_{TO.}}{X_{TO}})}{(\frac{\varepsilon_{CO.}}{X_{CO}})}}$$

$$GCR = \frac{1}{1 + (\frac{\varepsilon_{TO} X_{CO}}{\varepsilon_{CO} X_{TO}})} \quad (1)$$

$$\varepsilon_{TO}.X_{CO} < \varepsilon_{CO}.X_{TO} \quad (2)$$

- Case-I: if $\left(\frac{\boldsymbol{\varepsilon_{TO} X_{CO}}}{\boldsymbol{\varepsilon_{CO} X_{TO}}}\right) < \mathbf{1}$, GCR > 0.5
- Case-II: if $\left(\frac{\boldsymbol{\varepsilon_{TO} X_{CO}}}{\boldsymbol{\varepsilon_{CO} X_{TO}}}\right) = \mathbf{1}$, GCR= 0.5
- Case-III: if $\left(\frac{\boldsymbol{\varepsilon_{TO} X_{CO}}}{\boldsymbol{\varepsilon_{CO} X_{TO}}}\right) > \mathbf{1}$, GCR < 0.5

Case-I is considered for the better FGT design.

Therefore, it can be concluded that (i) high k-dielectric as the control oxide and low k-dielectric as the tunnel oxide enhance the V_{FG} (GCR), same materials are not recommended as the control oxide and the tunnel oxide, (ii) By lowering X_{CO} little bit, we can achieve further improvement in the V_{FG} (GCR) value but there is a limitation in the control oxide value, we can not go down that value (18nm).

Our proposed FGT and IBM Si-Channel-MLGNR-FG outperform other FGT devices because of low tunnel oxide dielectric constant and control oxide thickness product ($\boldsymbol{\varepsilon_{TO}.X_{CO}}$). According to equation (2), we have more room for development by using high k-dielectric as the control oxide. Our updated device should be like Figure 2-2. In future, we will concentrate on other insulator like HfO_2 and contact materials.

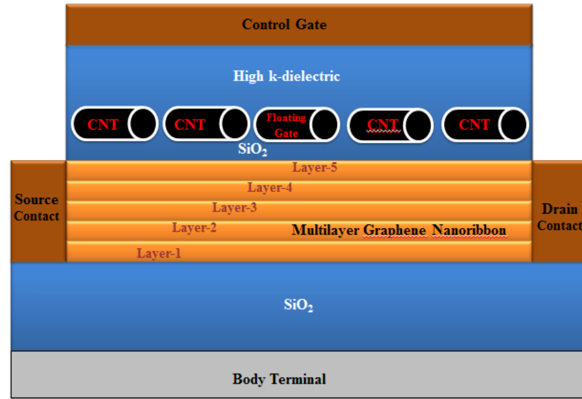


Figure 2-2: Updated MLGNR/CNT FGT. Here high k-dielectric is recommended as the control oxide and low k-dielectric is recommended as the tunnel oxide.

Chapter 3 : Physical and Electrical Parameters of the Proposed Graphene Flash Memory Device

3.1. Capacitance Model

In order to understand the dynamic behaviour of the proposed MLGNR/CNT floating gate transistor (FGT), its capacitive model has dervied. Figure 3-1 shows the simplified capacitive model of the proposed FGT. Here, the C_{FC}, C_{FG}, C_{FS} and C_{FD} are the capacitances of the floating gate (FG) with the channel, control gate, source and drain. There will be three additional capacitances (C_{SB}, C_{DB} and C_{CB}) inside the device. Here V_{GS}, V_S, $V_{DS,}$ V_C and V_B are the potentials of the control gate, source, drain, channel and bulk respectively and V_{FG} is the potential on the FG.

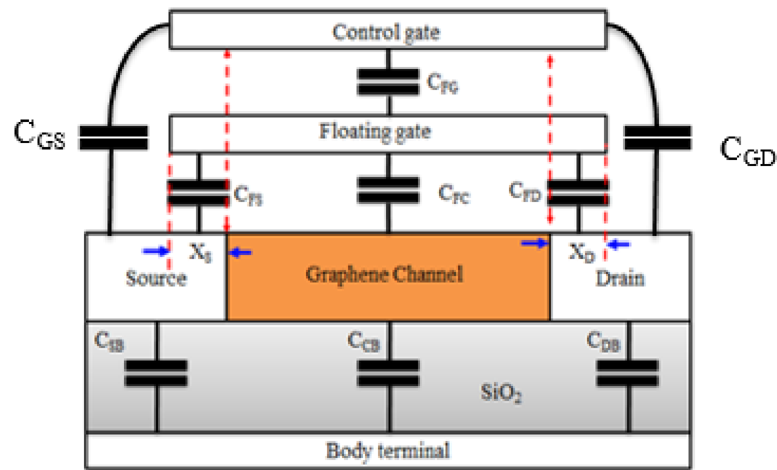


Figure 3-1: Capacitance model of the proposed MLGNR/CNT FGT considering fringing capacitance. X_S and X_D denote floating gate overlapping areas on source and drain respectively. C_{GS} and C_{GD} are fringing capacitances.

As the FG is connected with the control gate, source, drain and body terminals only through capacitors, the proposed flash memory cell can be expressed as a capacitor network as

shown in Figure 3-1. According to (3), the total capacitance of the cell (C_T) is equal to the sum of the capacitances of the network. Here C_{CB}, C_{SB} and C_{DB} are not important in the model because the values of these capacitors are close to zero. These capcitances arise due to the substrate on which graphene is grown or transferred. The substrate is around 300nm thick that leads to negligible capacitance. The change of voltage (ΔV_{FG}) on the FG can be express as in (4). Here, Q_{FG} is the total charge stored on the FG, which can be expressed by (5). To derive the model for the voltage on the floating gate (V_{FG}) we can consider two cases.

$$C_T = C_{FG} + C_{FS} + C_{FD} + C_{FC} \tag{3}$$

$$\Delta V_{FG} = \frac{Q_{FG}}{C_{FG}} \tag{4}$$

$$Q_{FG} = (V_{FG} - V_{GS})C_{FG} + (V_{FG} - V_S).C_{FS} + (V_{FG} - V_D).C_{FD} + (V_{FG} - V_C).C_{FC} \tag{5}$$

Case-1: Floating gate with small overlaps with the source and drain regions. Consider the fringing capacitances (C_{FS} and C_{FD}) between FG and the source and drain as shown in Figure 3-1. Using equations (3)-(5) we can derive the model for V_{FG} as in (6).

$$\mathbf{Q_{FG} = V_{FG}(C_{FG} + C_{FS} + C_{FD} + C_{FC}) - V_{GS}.C_{FG} - V_S.C_{FS} - V_D.C_{FD} - V_{Ch}.C_{FC}}$$

$$\mathbf{Q_{FG} = V_{FG}(C_T) - V_{GS}.C_{FG} - V_S.C_{FS} - V_D.C_{FD} - V_C.C_{FC}}$$

$$\mathbf{V_{FG}.C_T = Q_{FG} + V_{GS}.C_{FG} + V_S.C_{FS} + V_D.C_{FD} + V_C.C_{FC}}$$

$$\mathbf{V_{FG} = \frac{Q_{FG}}{C_T} + \left(\frac{C_{FG}}{C_T}\right).V_{GS} + \left(\frac{C_{FS}}{C_T}\right).V_S + \left(\frac{C_{FD}}{C_T}\right).V_D + \left(\frac{C_{FC}}{C_T}\right).V_C} \tag{6}$$

Case-2: Floating gate is perfectly aligned with the graphene channel with no overlap between FG and source(drain) as in Figure 3-2. The fringing capacitances (C_{FS} and C_{FD}) could be ignored. Then equation (5) can be simplified to (7). Again using equations (3) and (7) we can derive the model for V_{FG} as in (8).

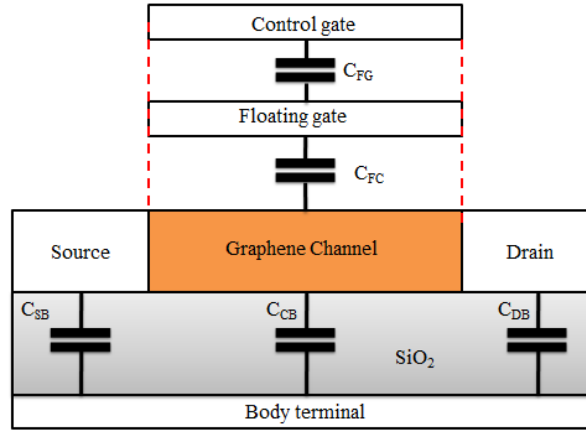


Figure 3-2: Capacitance model for FGT memory cell with no fringing capacitance between FG-drain and FG-source (Case-2).

$$\mathbf{Q_{FG} = (V_{FG} - V_{GS})C_{FG} + (V_{FG} - V_C).C_{FC}} \tag{7}$$

$$\mathbf{V_{FG} = \frac{Q_{FG}}{C_T} + \left(\frac{C_{FG}}{C_T}\right).V_{GS} + \left(\frac{C_{FC}}{C_T}\right).V_C} \tag{8}$$

For convenience, the coupling ratio terms, which are defined as the ratio of terminal voltage coupled to the floating gate, can be defined as follows:

GCR = control gate coupling ratio

DCR = drain coupling ratio

SCR = source coupling ratio

CCR = Channel coupling ratio

Thus, a variation in control gate voltage will result in a change in the floating gate voltage, $\Delta V_{FG} = \Delta V_{CG} \times$ GCR. The basic equation (6) for the capacitor network can be rewriiten in terms of the coupling ratio terms as in (9).

$$V_{FG} = \frac{Q_{FG}}{C_T} + (GCR.V_{GS}) + (SCR.V_S) + (DCR.V_D) + (CCR.V_C) \quad (9)$$

Initially, Q_{FG}=0, and for programming and erasing V_S=0V, $V_D \approx$ 0V. Therefore, V_{FG}=GCR.V_{GS} because the term CCR.V_C is negligible. The GCR is the key parameter, which defines the capacitive coupling ratio between the C_{FG} and the C_T as in (10). For faster programming GCR>0.60. The programming and erasing speed of flash memory depend on V_{FG}. So, it determines how fast a flash memory can be programmed and erased. The minimum programming and earse time of a device can be calculated from V_{FG} value.

$$GCR = \frac{C_{FG}}{C_T} = \frac{C_{FG}}{C_{FG} + C_{FS}} \quad (10)$$

We carefully analyzed the device structure to extract the capacitance model. The planar Graphene/SiO_2/CNT FGT has three additional capacitance in the device structure, because every graphene based device is grown on SiO_2/Si substrate. There are some fundamental changes in the capacitance model of Figure 3-1 for the proposed Graphene/SiO_2/CNT FGT compared to the model for the conventional planar Si/SiO_2/Poly-Si FGT. The values of the bottom capacitors (C_{SB}, C_{CB} and C_{DB}) are very less compared to the values of the top capacitors because of the 300nm thick SiO_2 insulator between the active region of the transistor and the substrate. That is why we have ignored the bottom capacitors (C_{SB}, C_{CB} and C_{DB}).

3.2.I-V Characteristics

The proposed FGT is a special type of the graphene field effect transistor (GFET) with an extra floating gate inserted inside the gate oxide to control the channel in addition to the

conventional control gate (for the regular GFET control gate is the only gate). Therefore, the current-voltage relation for the FGT can be obtained by replacing V_{GS} by V_{FG} in the GFET equations. The relation between V_{GS} and V_{FG} is determined by the capacitive coupling ratio, V_{FG}= GCR.V_{GS}. The current conduction in FGT devices differs from that of the conventional transistor having the same applied voltages because of the additional capacitances i.e. C_{FG}, C_{FS} and C_{FD}.

$$I_{DS} = \frac{We\mu V_{DS}\sqrt{n_0^2 + n^2}}{L + 2We\mu\sqrt{n_0^2 + n^2}\, R_C} \tag{11}$$

The relation between the drain current and voltage (I_{DS}-V_{DS} characteristics) can be given (11). Here, W is the width, e is the electron charge, μ is the mobility, n_o is the intrinsic carrier density, n is the modulated carrier density, L is the device length and R_C is the contact resistance. In previous works on graphene or CNT based FGT designs, detail analysis of I-V behaviors were not included. This paper, for the first time, presents the current-voltage relation in graphene and CNT based FGT. In the proposed FGT model, the contact resistance and top gate effects are included. We considered metal/graphene contact resistance both at the drain and source ends. Additionally, the carrier density, which is usually considered a constant, is estimated by considering both the floating gate, back gate and tunnel oxide effects. Detail derivation of the characteristic equations like (7) is omitted from the body of the paper for brevity. Figure 3-3 shows I_{DS}-V_{DS} characteristic, which suggests that current changes linearly with the drain-source voltage. For graphene device it is standard to set the value of V_{DS} in the range 0~600mV.

The carrier (electrons or holes) density in the source and drain areas are calculated by the equation (12). Where, V_{BG}^0 is the back-gate voltage at the Dirac point (minimum conduction) that determines the doping type and n_0 is the minimum MLGNR sheet carrier

density, which is determined by disorder and thermal excitation [64]-[65]. Ideally, V_{BG}^{0} should be 0V, but it shows a nonzero value due to the impurities in graphene.

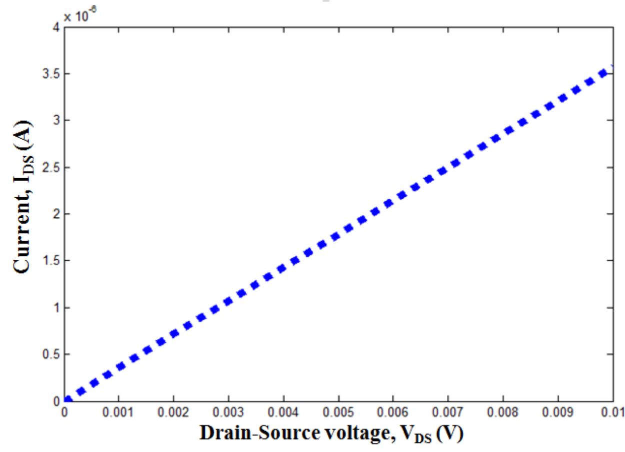
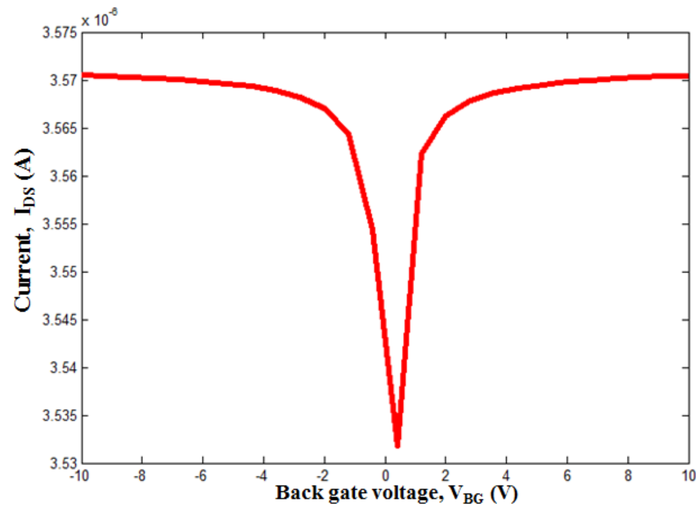
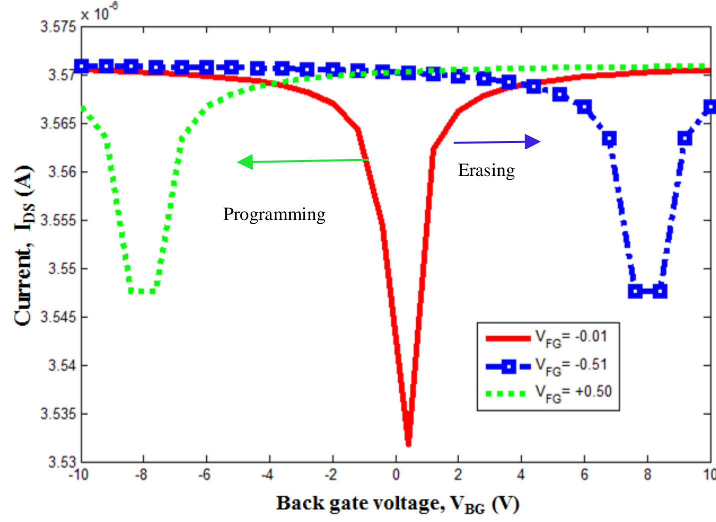


Figure 3-3: The I_{DS}-V_{DS} characteristic of the device. L = 10µm, W = 1.5 µm, V_{DS}=10mV for this computation. The velocity saturation of carriers is not considered in the simulation.



(a) When V_{FG} = -0.01V (≈0V)



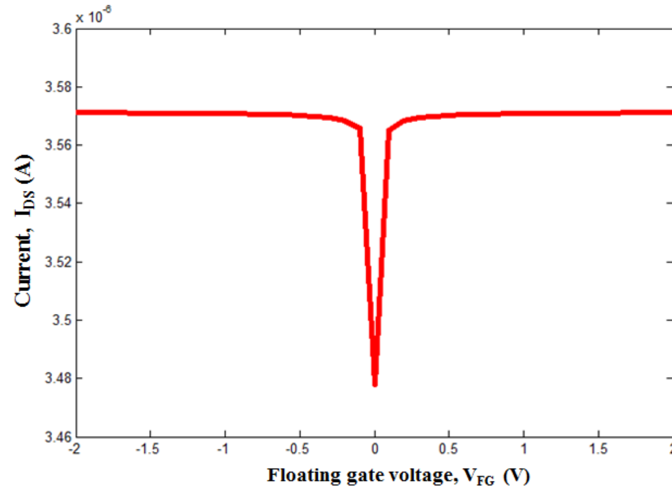
(b) Comparison when V_{FG}= -0.5V, -0.01V (≈0V), +0.51V

Figure 3-4: The I_{DS}-V_{BG} characteristics of the FGT for a fixed V_{DS} and V_{FG}. L = 10µm, W = 1.5 µm, V_{DS}=10mV, n_0=2.25x10^{11} C/m^2 for this computation.

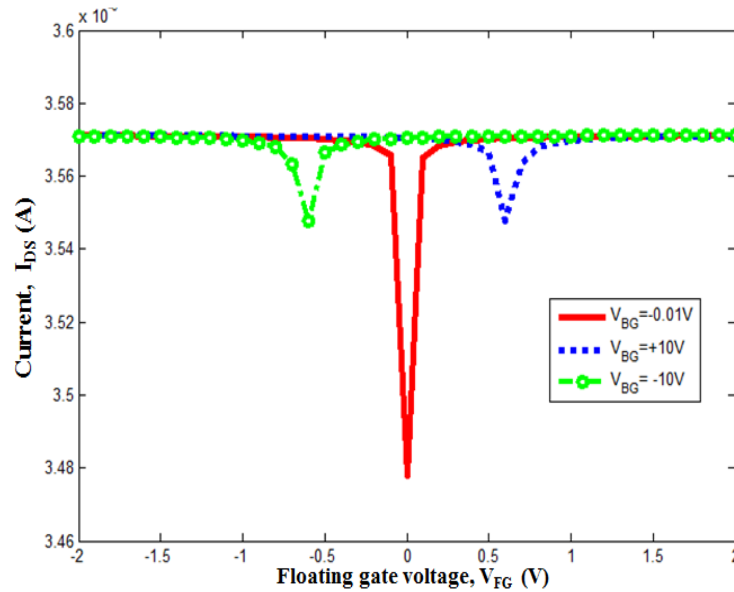
The carrier concentrations are computed by considering the impacts of both the floating gate and back gate voltages, where, C_{FG} is the FG to control gate capacitance per unit area, V_{FG} is the voltage on the floating gate, and V_{FG}^0 is the floating gate voltage at the Dirac point. This formula is used for the precise calculation of the carrier concentration in the FGT channel. I_{DS}-V_{BG} characteristics is shown in Figure 3-4a. The device shows minimum conductivity close to 0V. The same set of computation is done for both the positive and negative V_{FG}. Figure 3-4b shows that the minimum conductivity point shifts to the left for +V_{FG}. On the other hand, the minimum conductivity point shifts to the right for –V_{FG}. The I_{DS}-V_{BG} characteristic is highly dependent on the back gate oxide thickness. In order to realize the back gate influence, the back gate oxide should be thin enough to increase the carrier density in the channel. According to (12), C_{BG} would be close to zero if the back-gate-oxide is thicker and as a consequence, the

back gate tends to lose its control on the device operation. For graphene devices, 300nm thick SiO_2 back gate dielectric is the standard.

$$n \cong \sqrt{{n_0}^2 + [\frac{C_{BG}(V_{BG} - {V_{BG}}^0) + C_{FG}(V_{FG} - {V_{FG}}^0)}{e}]^2} \quad (12)$$



(a) When $V_{BG} \approx 0V$



(b) Comparison when V_{BG}= -10V, ≈ 0V, +10V

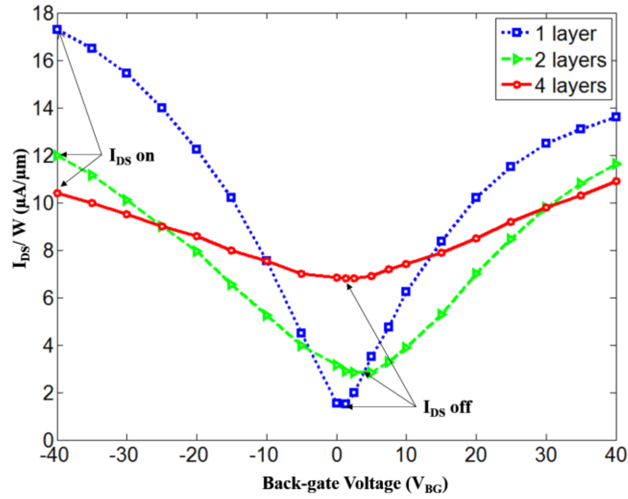
Figure 3-5: The I_{DS}-V_{FG} characteristics of the FGT for a fixed V_{DS} and V_{BG}. L = 10μm, W = 1.5 μm, V_{DS}=10mV, n_0=2.25x10^{11} C/m^2 for this computation.

The effect of the floating gate voltage can be explained by I_{DS}-V_{FG} curve as shown in Figure 3-5a. The variation of I_{DS}-V_{FG} characteristics for different V_{BG} values is also observed as shown in Figure 3-5b, which shows that the minimum conduction point shifts upward when $V_{BG} \neq 0V$. The result also suggests that the minimum conductivity point shifts to the left when V_{BG} is positive. But the minimum conductivity point shifts to the right when V_{BG} is negative.

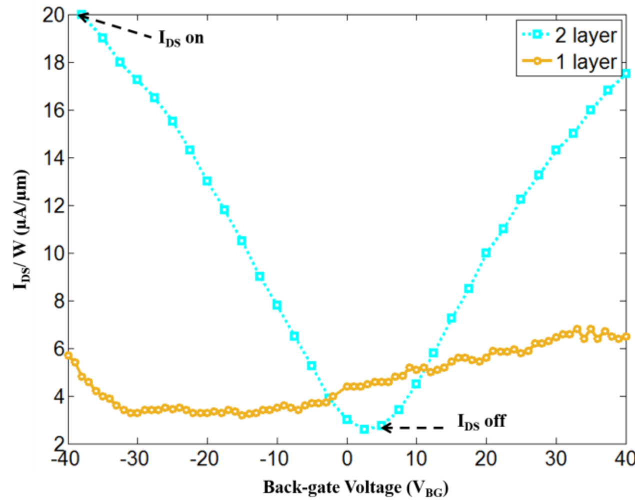
Therefore, the I_{DS}-V_{BG} and I_{DS}-V_{FG} curves show similar behavior but not identical because of the differences in the oxide parameters. If the same top gate and back gate dielectrics with identical geometric parameters are used, then these two characteristics would be identical. The ON-OFF current ratio of the proposed device is small because of the low bandgap of graphene. Researchers are actively working to find ways to increase graphene bandgap. Recently, the bandgap of graphene is opened up to 1.0 eV [66]. Therefore, the ON-OFF current ratio of the proposed device is expected to increase if this wide bandgap graphene is used in our design.

3.3.Layer-by-layer I-V Characteristics Comparison

To realize the MLGNR channel characteristics of the proposed FGT, the current-voltage curve of the device is plotted as a function of the back-gate voltage and the number of MLGNR layers. In the sub-µm regime, the single layer GNR channel device shows better on/off ratio than the multilayer GNR channel device (Figure 3-6a). But, in the sub-nm regime, the single layer GNR channel device is prone to noise (Figure 3-6b).



(a) Sub-μm channel



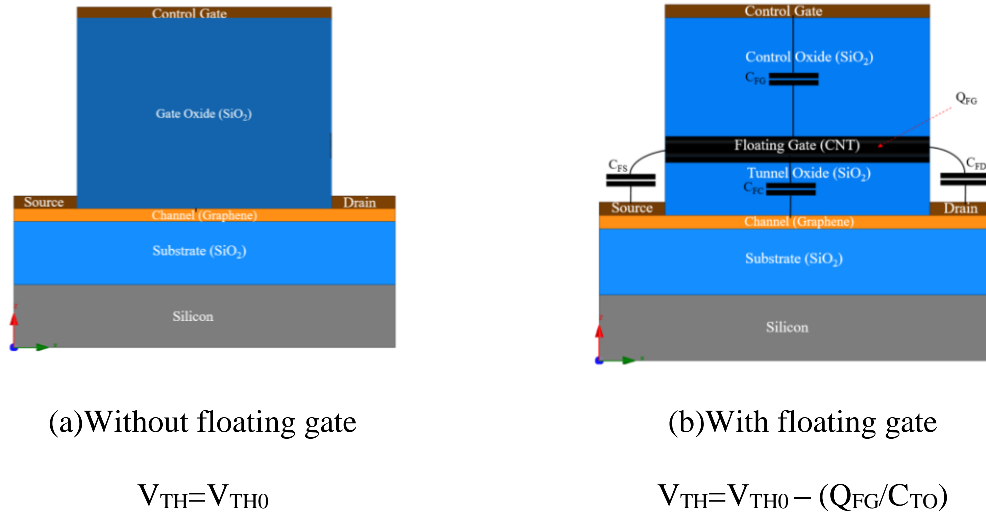
(b) Sub-nm channel

Figure 3-6: Layer-by-layer I_{DS}-V_{BG} characteristics comparison of the long multilayer graphene nanoribbon channel transistor. This figure is adopted from [67].

3.4. Threshold Voltage (V_{TH})

Figure 3-7 shows the side by side comparison between a regular GFET without the floating gate and the proposed FGT with the floating gate. FGT has a charge, Q_{FG}, at a distance,

X_{TO}, from the graphene channel. V_{TH} in the FGT depends on the quantity of charge per unit area, the separation distance of the charge layer from the MLGNR surface, and the permittivity of the oxide between the charge layer and MLGNR channel. The regular GFET does not have the option to achieve different V_{TH} for memory applications. In a flash memory, the floating gate offers a suitable zone for the charge trapping, which can be used to obtain different values of V_{TH}. There are other devices that serve the similar purpose. For example, the silicon oxide nitride oxide silicon (SONOS) transistor traps charges within the nitride layer.



(a)Without floating gate

$V_{TH}=V_{TH0}$

(b)With floating gate

$V_{TH}=V_{TH0} - (Q_{FG}/C_{TO})$

Figure 3-7: The threshold voltage shift (ΔV_{TH}) because of the charge in the floating gate.

The threshold voltage controls the source-to-drain current of a transistor as a function of the control gate voltage (V_{GS}). The window of the flash memory is defined as the threshold voltage change (ΔV_{TH}) between the erased state and the programmed state. This is the voltage gap, which must be reliably distinguished by the sense amplifier [33]. In a graphene flash memory, ΔV_{TH} is basically the added voltage needed to compensate the trapped charges underneath the control oxide induced by the programming process. ΔV_{TH} can be expressed as in (13). Here, X_{TO} and ε_{TO} are the thickness and the permittivity of the control oxide, A is the

area of the floating gate, and ΔQ_{FG} is the stored charge after programming. By using this relation between ΔV_{TH} and ΔQ_{FG}, stored charges in the flash memory can be estimated.

$$\Delta V_{TH} = \frac{X_{TO}}{\varepsilon_{TO}}\left(\frac{1}{A}\right)\Delta Q_{FG} \tag{13}$$

Here, X_{TO} and A are the device dimension parameters, which are fixed after the device fabrication. The variation of ΔV_{TH} in terms of tunnel oxide thickness is illustrated in Figure 3-8. It is observed that ΔV_{TH} increases linearly with the tunnel oxide thickness. For tunnel oxide thickness in contemporary FGT devices, 5nm is a standard value, because below 5nm the tunneling current increases significantly, which leads to the device oxide breakdown. Again, the programming and erasing voltage will be high for tunnel oxide thickness above 5nm. Therefore, carefully selecting the correct value of X_{TO} is crucial. Figure 3-8 shows that V_{TH} value is 0.065V for 5nm tunnel oxide thickness. Figure 3-9 shows that ΔV_{TH} is a strong function of the floating gate area. It is observed that low floating gate area is required when higher ΔV_{TH} is desired.

Figure 3-10 shows that ΔV_{TH} and ΔQ_{FG} exhibit a linear relationship. ΔQ_{FG} is the only parameter that can alter ΔV_{TH} after device fabrication. High charge accumulation on the floating gate leads to high ΔV_{TH}. The magnitude of V_{TH} shift, from 0 to 1 state, refers to the memory window. Higher memory window is desired for the optimum FGT performance.

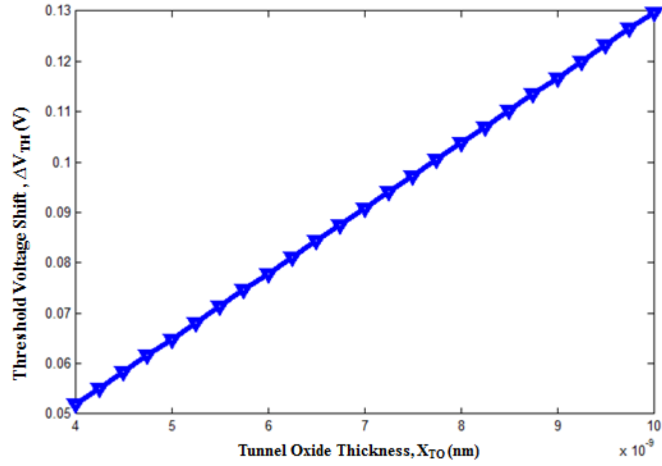


Figure 3-8: The threshold voltage variation (ΔV_{TH}) in terms of the tunnel oxide thickness (X_{TO}). A=2.5x10^{-8}m^2, ΔQ_{FG} = 1.12×10^{-11}C.

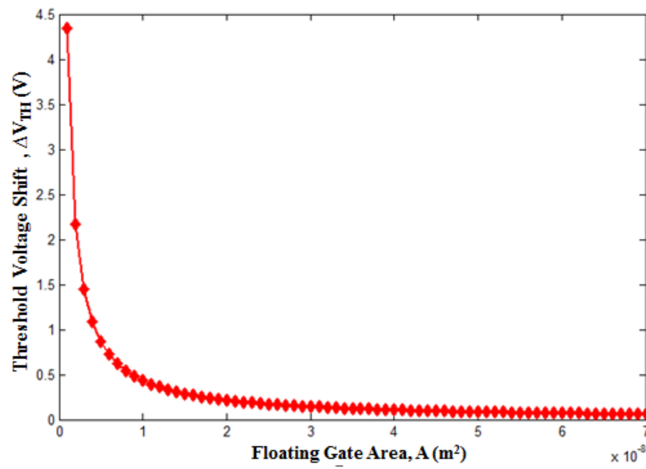


Figure 3-9: The threshold voltage variation (ΔV_{TH}) in terms of the floating gate area (A). When X_{TO} =5nm, ΔQ_{FG} = 3x10^{-11}C.

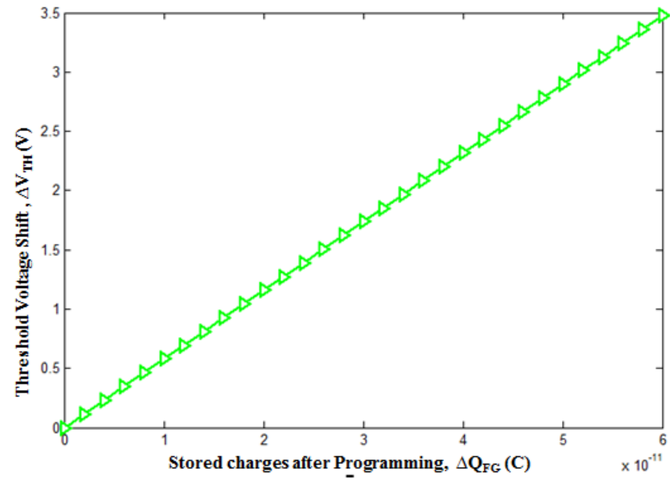


Figure 3-10: The threshold voltage variation (ΔV_{TH}) in terms of the stored charges after programming (ΔQ_{FG}). When X_{TO} =5nm, A=2.5x$10^{-8}m^2$.

Chapter 4 : Programming and Erasing Operation of the Proposed Graphene Flash Memory Device

4.1.Programming and Erasing Mechanism

In the proposed floating transistor the logic ‘0’ and ‘1’ states are determined by the programming and erase operations respectively. Under the influence of a positive control gate voltage electrons are accumulated on the floating gate (programming) that translates to logic state ‘0’. A negative voltage applied at the control gate leads to the depletion of electrons (erase) that translates to the logic state ‘1’. The electron accumulation and depletion are accomplished by tunneling - a process by which an electron passes through a barrier without physical conduction path. Ideally, an insulating oxide barrier doesn’t allow charge to pass through it. However, at high electric field and thin oxide thickness tunneling takes place. The tunneling effect becomes more prominent as device dimensions enter deep into nanometer scale while electric field strength is on the rise as supply voltage scaling is slowed. While for non-memory device tunneling through gate oxide is an undesired phenomenon the operation of floating gate transistors in nonvolatile memory is dependent on tunneling. Therefore, analyzing the tunneling mechanism in the proposed MLGNR/CNT based FGT is a very critical part of understanding its programming and erasing operation and the evaluation of our concept.

4.2.Why Fowler Nordheim (FN) Tunneling Mechanism for Programming and Erasing?

There are several mechanisms that allow charge to pass through insulating oxide. FN programming is achieved by applying a high voltage (around 15-20V for conventional CMOS FGT) at the control gate terminal while drain, source and bulk are grounded. For oxide layers thicker than 6nm, the tunneling current mechanism is explained by Fowler-Nordheim electron

tunneling in MOS structures [31]. The Fowler Nordheim tunneling mechanism is widely used in non-volatile memory (NVM) for mainly three reasons: (i) tunneling is a pure electrical phenomenon, (ii) it requires very small programming current (< 1nA) per cell thus allowing many cells to be programmed at a time [33], and (iii) it allows very fast programming, which is a fundamental requirement for NVM technologies. FN tunneling is adopted in NAND flash memory, which is the most popular, dense and cost effective.

Channel hot electron (CHE) programming consists of applying a relatively high voltage (4~6 V for CMOS FGT) at the drain and a higher voltage (8~11 V for CMOS FGT) at the control gate while source and body are grounded. With this biasing condition a fairly large current (0.3 to 1 mA for CMOS FGT) flows in the cell and the hot electrons generated in the channel acquire sufficient energy to jump the gate oxide barrier and get trapped into the floating gate. Most NOR-type Flash memories utilize CHE programming. A third tunneling phenomenon, known as direct tunneling, can take place with ultra-thin oxide layers (2-5nm) at low or no biasing voltages [32]. There is a debate whether FN or direct tunneling is appropriate for 5nm~6nm oxide thickness because some researchers demand that FN tunneling is dominant for oxide thickness ≥ 4nm [26]. It is evident that FN tunneling is more dominant than direct tunneling when high electric field is applied. Most of the emerging NVM designs use a programming voltage around 15-20V. To be in coherence with the currently used programming voltage we anticipate using a programming voltage around 15V in our proposed design. That's why we mainly focus on FN tunneling based programing.

4.3.How Fowler Nordheim (FN) Tunneling Works?

Fowler-Nordheim tunneling is the process where electrons tunnel through a barrier (gate oxide of a transistor) under the influence of a high electric field. It is a quantum mechanical process, where the electrons are injected by tunneling into the conduction band of the oxide through a triangular energy barrier (Figure 4-1). At high electric field band-bending takes place that results in apparent thinning of the barrier.

The defining parameter for FN tunneling is the potential drop (V_{OX}) across control oxide. V_{OX} should be greater than the barrier ($V_{OX} > \Phi_B$). The carriers (electrons) see a triangular barrier as in Figure 4-1. The tunneling current (J_{FN}) is dependent on the barrier (Φ_B) seen by the carriers from the channel and the electric field across tunnel oxide as illustrated in (1). The dependence is dominated by the exponential term. From (1), it is observed that J_{FN} depends exponentially on Φ_B. Therefore, higher Φ_B leads to significantly lower J_{FN}. Higher electric field (E) leads to larger tunneling current. Very high control gate voltage (V_{GS}) is used in order to realize only the Fowler-Nordheim tunneling effects on the device operation while effects from other sources are minimized.

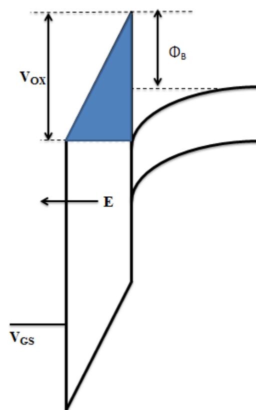


Figure 4-1: Fowler-Nordheim tunneling band diagram.

$$J_{FN} = \frac{k_1 E^2}{\emptyset_B} \exp\left(\frac{-k_2 \emptyset_B^{\frac{3}{2}}}{E}\right) \tag{14}$$

$$C_T = C_{FC} + C_{FS} + C_{FB} + C_{FD} \tag{15}$$

$$V_{FG} = (GCR.V_{GS}) + \frac{Q_{FG}}{C_T} \tag{16}$$

During the programming let us consider that the initial charge Q_{FG}=0. With a voltage V_{GS}=15V at the control gate of the MLGNR-CNT FGT and a GCR value of 0.6 the value of V_{FG} would be 9V according to (3). This would lead to a voltage scenario as in Figure 3-1 that will result in a large tunneling current density (J_{in}) from the channel to the floating gate. On the other hand outward tunneling current density (J_{out}) is comparatively low because of the lower potential difference (15V-9V=6V) and thicker insulating oxide layer between the floating gate and the control gate. The thickness of the control oxide is always greater than the tunnel oxide. Therefore, J_{in} is much higher than J_{out} (Figure 4-2.). The relative strength of J_{in} and J_{out} are drawn along the Y-axis in Figure 4-2 for illustration.

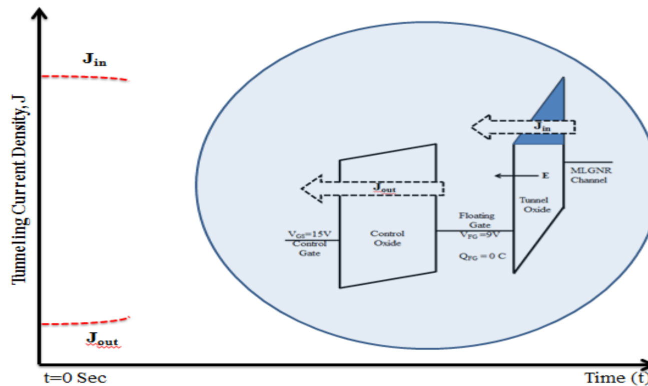


Figure 4-2: Tunneling current in time. Tunneling mechanism is shown in the insert at t=0 Sec.

As time progresses, more electrons are accumulated on the floating gate taking its potential below 9V (which was the potential of the floating gate for a given GCR and programing voltage when there was no charge accumulation). Negative charge accumulation on floating gate lowers V_{FG}, which leads to lower potential difference between the source and the floating gate. As a consequence J_{in} decreases gradually as shown in Figure 4-3. However, during this process the potential difference between the floating gate and the control gate increases, which leads to higher J_{out} as shown in Figure 4-3. As long V_{FG} is larger than the potential difference between the control gate and the floating gate J_{in} remains larger than J_{out}. At one time point $t = t_{sat}$ J_{in} will be equal to J_{out}. The negative charge accumulated at t_{sat} when J_{in}=J_{out} represents the maximum charge that can be accumulated on the floating gate. This provides the range of programing voltage and time. The device will not useful as a nonvolatile memory cell for the range where J_{in}<J_{out}.

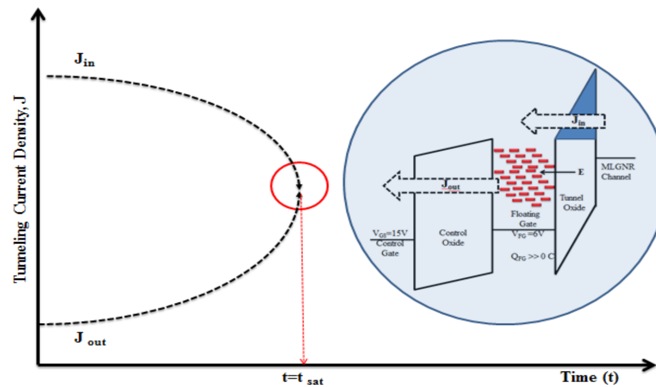


Figure 4-3: Tunneling current in time.

An important part of this analysis is to estimate J_{in} and J_{out}, both of which can be modeled as FN tunneling current. One of the most widely approached FN tunneling current (J_{FN}) in the MOSFET structure is the Wentzel-Kramers-Brillouin (WKB) approximation as

shown in (4) [28]. The parameters A and B depend on the work function or the barrier height (Φ_B) at the interface between the tunneling oxide and the electron emitter and the effective mass of the tunneling electron m_{ox}. The work function is a property of the surface of the material. It depends on the crystal structure and the configurations of the atoms at the surface. A and B can be derived from FN plot (J_{FN}/E^2 vs. 1/E) as in [26]-[28].

4.4.Methodology of the Programming and Erasing Current Density Simulation

The Fowler Nordheim (FN) mechanism is mostly used to realize programming and erasing current density (J_{FN}) of a floating gate transistor structure [28]. The programming and erasing tunneling current density (J_{FN}) can be calculated by (17)-(20). The parameters A and B depend on the work function or the barrier height (Φ_B) at the interface between the tunneling oxide and the electron emitter and the effective mass of the tunneling electron m_{ox}. The work function is a property of the surface of the material. It depends on the crystal structure and the configurations of the atoms at the surface. A and B can be derived from FN plot (J_{FN}/E^2 vs. 1/E) as in [26]-[28]. Here, the induced electric field E is given by (18). By replacing E in (17) we get J_{FN} as in (19). For source voltage V_S =0V, J_{FN} will be given by (20).

$$J_{FN} = AE^2 \exp[-\frac{B}{E}] \quad (17)$$

Here, $A = \frac{q^3}{16\pi^2 h \emptyset_B}$ and $B = \frac{4}{3}\frac{(2m_{ox})^{\frac{1}{2}}}{qh}\emptyset_B{}^{\frac{3}{2}}$

$$E = \frac{V_{FG} - V_S}{X_{TO}} \quad (18)$$

$$J_{FN} = A(\frac{V_{FG} - V_S}{X_{TO}})^2 \exp[-\frac{B}{(\frac{V_{FG}-V_S}{X_{TO}})}] \quad (19)$$

$$J_{FN} = A(\frac{V_{FG}}{X_{TO}})^2 \exp[-\frac{B}{(\frac{V_{FG}}{X_{TO}})}] \quad (20)$$

4.5.Programming and Erasing Operation

The subsequent paragraphs present the analysis of tunneling current during the programming and erasing operation of the proposed floating gate transistor based on the above models.

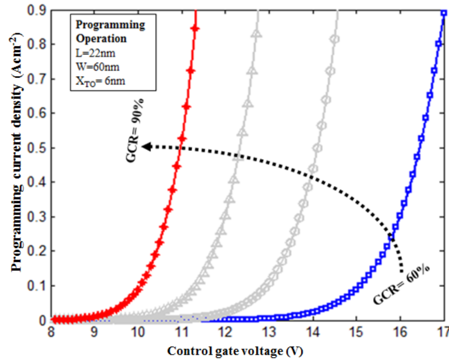


Figure 4-4: The programming current density versus control gate voltage for four different GCR.

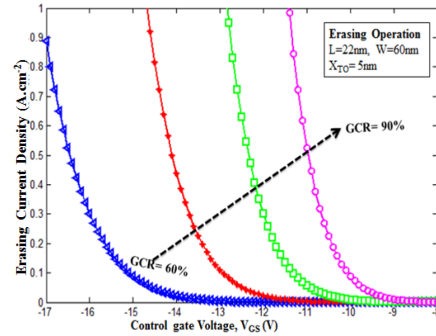


Figure 4-6: The erasing current density versus Control gate voltage for four different GCR (%). X_{TO}=5, V_{GS} <0V.

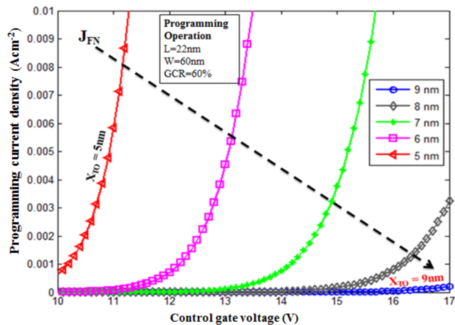


Figure 4-5: The programming current density versus control gate voltage for five different tunnel oxide thicknesses (X_{TO}).

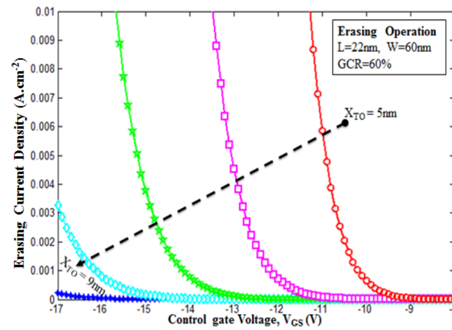


Figure 4-7: The erasing current density versus control gate voltage for five different

Here, GCR=60%, V_{GS} =10-17V.

tunnel oxide thicknesses (X_{TO}). GCR=60%, $V_{GS} < 0$V.

Figure 4-4 shows the dependence of the programming current density on the control gate voltage for a given control gate coupling ratio (GCR). This set of graph is generated from equation (9) and (20). The programming current increases with the increase of both the control gate voltage and GCR (Figure 4-4). Figure 4-5 shows the programming current variation with V_{GS} for different tunnel oxide thickness (X_{TO}). It is observed that for a given X_{TO}, the programming current increases with V_{GS}. However, the programming current increases significantly when X_{TO} is less than 7nm. According to ITRS 2011, semiconductor industry has already adopted 6nm tunneling oxide for 18-nm and 22-nm technology nodes. While 5nm tunnel oxide is predicted for 8-14nm technology nodes. Therefore, for technology nodes below 20nm, high programming current density will affect the reliability of the tunnel oxide.

During the erasing operation a negative voltage would be applied at the control gate. We have performed the same set of analysis (as in Figure 4-4 and Figure 4-5) for the erasing operation. Figure 4-6 shows that erasing current increases as the control gate voltage (V_{GS}) becomes more negative for a given GCR. Higher GCR leads to higher current density because large control gate coupling will increase electron depletion rate from the floating gate to the MLGNR channel. Figure 4-7 shows the erasing current variation with V_{GS} for different X_{TO}. It is seen erasing current density increases with the increase of V_{GS} in the negative direction for a given X_{TO}. The tunneling current increases significantly when X_{TO} is less than 7nm similar to the programing operation.

Chapter 5 : Reliability Analysis of the Proposed Graphene Flash Memory Device

5.1.Retention Characteristics

After programming a flash memory, how long trapped charges will be trapped in the FG? This time is defined by the retention time. The nonvolatile memory retention characteristics of the floating gate transistors (FGT) are strong function of both applied drain voltages and tunnel oxide thickness. It is realized that a high drain voltage can accelerate the charge loss mechanism for FGT. In the retention characteristic experiment, the floating gate (FG) is extended to the drain region intentionally, which allows clear realization of the leakage current from FG to drain.

The charge-retention V_{TH} equation is derived based on the assumption that Fowler-Nordheim tunneling through the tunnel oxide is the only charge loss mechanism [68]. This expression permits the charge retention characteristics to be projected for a floating-gate transistor with thin gate oxide which is operated under bias conditions. It is shown that the retention time is related to both the bias voltages and the device parameters, specifically the control oxide thickness and capacitances. FGT is “programmed” into the high threshold voltage (V_{TH}) state by electrically injecting electrons into the FG. After the injection, these electrons ideally should be stored on the FG for more than 10 years at room temperature, which is the industry standard for a standard flash memory. However, such extended retention time may not be achieved if the control gate is connected to the ground while the drain terminal is biased positive. Under such environments, these electrons slowly leak out by the Fowler-Nordheim tunneling process. This leakage current mainly flows through the thin tunnel oxide

between the FG and the drain region. The leakage current density (J) can be estimated by (21). is associated to the electrical field across the thin tunnel oxide as

$$J = AE^2 \exp(-\frac{B}{E}) \tag{21}$$

Here A and B are two constants, E is the electrical field, which is defined by (22). A and B constants are calculated from the I-V characteristics.

$$E = \frac{V_D - V_{FG}}{X_{T0}} \tag{22}$$

Here, V_{FG} is the FG voltage, V_D is the drain voltage, X_{TO} is the thin tunnel oxide thickness. The FG voltage (V_{FG}) is calculated by (23). The FG charge (Q_{FG}) of any time (t) is estimated by (24).

$$V_{FG} = \frac{C_{FD}V_D - Q_{FG}(t)}{C_T} \tag{23}$$

$$\text{With} \qquad Q_{FG}(t) = Q_0 - P\int J(t)dt \tag{24}$$

Here, C_{FD} is the capacitance between the drain and FG. C_T is the total capacitance on the FG, and P is the area of the thin oxide between drain and FG. J(t) and Q_{FG}(t) are function of time.

The threshold voltage (V_{TH}) of the FGT is the minimum voltage, which creates conduction channel between source and drain. Therefore, V_{TH} is the minimum value of the V_{FG}. The the threshold voltage (V_{TH}) equation (25) is derived by solving (21)-(24).

$$V_{TH}(t) = V_{T0} - \left(1 - \frac{C_{FD}}{C_T}\right)V_D + (\frac{C_T}{C_{FG}})\frac{bX_0}{\ln[\frac{Pabt}{X_0C_T} + \exp(H)]} \tag{25}$$

With

$$H = \frac{bX_0}{\left[V_D\left(1-\frac{C_{FD}}{C_T}\right)+(V_{Ti}\ -V_{T0})\right]\frac{C_{FG}}{C_T}}$$

Where V_{T0} is the threshold voltage with no electrons on the floating gate, V_{Ti} is the threshold voltage with initially stored electrons and C_{FG} is the capacitance between the control gate and the floating gate. According to (25), the charge-retention characteristic is sensitive to the device parameters, including X_{T0}, P, C_T, C_{FD}, and C_{FG}, and V_D.

Figure 5-1 shows the threshold voltage (V_{TH}) variation of FGT as a function of the retention time. It is clearly shown that only <20% data loss after 10 years when tunnel oxide thickness is 5nm (blue curve). The same set of analysis is done for X_{TO}=10nm, which also shows similar result. Therefore, this flash memory shows industry standard performance.

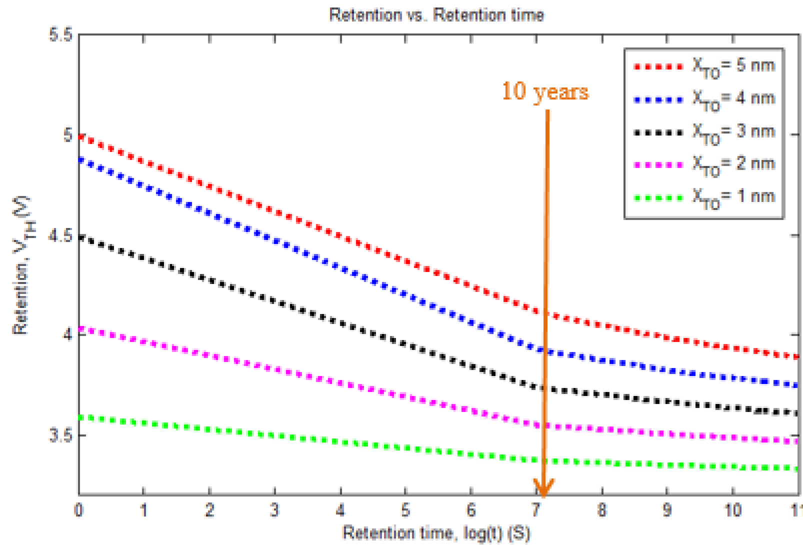


Figure 5-1: V_{TH} variation of FGT with the retention time. The parameter is the tunnel oxide thickness.

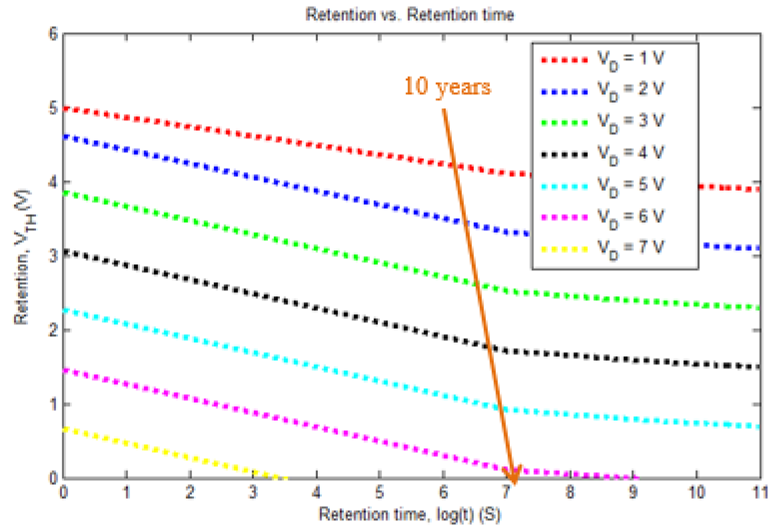


Figure 5-2: V_{TH} variation with the retention time for the Si/MLGNR. X_{TO} =10nm. The parameter is the Drain voltage (V_D).

Computations from (25) have been carried out for the FGT. The charge retention curves calculated for the FGT under different drain bias conditions are shown in Figure 5-2. It is clearly seen that higher drain voltage can significantly reduce the charge retention time. Similar calculations for a device operated with a fixed drain voltage but with tunnel oxide thicknesses (X_{TO}) ranging from 10 nm to 5 nm are shown in Figure 5-1. It is observed from Figure 5-1 how strongly retention time depends on the tunnel oxide thickness.

Chapter 6 : Radiation Hardness Analysis of the Floating Gate Transistor

As the device size is shrinking down to nanometer range, the impacts of radiations on circuit and device performance and reliability would become more prominent. In the recent time study of radiation hardness of micro & nano-electronic devices for extreme conditions are gaining wide spread attention. The radiation effect on the floating gate transistor (FGT) used in flash memory leads to charge loss from the programmed floating gate (FG). Due to the imposture to certain type of radiation, an extra electron/hole pair can be generated in the device. For example, a minimum of 10-Kev X-rays exposure would initiate this process. In the FGT, the radiation effect can be neglected if the oxide thickness is 40-47.5 nm [69]. But it is no longer negligible because the oxide thickness is going down to 10 nm in scaled FGTs. Radiation induced charge in the oxide depends on several physical mechanisms i.e. electron-hole pair generation and election-hole recombination. The electron-hole recombination depends on the applied electrical field and linear energy transfer. Even the effect changes over time, i.e. the change of threshold voltage (ΔV_{TH}) varies over the 10^{-6}~10^{8} Sec time scale. When V_G>0V, holes are trapped into the oxide due to the radiation effect. These trapped holes creates conduction, which leads to "ON" state even when V_{GS}=0V [70]. In this research, we have presented how threshold voltage of the FGT is affected by the radiation. To the best of our knowledge, this is the first work to present the analysis of radiation hardness of a flash memory device. An analytical model has been developed, which shows direct relation between radiation level and threshold voltage (V_{th}). This equation directly shows how dynamic characteristics are changed due to the radiation exposure.

6.1. Mechanism of Radiation Effect

The changes in characteristics of a FGT due to radiation can be explained by four major steps as shown in Figure 6-1. The FGT is a modified MOS structure. Therefore, according to device point of view, the radiation effects on the FGT can be explained by the simplified MOS structure.

Step-1: Schematic energy band diagram for MOS structure is illustrated to understand each step of V_{TH} variation. When a positive voltage is applied to the control gate, the electrons flow towards the floating gate and holes to the substrate. Due to irradiation, electron hole pair is generated in SiO_2, which is considered as the most sensitive part in the MOS structure. As electrons are more mobile than hole, they swept out in picoseconds or less. In the first picosecond, recombination of electrons and holes takes place; and holes that escape from recombination are relatively immobile and remain near the point of generation, and these holes cause the negative threshold shift in the MOS transistor. This initial stage leads to the maximum drift in the V_{TH} [70].

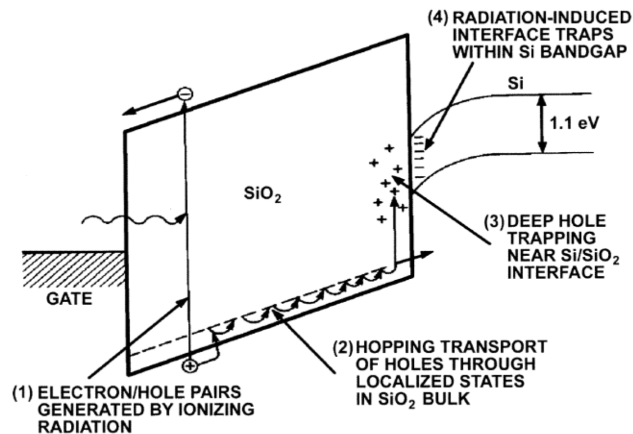


Figure 6-1: The change of band energy inside the FGT under irradiation [70].

Step-2: Holes tends to shift towards Si/SiO_2 interface that causes short-term recovery in the V_{TH}, which depends on mainly applied electrical field, temperature and oxide thickness.

Generally, it takes about 1sec at room temperature but it may need extended time at low temperature [70].

Step-3: Holes reach to silicon interface, fraction of holes transported to deep long lived trap states. These trapped holes cause the threshold voltage to make a negative shift. This effect continues for hours to years. Gradual annealing can recover the memory from this damage [70].

Step-4: The radiation induced traps at the Si/SiO_2 interface are determined by the Fermi level. Generally interface traps are highly dependent on oxide processing [70].

Thus, it can be summarized that radiation induces charge in the oxide, which is dependent on several physical mechanisms like electron-hole pair generation and election-hole recombination. The electron-hole recombination depends on the applied electrical field and linear energy transfer.

6.2. V_{TH} Variation

Figure 6-2 shows the distributions of the threshold voltage (V_{TH}) for the memory device in both programmed ("0") and erased states ("1"). Here the impacts are shown before and after the exposure to radiation. The V_{TH} of the FGT in the programming ("0") state is high because a large amount of electrons are stored in the floating gate. As a consequence, higher control gate voltage is needed to form the channel in the "0" state. In the programming ("0") state, an electron-hole pair needs 17eV energy around the floating gate (FG) and oxide region by photoemission, which is defined by a process where electrons are emitted from solids under irradiation with photons of sufficiently low wavelength and high energy. Under irradiation, the threshold voltage of programming ("0") state reduces uniformly. Therefore, a comparatively

lower control gate voltage creates the conducting channel when the FGT is affected by radiation. On the other hand, the reduction of due to radiation V_{TH} in the erased state (“1”) is less prominent.

Portion of the generated electron-hole pairs are recombined, which depends on the electric field around the oxide. Higher electric field leads to lower recombination as more electrons can escape from the recombination. The photoemission is responsible for injection of holes, which escape from the recombination into the FG. These positive holes are recombined partially with the negative electron in the FG. The electrons, which are stored in the FG, get enough energy to jump over the oxide layer barrier when exposed to radiation and by photoemission [69].

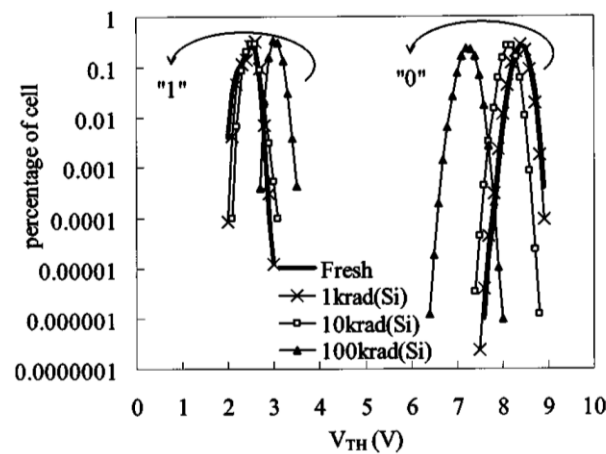


Figure 6-2: Probability distribution of the threshold voltage for the FGT device for both programming and erasing states before and after irradiation [69].

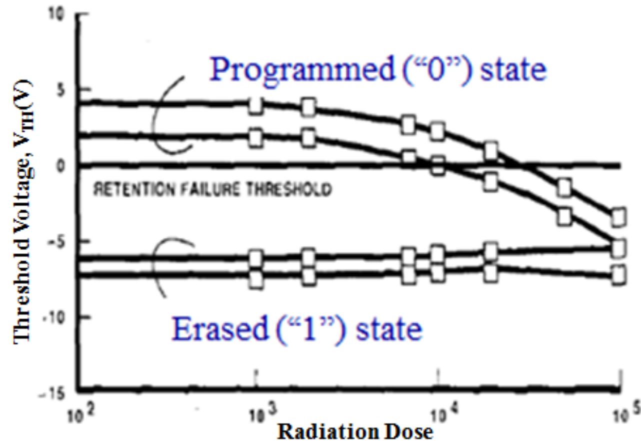


Figure 6-3 : Threshold voltage data as a function of radiation dose [71].

To observe the V_{TH} variation due to radiation effect, in [71] a memory cell is exposed to cobalt-60 radiation with a dose rate greater than 100rad.s^{-1}. The V_{TH} variations are observed over 100krad. The V_{TH} in "0" state is seen to go down significantly even to negative values (see Figure 6-3). While for the "1" state, the V_{TH} increases slightly. Figure 6-3 shows that the V_{TH} in programming state ("0") goes down whereas the V_{TH} in the erasing ("1") state increases slightly due to the radiation effect. Therefore, under high radiation doses the logic "0" can be read as logic "1" incorrectly [71].

6.3. Time Dependent Effect

Even the radiation effect changes over time, i.e. the change of threshold voltage (ΔV_{TH}) varies over the 10^{-6}~10^{8} Sec time scale. Figure 6-4 shows that ΔV_{TH} is not fixed after radiation exposure. When V_{GS}>0V, holes are trapped into the oxide due to the radiation effect. These trapped holes shifts the operation of the FGT "OFF" to "ON" state even when V_{GS}=0V [70]. Therefore, it gives a wrong reading.

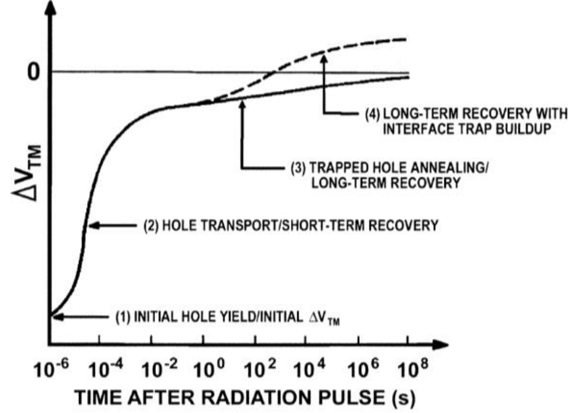


Figure 6-4: Time dependent post irradiation threshold voltage change of the FGT [70].

6.4. Result and Analysis

The change of V_{TH} depends on the charge loss of the FG, which is caused by the photoemission and electron/hole pair generation in the tunnel oxide and control oxide. The change of V_{TH} can be expressed by (26).

$$\Delta V_{TH} = \frac{\Delta Q}{C_{FG}} = \frac{\Delta Q_{TO} + \Delta Q_{CO} + \Delta Q_{PH}}{C_{FG}} \tag{26}$$

Here, ΔV_{TH} is the change of the threshold voltage, ΔQ is the total charge loss, C_{FG} is the capacitance between the floating gate and the control gate, ΔQ_{TO} and ΔQ_{CO} are the charge losses in the tunnel oxide and control oxide respectively, and ΔQ_{PH} is the charge loss due to photo emission.

According to the conventional FGT geometry, the horizontal area of the FG is parallel to the substrate and the lateral area is perpendicular to the substrate. In the existing semiconductor industry, horizontal and vertical FG areas are equal [1]. Radiation causes both electron and hole generation in the surrounding oxides. Therefore, ΔQ_{TO} and ΔQ_{CO} linearly depend on both A_{FGH} and A_{FGV}. ΔV_{TH} depends on charge density per area, rather than on the

absolute number of stored electrons [9]. In principle, photoemission can happen wherever the electric field is nonzero, i.e., it can depend on both the planar and lateral dimensions of FG. Equation (1) can be rewritten as in (2).

$$\Delta V_{TH} = \frac{(\Delta Q_{TO}).(A_{FGH})+(\Delta Q_{CO}).(A_{FGH})+(\Delta Q_{PH})}{C_{FG}} \quad (27)$$

Here, A_{FGH} is the horizontal area and A_{FGV} is the vertical area of the floating gate. Here, C_{FG} is the function of thickness and process of the control oxide. It should be noted that ΔV_{TH} equation of FGT is completely different from charge trap memory, which explained in [69], because of the structural and charge trapping mechanism differences.

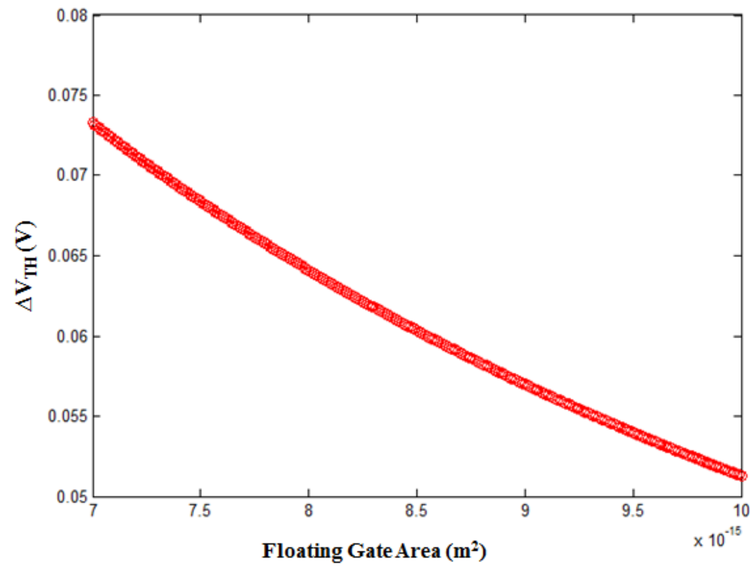


Figure 6-5: ΔV_{TH} variation as a function of the floating gate area.

Figure 6-5 shows ΔV_{TH} variation with respect to floating gate area for a fixed radiation exposure and oxide thicknesses. It is observed that ΔV_{TH} is inversely proportional to the floating gate area. 20 nm thick SiO_2 control oxide is considered for the computation. The floating gate area, A_{FG} is varied from 0.007~0.01μm^2. The above-mentioned values are

industry standard, which leads to better ΔV_{TH} estimation. For convenience, the radiation exposure is assumed fixed and the fringing effects are neglected.

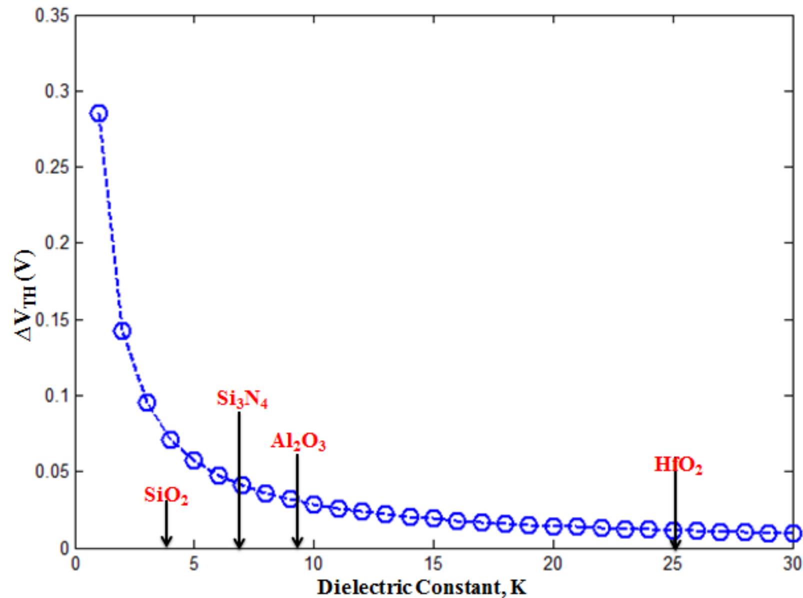


Figure 6-6: ΔV_{TH} shift as a function of dielectric constant.

Figure 6-6 illustrates how threshold voltage changes for different oxide materials. It clearly shows that high-K oxides exhibits low V_{TH} shift which leads high radiation hardness. Therefore, high-k oxide is recommended as the control oxide to make the circuit radiation hard. A comparative study is done for the most popular oxides [73] (SiO_2, Si_3N_4, Al_2O_3 and HfO_2) in the current semiconductor industry. This study suggests that if high k-dielectric oxide is used as the control oxide, the V_{TH} variation tends to be less and at a certain higher value of dielectric constant (k) the variation tends become zero, which leads to better radiation hardness. According to the analysis, HfO_2 is the best control oxide choice for flash memory when radiation hardness is the major concern.

Many researches have shown that how V_{th} changes after the device is kept under radiation. For CAD tool and IC designer community it is required to translate the radiation effect quantitatively. Keeping that in mind, we have considered a black box where a FGT/MOSFET is kept as shown in Figure 6-7. The role of the model is to compute V_{TH} values for increasing radiation levels for given device which is already fabricated or designed i.e. other parameters will not change. We are stable to the condition because the experimental results which are available followed the approach.

Figure 6-7: Black box of a flash memory under radiation exposure.

The variation of the V_{TH} as a function of radiation data are collected from the experimental results [71],[72]. Then the data is statistically analyzed. These steps and data are not provided in the paper because of space limitation. The statistical analysis is concluded by the result shown Figure 6-8, where x-axis presents TID (dose of radiation in the Krad(SiO_2) unit) and y-axis represents V_{TH}.

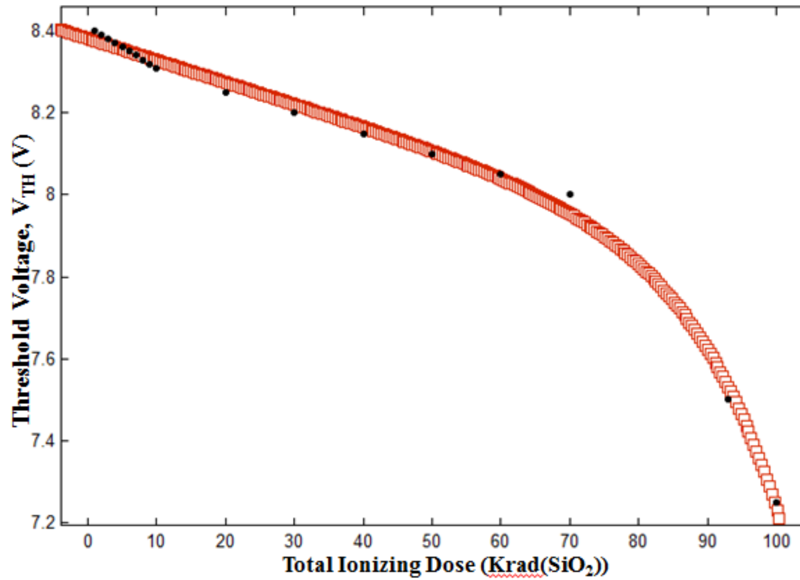


Figure 6-8: Threshold shift as a function of total ionization dose (TID).

Figure 6-8 shows that V_{TH} decreases as a function of the radiation level. As the radiation exposure increases, V_{TH} tends to fall rapidly. The black dots are the experimental value collected from [72], while the continuous red curve represents the simulated result. It should be noted that TID(Krad(SiO_2)) is a well-defined universal radiation measurement unit, which is very popular in experimental and commercial radiation measurement. In order to validate the model, the result is verified with experimental research works. The simulated result of the V_{TH} variation with radiation shows good agreement with the experimental data of [71],[72].

Chapter 7 : Benchmarking of the Proposed Graphene Flash Memory Device

7.1. Programming Voltage Benchmarking

The programming tunneling current of our proposed device is compared with the existing FGTs in Figure 7-1. It is clearly shown that our device require less programming voltage than other existing FGTs. Figure 7-1 shows that our proposed MLGNR-SiO_2-CNT FGT can be programmed at a very reduced voltage (13.1V), while no programming (~0 tunneling current in Figure 7-1) is possible for the conventional Si-SiO_2-PolySi FGT [33] and Si-SiO_2-MLGNR [9] FGT. Therefore, for low power programming operation our proposed MLGNR-SiO_2-CNT FGT outperform the existing devices. Under high programming voltage, our MLGNR-SiO_2-CNT FGT gain high programming current for little increment of V_{GS}, while the programming current of the conventional devices [9], [33] increase very slowly which require high $V_{GS.}$ For example, existing FGTs need more than V_{GS}=15V for 0.01 A/cm^2 programming current while our device (red Figure 7-1) needs around V_{GS}=13.1 V only.

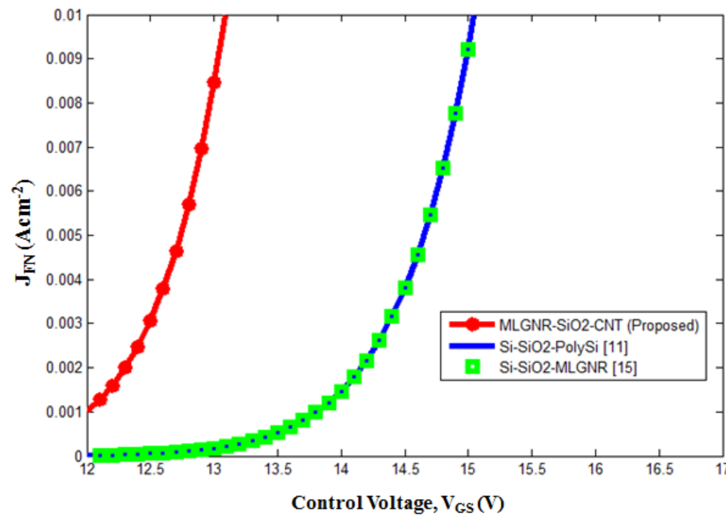


Figure 7-1: Programming Voltage Benchmarking of our proposed MLGNR-SiO_2-CNT FGT design with the existing FGTs.

The reason of the low programming voltage of the proposed FGT is the low channel to Tunnel oxide barrier. According to the Table 7-1, electrons face less barrier (2.75eV) in our proposed design than the conventional silicon FGT (3.07eV) and Si-SiO_2-MLGNR FGT(3.07eV). It is concluded for faster programming and erasing higher FN tunneling current density (J_{FN}) can be achieved by higher control gate voltage and scaling down the thicknesses of the control gate oxide and tunnel oxide. However, higher tunneling current will severely damage the oxide's reliability. Therefore, an optimization among these crucial parameters is recommended. It is also clear that our proposed MLGNR-SiO_2-CNT outperform the existing FGT design including graphene based design.

Table 7-1: Comparative Analysis between Silicon and the emerging FGTs

Channel-Tunnel Oxide-FG	Channel to Tunnel oxide barrier	FG-Tunnel oxide barrier
Si-SiO_2-PolySi [33] [Conventional]	3.07eV	3.07eV
Si-SiO_2-MLGNR [9] [IBM]	3.07eV	3.65eV
MLGNR-SiO_2-CNT (Proposed)	2.75eV	3.65eV

7.2. Power Consumption Benchmarking

The benchmarking is done using identical physical and operating conditions, applied voltage, and tunneling mechanism for the proposed and other FGT devices. The programming power is the power, which is consumed due to the tunneling of electrons from the channel to the floating gate when a high positive voltage is applied at the control gate. The programming power is a function of the programming voltage, channel-to-tunnel oxide barrier-height, tunnel oxide dielectric constant and thickness, control oxide dielectric constant and thickness, and floating gate area. The erasing mechanism is opposite of the programming. The erasing power is required to tunnel electrons from the floating gate back to the channel by applying a high negative voltage at the control gate. The erasing power is a function of the erasing voltage, floating gate to tunnel oxide barrier height, tunnel oxide dielectric constant and thickness, control oxide dielectric constant and thickness, and floating gate area. In the reading mode, minimum power is needed to run the device. Usually much lower control gate voltage is needed in the erasing mode compared to the programming mode. Therefore, the control gate voltage required in the programmed state is used as the reading voltage because it satisfies all conditions.

The benchmarking information of the proposed FGT is shown in the Table 7-2. It can be observed that compared to the conventional silicon FGT and other emerging designs proposed in [9] and [10] the power consumptions of our design in offers a very good trade-off. Our proposed design consumes the least amount of power during the reading mode. In the erasing mode, the power consumption is among the two lowest values. Only in the programing state, the power consumption is higher than two FGT designs included in the comparative

analysis. With proper dimensional optimization and appropriate dielectric material selection the programming power of the proposed design can be significantly reduced.

Table 7-2: Comparison of the power consumption in the proposed MLGNR-CNT FGT and other existing and emerging FGT devices.

Manufacturer		Si-FGT	IBM [9]	Our Design	Andras Kis [10]
Technology Feature		15nm	15nm	15nm	15nm
Programming/ Erasing Voltage		3.3V/ -3.3V	3.3V/ -3.3V	3.3V/ -3.3V	3.3V/ -3.3V
Power Consumption	Programming	0.22nW	0.22nW	0.43nW	3.13nW
	Erasing	0.22nW	0.069nW	0.069nW	1.49nW
	Reading	1.08 nW	1.08 nW	0.036 nW	0.14nW

7.3. V_{FG} Benchmarking

In order to realize floating gate voltage (V_{FG}), we have applied same program-erase voltage (±17V). Simulation result shows that our proposed MLGNR-CNT FGT outperforms other flash memory designs (Figure 7-2). Our analysis shows that our proposed MLGNR-CNT-FGT is able to couple more V_{FG} than MoS_2/Graphene and Si-FGT. The motivation behind this design is the optimized reduced control oxide thickness which leads to high C_{FG} capacitance value. Therefore, high GCR is achieved which further leads to high V_{FG}. Again,

we can boost the performance of our MLGNR-CNT FGT, by using high k-dielectric material (HfO_2/Al_2O_3) as a control oxide while low dielectric material should be used as a tunnel oxide.

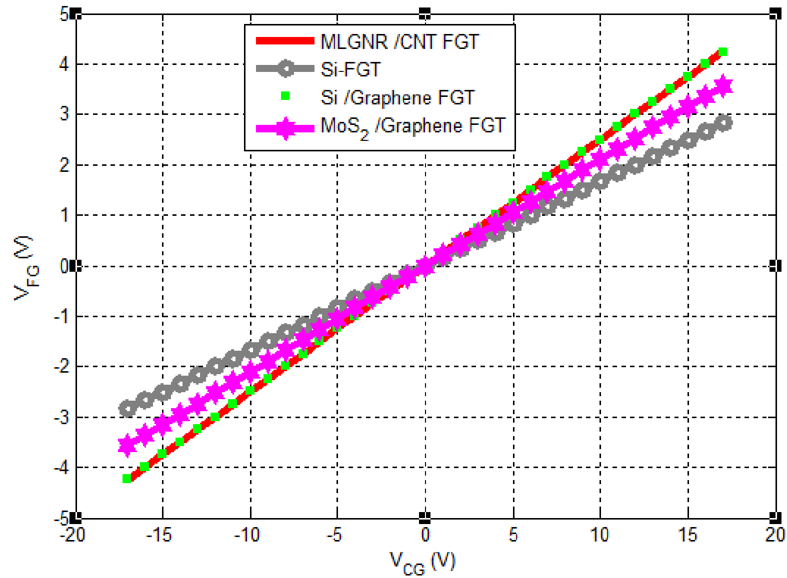


Figure 7-2: The V_{FG} comparison of our proposed MLGNR-Channel CNT FG FGT with the IBM Si- Channel-MLGNR-FG, MoS_2 channel-MLGNR FGT, conventional Si-FGT flash memories. Our Proposed MLGNR-Channel CNT FG FGT shows better performance than

Chapter 8 : Graphene Field Effect Transistor (GFET) Generalized Model

8.1.Generalized Model

The general model of GFET is shown in Figure 8-1. It's a back gate only device, which have gate voltage only at the back gate. Graphene is grown on the SiO_2(300 nm)/Si, which is the standard substrate for GFET. Source and drain metal contact are grown on the Graphene channel.

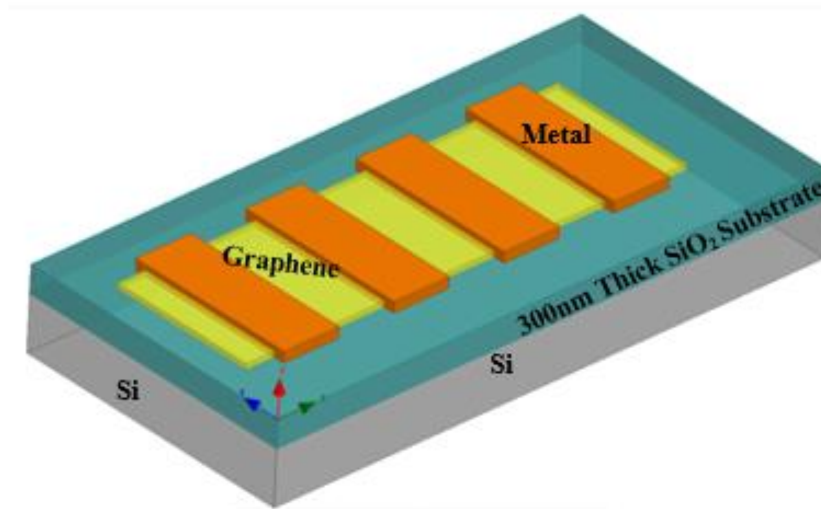


Figure 8-1: GFET general model. Top gate is not shown in the device.

8.2.Limitations

- No general model
- No feasible device
- Only simulate this experimental data
- Major Parameters i.e. voltage, oxide, thickness are not considered
- Dirac point is not considered
- No I-V characteristics equation

8.3. Comparison of Back Gate, Top Gate and Dual Gate GFET

The Back Gate, Top Gate and Dual Gate GFET are shown side by side in Figure 8-2. The comparison between the Back Gate, Top Gate and Dual Gate GFET is shown in Table 8-1.

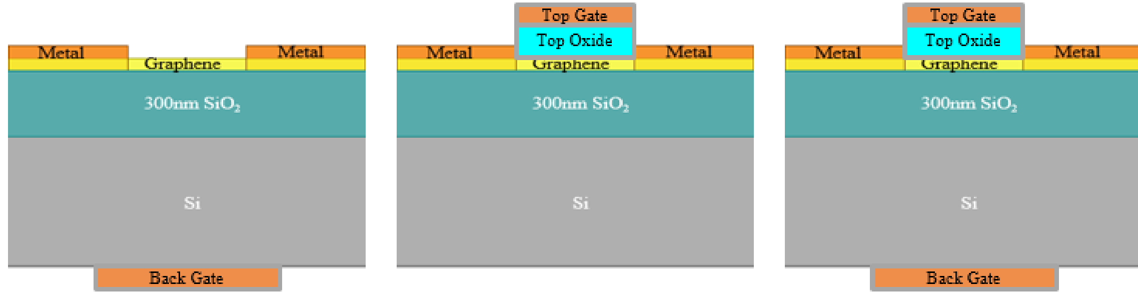


Figure 8-2: The cross-section of the Back Gate, Top Gate and Dual Gate GFET.

Table 8-1: The comparison between the Back Gate, Top Gate and Dual Gate GFET.

Back Gate GFET	Top Gate GFET	Dual Gate GFET
Use Back Gate only	Use Top Gate only	Use both Top and Back Gates
Thick Back Gate oxide i.e.270-300nm	Thin Top Gate oxide i.e.1-10nm	Thick Back Gate oxide i.e.270-300nm & Thin Top Gate oxide i.e.1-10nm
Impractical	Practical	Practical
Most Experimental data available	Insufficient data	Insufficient data
High Gate voltage	Low Gate voltage	Low Gate voltage

Less Electrostatic Control	More Electrostatic Control	Most Electrostatic Control

8.4.Validation

Considering channel resistance contact resistance when top gate and back gate has no influence on the channel, the total resistance (R_T) of GFET between source and drain [60]-[61] can be expressed by the simple registence registor network

$$R_T = R_C + \frac{L}{We\mu\sqrt{n_0^2 + n^2}} \quad (28)$$

Where, R_C is the contact resistance, L is the channel length, W is the channel width, e is the electronic charge, μ is the mobility, n is the modulated carrier concentration and n_0 is the residual carrier concentration. The R_T variation for different V_{BG} is explained in Figure 8-3. Table 8-1 shows the validation of the proposed model. The maximum value of R_T=2.833kΩ is observed. This result shows good agreement with the existing experimental results of [60]-[61], [63].

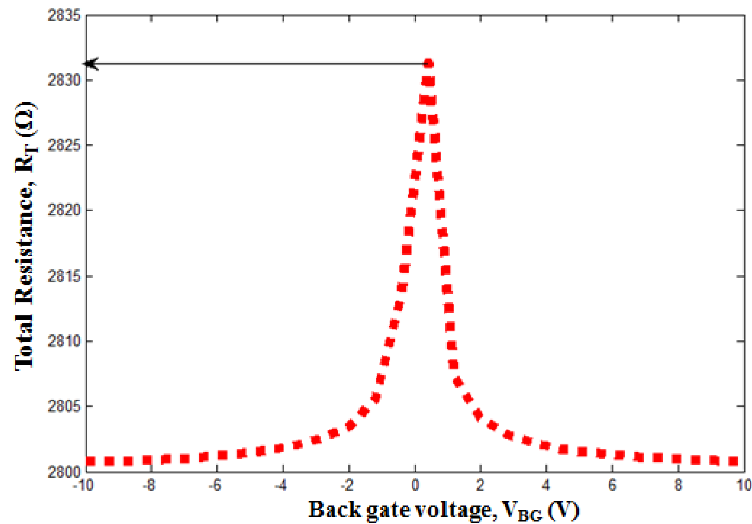


Figure 8-3: The resistance between the source and drain for different back gate voltage (R_T - V_{BG}). L = 10μm, W = 1.5 μm, R_C = 2.8kΩ, μ=7700cm^2/Vs, V_{DS}=10mV for this computation.

Table 8-2: The validation of the proposed model.

V_{BG}	Experimental R_T	Model R_T	% of error
-10	3.5	3.8013	-8.60857
-5	3.6	3.8025	-5.625
0	3.8	3.88	-2.10526
5	3.6	3.8026	-5.62778
10	3.56	3.8013	-6.77809

8.5.Result and Analysis

The R_T can be converted to the I_{DS}-V_{DS} relationship by replacing $R_T=V_{DS}/I_{DS}$, then equation (28) becomes

$$\frac{V_{DS}}{I_{DS}} = R_T = R_C + \frac{L}{We\mu\sqrt{n_0^2 + n^2}}$$

$$I_{DS} = [\frac{1}{R_C + \frac{L}{We\mu\sqrt{n_0^2+n^2}}}]V_{DS} \tag{29}$$

Now, the I_{DS}-V_{DS} characteristic is shown in Figure 8-4. The I_{DS}-V_{DS} curve shows linear behavior. Up to V_{DS} =600mV is the standard drain to source voltage because beyond this limit graphene devices show overheating problem. This result shows good agreement with the existing experimental results of [62] in the low mV range, which is the standard operating condition for GFET.

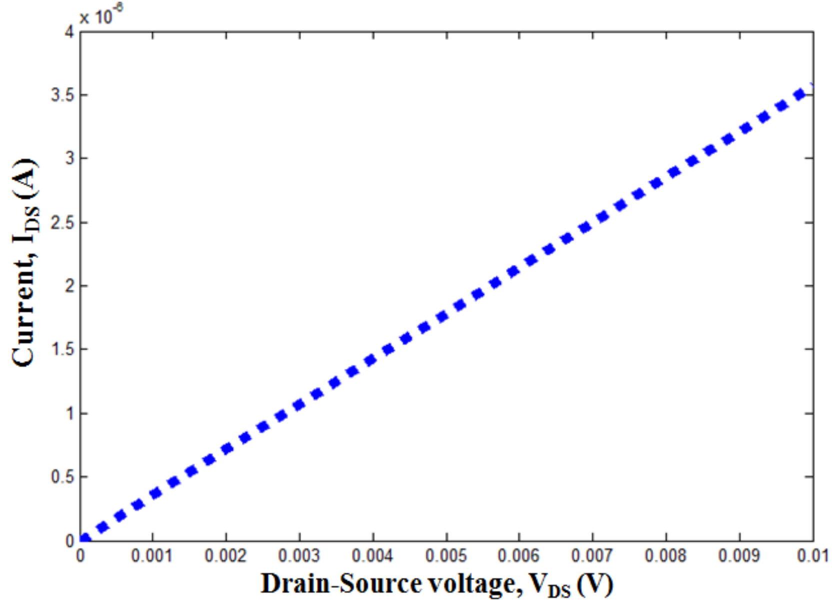


Figure 8-4: The I_{DS}-V_{DS} characteristic of the device. L = 10µm, W = 1.5 µm, R_C = 2.8kΩ, µ=7700cm^2/Vs, V_{DS}=10mV for this computation.

The mobility of the device can be determined by the equation (30).

$$\mu = \frac{g_m L}{V_{DS} W C_{BG}} \tag{30}$$

Here, g_m is the transconductance and C_{BG} is the back gate capacitance, which can is computed by parallel plate capacitor formula.

The carrier concentrations (electrons or holes) in the source and drain regions can be calculated by the equation (35) [62]. Where, V_{BG}^0 is the backgate voltage at the Dirac point (minimum conduction) and n_0 is the minimum sheet carrier concentration which is determined by disorder and thermal excitation [64]-[65]. The V_{BG}^0 determines the doping type. Ideally, it should be 0V but it shows a nonzero value due to the impurities in the graphene. Figure 8-6 shows the effect of Dirac point or minimum conductivity point shift (V_{BG}^0=0V to V_{BG}^0=+4V)

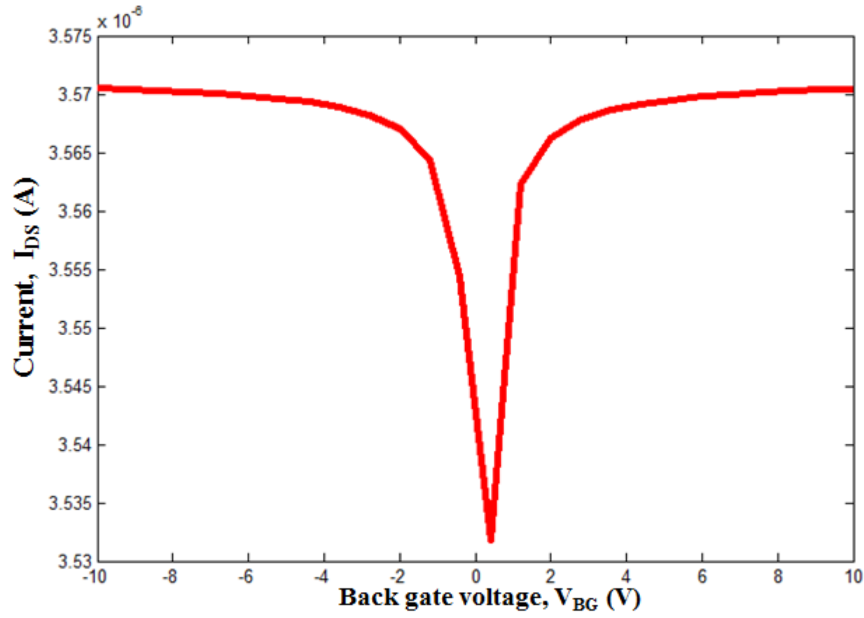
in the I_{DS}-V_{BG} characteristics of the GFET. This result shows good agreement with the existing experimental results of [62].

Under the top gate, the carrier concentrations (electrons or holes) is calculated by both the top and back gates, according to (34) [62], where, the C_{TG} is the effective top-gate capacitance per unit area, V_{TG} is the top gate voltage and V_{TG}^0 is the topgate voltage at the Dirac point. So, this formula should be used for precise carrier concentration in the graphene device channel.

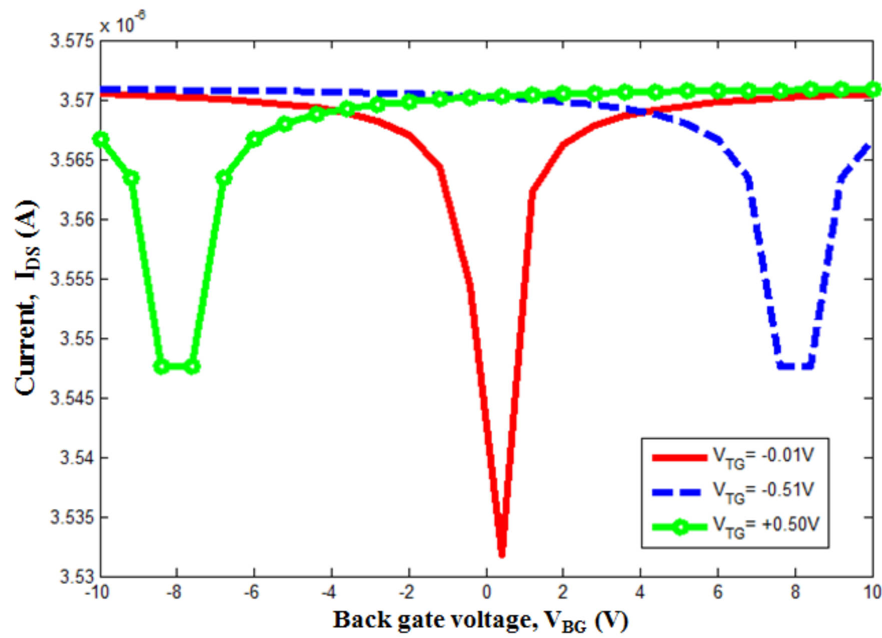
$$n \cong \sqrt{n_0^2 + [\frac{C_{BG}(V_{BG} - V_{BG}^0)}{e}]^2} \tag{31}$$

$$n \cong \sqrt{n_0^2 + [\frac{C_{BG}(V_{BG} - V_{BG}^0) + C_{TG}(V_{TG} - V_{TG}^0)}{e}]^2} \tag{32}$$

The I_{DS}-V_{BG} characteristics is shown in Figure 8-5a. The device shows minimum conductivity close to 0V. The same set of computation is done for the positive and negative V_{TG}. Figure 8-5b shows that the minimum conductivity point shift to the left for the $+V_{TG}$. On the other hand, the minimum conductivity point shift to the right for the $-V_{TG}$. The I_{DS}-V_{BG} characteristic is highly depends on the back gate oxide thickness. In order to realize the back gate influence clearly, the back gate oxide should be thin enough to increase carrier density in the channel. If the back gate oxide is thick, according to the (34), the C_{BG} would be close to zero. Therefore, the back gate tends to loss its control on the device operation. For the graphene transistor, 300nm SiO_2 back gate dielectric is the standard. This result shows good agreement with the existing experimental results of [60],[62].



(a) When $V_{TG} \approx 0V$



(b) Comparison when V_{TG}= -0.01V, -0.5V, +0.51V

Figure 8-5: The I_{DS}-V_{BG} characteristics of the GFET for a fixed V_{DS} and V_{TG}. L = 10μm, W = 1.5 μm, R_C = 2.8kΩ, μ=7700cm^2/Vs, V_{DS}=10mV, n_0=2.25x10^{11}cm^{-2} for this computation.

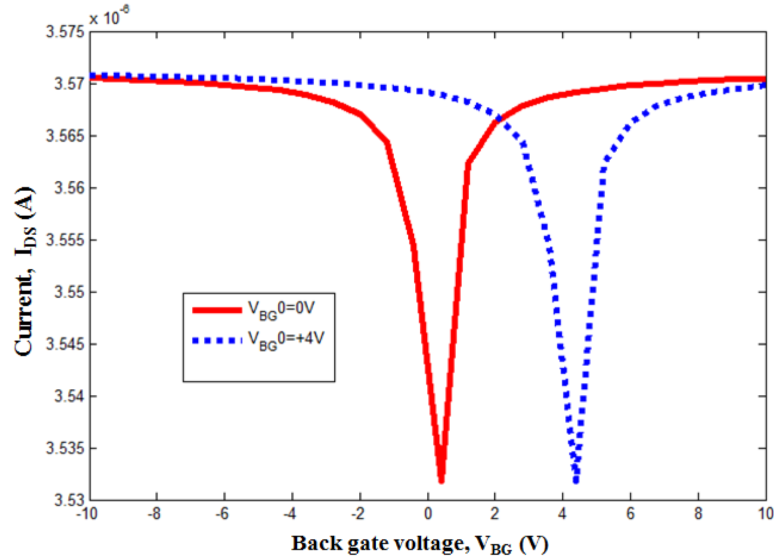
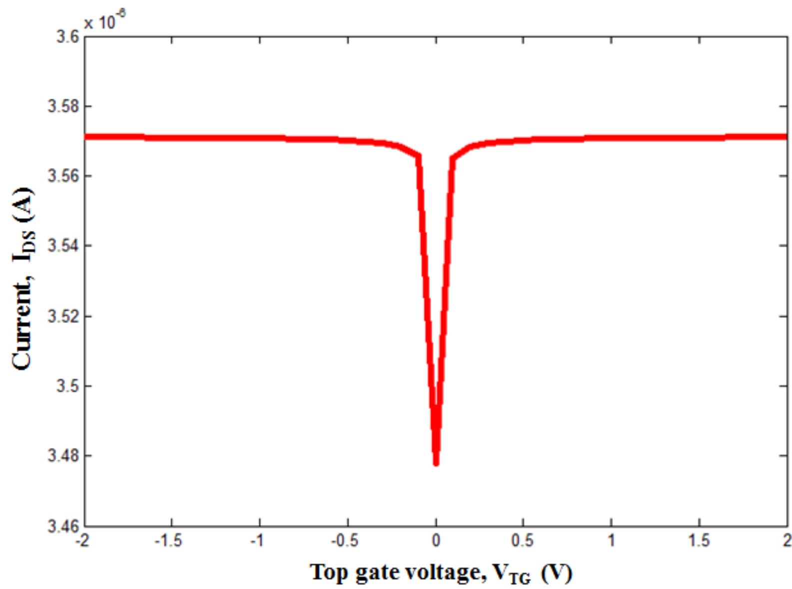


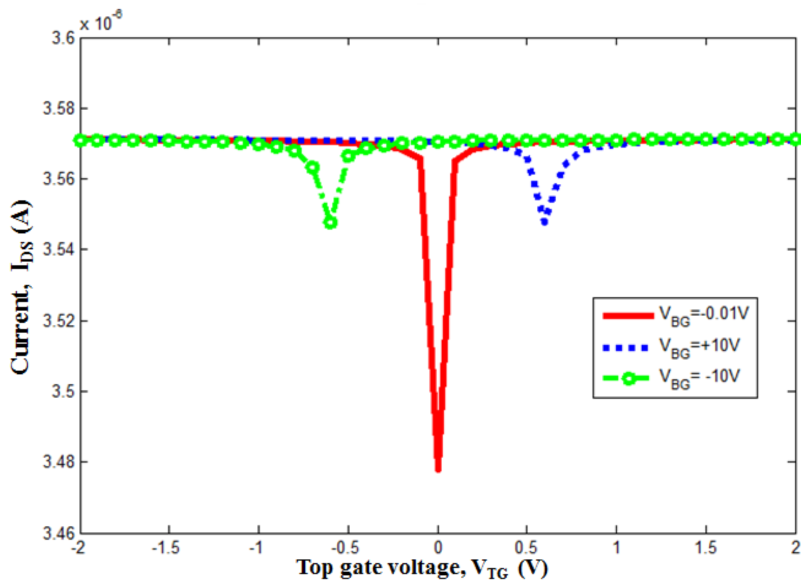
Figure 8-6: The effect of the Dirac point shift in the I_{DS}-V_{BG} characteristics of the GFET.

The top gate influence on the device can be explained by the I_{DS}-V_{TG} curve, which is shown in Figure 8-7a. The minimum conductivity point is also observed here which is similar to the previous I_{DS}-V_{BG} characteristics (Figure 8-5). Then, the I_{DS}-V_{TG} variation is computed for different V_{BG} value, which is summarized in Figure 8-7b. Figure 8-7b shows that the minimum conduction point shift upward when $V_{BG} \neq 0V$. The result also suggests that the minimum conductivity point shifts to the left when V_{BG} is positive. But the minimum conductivity point shifts to the right when the V_{BG} is negative. This result shows good agreement with the existing experimental results of [60],[62].

Therefore, the I_{DS}-V_{BG} and I_{DS}-V_{TG} show similar behavior but not equal because of the different oxide parameters. If the same top gate and back gate dielectric are used, then these two characteristics would be identical image.



(a) When $V_{BG} \approx 0V$



(b)Comparison when V_{BG}= -10V, ≈ 0V, +10V

Figure 8-7: The I_{DS}-V_{TG} characteristics of the GFET for a fixed V_{DS} and V_{BG}. L = 10μm, W = 1.5 μm, R_C = 2.8kΩ, μ=7700cm^2/Vs, V_{DS}=10mV, n_0=2.25x10^{11}cm^{-2} for this computation.

Figure 8-8 shows the experimental result of the graphene transistor, published by the IBM. It shows that the I-V curve is moving from its original position due to the oxide materials and process variations [60]. The similar type of experiment is also done in [61].

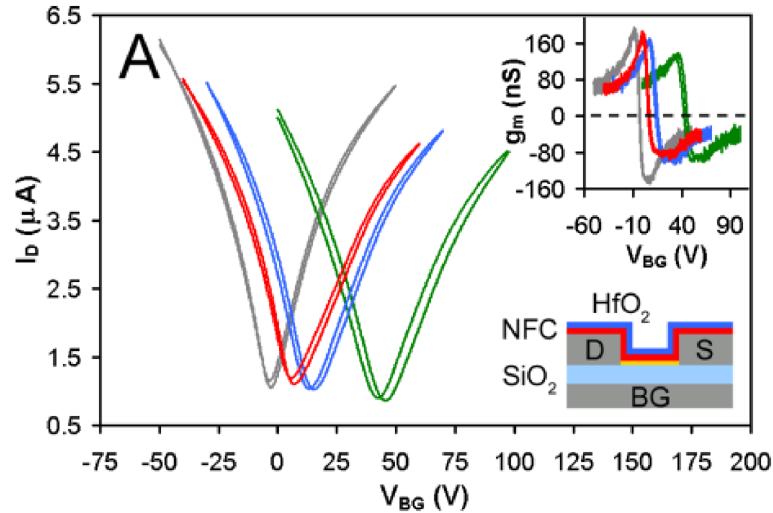


Figure 8-8: Two-point back-gated measurements of graphene flakes. (A) Transfer characteristics and corresponding transconductances (inset) after the different stages of buffered dielectric processing: before processing (grey), after NFC polymer deposition (green), after HfO_2 deposition (blue), and after 50 W O_2 plasma treatment for 30 s (red). The schematic shows the completed device configuration [60].

Chapter 9 : MoS_2 FET Device and Contact Characterization and Modelling based on Modified Transfer Length Method (TLM)

9.1.Introduction

Two-dimensional (2D) materials like molybdenum disulfide (MoS_2) offers promising solutions for future electronic and photonic devices [74]-[75]. Recently, MoS_2 has emerged as the new super-material for the next generation logic, memory, sensor, optoelectronic and many other nanoelectronic applications. MoS_2 transistors are anticipated to have very high electron mobility, high drive current, reduced subthreshold swing, high on/off current ratio (10^6~10^8) and higher immunity to short channel effects [76]-[81]. MoS_2 transistors would provide several other advantages over silicon (Si) devices. Due to the 2D planner structure of MoS_2 the surface scattering in MoS_2 is significantly lower than Si and it can be scaled down to the sub-nanometer (nm) range. The dielectric constant of MoS_2 (~3.3) is lower than Si that provides MoS_2 transistor higher robustness against short channel effect (SCE) compared to silicon MOSFET [80], because SCE is directly proportional to the dielectric constant of the channel material [82]. Another critical parameter is the Transfer length, which estimates the distance beyond which Coulomb interactions can be ignored. The thickness of a monolayer MoS_2 (~0.65nm) is lower than its Transfer length (0.7 nm) [79]-[80], which allows better electrostatic control than conventional MOSFET over the channel conduction. The Transfer length, is the measure of how distant the electrostatic influence persist. At each Transfer length, the applied electric potential will drop by 1/e. Therefore, the monolayer MoS_2 transistor would outperform the conventional MOSFET [91] in terms of the electrostatic gate control. High density of states (the density of states gives the number of allowed electron states per unit volume at a given

energy) in MoS_2 ensures improved electrical performance even in the deep sub-nanometer regime because of the availability of sufficient number of electrons [85]. Some MoS_2 based logic and integrated circuit designs are demonstrated in [88]-[89]. Currently, researchers are exploring MoS_2 based devices for conventional as well as ultra-high-frequency and ultra-low-power applications. MoS_2 can also be used for the sensing application as well. Contact resistance would be a very crucial factor in all MoS_2 based devices, particularly in the ULP devices like sensors [87].

Although MoS_2 transistor shows great potentials for post silicon applications, it still has two major drawbacks: (i) dielectric integration problem and (ii) large contact resistance. The dielectric issue arises from the lack of dangling bond on the MoS_2 surface, while the Schottky barrier at the metal-MoS_2 interface is responsible for the high contact resistance. An electron can easily tunnel through the metal-MoS_2 interface if the semiconductor material is heavily doped. However, no controlled doping method is still developed for MoS_2 based devices [84]. The on-off switching in MoS_2 transistors are not only achieved by accumulating/depleting the carrier density in the channel, but also by changing source/drain junctions [83]. This is the fundamental difference between MoS_2 transistor and Si MOSFET. To the best of our knowledge there is no precise modeling and analysis approach developed yet for MoS_2 transistor to measure its effective mobility and resistance, which are difficult to predict accurately because of its complex tunneling mechanism in the Schottky region with the gate bias. In this paper, we have investigated the complex tunneling phenomena of metal-MoS_2 contact by using simple analytical models (equations) that are capable of solving some key fundamental parameters of metal-MoS_2 contact. Here, we have focused on sheet resistance

(R_{Sh}), contact resistivity (ρ_c), contact resistance (R_C) and transfer length (L_T) that define the metal-MoS_2 contact.

9.2.Metal-MoS_2 Contact Model

Researchers have been exploring carbon nanotube (CNT) and graphene for the last two decade for different device applications. Overcoming the contact limitation has been one of the critical challenges for CNT and graphene based devices. Similar challenges are also encountered in the case of MoS_2. For our analysis, we are using the modified TLM physical model of metal-MoS_2 contact as illustrated in Figure 9-1: [83]. The structure is a modified Transmission Line Measurement or Transfer Length Measurement (TLM) structure. Using TLM model contact resistance, sheet resistance, contact resistivity and transfer length can be determined [86]. Table 9-1 shows the comparison between 4-point, VDPM, TLM and modified TLM methods. Multiple field effect transistors are used for the TLM measurement, which is directly related to the transistor application. Unlike TLM, the Van der Pauw method (VDPM) uses a material sheet, which doesn't ensure FET conditions. In conclusion, TLM is more relevant to transistor application while VDPM is more relevant to the material characterization.

Table 9-1: Comparison between 4-point,VDPM, TLM and modified TLM methods.

Properties	4-Point	VDPM	TLM	Modified TLM
Number of Contacts	4	4	>2	>2

Material Characterization	Yes	Yes	Yes	Yes
FET Fabrication	No	No	Yes	Yes
FET Characterization	No	No	Yes	Yes
Contact Resistance measurement	Yes	Yes	Yes	Yes
Contact length	Fixed	Fixed	Fixed	Vary
Contact spacing	Fixed	Fixed	Fixed	Vary
Sample	Uniform	Uniform	Uniform	Different
Measured Data	Less	Less	Less	More

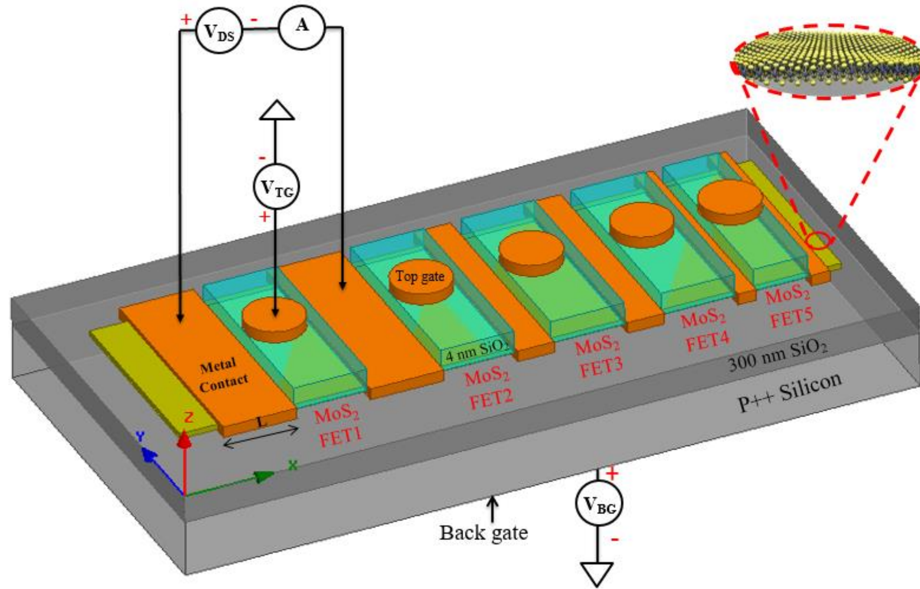
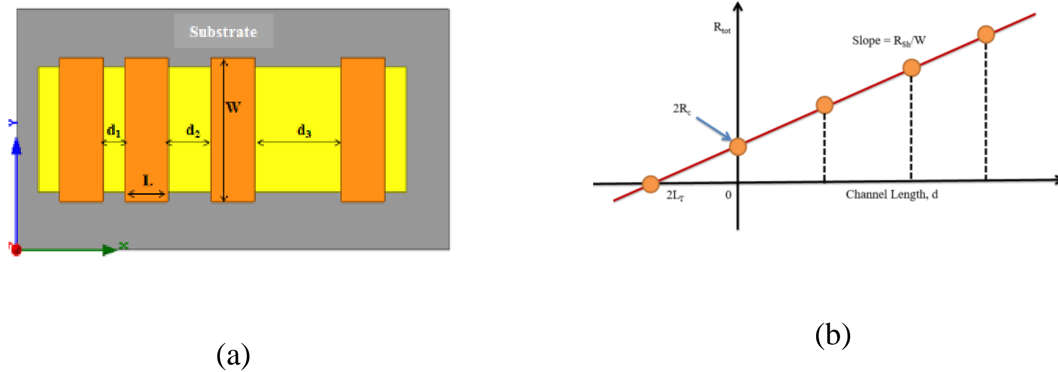


Figure 9-1: 3D view of the proposed modified metal-MoS_2 TLM structure of a series of MoS_2 transistors. The electrical connections are also shown. The extra benefit of the proposed modified metal-MoS_2 TLM structure is the varying contact length (L) consideration, which is absent in the basic TLM structure (Figure 9-2a).



(a)

(b)

Figure 9-2: Physical and mathematical representation of the basic TLM method. (a) Basic TLM structure; (b) Determination of R_C and L_T parameters of metal-semiconductor contact by using TLM method, which can be customized for different contact dimensions.

In our analysis, we are utilizing the TLM technique, because it is widely used in semiconductor physics and engineering to determine the contact resistance between a metal and a semiconductor. In the interest of general readers, we have summarized the features of the basic TLM approach (Figure 9-2a):

a) It consists of a set of metal contacts with identical geometry (fixed contact width W and contact length L) and different spacing d.
b) Probes are applied to the pairs of contacts, and the resistance between them is measured by applying a voltage across the contacts and measuring the resulting current.
c) If several such measurements are made between the pairs of contacts that are separated by different distances, a plot of resistance versus contact separation can be obtained.
d) Here we find a linear line whose intercept with the y axis represents two times of the contact resistance (R_C) and the slope represents the sheet resistance (R_{Sh}) (Figure 9-2b)
e) According to TLM model, the total resistance (R_{tot}) is related to the metal/semiconductor contact resistance (R_C) and sheet resistance (R_{Sh}) according to the Figure 9-2. (33) [83]. Here, d is the spacing between the two contacts, and W is the channel width.

$$R_{tot} = 2R_C + R_{Sh}\frac{d}{W} \quad (33)$$

The potential fabrication process of the TLM structure of the metal-MoS_2 contact would include the following steps. First, a 300 nm thick SiO_2 layer would be thermally grown on a P++ silicon wafer. The silicon and SiO_2 would act as the gate and gate dielectric respectively. Second, a single-layer MoS_2 film can be grown by Chemical Vapor Deposition (CVD) method, followed by an etching process to obtain a single-layer rectangular shape MoS_2 with a uniform width. Third, 4 nm SiO_2 is sputtered on the MoS_2 channel. This SiO_2 acts as the top gate oxide. Fourth, Ti/Au metal contact pairs with various contact lengths (L = 0.2 to 2μm

[83]) can be used as the source/drain contact metal. The dimension L is defined in Figure 9-2. Usually, multiple MoS_2 transistors can be grown on the same MoS_2 sheet as shown in Figure 9-1:. This would help compare the contact resistance parameters of multiple devices with different dimensions but identical process parameters.

The total resistance (R_{tot}) of a single MoS_2 transistor can be measured by the two-probe method. Biasing determines source and drain terminal. Here the left most terminal is source if it is connected to the lower potential than the right terminal. Usually, the source is connected to the ground. The back gate voltage (V_{BG}) is applied at the P++ Silicon back gate while top gate voltage (V_{TG}) is applied at the top of top gate oxide. The total resistance (R_{tot}) between the source and the drain contact of a particular FET in the structure of Figure 9-1: would depend on the contact and sheet resistances. The contact resistance (R_C) and sheet resistance (R_{Sh}) can be calculated from the modified TLM structure by using (33).

According to the model, current encounters two resistances: (i) the impedance from the Schottky barrier, ρ_c, and (ii) the sheet resistor R_{Sh}. The current always takes the minimum resistive path from the metal to the semiconductor. The voltage is the highest near the contact edge and drops nearly exponentially with the distance. We have analyzed the dependence of different parameters of metal-MoS_2 contact on the back gate and top gate voltage. For our analysis we have used a back gate voltage (V_{BG}) in the range of 0-100 V. For this type of theoretical analysis, this range of high back gate voltage is normally used [83]. We have developed analytical models for various parameters and compared the results obtained by the models with the experimental results of [83]. V_{BG}, V_{TG} =0~50 V is used in our simulation because 50~100 V does n't show any significant change both in the experiment and simulation.

The electrical model of the metal-MoS_2 contact is illustrated in Figure 9-3. At the metal-MoS_2 interface, two white areas (shown in Figure 9-3) represent the contact resistance (R_C). The R_{Sh} represents the resistance of the MoS_2 channel. The R_{tot} drops exponentially with the contact length (L) [83].

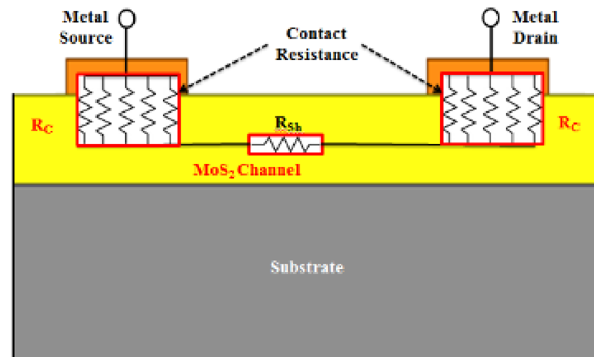


Figure 9-3: The electrical model of the metal-MoS_2 (semiconductor) contact. Here R_{Sh} is the channel resistance (sheet resistance) and R_C is the contact resistance.

9.3.Device Structure

MoS_2 FET has been designed and fabricated by the research community on the 270-300 nm substrate, which needs high back gate voltage (20-100V) to operate. Such high voltage is not practical for any real application. However, historically MoS_2 FET have been researched in the academic research labs, which use $MoS_2/SiO_2/Si$ samples available in the market. To minimize additional fabrication complexity, they use Si back gate, which is isolated by around 300nm thick SiO_2. That is why a high back gate voltage (20-100V) is needed to realize the channel characteristics. Since all of the previous and current research are still at the proof-of-concept stage, this voltage number is not an issue. To achieve low power MoS_2 FET, a thin high-dielectric oxide can be fabricated on top of the MoS_2 channel. A top gate can be placed on this thin oxide. None of the previous work analyzed the impact of the top gate on the contact

behavior of MoS_2 FET. For the first time, we have presented the analysis of the combined effects of the top and back gates.

The proposed model is used to estimate R_{Sh}, R_c and L_T for the back gate, top gate and double gate MoS_2 FET for the first time. The pros and cons of the back gate, top gate and dual gate MoS_2 FETs are discussed in the Table 9-2. The physical, material and electrical parameters of the metal-MoS_2 contact that would determine the contact properties, are also included in the proposed model.

Table 9-2: Comparison between the back gate, top gate and dual gate MoS_2 FETs.

Device Type	Back Gate GFET	Top Gate GFET	Dual Gate GFET
Gate Used	Back Gate only	Top Gate only	Both Top and Back Gates
Gate oxide	Thick Back Gate oxide i.e.270-300nm	Thin Top Gate oxide i.e.1-10nm	Thick Back Gate oxide i.e.270-300nm & Thin Top Gate oxide i.e.1-10nm
Feasibility	Impractical	Practical	Practical
Experimental Data Availability	Most	Insufficient	Insufficient
Gate Voltage	High	Low	Flexible

Electrostatic Control	Less	More	Most

9.4.Carrier Density Calculation

The modulated carrier density (n) in the MoS_2 channel is calculated by MoS_2 material parameter i.e. intrinsic carrier density (n_0); top gate oxide parameters i.e. dielectric constant, thickness, area; back gate oxide parameters i.e. dielectric constant, thickness, area; electrical parameters i.e. V_{TG}, V_{BG}.

The electrostatic actions of the top and back gate voltages would significantly increase the carrier (electron/hole) density. The carrier concentration in presence of the top and back gate biases can be calculated by (34), where C_{TG} is the effective top-gate capacitance, V_{TG} is the top gate voltage, C_{BG} is the effective back-gate capacitance and V_{BG} is the back gate voltage. This model can be used for the precise calculation of carrier concentration in a MoS_2 FET channel.

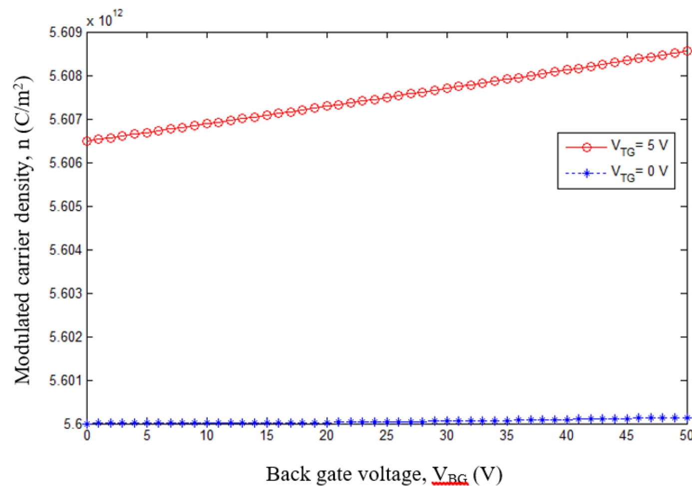


Figure 9-4: The n-V_{BG} for the fixed V_{TG}. The comparison between the V_{TG} =0V and 5V are provided. Here d_{BG}= 270 nm, d_{TG}=4nm, A=1μm^2.

Figure 9-4 shows the variation of modulated carrier density (n) as a function of V_{BG} with a fixed V_{TG}. If the device has the back-gate only (no top-gate), equation (34) can be converted to (35), because $C_{TG}V_{TG}$=0. This can be true either if the top-gate is connected to the ground or if there is no top-gate oxide. From Figure 9-4 it can be observed that the value of n is almost constant when V_{TG}=0V. The value of n increases linearly with V_{BG} when V_{TG}=5V. The value of n for V_{TG}=5V is larger the value of n for V_{TG}=0V for a particular V_{BG}.

$$n \cong \sqrt{{n_0}^2 + \left(\frac{C_{BG}V_{BG} + C_{TG}V_{TG}}{e}\right)^2} \tag{34}$$

$$n \cong \sqrt{{n_0}^2 + \left(\frac{C_{BG}V_{BG}}{e}\right)^2} \tag{35}$$

$$n \cong \sqrt{{n_0}^2 + \left(\frac{C_{TG}V_{TG}}{e}\right)^2} \tag{36}$$

$$R_{Sh} = \frac{S_1 n_0 dT^{-2}}{nW} \exp\left[-\frac{S_2 n(V_{BG}+V_{TG})}{n_0 q \emptyset_B k_B T}\right] \tag{37}$$

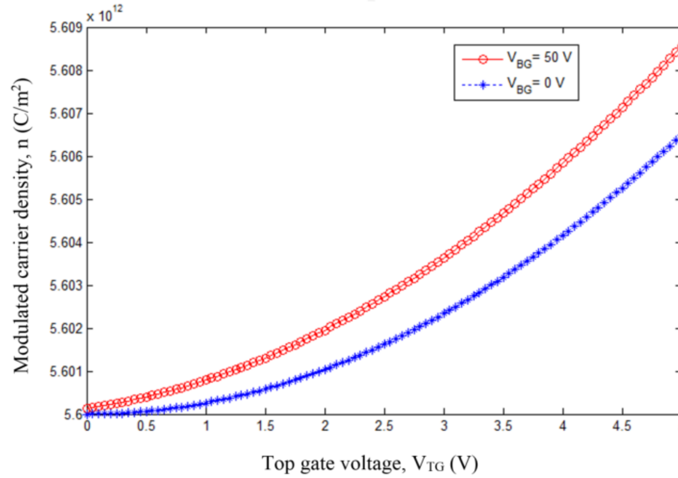


Figure 9-5: The n-V_{TG} for the fixed V_{BG}. The comparison between the V_{BG}=0V and 5V are provided. Here d_{BG}= 270 nm, d_{TG}=4nm, A=1μm^2.

Figure 9-5 shows that the value of n increases exponentially with the increase of V_{TG} for a fixed V_{BG}. It is observed that for a certain V_{TG} the value of n is higher with V_{BG}=50V than in V_{BG}=0V. If the device has top-gate only (no back-gate), then equation (34) can be converted to (36), because $C_{BG}V_{BG}=0$. This can be true either if the back-gate is connected to the ground or if there is no back-gate. These cases are explained in Figure 5. Figure 5 shows the comparison between the two cases, which suggests that the electrostatic control of V_{TG} is more than V_{BG} on the value of n. In conclusion, the modulated carrier density (n) in the channel can be computed by using (34)-(36) for different bias conditions and FET designs.

9.5.Sheet Resistance (R_{Sh})

R_{Sh} drops exponentially with the back gate voltage [83]. This experimental work has two major drawbacks. First, it has no verified mathematical model. Second, it have used only back gate. So, there is no analysis for the top gate and dual gate MoS_2 FETs.

To address these aforementioned drawbacks, a new R_{Sh} model is proposed by the equation (37), which is capable to simulate the top gate, back gate and dual gate MoS_2 FETs for the first time. R_{Sh} of the MoS_2 channel is calculated by MoS_2 material parameter i.e. intrinsic carrier density (n_0); top gate oxide parameters i.e. dielectric constant, thickness, area; back gate oxide parameters i.e. dielectric constant, thickness, area; electrical parameters i.e. V_{TG}, V_{BG}. These parameters are included in the proposed model by plugging in (34) into (37). Additional parameters are added for the first time to calculate R_{Sh} are MoS_2 physical parameters d, W; exponential term of electrical parameters i.e. V_{TG}, V_{BG} and temperature.

Two new constants S_1=4.9135x10^8, S_2=9.2328x10^{-42} are added in the proposed model to validate with the experimental data of [83]. The value of S_1, S_2 depends on the parameters, which are not considered in the proposed R_{Sh} model such as process corners (SS, TT, FF) and doping. Later, R_{Sh} model is validated with the available experimental data. The proposed analytical model shows a good agreement with the experimental results of [83] (Figure 9-6).

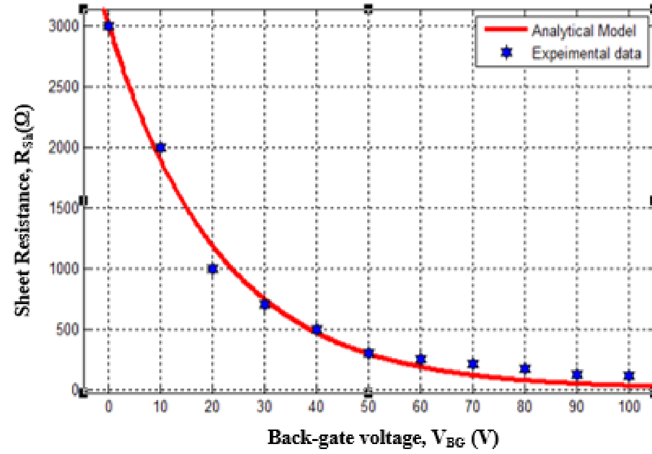


Figure 9-6: The sheet resistance (R_{Sh}) model validation as a function of back-gate voltage (V_{BG}).

The current distribution in a multilayer MoS_2 FET migrates toward the layers that are close to the substrate, when the gate bias is enhanced. Therefore, at any specified gate bias the current mainly runs through the bottom layers [93]. R_{Sh} is the resistance of the active channel region of the MoS_2 FET. We can find R_{Sh} by using TLM technique. In our model, we have introduced both back gate and top gate voltage effects in equation (33). This model also can be customized for the back gate, top gate and dual gate MoS_2 devices. R_{Sh} decreases exponentially with the increase of the back gate bias, because higher back gate bias raises the Fermi level in MoS_2 up, which induces higher carrier density and reduces the sheet resistance [83]. Figure 9-7 shows R_{Sh} variation with V_{BG} for different V_{TG}. A reasonably good match is

found between calculated and experimentally measured data (R_{Sh} vs. V_{BG} for V_{TG}=0 V). Like the back gate, the top gate is electrostatically coupled with MoS_2 channel. Therefore, R_{Sh} also drops exponentially with V_{TG}, according to (37). Figure 9-8 shows R_{Sh} variation with V_{TG} for different V_{BG}.

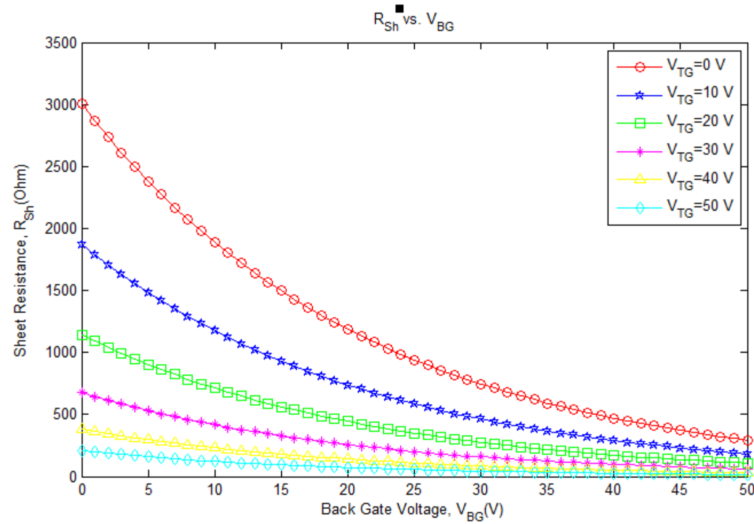


Figure 9-7: R_{Sh} variation with V_{BG} for different V_{TG}.

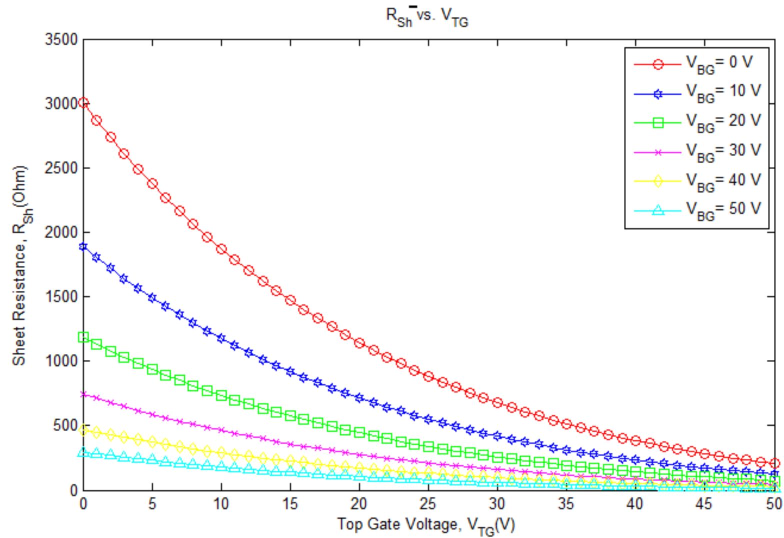


Figure 9-8: R_{Sh} variation with V_{TG} for different V_{BG}.

R_{Sh} also drops exponentially with n/n_0, which is confirmed by comparing our model with the experimental data. Here, n/n_0 shows better agreement than any constant. The physical significance of n/n_0 is how many times the charge carrier density of MoS_2 channel is enhanced under certain top gate and back gate voltage, compared with the intrinsic or no bias condition. Therefore, n/n_0 reduces R_{Sh} of MoS_2 channel. According to equation (37), the coefficient of exponential part is the initial value of R_{Sh}. Usually, R_{Sh} and n has an inverse relationship, which is confirmed by fitting experimental data with our proposed model. R_{Sh} is proportional to d and inversely proportional to W as shown in Figure 9-9. A reasonably good match is found between calculated and experimentally measured data.

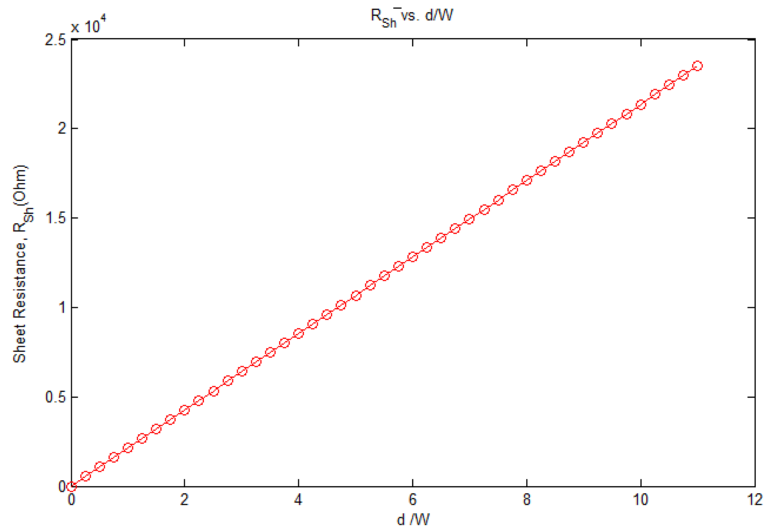


Figure 9-9: R_{Sh} variation with d/W.

In the conventional MOSFET, the temperature rise increases R_{Sh}, which leads to low channel current. But the temperature dependency of MoS_2 FET is complicated. In MoS_2 FET, the channel current is proportional to $T^2exp(-k_BT)$ [95]. Therefore, R_{Sh} is proportional to $T^{-2}exp(k_BT)$, which leads to R_{Sh} drop as a function of the temperature. This temperature dependency is added in the proposed model. Figure 9-10 shows R_{Sh} variation with the

temperature. R_{Sh} variation is simulated at three major temperature corners: -40° C (cold temperature), 27° C (room temperature), and 125° C (hot temperature). In MoS_2 FET, at low temperatures, the mobility is restricted by ionized impurity scattering. At room temperature, the mobility decreases by enhanced optical phonon and acoustic phonon scattering [90].

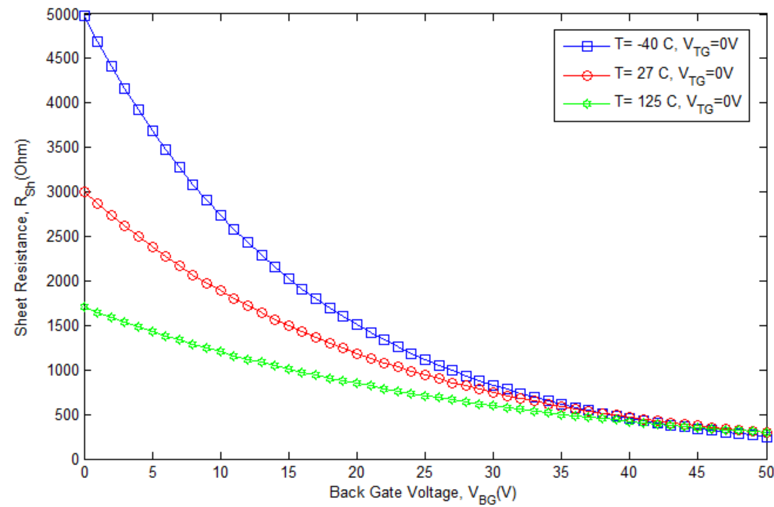


Figure 9-10: R_{Sh} variation with the temperature and V_{BG}.

9.6.Contact Resistance (R_C)

A theoretical R_C model is presented in [80] as shown in equation (38) by assuming only thermionic current for simplicity. where h, m*, Φ_B, e, k_B, T and t are Planck's constant, effective mass, Schottky barrier height, electron charge, Boltzmann constant, temperature and thickness of MoS_2 monolayer, respectively. Based on the equation (38), R_C is analyzed in [107]. This model failed to mimic R_C behavior correctly because this model [80], [107] shows good results only for a specific set of values. Most of the cases, these models generate $R_C = \infty$, which is not practical. Therefore, a broad range general model is needed to calculate R_C accurately. Another drawback of the R_C model is that it is not validated with any experimental data.

The metal-MoS_2 contact resistance (R_C) drops exponentially with the increase of the back gate voltage [83]. This experimental work has two major drawbacks. First, it has no verified mathematical model. Second, it have used only back gate. So, there is no analysis for the top gate and dual gate MoS_2 FETs.

To address these aforementioned drawbacks, a new R_C model is proposed by the equation (39), which is capable to simulate the top gate, back gate and dual gate MoS_2 FETs for the first time. Here, two new electrical parameters V_{TG}, V_{BG} are introduced. Two new constants N_1, N_2 are added in the proposed model to validate with the experimental data of [83]. The value of N_1, N_2 depends on the parameters, which are not considered in the proposed R_C model such as process corners (SS, TT, FF) and doping.

Theoretically, R_c can be calculated by (40) from R_{tot}, R_{sh} and the area (A). The decreasing trend in the R_C can be attributed to the increasing carrier density in the MoS_2 under the metal contacts. The proposed model shows good agreement with the experimental result.

Mathematically, ρ_c and R_C are related to each other by the cross-sectional area to length ratio (A/L) as in (41). Either of these two parameters has to be calculated to get the value of the other. Experimentally it is easier to measure R_C than ρ_c. The proposed model of ρ_c is validated with the experimental data of [83] (Figure 9-12).

$$R_C = \frac{h^3}{4\pi e^2 m^* t k_B T} \exp[\frac{e\varphi_B}{k_B T}] \tag{38}$$

$$R_C = \frac{N_1 h^3}{4\pi e^2 m^* t k_B T} \exp[\frac{e\varphi_B}{k_B T} - N_2(V_{BG} + V_{TG})] \tag{39}$$

$$R_C = R_{tot} - (R_{Sh} A) \tag{40}$$

$$\rho_c = \frac{R_c A}{L} \tag{41}$$

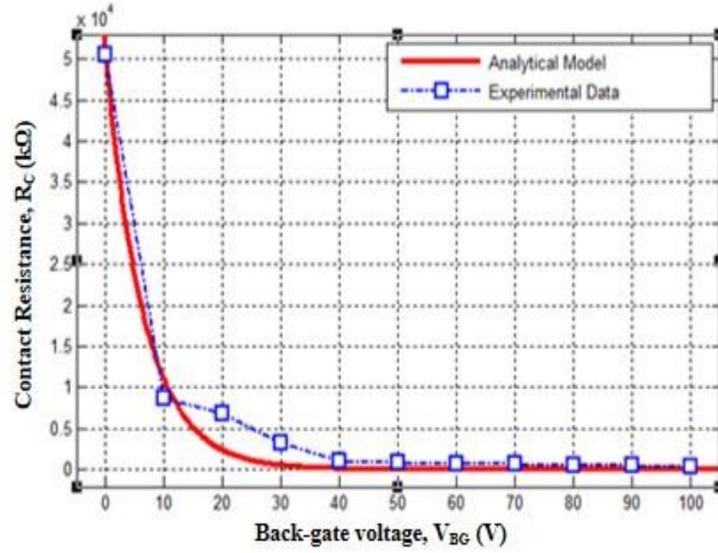


Figure 9-11: The contact resistance (R_C) model validation as a function of back-gate voltage (V_{BG}).

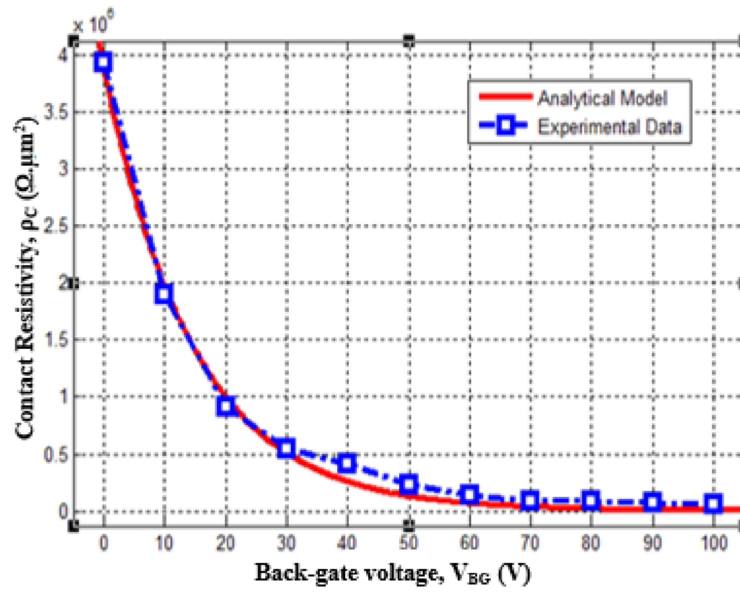


Figure 9-12: The contact resistivity (ρ_c) model validation as a function of the back-gate voltage (V_{BG}).

Figure 9-13 shows R_C variation as a function of both V_{BG} and V_{TG} for the first time. Like the back gate, the top gate is electrostatically coupled with MoS_2 channel. According to (39), R_C also drops exponentially with V_{TG}.

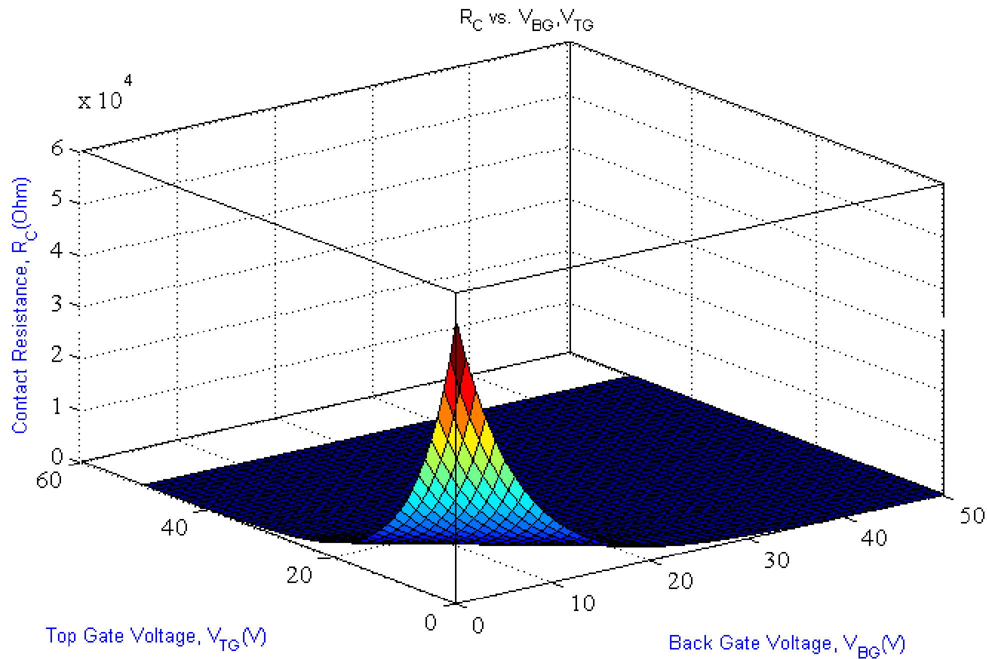


Figure 9-13: R_C variation with V_{BG} and V_{TG} when other parameters are fixed.

Figure 9-14 shows R_C variation as a function of V_{TG} and temperature for the first time. The variation of R_C is simulated at three major industry standard temperature corners: -40° C (cold temperature), 27° C (room temperature), and 125° C (hot temperature). As the temperature increases -40° C to 125° C, R_C drops. In MoS_2 FET, R_C is proportional to $T^{-1}\exp(1/K_BT)$. Therefore, the high temperature helps to reduce R_C.

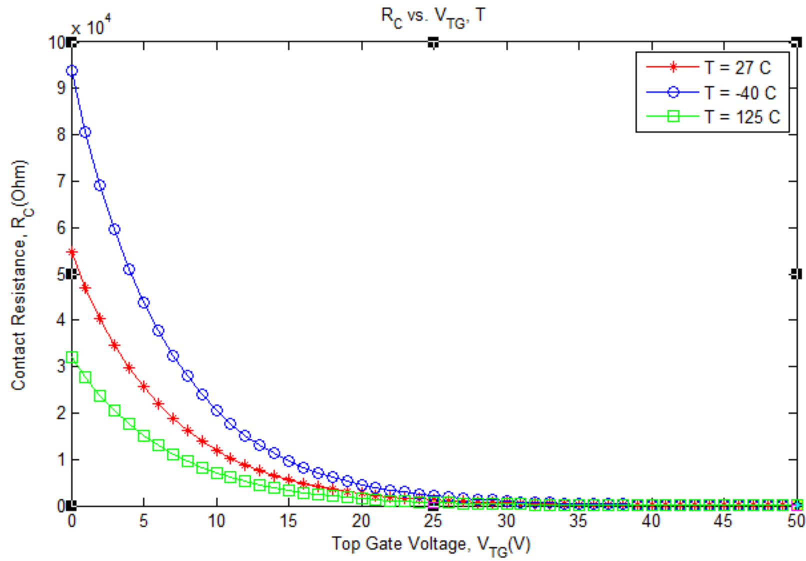


Figure 9-14: R_C variation with V_{TG} and T when other parameters are fixed.

Figure 9-15 shows R_C variation as a function of V_{TG} and number of layers for the first time. According to the analysis, R_C is inversely proportional to the number of layers. Therefore, higher number of MoS_2 layers help to reduce R_C.

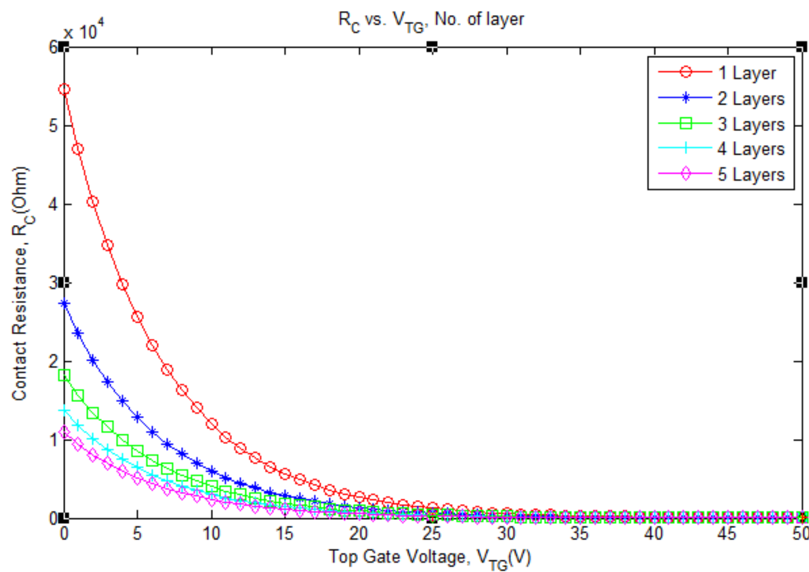


Figure 9-15: R_C variation with V_{TG} and no. of layers when other parameters are fixed.

9.7.Transfer Length (L_T)

L_T is the transfer length, which means that if we have an infinite contact length, how long does it takes for the potential on the contact to drop to 1/e. It is mostly an intrinsic property determined by the contact resistivity and the sheet resistance. L_T is directed along the transport direction. The relation between L_T and V_{BG} can be expressed by (42) [83]. A greater contact length ensures smooth carrier injection. The variation of L_T with V_{BG} is shown Figure 9-16. The L_T drops exponentially with V_{BG}. This indicates ρ_c drops faster than R_{Sh} with the increase of the gate bias. The simulation result of the proposed model shows good agreement with the existing experimental work of [83]. So it can be said that the contact is more sensitive to the gate voltage than channel (i.e. R_{Sh}).

$$L_T = \sqrt{\frac{\rho_c}{R_{Sh}}} \tag{42}$$

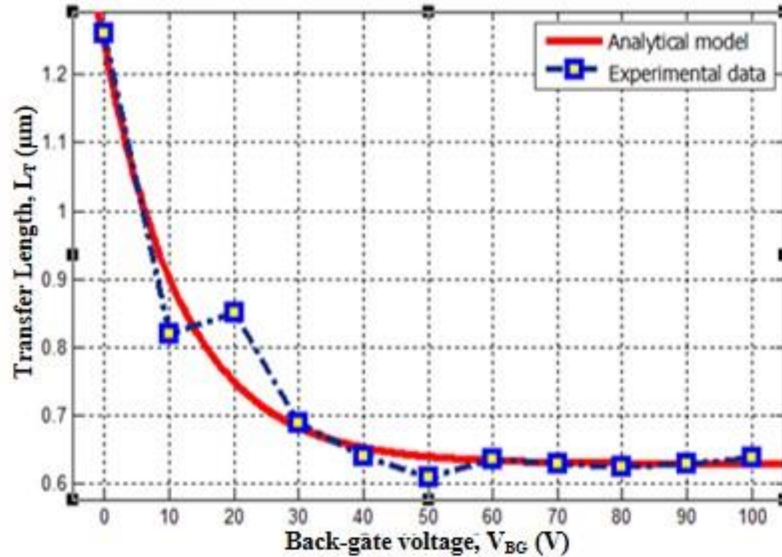


Figure 9-16: The transfer length (L_T) model validation as a function of back-gate voltage (V_{BG}).

Smaller contact dimension gives more precise L_T value. L_T drops from 1.26μm to 0.63 μm (Figure 9-16), when the gate bias is increased from 0V to 100V. The 2 μm contact length shows 2 times larger contact resistivity than 0.2μm contact length [83], because larger potential drop occurs with the increase of the contact length.

9.8. Impact of Doping on Contact Property

In 2D thin MoS_2 sheet, traditional doping (like ion implantation as in silicon) is not feasible. Therefore, other approaches like chemical and molecular doping are being explored. Still there is a lack of understanding about the methods to perform controlled doping of MoS_2. MoS_2 devices are limited by the Schottky barriers (SBs) at the metal/semiconductor interfaces [79], [92]. Therefore, electrical properties are hindered by the contact resistances rather than the intrinsic properties of the material. Analysis of the impact of doping on the contact properties is a huge research task itself. Here a very brief discussion is presented based on relevant work from other researchers. Our future work will address this issue in detail. In the literature, the polyethyleneimine (PEI) molecules have been proposed as the dopants to chemically dope multilayer MoS_2 flakes to lower the sheet and contact resistances. Both R_{Sh} and R_C are improved by the PEI chemical doping. It is reported that R_{Sh} is reduced 2.6 times by the PEI doping, which decreases from 19.99±3.31kΩ/□ to 7.65±1.81 kΩ/□. While R_C drops around 20% by the PEI doping, which decrease from 5.06±1.70Ω.mm to 4.57±1.80 Ω.mm. The reductions of R_C and R_{Sh} are achieved due to the effective Schottky barrier lowering, which leads to high carrier injection. Although PEI doping lowers R_{Sh}, and R_C, the on/off current ratio is reduced from $\sim 10^5$ to $\sim 10^2$ in the MoS_2 FET [84].

9.9.Impacts of Different Metals on Metal-Mos_2 Contact

The bandgap of both MoS_2 bulk and flake is the same, which is ~1.2eV [94]. Besides, the work function (Φ_{MoS2}) and electron affinity (χ_{MoS2}) of the flakes are 4.6–4.9 eV and ~4.0 eV respectively [95]-[98]. Usually, Au/Ti is used as the source and drain contact to the MoS_2. The work functions of Au (Φ_{Au}) and Ti (Φ_{Ti}) are 5.4 eV and 4.3 eV [95]. Therefore, the Schottky barrier (Φ_B) between Ti and MoS_2 is very small, which is good for the MoS_2 contact. It is known that the low work function metal give n-type behavior and the high work function metal give p-type behavior and the resultant Schottky barrier height (Φ_B) can be predicted by (43) [99].

$$\Phi_B = \Phi_m - \chi \tag{43}$$

Where, Φ_m and χ are the bulk metal work function and semiconductor electron affinity, respectively [99]. However, this is true for several cases while exceptions are discussed below.

a. If reaction is occurred between metal and MOS_2, the schottkey barrier height can not be calculated by (43). For example, the post XPS analysis of the Cr/MoS_2 and TiN/MoS_2interfaces reveals that both the Cr and TiN react with the underlying MoS_2 [100].

b. If the fermi level pinning (equal) is occurred for metal just below the conduction band of MOS_2 then the resultant schottky barrier height will be different from the theoretical equation value. For example Au and Pd give n-type behavior though the work function is high [100].

c. Though Au does not do any chemical reaction with MoS_2 but shows n-type behavior, it is occurred because of the defect present in MoS_2. It has two types of defects. In the defect region where the concentration of sulfur is lower than that of the Mo, that region shows n-type behavior. In the defect region where the concentration of sulfur is higher than that of the Mo

that region shows p-type behavior. If the defects can be increased, the current would be increased [100].

It can be concluded that the intrinsic defects in the MoS_2 dominate the metal-MoS_2 contact resistance and provide a low schottky barrier, which is independent of metal contact work function [100]. The effect of sulfur vacancy in MoS_2 based devices has been illustrated in [101].

It is observed that the high work function metals nickel (Φ_m=5.0eV) and platinum (Φ_m=5.9 eV) give n-type behavior because the Pt/MoS_2 and Ni/MoS_2 interfaces are strongly impacted by the fermi level pinning close to the MoS_2 conduction band, which is the similar to III−V materials. On the other hand, the lower work function metal contacts give the higher carrier injection and lower contact resistance [95].

The current intensity of the MoS_2 transistor is not only dependent on metal nature but also dependent on the number of layers/thickness of the MoS_2. The effective field effect mobility of the MoS_2 is a nonmonotonic function of MoS_2 layers. For high performance MoS_2 device applications, 6−12 nm thick is ideal [95].

The mobility values were reported for a finite layer thickness of around 10 nm are 21, 90, 125, and 184 $cm^2/V. s$ for the Pt, Ni, Ti and Sc contacts respectively. The field effect mobility up to 700 $cm^2/V. s$ has been achieved by covering the top of the backgated MoS_2 transistor with a thin layer of 15-nm thick Al_2O_3[95].

Depending on the thermionic emission and tunneling current, the true Schottky barrier height ϕ_{B0} (actual) can be estimated by (44) [95].

$$I_{DS} = AT^2 \exp[\frac{q\emptyset_B}{K_B T}\left\{1 - \exp(-\left(\frac{qV_{DS}}{k_B T}\right))\right\}] \qquad (44)$$

Where, ϕ_B is the effective barrier height, I_{DS} is the current through the device, A is the Richardson's constant, k_B is the Boltzmann constant, q is the electronic charge, T is the temperature, and V_{DS} is the source to drain bias. The metal-MOS_2 is not an ohmic contact because the thermally assisted tunneling current contributes to one of the portion of the total current [95]. Figure 9-17 shows the barrier between metal and single layer MoS_2. The Sc and Ti inject electrons, while Ni and Pt inject holes [95].

The current through Metal-MoS_2 contact increases when the Schottky barrier height is small, which leads to high carrier injection efficiency and reduced contact resistance. The current flow through different Metal-MoS_2 is shown in Figure 9-17. According to the Figure 9-17, the lower work function material (like Scandium (Sc) shows improved contact because of its high carrier injection and reduced contact resistance [95]. The theoretical and practical metal-MoS_2 Schottky barriers and their corresponding doping type are illustrated in Table 9-3.

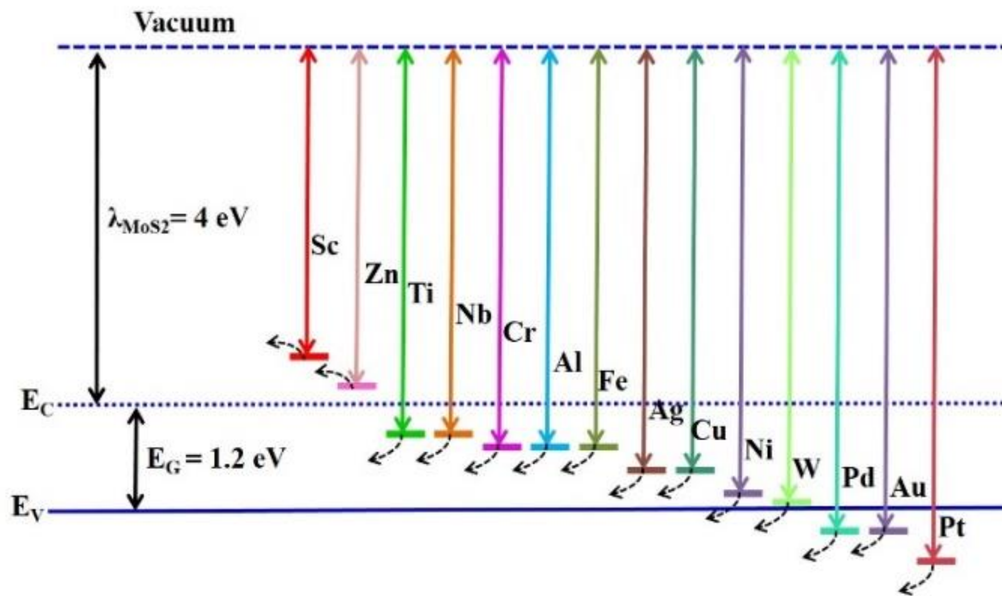


Figure 9-17: Predicted line-up of metal Fermi level with the electronic bands of MoS_2 if only the difference of the electron affinity of MoS_2 and the work function of the corresponding metal is considered.

Table 9-3: Doping types of metal-MoS_2 when $\chi_{MoS2} = 4.00$ eV.

Metal	Theoretical Doping Type (n-type/p-type)	Practically Doping Type (n-type/p-type)	Metal Work function Φ_m(eV)	Metal-MoS_2 Schottky Barrier(Theoretical)	Metal-MoS_2 Schottky Barrier(Practical)
Sc	n	n [95]	3.5 [95]	-0.5	0.03 [95]
Zn			3.6		
Ti	n	n [95]	4.3 [95]	0.3	0. 05 [95]
Nb	n	n [102]	4.3[103]	0.3	
Cr			4.5 [103]		
Al	n	n (expected)	4.5 [104]	0.5	0.55 [104]
Fe			4.5 [103]		
Ag			4.64 [105]		
Cu			4.65 [103]		
Ni	p	n [95]	5.0 [95]	1.0	0.15 [95]

W	p		5.1 [104]	1.1 [104]	
Pd	p	p [102]	5.4 [103]	1.4	0.78 [106]
Au	p	n [102]	5.4 [104]	1.4	0.045 [91]
Pt	p	n [95]	5.9 [95]	1.9	0.23 [95]

Blank= not available

Photovoltaic effect can be observed in MOS_2 if the source and drain contact are doped differently that is one side is the hole doped (Pd contact) and another side is electron doped (Au contact). At that time they behave like pn diode and the the photovoltaic effect arises from the built-in potential of the space charge accumulated at the source and drain contacts of the MoS_2. Its efficiency is 2.5% for multilayer MoS_2 but much higher conversion efficiency is expected for single layer MoS_2 diode because of its direct bandgap.

Since $E_{F,Pd} < E_{F,MoS2} < E_{F,Au}$, charge transfer occurs at the interfaces, causing doping of the MoS_2 channel and accumulation of space charge in the contact region, yielding Schottky barriers and either upward (hole doping) or downward (electron doping) bending of the conduction and valence band edges. Here E_F denotes the band energy.

For electron-doping (n-type) Au contacts, when a positive gate voltage is applied, the bands shift downward, the Schottky barrier becomes thinner, rises tunneling current through the conduction band. For negative gate voltages, the bands shifts upward, big barriers at the contacts restrict the source-drain current through the valence band. On the other hand, the hole-doping (p-type) Pd contacts show the opposite characteristics because $E_{F,Pd} < E_{F,MoS2}$.

Therefore, P-N junction and photovoltaic effect two types of metal contacts are required. One metal contact would be responsible for p-type doping while the other contact would be responsible for n-type doping.

Chapter 10 : 2.5D Silicon Interposer Design in 40nm-Technology for 2D-IC and 3D-IC

10.1. Introduction

To get high density and better communication speed between two chips, numerous Silicon Interposers (SI) have been proposed. In SI, multiple dies are mounted on the single silicon substrate, where TSVs and multilayer (i.e.M1~M6) interconnects are used for chip-to-chip communication [114].

10.2. What is Silicon Interposer?

Figure 10-1 shows multiple chips are mounted on the Silicon Interposer, which allows TSVs connection through it. It allows high density, power integrity and transmission speed between chips.

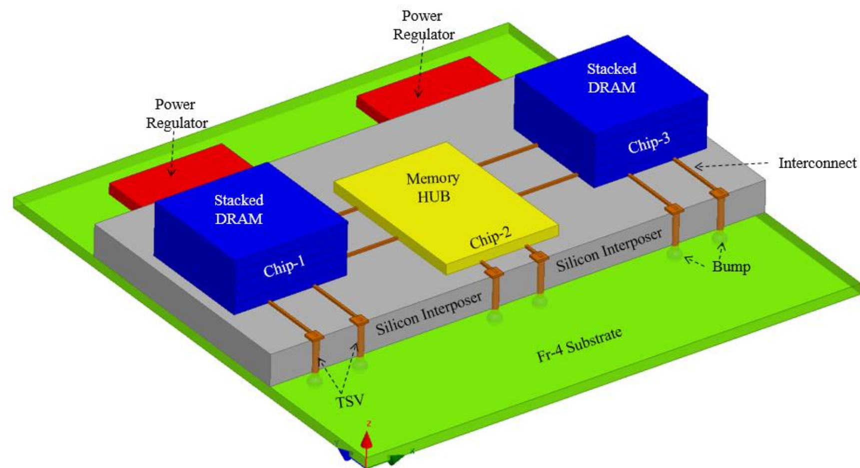


Figure 10-1: A complete Silicon Interposer, where three active chips are mounted. These chips communicate with external I/Os by TSVs, interconnects and bumps. The finished Silicon Interposer and Chips assembly is packaged in a Fr-4 substrate.

TSVs (Through Silicon Via) and multilayer interconnects (RDLs) are embedded inside the Silicon Interposer. In 2.5D-ICs, different dies are not vertically stacked. These chips are placed next to each other on a common Silicon Interposer. An interposer is an inactive device that allows dies placement on it. It provides Chip-to-Chip communications by using interconnects. It also provides Interposer-package connections by using interposer level TSVs and micro-bumps. Chip level TSVs are used for die-to-die communications while interposer level TSVs are used for die-to-package interconnections. Therefore, any chip mounted on the interposer can communicate with external components and circuits through the Interconnect-TSV-Bump network. The interposer includes a redistribution layer (RDL) of wires and the silicon substrate. The RDL is a structure of multiple metal layers at the top of the interposer that provides horizontal interconnections between different dies. A Silicon Interposer contains a cluster of TSVs that provide vertical interconnections between dies and the package. The interposer is connected to the package by using C4 bumps. Each C4 bump contacts one TSV at the interposer bottom. Thus, the pitch of the TSVs is comparable to the pitch of the C4 bumps. In the Silicon Interposer fabrication, defects are observed during the process of die bonding and assembly. Moreover, the process variation in interconnects leads to parametric faults [4]. Typical defects in the interposer include resistive shorts and opens, which lead to increased interconnect delay, deviated characteristics and delay defects. Therefore, interposer testing is essential to screen defective 2.5D-ICs [118].

10.3. 2.5D-IC vs. 3D-IC

The interposer based 2.5D integrated circuit (IC) is getting popularity as a provisional alternative solution to 3D-IC. 2.5D-IC offers easier integration, better heat dissipation and low

cost. While 3D-IC offers better performance than 2.5D-IC by complex integration, high heat dissipation and high cost penalties. In 2.5D-IC, multiple dies are bonded side by side on a large interposer (which is often a piece of silicon with several routing layers but no device layer). The quality of the interposer is enormously important because multiple known-good dies (KGDs) are attached to the common platform. Any defect in the interposer (either catastrophic or parametric) may cause potential chip failure and reliability degradation. As a result, a comprehensive test of the interposer is important.

10.4. What is the difference between 3D Packaging, 3D-IC and 2.5D Interposer?

The three dimension (3D) packaging is defined by traditional methods of interconnect at the package level (i.e. wire bonding and flip chip) to attain vertical stacks. Examples of 3D packages include package-on-package (PoP) where individual die are packaged, and the packages are stacked and interconnected with wire bonds or flip chip processes and 3D wafer-level packaging (3D WLP) that uses redistribution layers (RDL) and bumping methods to create interconnects.

In 3D packaging, dies in the package talk using off-chip communication, looks like they are mounted in a separate package. Typically, 3D-ICs are categorized into 3D stacked ICs (3D-SICs), which denotes to piling IC dies and connecting them with TSVs. However, the real 3D-IC utilizes fabrication processes to stack multiple transistor layers on a single chip.

2.5D interposer is a configuration where dies are mounted side-by-side on the Silicon, Glass and Organic Interposer (substrate) by utilizing TSVs through the interposer. The glass/organic laminate is used as the interposer substrate while Vias are called through glass vias

(TGV) and through substrate via (TSV) respectively. Communication between the dies takes place via circuitry fabricated on the interposer.

10.5. Testing Benefits

Usually, the Interposer is fabricated by the high-yield process. However, the electrical characteristics in silicon could still deviate from its expected behavior due to the process variation, mechanical stress, and bonding effects. Fine-pitch micro-bumps are susceptible to open/bridging defects [120]-[122]. A micro bump could exhibit high resistance, which is induced by the thermal and mechanical stress of the bonding process. Even it does not lead to a full open circuit failure every time [120]-[122]. The number of interconnects/RDLs, TSVs, micro-bumps on the interposer is increasing rapidly (i.e. thousands because of the adoption of the wide I/O memory). Therefore, comprehensive interposer testing is required. For the timing validation, it is desirable to estimate the propagation delay of each conducting RDL, TSV, micro-bump in the Silicon Interposer.

10.6. Major Challenges

1) The interconnect/RDL fabrication in the Silicon Interposer with Width <4µm and spacing <4µm is challenging [113]-[114].
2) Because of the high bump volume short circuit among 40µm pitch Sn/Pb solder bumps occurs in the bonding process [113].
3) Few flaws among Cu-TSVs and Cu-land are observed at the level-2 interconnection after thermal cycle test because of the CTE (Coefficient of Thermal Expansion) discrepancy between the Silicon Interposer and organic substrate [113]-[114].

4) In the reflow process (260ºC), power and ground lines are delaminated at the sputtered Ti layer and SiO_2 interface, which leads to CTE discrepancy between Si-substrate and Cu layer[113]-[114].
5) In the level-1 interconnection, Au-In alloy allows transient liquid phase (TLP) diffusion bonding in low temperature (160-200ºC) because of the high melting point (495ºC) [114].
6) High stress at the level-2 interconnection, between Silicon Interposer and Cu-TSVs [114].
7)

10.7. CAD Design Challenges

3D-IC is facing several challenges, including the high Joule heating, TSV-introduced overhead, power delivery, clock delivery, design complexity of CAD, material processing, manufacturing, testing, lack of standard. Computer aided design (CAD) tools are not matured yet for 2.5D-IC/3D-IC design and simulation. This is a big concern in the development of 2.5D-IC/3D-IC design. Our existing CAD tools are needed to upgrade with 2.5D-IC/3D-IC features [110]. CAD tools must be developed in such a way that can analyze dynamic characteristics (power, performance, temperature) of the 2.5D-IC/3D-IC physical layouts. 3D MAGIC, Virtuoso Layout Editor with 3D layers, MicroMagic MAX-3D CAD tools are currently available for 2.5D-IC/3D-IC design. But they are not complete tools that allow schematic, layout design and analyze power, performance, area and temperature issues.

In this research work, the 2.5D-IC/3D-IC design and verification challenges are focused. Four metal layers (M1-M4) interconnects with width= 2µm, spacing= 2µm are designed and verified in 40nm-technology. Our hierarchical methodology allows both 2.5D-IC and 3D-IC

physical design and verification, which resolves these CAD limitations.

10.8. Physical Layout Design

Figure 10-1 shows the block diagram of 2.5D-IC where two 3D memory stacks and a buffer switch are mounted on the Silicon Interposer. Both 3D memory stacks are connected with MHUB (buffer switch). The Silicon Interposer is attached to a conventional package with a connector system. The package will provide power and support for testing of the chip. The package contains a FPGA, which allows connections with the Silicon Interposer. The FPGA also serves as the bridge between the buffering switch on the Silicon Interposer and the Mentor Graphics Veloce verification interface. This interface will make it possible to provide sophisticated sequences of test transactions based on testing algorithms developed during device verification. The physical layout is designed by the Micromagic MAX and the Global foundry 40nm technology library. Figure 10-2 shows the physical layout of the 3D IC on Silicon Interposer.

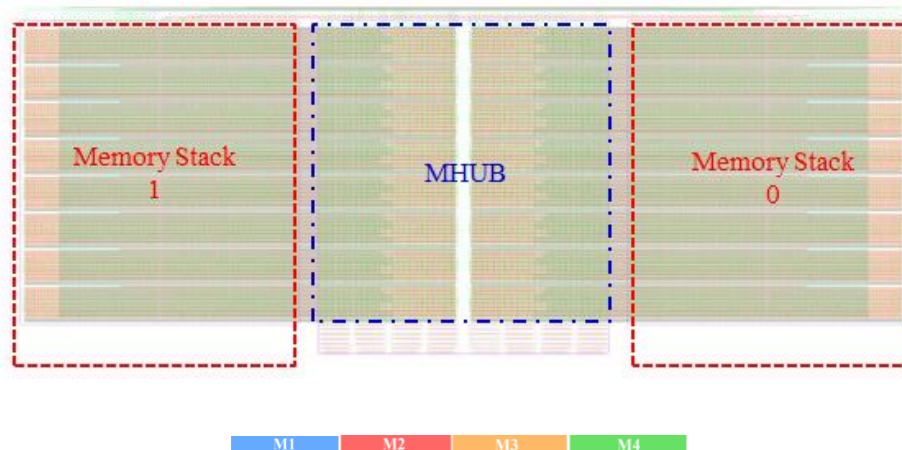
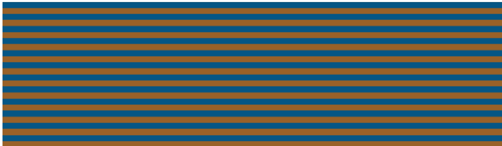


Figure 10-2: The physical layout (GDS) of 2.5D-IC, including two memory stacks, MHUB, Silicon Interposer. M1 and M3 interconnects are used to connect memory stack and MHUB horizontally. While M2 and M4 interconnects are used to connect power and ground vertically.

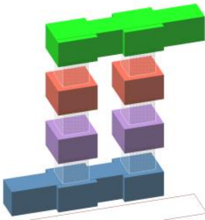
The usage of horizontal (M1, M3) and vertical (M2, M4) metal interconnects convention is fixed to minimize any complexity of the physical layout design, verification, fabrication and testing steps.

10.9. Interconnect

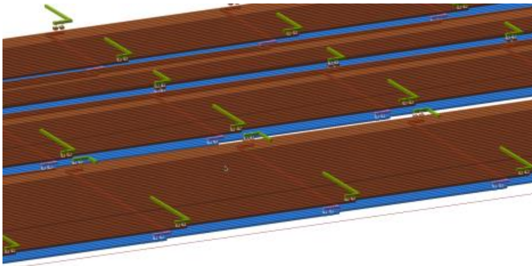
Four metal layers (M1, M2, M3, M4) are used for signal and power routing. M1 and M3 (Figure 10-3) are used to connect horizontal routing. This routing mainly facilitates signal lines. The pitch of these signal lines are only 2μm, which is the densest routing for 2.5D-IC interposer ever reported. While the vertical M2 and M4 metal layers are used for power rail connections. Although the color of four metal layers are different, only copper is used for every M1-M4. But each metal layer is isolated from other metal layer by an insulation.



(a) Top view



(a) 3D Vias and interconnect

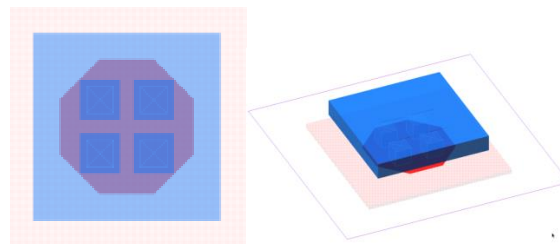


(c) 3D routing (Interconnects)

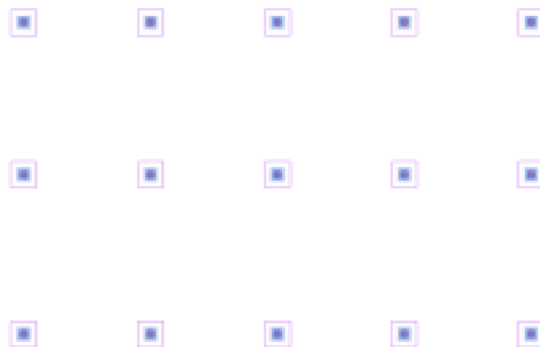
Figure 10-3: Routing design for connecting memory stack and MHUB. M1 (Blue) and M3 (Brown) are used for vertical interconnection. The width and thickness of each interconnect line is 2µm X 2µm. The lengths of interconnects are not fixed. Via V1 connects M1 and M2. Via V2 connects M2 and M3. Finally, via V3 connects M3 and M4.

10.10. Through Silicon Via (TSV)

The diameter of the signal TSV is smaller than the diameter of the power/ground TSV because very high power flows through these power/ground TSVs to power the stacked dies. The Cooper TSV is used in the designed as shown in Figure 10-4. The number of TSVs depends on the requirement. The diameter/width and height of the Copper TSV are 10µm and 100µm respectively. Figure 10-4 shows how a TSV is connected with the circuit with M1. M1is connected on the top of the TSV by four Vias to ensure good connectivity with the level-1 metal interconnect.



(a) Top view



(b) TSV array

Figure 10-4: The physical layout design of each TSV in the Interposer design. (a) Single TSV with Via and M1 connection, (b) TSV array in a specific area.

10.11. Silicon Interposers

TSVs are fabricated inside the Silicon Interposer by drilling. It reduces the extra costs of advanced logic and wafer thinning challenges. The Silicon Interposer of our design is shown in the whole 16 layers memory stacks and MHUB (Buffer switch) are designed on Silicon Interposer as shown in Figure 10-5. The connection pads are shown in Figure 10-5.

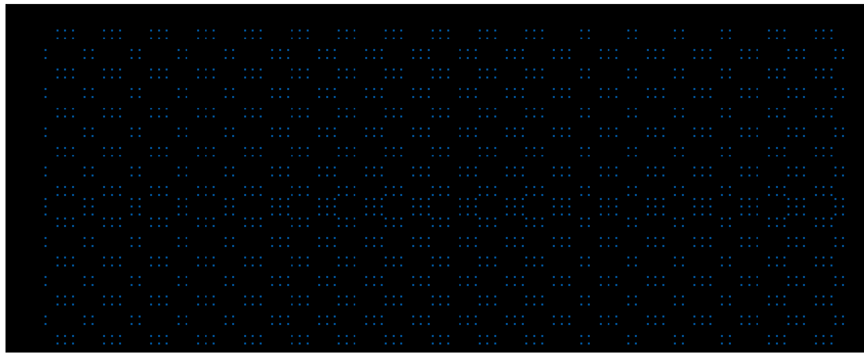
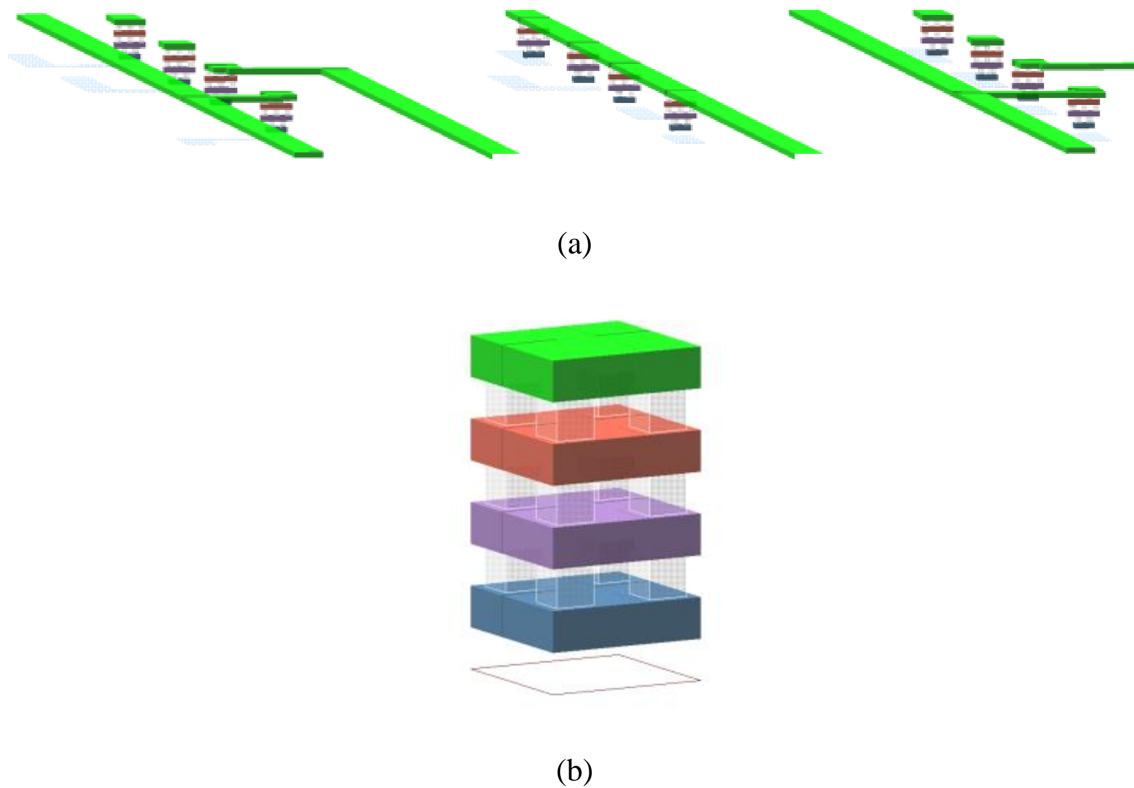


Figure 10-5: Pin array of the Silicon Interposer.

10.12. Power Rail

The power rail of the Silicon Interposer is designed by M4 as shown Figure 10-6a. It ensures power to every area. Figure 10-6b shows a Via ladder to connect M1 and M4 (power rail). The power rail carries huge power. So, four parallel Vias are used to connect two metal layers i.e. M1-M2, M2-M3, M3-M4.



(a)

(b)

Figure 10-6: The power rail for the 2.5D-IC.

10.13. Physical Verification

The design rule check (DRC) is performed according to the global foundry 40nm design rules. The rule file is customized according to the design rules for the TSV, RDL and Via (Table 10-1). Few exceptions are used when the width of the Via is greater than 2µm. No extra space is available in the physical design for the Via fins. That's why DRC rules are customized by adding these exceptions. Additionally, TSV design rules are added to the design rule file. Calibre interactive nmDRC (from Mentor Graphic) is used for DRC check. The parasitic are extracted by Calibre interactive PEX (from Mentor Graphic).

Table 10-1: Design rules of the Silicon Interposer [127].

Wafer Size	**200mm or 300mm**	
TSV Types	Via First / Cu fill Via Last / Cu Liner / PI Fill	
TSV Diameter	Via First Via Last	5~10μm 50~ 100μm
TSV Aspect Ratio	Via First Via Last	10:1 5:1
TSV Pitch*	50 μm	*either Via First or Via Last
Front Side Redistribution Layer	Planarized Cu Design Rules # of Front Side Layers:	2μm Line/2μm Space/2μm Thickness 4 nominal, more possible
Back Side Redistribution Layer	Planarized Cu # of Back Side Layers: Back Side RDL Design:	15 μm Line / 5 μm Space / 3 μm Thickness

10.14. Methodology

The research methodology of 2.5D-IC physical design and verification is illustrated in Table 10-2. The methodology is discussed step by step in the following subsections.

a) The Global foundry (GF) 40nm technology library is customized for the design.

b) Standard cells are used from the Global foundry database.

c) Custom cells are designed in the micromagic MAX.

d) This is a hierarchical design. So, the custom cells and standard cells are placed hierarchically.

e) In the floor planning the positions of C4 bumps, TSVs, RDLs are changed manually.

f) Verification: Although MAX tool has its own DRC check tool, Mentor's Calibre is used for DRC check to ensure industry standard.

g) Finally, DRC clean MAX file output is ready. Now GDS file is generated for standard fabrication.

h) LEF file is generated for the place and route (PnR).

i) LIB file is generated for timing analysis by the Cadence Encounter.

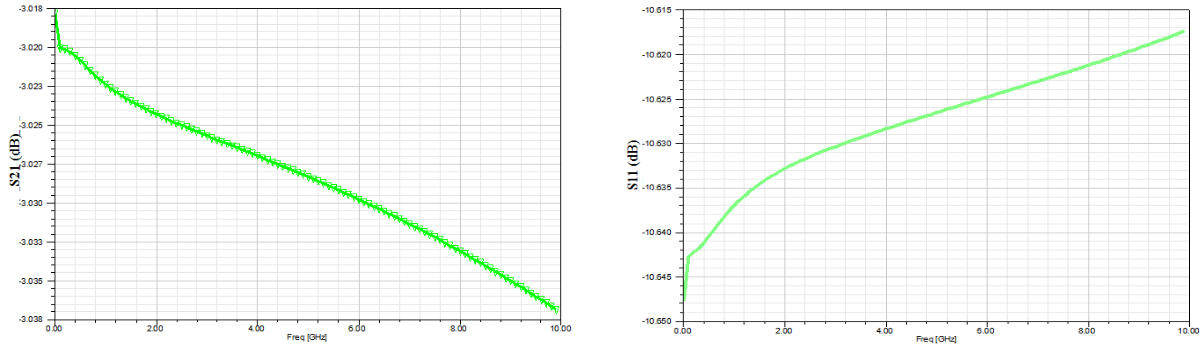
Table 10-2: Important physical design and verification steps of 2.5D-IC/3D-IC including industry standard CAD tools.

	Step	Industry standard CAD tools	Available at UMKC
Verilog/VHDL design	HDL Design	modelsim	SynaptiCAD
RTL Synthesis	RTL to Logic	Synopsys synthesis tools: Design Compiler/ Design Vision	Cadence: RTL Compiler
	Logic Optimization		Synopsys synthesis tools: Design Compiler/ Design Vision
	Logic to Technology		
	Timing, Area Optimization		
Physical Design	Physical Layout Design	Cadence: Virtuoso/ Micromagic: MAX	Cadence: Virtuoso
Floor Planning		Cadence: Encounter	Cadence: Encounter
Power Planning	VDD, VSS, GND placement	Cadence: Encounter	Cadence: Encounter
PnR	Place and route	Cadence: Encounter	Cadence: Encounter
Physical Verification	DRC Check	Mentor Graphic's Calibre: DRC	Cadence: Assura
	LVS check	Mentor Graphic's Calibre: LVS	Cadence: Assura
	Parasitic extraction	Mentor Graphic's Calibre: PEX	Cadence: Diva
Output Files	MAX file generation	Micromagic: MAX	Micromagic: MAX
	GDSII file generation	Micromagic: MAX	Micromagic: MAX
	.lef file generation	Micromagic: SUE	Micromagic: SUE
	.lib file generation	Cadence: Encounter	Cadence: Encounter
Sign-off and Tape-out	Formal Verification	Synopsys: VCS	modelsim
	Static Timing Analysis	Cadence: Encounter/ Synopsys: Prime time	Cadence: Encounter

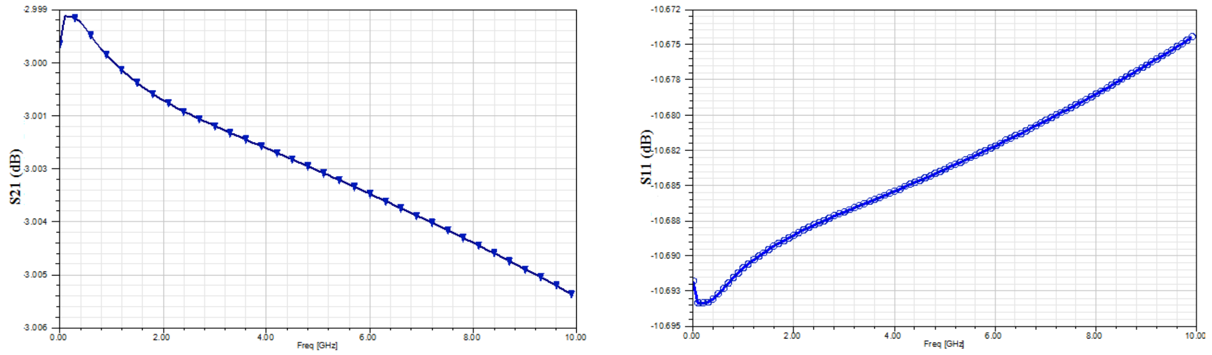
10.15. Signal Integrity of TSV

The effect of TSV height variation is very crucial in 2.5D-IC design. In order to realize the effect mathematically, the height of the three different TSVs are varied but other parameters are kept fixed. Figure 10-7a shows the high frequency analysis for the TSV with H_{TSV}=100 µm. Figure 10-7b illustrates the high frequency analysis for TSV with H_{TSV}=50 µm. Figure 10-7c presents the high frequency analysis for the TSV with H_{TSV}=25 µm. At the low frequency an irregular behavior is observed. It is observed that S21decreases at the high frequency for the three cases, which

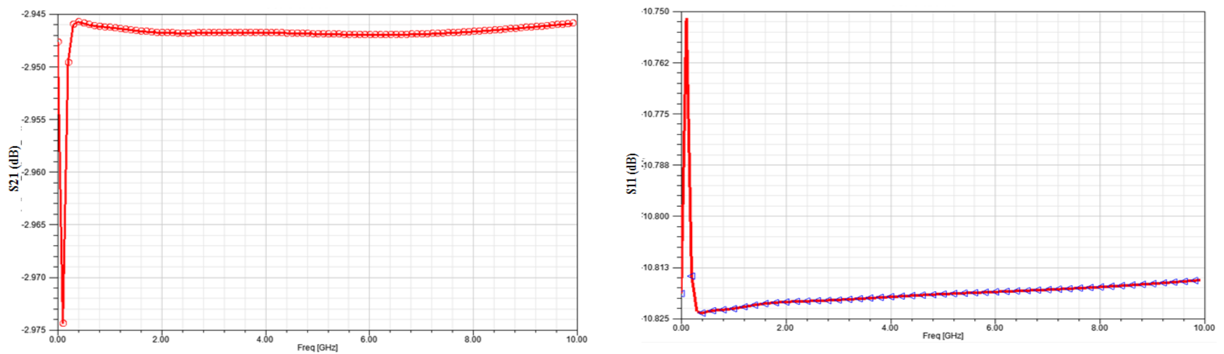
suggest that the insertion loss increases at the high frequency. On the other hand, S11 increases at the high frequency for three cases, which suggests that the return loss drops at the high frequency.



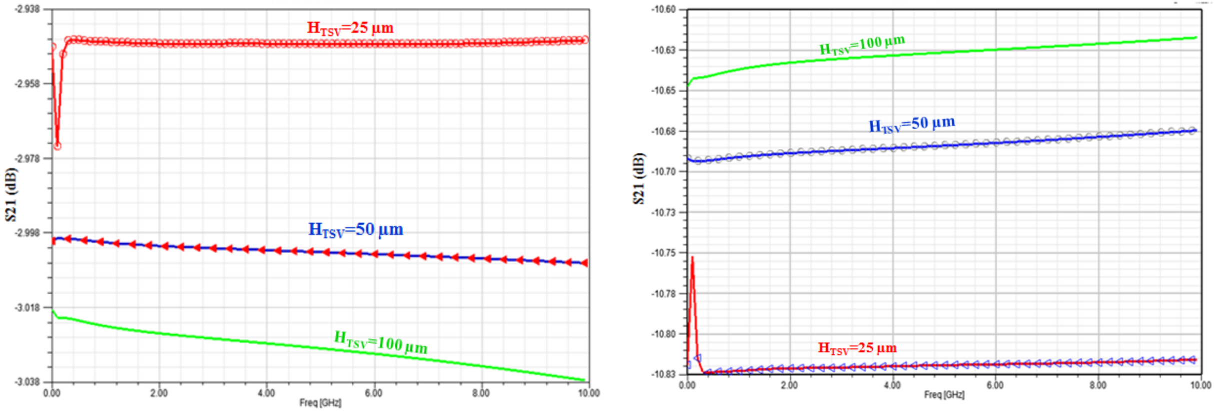
(a) H_{TSV}=100 µm, D_{TSV}=10 µm.



(b) H_{TSV}=50 µm, D_{TSV}=10 µm



(c) H_{TSV}=25 µm, D_{TSV}=10 µm.



(d) Comparison

Figure 10-7: The effect of TSV height variation in high frequency domain. (a) H_{TSV}=100 µm, D_{TSV}=10 µm, (b) H_{TSV}=50 µm, D_{TSV}=10 µm, (c) H_{TSV}=25 µm, D_{TSV}=10 µm, (d) comparison among the three cases shows that S21 (100 µm) < S21(50 µm) < S21(25 µm) and S11(100 µm) > S11(50 µm) > S11(25 µm).

To be more specific, the results of three cases are compared. The comparisons of S11 and S12 for different TSV heights are illustrated in Figure 10-7d. It is observed that that the insertion loss increases (S21 decreases) when the TSV height is increasing. But the return loss is decreasing (S11 increasing) when the TSV height is increasing.

The heights of the TSVs are kept constant at 32µm. The diameter of TSVs varies from 6µm to 10µm. It is clear that the insertion loss drops faster if the TSV diameter is decreased because the signal is getting less cross-sectional area in the TSVs as shown in Figure 10-8. However, for any given TSV height and diameter, the insertion loss reduces with the frequency.

Figure 10-9 shows that for a given TSV height and diameter, S11 exhibits overshoot at the low frequency but S11 increases significantly at the high frequency. According to Figure 10-9, at

the low frequency three TSVs (R_{TSV}=3µm, 4µm, 5µm) show an inconsistent return loss (S11). But as the frequency increases 3µm TSV has the lowest return loss and 4µm and 5µm TSVs has higher return loss.

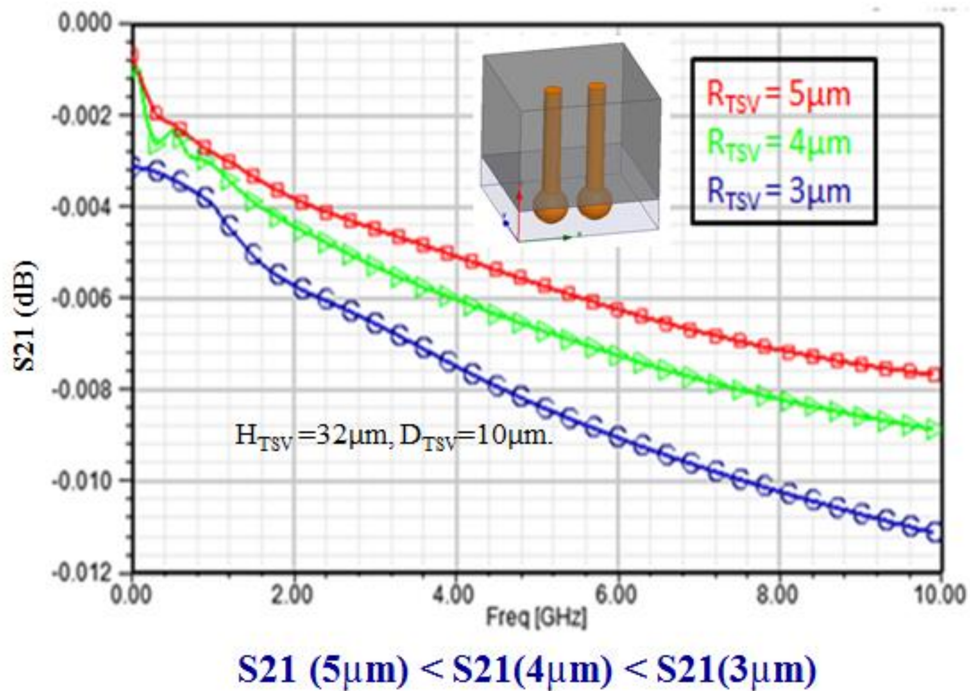


Figure 10-8: Insertion loss (S21) measurement of Cu TSV for three different diameter. H_{TSV} =32µm, D_{TSV}=10µm. $D_{TSV}=2R_{TSV}$. S21 (5µm) < S21(4µm) < S21(3µm).

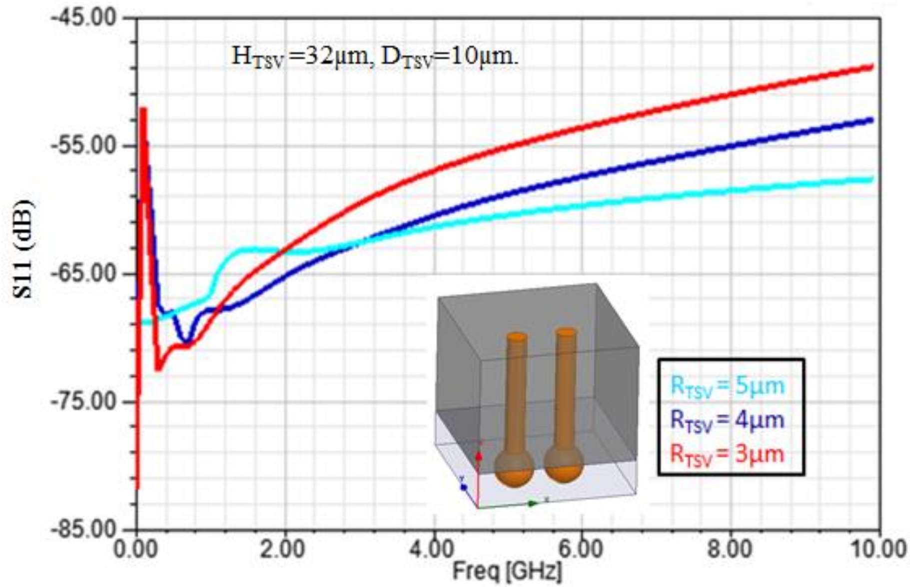


Figure 10-9: Return loss (S11) analysis of Cu TSV for three different diameters. H_{TSV} =32µm, D_{TSV}=10µm. Upto 3GHZ S11 shows overshoot, beyond that limit S11(5µm)>S11(4µm)>S11(3µm).

10.16. Comparison

The dimension of our Silicon Interposer is bigger than the previous reported designs. The diameter of our TSVs are 5~10µm (Via First) 50~100µm (Via Last), which is less than the diameter of the existing designs [113]-[114]. This enable less area overhead by TSV. Moreover, they did n't clearly mentioned whether these diameters are for Via First or Via Last.

The aspect ratio of our TSVs are 10:1(Via First) and 5:1(Via Last). This data is not provided by the previous authors. The uniform pitch of 50µm is used in our TSV design, which is better for big system design. But existing designs used multiple TSV pitch, which increases complexity in chip design.

Both front side and back side RDLs are considered in our design, while only front side RDL is considered in [113]-[114]. Four RDL (Redistribution Layer) are used in our design. More RDLs can be used in our design but only three RDL is used in [113]-[114]. The dimension (Line x Width x Thickness) of our RDL is 2µm x 2µm x 2µm. While the line value of [113]-[114] is not provided. Additionally, different width and thickness are used, which leads to design rule and physical layout complexity. Therefore, designs reported in [113]-[114], are not fit for automated CAD tools based design. Manual design and DRC check are the only solution for [113]-[114]. Therefore, to overcome these drawbacks, our procedure is more appropriate and automated for industry standard application. This design can be fabricated in both 200mm and 300mm wafer while no information is provided for previous reported Silicon Interposers.

Table 10-3: Comparison of our Silicon Interposer design with the existing Silicon Interposer designs [113]-[114].

	Parameters	Previous Silicon Interposer [113]	Previous Silicon Interposer [114]	Our Silicon Interposer Design
Technology node	nm			40nm
Silicon Interposer	Size	11x11 mm	22x12 mm	22x44mm
	Thickness	200µm	200µm	
TSV (Signal/Ground)	Pitch	800µm	150µm/300µm	50µm (Via First or Via Last)
	Diameter	60µm	60µm/120µm	5~10µm(Via First) 50~ 100µm(Via Last)
	Aspect Ratio			10:1(Via First) 5:1(Via Last)
RDL (Front side)	Line			2µm
	Thickness	3µm	2µm	2µm
	Pitch	8µm	1.6µm	2µm
	Layer	3	3	4 (nominal, more possible)

RDL (Back side)	Line			15 µm
	Thickness			5 µm
	Pitch			3 µm
Wafer	Size			200mm /300mm
Year		2008	2009	2015

** Blank means data is not available.

Chapter 11 : Conclusion and Future Work

The proposed MLGNR/CNT floating gate transistor for nonvolatile memory has the potential to utilize all the excellent electrical, physical, thermal, and material properties of graphene nanoribbon (GNR) and carbon nanotube (CNT). It opens the door for a new class of memory devices using graphene nanotechnology. Our preliminary concept is briefly presented in our recent conference paper [50]. In [50], we did not provide any analysis and modeling of the operation, physical and electrical behaviors, and the impacts of different parameters. Here we provided detail description of the design and the underlying scientific explanation behind the concept. We have performed analysis of the electrical behaviors and dynamic characteristics of the device. We have also derived the capacitive model of the device and performed analysis of the impact of scaling oxide thickness on performance. Through our modeling and analysis we have identified some critical electrical, physical, and geometrical parameters that would influence the operation and performance of the device.

It is concluded that for faster programming and erasing higher tunneling current density (J_{FN}) can be achieved by higher control gate voltage and scaling down the thicknesses of the control gate oxide and the tunnel oxide. However, higher tunneling current will severely damage the oxide's reliability. Therefore, optimization of these crucial parameters is recommended based on specific requirements. Our future work will focus on more accurate models for J_{FN} and other physical and electrical aspects need to be developed.

The scaling of the control and tunnel oxides in the proposed MLGNR/CNT FGT is discussed in details. It is clear that the coupling capabilities of the control gate and the channel are the functions of both the control and the tunnel oxides' thicknesses. In other word, if the tunnel oxide is scaled down, the CCR rises while the GCR drops. On the other hand, if the

control oxide is scaled down the GCR increases while the CCR falls. From these discussions, the 6nm tunnel oxide thickness and greater than 12nm control oxide thickness are recommended for the MLGNR/CNT FGT. The above statement is again supported by the tunneling current analysis through the tunnel oxide, which states that the tunneling current increases significantly when the tunnel oxide (SiO_2) is scaled down from 6nm to 5nm. Selecting proper insulation materials for the control and tunnel oxides is another important task. The GCR of the MLGNR/CNT FGT can be further improved by using high-k dielectric oxide on the control side and low-k dielectric oxide on the tunnel side of the gate. This would obviously increase design complexity. Our future work will focus on emerging insulation oxides like HfO_2 and Al_2O_3 as alternatives to SiO_2.

Our analysis reveals that the proposed device is capable of accumulating minimum required charge at a reduced voltage, which is a direct indication of low power design. It is observed that the control gate voltage is solely responsible for tunneling and accumulating electron in the floating gate. Another related issue is the retention of the accumulated charge. The retention property is still under detail investigation. It depends on the potential well at the floating gate. Higher potential well is better for retention. The potential well of our MLGNR-SiO_2-CNT structure is 3.65eV, while the conventional silicon FGT has a potential well of 3.07eV. Therefore, it can be predicted that our proposed device would have higher retention capability than the conventional Silicon FGT. Many contemporary works indicate that graphene (CNT and GNR) as floating gate material has good charge retention capacity. We propose CNT as floating gate, because we anticipate that a CNT layer would have better retention capacity than a GNR layer of similar dimension.

Considering the growing interest for graphene and carbon nanotube based devices for the next generation nanoelectronic applications, the proposed FGT would open the door for a new class of memory devices. The preliminary concept of this new generation of FGT is published in our recent journal paper [52]. For a new device concept to be validated there are many design, operation and reliability issues that need to be thoroughly investigated. A single journal paper cannot contain all these investigation. Therefore, this is a work in progress. In this paper, we have performed detail analysis of the dynamic behavior and current-voltage (*I*-*V*) characteristics of the proposed FGT. The dynamic behavior and the *I*-*V* characteristics are dependent on the internal device parameters. Therefore, we first derived the capacitive model of the proposed FGT. Then we have analyzed the voltage and charge accumulation on the CNT floating gate and investigated the impact of the terminal voltages and device parameters on the floating gate voltage and charge. The current-voltage characteristics as a function of MLGNR channel length and the number of GNR layer in the channel is also investigated to predict the channel characteristics of the proposed FGT device for different physical and geometrical conditions. The threshold voltage variation (ΔV_{TH}) is also investigated to determine the memory window of the proposed device. Finally, the programming, erasing and reading power consumptions of the proposed FGT are compared with the existing and emerging FGT devices. There are many other issues that need to be resolved. For example, the operation and the programming/ erasing process of the proposed FGT need to be validated through some experimental work and a methodology to control and optimize the operation must be developed. Also, an analysis of the impact of scaling the geometric and material parameters on the operation and reliability of the device is required. Our group is currently addressing some of these challenges.

Although the proposed concept of a new MLGNR-CNT based FGT seems promising, there are many issues and challenges that need to be analyzed and resolved as highlighted in this concluding section. The concept validation and the related analyses are based on simulation and mathematical modeling. We considered no gap between two adjacent graphene layers in the MLGNR channel to simplify our simulation. It is still an unresolved question whether there will be any gap or separating material between adjacent GNRs in a MLGNR structure for transistor and interconnect applications. In future we will attempt to perform some experimental work to complement our ongoing work.

In the reliability analysis, we have simulated the retention characteristics of the proposed GFGT. The the retention of the proposed GFGT, is a strong function of the drain voltage and tunnel oxide thickness. A mathematical model of FGT is proposed where the threshold voltage (V_{TH}) is considered as the key parameter. The V_{TH} of the FGT drops when radiation exposure increases. From our analysis, we have observed that the variation of V_{TH} in the FGT is (i) inversely proportional to the floating gate area, (ii) directly proportional to the control oxide thickness, and (iii) drops exponentially at the higher value of dielectric constant. Therefore, the mathematical model will be useful to analyze the radiation hardness of flash memory design and allow trade-off between important parameters. Our future work involves the radiation hardness test at every single design step of a device which will allow designers more flexibility in the radiation hardened memory design in future.

The physical, material and electrical parameters that would determine the Metal-MoS_2 contact property, are investigated. Both the top gate and back gate effects on the carrier concentrations are analyzed for the first time. Part of back gate effects is validated with the experimental data of [83] because it used back gate only. The top gate, back gate and combined

effects will be analyzed if the complete data is available in future. There is a fundamental difference between MoS_2 transistor and Si MOSFET. But there is no precise model exists for MoS_2 transistors as like Si MOSFETs to measure contact properties and sheet resistance. By using our analytical model fundamental parameters i.e. sheet resistance (R_{Sh}), contact resistivity (ρ_c), contact resistance (R_C) and transfer length (L_T) can be easily calculated, which leads to better Metal-MoS_2 contact design. We also discussed how the contact model can be integrated with modern IC EDA/CAD tools. Finally, a detailed database is provided for different contact material and predictive characteristics.

This work clearly explains how industry resolves 2.5D-IC/3D-IC design by using available IC design and verifications CAD tools. Different tools are used to ensure precise physical design. These standard 2D-IC tools are customized for this design. It's better if a company can come up with a consolidated 2.5D-IC/3D-IC design and verification tool. Later GDS, LEF, LIB industry standard files are generated for fabrication and further analysis. This design is done by 40nm technology but the same methodology is applicable for less than 40nm (i.e. 20nm) by using the specific technology (i.e. 20nm) library. The 3D EM full wave field solver simulations are done for TSVs, bumps, RDLs but all analysis are not placed because of the space limitation and confidentiality. We are unable to present few confidential specifications and issues because of our company policy. Our future research includes the low cost and simple Embedded Multi-die Interconnect Bridge (EMIB) 2.5D package in Intel14nm technology, which is a breakthrough for very high density interconnects between dissimilar chips on a single package.

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