NOVEL NON PRECHARGING SINGLE BITLINE

8T STATIC RANDOM ACCESS MEMORY

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8T STATIC RANDOM ACCESS MEMORY

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University of Missouri - Kansas City, 2013

ABSTRACT

Novel 8T SRAM design, employs individual bit-line (BL) and word-line (WL) for each operation. The read operation uses read word-line (RWL) and read bit-line (RBL) respectively. On other hand the write operation employs write word-line (WWL) and write bit-line (WBL). Due to single BL and WL the power consumption of the proposed 8T SRAM cell is significantly less.The proposed design avoids the stability and reliability issues of the conventional 6T and other existing SRAM cells. The read stability and the write ability of the proposed design are better compared to the standard 6T and other 7T, 8T and 9T SRAM designs. The proposed 8T SRAM is as good as the 10T design without the overheads. The power consumption of the proposed 8T SRAM cell is significantly lower than other SRAM cells. The proposed design is ratio-less, which makes the construction and operation of the proposed SRAM much simpler and the response time much faster. The proposed cell design and its reliability and stability have been analyzed for 45nm technology. We have also analyzed the static noise margin (SNM) and the stability of the proposed design. In this analysis, we have used three methods. First, the traditional SNM method with the butterfly curve is introduced. Second, the N-curve method is used. And finally, we used the bit-line voltage method. We have also analyzed the impact of some process and parametric variations. The write ability of the proposed design is also compared to that of the conventional 6T SRAM.

APPROVAL PAGE

The faculty listed below, appointed by the Dean of the School of Computing and Engineering have examined a thesis titled “Novel Non Precharging Single Bit-line 8T Static Random Access Memory” presented by Mahmood Uddin Mohammed, candidate for the master of science degree, and certify that in their opinion it is worthy of acceptance.

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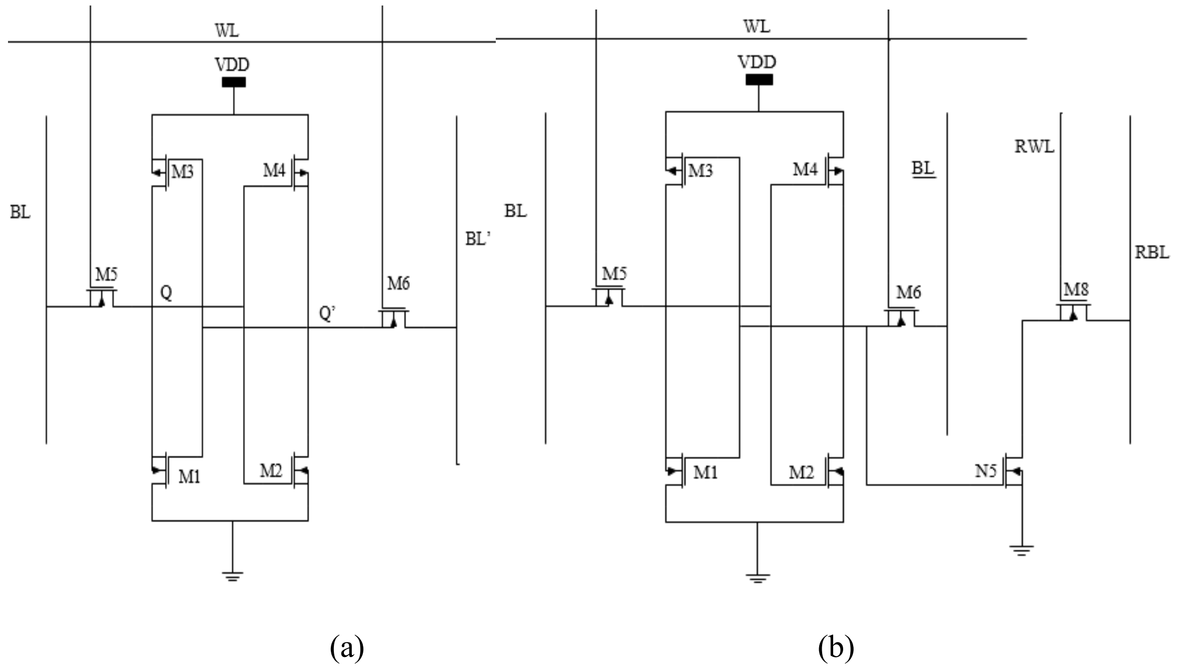
CHAPTER 1

INTRODUCTION

Low power design has become increasingly more important for diverse applications due to the growing demands for more functionality at higher energy efficiency, particularly in mobile and wireless devices. With the increase in required memory capacity and density, it has become very critical to ensure lower power consumption and higher speed of the memory cells and blocks, because memories form a large part of any system and the overall system performance is heavily dependent on the memory. Various techniques are employed to reduce power consumption and improve noise margin in memory design, which include circuit partitioning, dual threshold voltage scheme, increasing the thickness of the gate oxide for noncritical circuits, and many more. We propose a new 8T SRAM design, where the reading and writing operations are electrically separated to lowerpower consumption and improve noise margin. The proposed circuit is much simpler and energy efficient in terms of operation and more robust in terms of noise stability due to its ratio-less design feature. The rest of the paper is organized as follows. Section II provides a brief overview of the existing SRAM designs. Section III presents the proposed 8T SRAM circuit, which has the potential to overcome many limitations of the conventional SRAM designs. Section IV provides the analysis of the area and power overheads of the proposed 8T SRAM. Section V investigates the static noise margin (SNM) and the stability of the proposed 8T SRAM.Section VI explores the impact of process and parametric variation on the proposed cell. Finally, Section VII concludes with a brief overview of our ongoing and future work.



(a) (b)

Figure 1: (a) 6T SRAM circuit including two access transistors (M5 and M6), two cross coupled inverters (M1-M3 and M2-M4), two bit-lines (BLs) and one common word-line (WL)[1]; (b) 8T SRAM circuit, which has two additional stack transistors (N5 and N6), one additional bit-line (RBL) and two dedicated word-lines (WWL and RWL)[3].

CHAPTER 2

EXISTING SRAM DESIGNS

In this section, we provided a brief background of the existing SRAM cell designs. Different groups proposed many SRAM designs that use between 6 to 10 transistors per cell. Accordingly, these cells are known as 6T, 7T, 8T, 9T and 10T cells. In the next few subsections, we briefly discussed the most widely investigated SRAM cells from each group.

2.1 Conventional 6T SRAM

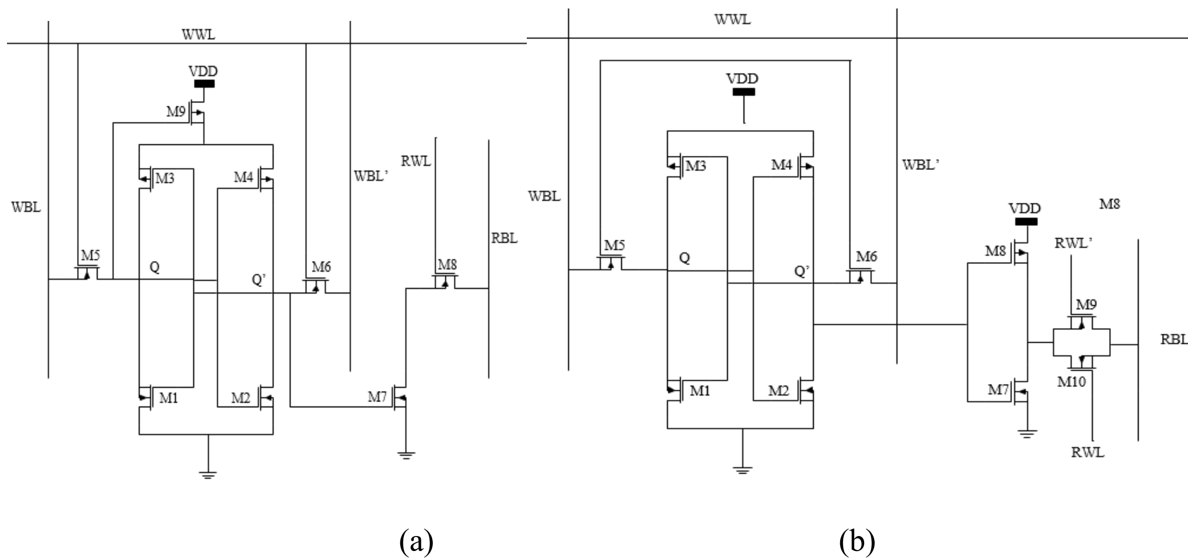
The conventional 6T SRAM cell as shown in Figure 1(a) has been the industry standard from the beginning of the SRAM era. Reliable read and write operations are the key consideration in SRAM design. Due to the simplicity and symmetry of the 6T SRAM cell circuit it is very area efficient. However, special attention should be given for properly sizing the transistors to avoid read and write upsets, because the design is based on ratioed logic principle that requires strict sizing ratios to ensure stable read and write operation. In the conventional 6T SRAM, two bit lines are used to store the data. The two BL architecture in 6T cell makes inadvertent toggling during read operation for cross coupled inverter. This increase the chances of errors during read operation. Besides, 6T SRAM cell fails to operate in the subthreshold region because of the process variation and reduced voltage level[*1*]. Therefore, 6T SRAM cell is not suitable for ultra-low-power circuits that would be operated in the subthreshold region.

As improvements over the conventional 6T SRAM cell, many designs of 8T, 9T and l0T SRAM cells have been proposed.These designs use different techniques to improve the functionality and stability of SRAM cell.Some of these techniques are (i)using separate read mechanism, (ii) feedback cutting, (iii) asymmetric design, and (iv) one-sided access[*1*]-[4].

2.2 8T SRAM

In 8T SRAM as shown in Figure 1(b), there are two additional stack transistors that provide the access to the cell through the additional read bit-line (RBL). It has two dedicated word-lines (WWL and RWL). Everything else is similar to the standard 6T SRAM. The reading operation of this 8T SRAM is separated from the rest of the cell, whichincreases the read static noise margin (RSNM). Higher noise margin ensures better read stability and robustness. The read operation of 8T SRAM does not disturb the storage data of cell. However, 6T SRAM is vulnerable to read upset, because in 6T the access transistor pulls the “0” storage node above the ground, which degrades the SNM.

The performance of 8T SRAM during the read operation is determined by the strength of the read stack transistors.To improve the read stability of 6T SRAM cell both halves of the cells should be enlarged. But in 8T SRAM, the read stability can be improved by increasing the size of the stack transistorsonly[3].However, the design of this 8T SRAM cell is still ratioed and its write operation is still similar to the conventional 6T SRAM.



(a) (b)

Figure 2: (a) 9T SRAM cell circuit[3]and (b) 10T SRAM cell circuit[5].

2.3 9T SF-SRAM CELL

There are several designs that utilize 9 transistors per cell. One of the most widely investigated 9T SRAM cell is the 9T Supply-Feedback SRAM (9T SF-SRAM) as shown in Figure 2(a), which consists of an addition supply gating transistor (M9) compared to the 8T SRAM cell described above. Everything else is similar to the 8T SRAM. To increase the write ability, 9T SRAM employs supply feedback approach. This approach is executed by connecting M9 in the feedback loop with the storage node (Q). This weakens the pull up path of the cell during the write operation. As a consequence, flipping of the cell data is much easier during the write operation. Moreover, the internal gating generates a small voltage drop at the drain of M9 during the hold stage. This results in lower leakage currents at the expense of the reduction in hold static noise margin (HSNM).Besides, the extra transistor (M9) increases the area and reading time. Power consumption of 9T SRAM is also higher than the previous designs. Also, due to the asymmetric circuit construction, the complexity and area consumption of this design would be much higher[3].

2.4 10T Single-Ended SRAM

The conventional 6T, 8T and 9T SRAM designs require pre-charging of the bit-lines during the read operation. This pre-charring imposes serious energy and timing constraints on the design and operation of high-density and high-capacity SRAM applications. Figure 2(b) shows the circuit of a non-precharge 10T SRAM with a single-ended read BL. It is similar in structure to the 8T SRAM. There are two additional PMOS transistors (P3 and P4) as shown in Figure 2(b). It is a combination of the standard 6T SRAM cell, an inverter and a transmission gate. RWL controls the NMOS transistor (N6) at the transmission gate and RWL' controls the PMOS transistor (P4) at the transmission gate, which is the inverted signal

of the read WL (RWL). As RWL and RWL' are activated, the transmission gate is triggered and the stored node gets coupled to RBL through the inverter[5]. In this 10T SRAM design, the precharge circuitry is eliminated, because the inverter fully charges/discharges the RBL.No power is consumed by the RBL if new arrived data is similar to the previous state. Therefore, 10T single-ended SRAM cell consumes no additional power if consecutive "0"s or "1"s are read out. The charge and discharge powers are only consumed if the readout data is different from the previous state. The transient probability on RBL is 50% for 10T single-ended SRAM in a sequence of random data, thereby reducing power consumption significantly during the read operation[5]. However, additional devices and required wirings impose higher area overheads compared to 8T and 9T SRAMs.

CHAPTER 3

PROPOSED 8T SRAM

The proposed 8T SRAM is a ratio-less design and is much simpler, because there is no size ratio restriction. Whereas in 6T SRAM, special attention must be given to size the transistors to avoid read upset or data flipping at the storage node[4].For example, if we want to design SRAM cell using 90nm technology node most of the transistor sizes for the 6T SRAM design have to be several times larger than the minimum size (90nm) transistor to satisfy the size restrictions related to the cell ratio (CR) and the pull-up ratio (PR) of the 6T SRAM. Whereas, the proposed 8T SRAM can be designed using the minimum sizes of the transistors.

Table 1 shows the transistors' width comparison for the 6T and proposed 8T SRAM cells to be implemented in 90nm.Accurate sizing of 6T SRAM transistors is required to avoid accidental writing of a "1" into the SRAM cell during a read "0" operation. This type of malfunctioning is called read upset. The previous 8T SRAM [*2*]is also to some degree dependent on the size ratio of the transistors. There are several 7T SRAM cell designs that have the same limitation[6]. Our proposed 8T SRAM cell offers immunity against this type of read upset by employing the inverter (M7-M8), which isolates the storage node (Q') from the RBL in the proposed design. Therefore, the read out of the node Q' value can be performed without disturbing the stored data.

Table 1: 6T SRAM and proposed 8T SRAM transistors width.

Width (nm)	6T SRAM	Proposed 8T SRAM
Pull up transistors	90	90
Access transistors	180	90
Pull down transistors	240	90

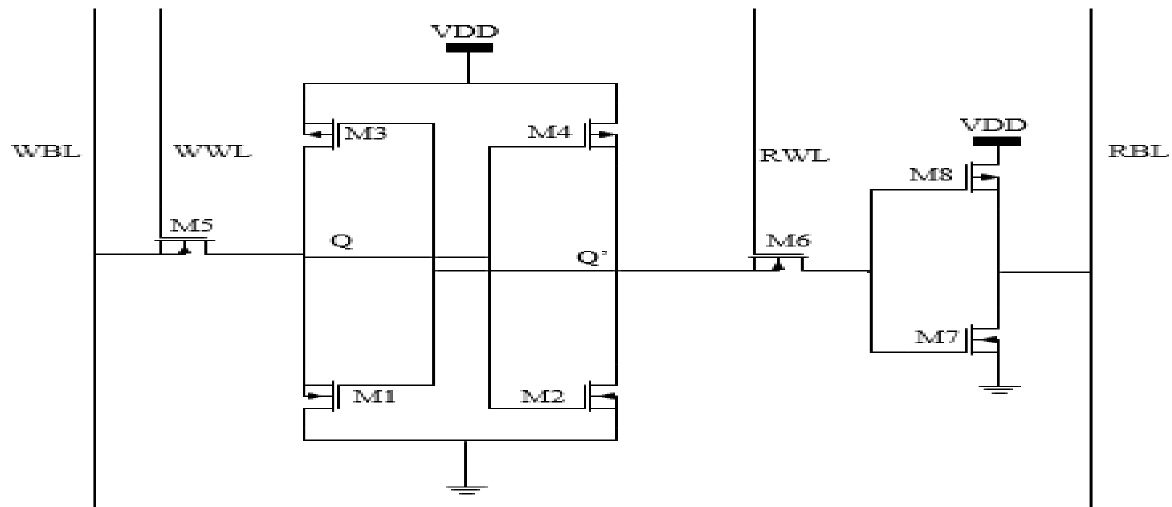


Figure 3: Proposed 8T SRAM with two access transistors, two cross coupled inverters, one WBL, one RBL, one WWL, one RWL and an additional inverter for the read operation.

In theconventional 6T SRAM cell two bit-lines (BL) and one word line (WL) are used during the read and write operations. Whereas, in the proposed design only one BL and one WL are used. This effectively reduces the power consumption during the read and write operations of the proposed design.The standard 6T SRAM shows low read stability and write ability in the sub-nm regime.The proposed design offers higher read stability and write ability in the sub-45nm region.

The proposed 8T SRAM design have similar attributes like the 10T SRAM. The design eliminates pre-charging circuit, as the inverter fully charges/discharges the RBL. As a result, significant reduction can be achieved in power consumption and overall area of the memory system. This is a huge improvement over the standard 6T SRAM and other 7T, 8T and 9T SRAM cells, all of which require pre-charging of the bit lines during the read operation that increases power consumption of the memory cell significantly.The proposed 8T SRAM consumeno additional power if consecutive “0”s or “1”s are read out.Enormous amount of power can be saved during the read operation of the proposed design, because the transient probability on the RBL is reduced to 50%. Therefore, the proposed 8T SRAM cell design offers the robustness and energy efficiency of the previously 10T SRAM cell design[5] without the additional area overheads for the extra devices.

The limitations of the conventional 6T/7T/8T SRAM cells are summarized as in Figure 4, which also identifies the positive aspects of the proposed 8T SRAM cell. Table 2 provides a comparison of existing SRAM cells and the proposed design.

Conventional 6T/7T/8T SRAM

- Ratioed logic.
- Precharges all BLs during the read operation
- High leakages and parasitic.
- High power consumption.
- Slow Reading.
- High power consumption in the read operation.
- Whole circuit is active during the read and write operation.
- Low stability during the read operation.

Potential Solution

Proposed 8T SRAM

- Rarioless logic.
- No precharging is needed.
- Low leakages and parasitic.
- Low power consumption.
- Fast Reading.
- 50% less power consumption in read operation, if output is same as previous state.
- Partial circuit is active during the read and write operation.
- High stability during the read operation.
- Transistor sizing based is not dependent designing rules.
- Pre-charging circuit is present, hence reduced memory system area.

Figure 4:Representing the need of the proposed 8T SRAM to overcome problem faced by the conventional designs.

The operation of the proposed design is explained in two parts: the writing part (Figure 5) and the reading part (Figure 9). The writing part consists of the access transistor (M5), WWL, WBL and the two cross coupled inverters of the SRAM cell. While, the reading part consists of the access transistor (M6), the extra inverter (M7-M8), RWL, RBL and the cross-coupled inverters of the SRAM cell.

Table 2: Comparison of existing designs and proposed 8T SRAM.

SRAM Design	Conventional 6T [1]	Single bitline7T [6]	8T SRAM [2]	Single Ended 8T [3]	Proposed 8T	9T [3]	10T Single End [5]
Transistor Count	6	7	8	8	8	9	10
Pre-charging Circuit at the output needed	Yes	Yes	Yes	No	No	Yes	No
Area Efficient	Yes	No	No	No	No	No	No
Symmetry	Yes	No	No	Yes	Yes	No	No
Active Write Bit-line	2	1	2	2	1	2	2
Active Transistor during "Write" Operation	6	5	6	6	5	6	6

Table 3: Comparison of existing designs and proposed 8T SRAM (continued).

SRAM Design	Conventional 6T [*1*]	Single bitline7T [6]	8T SRAM [*2*]	Single Ended 8T [3]	Proposed 8T	9T [3]	10T Single End [5]
Active Transistor during "Read" Operation	6	6	6	6	7	7	8
Read margin	Less	More	More	More	More	More	More

3.1 Write Operation of the Proposed 8T SRAM

Figure 5shows the active circuit during the write operation. During the write operation, WBL and WWL are activated while RWL is deactivated. The access transistor M5 is on while M6 is turned off because RWL is deactivated. As a result, the write operation is separated from the read operation. This separation prevents accidental data flipping.Since all the transistors in the proposed 8T SRAM can have the same size (minimum size), it can avoid strict transistor ratio requirement imposed on conventional 6T SRAM cell write operation.

Figure 6 shows the write "0" operation.During the write "0" operation, WWL is active, RWL is deactivated and WBL is low. At the storage nodes, Q = 0 and Q' = 1.Figure 7 shows the write "1" operation. During the write "1" operation, WWL is active, RWL is deactivated and WBL is high. At the storage nodes, Q = 1 and Q' = 0.

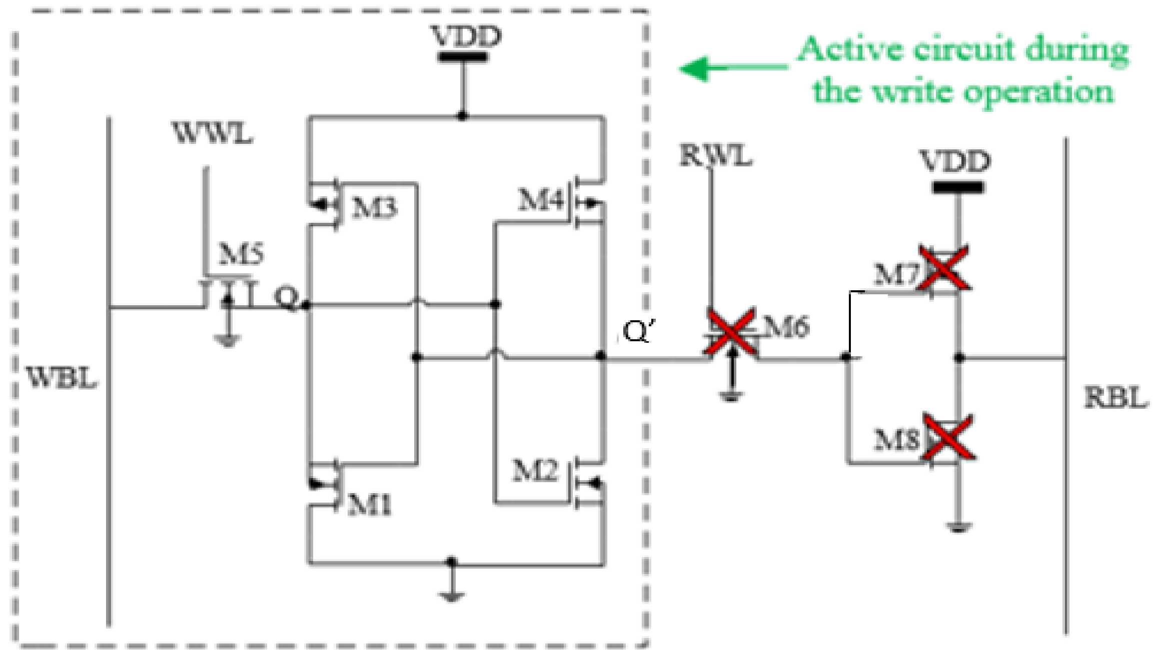


Figure 5: The active circuit during the write operation of the proposed 8T SRAM.

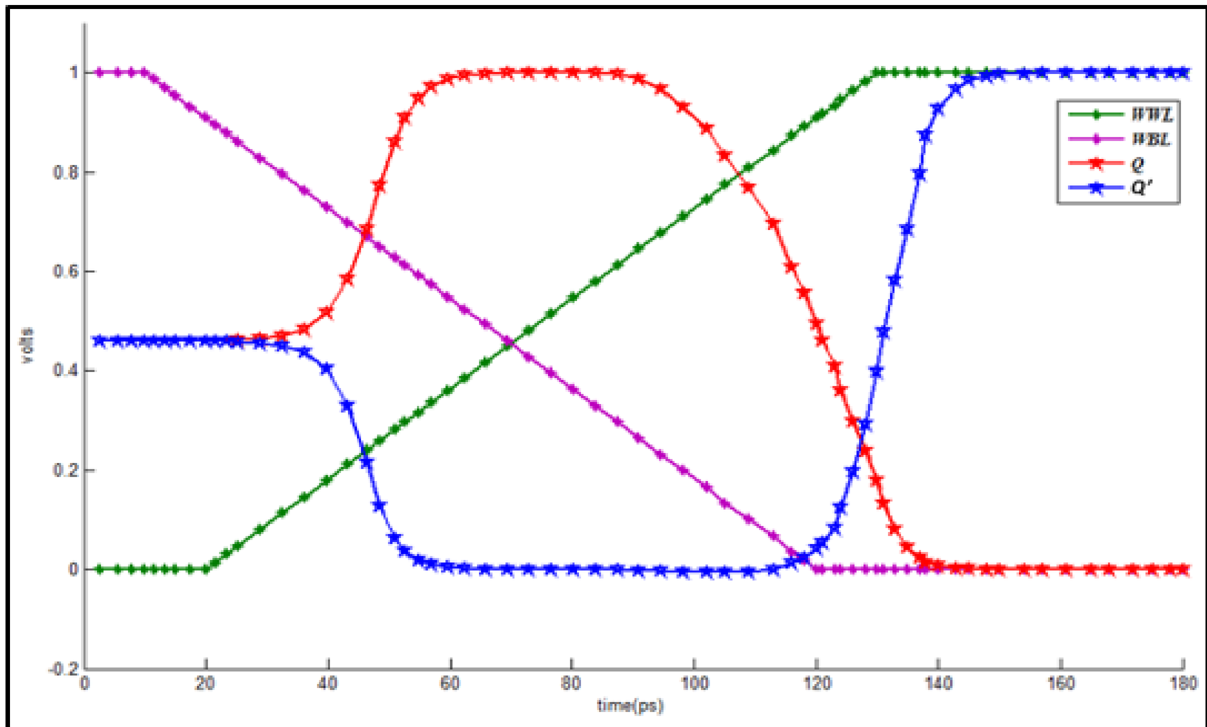


Figure 6: Write "0" operation in 45nm technology.

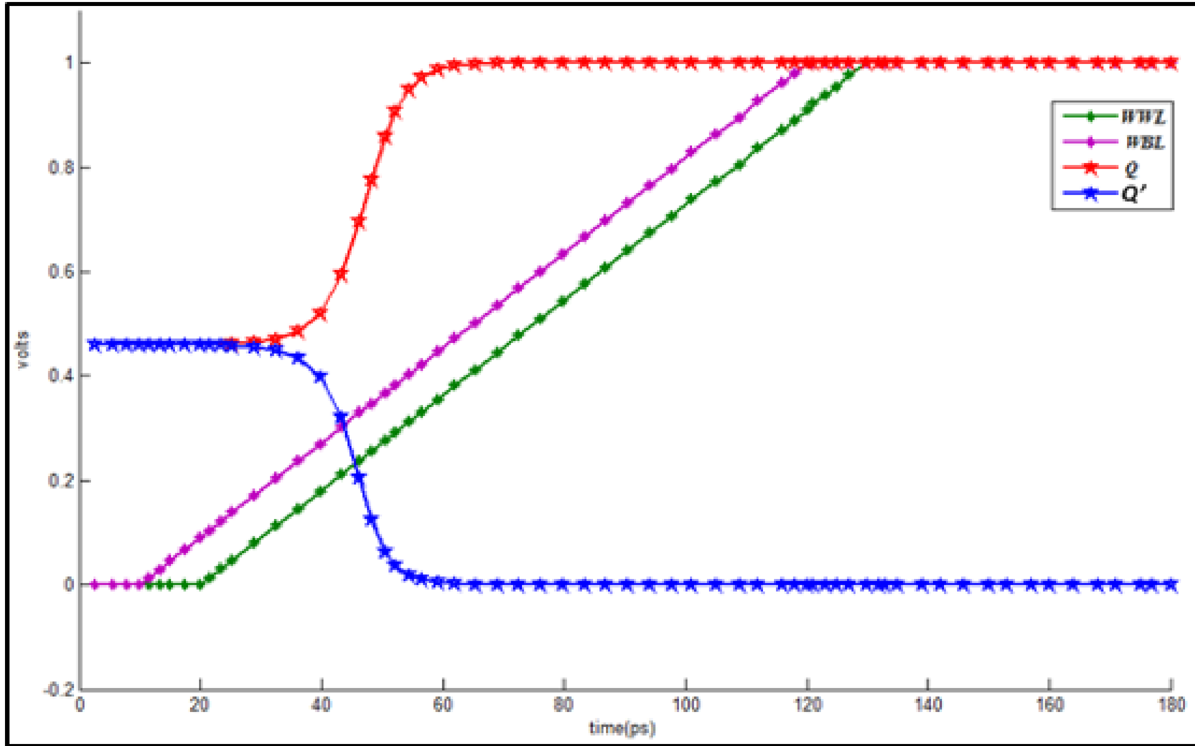


Figure 7: Write “1” operation in 45nm technology.

Only five transistors are activated during the write operation. Therefore, the power consumption during the write operation in the proposed design is less compared to its read operation.Moreover, due to the separation of the write operation from the read operation, the write static noise margin (WSNM) of the proposed 8T SRAM design would be higher than that of the 6T SRAM. Figure 8shows the variation in WSNM of 8T and 6T SRAM with the supply voltage.

3.2 Read Operation of the Proposed 8T SRAM

Figure 9 shows the active circuit during the read operation. During the read operation, only RWL is activated, while WWL and WBL is deactivated. Transistor M6 is triggered when RWL is activated. The read part is separated from the write part, as WWL and WBL are deactivated and transistor M5 is off. The storage node Q’ is isolated from the local RBL through the

inverter (M7-M8). Therefore, the stored value at Q' is not disturbed, which increases the read static noise margin (RSNM). Figure 12 shows the variation in RSNM of 8T and 6T SRAM with supply voltage.

Data stored at Q' is transferred through the transistor (M6), which is fed as input to the inverter (M7-M8). Figure 10 shows the read "0" operation. During the read "0" operation, WWL and WBL are deactivated, while RWL is activated. The final storage value at Q is 0. Figure 11 shows the read "1" operation. During the read "1" operation, WWL and WBL are deactivated, while RWL is activated. The output at Q storage node is 1.

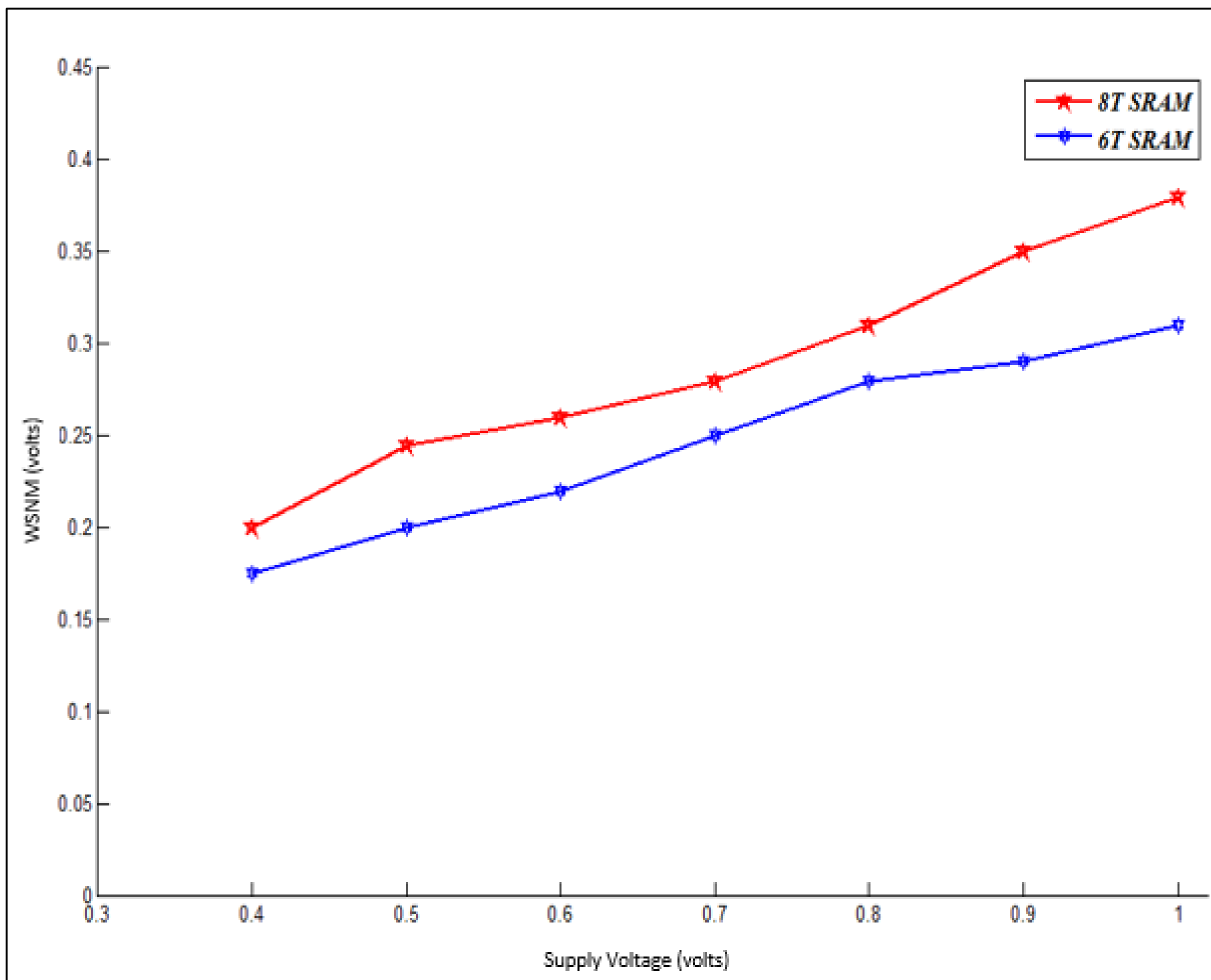


Figure 8: Variation of WSNM with supply voltage for 8T and 6T SRAM.

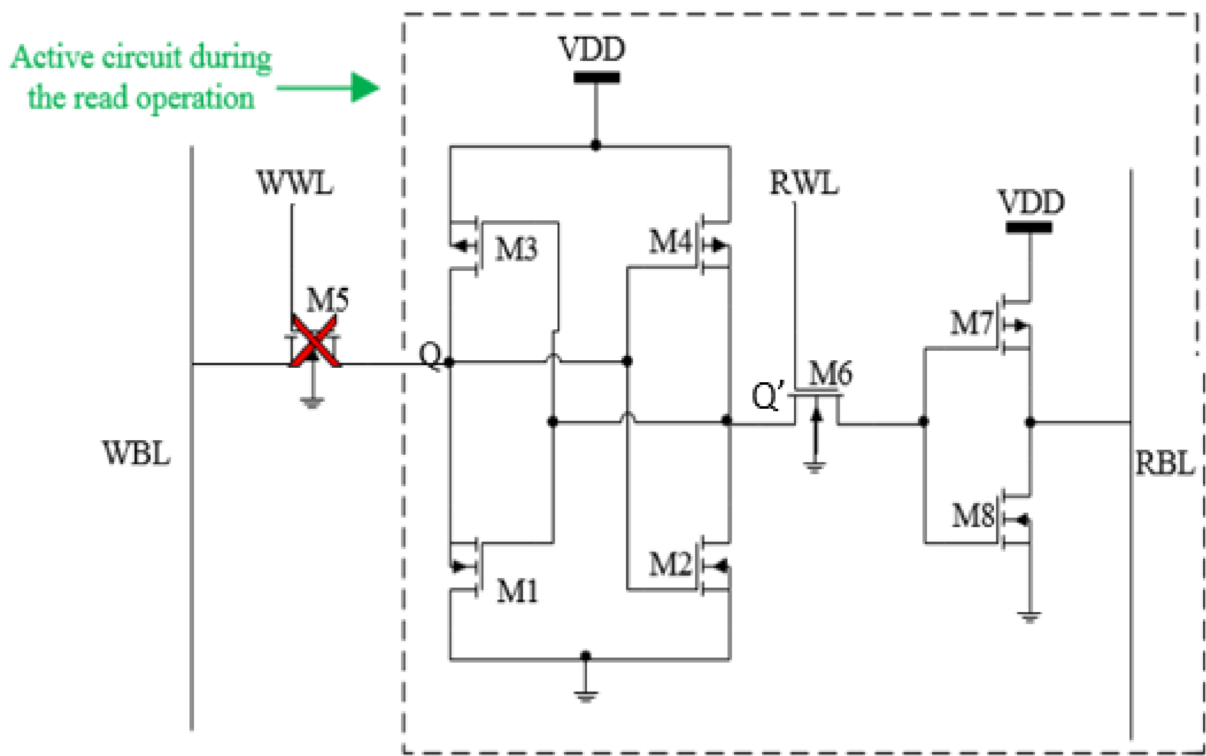


Figure 9: Active circuit during the read operation of the proposed 8T SRAM.

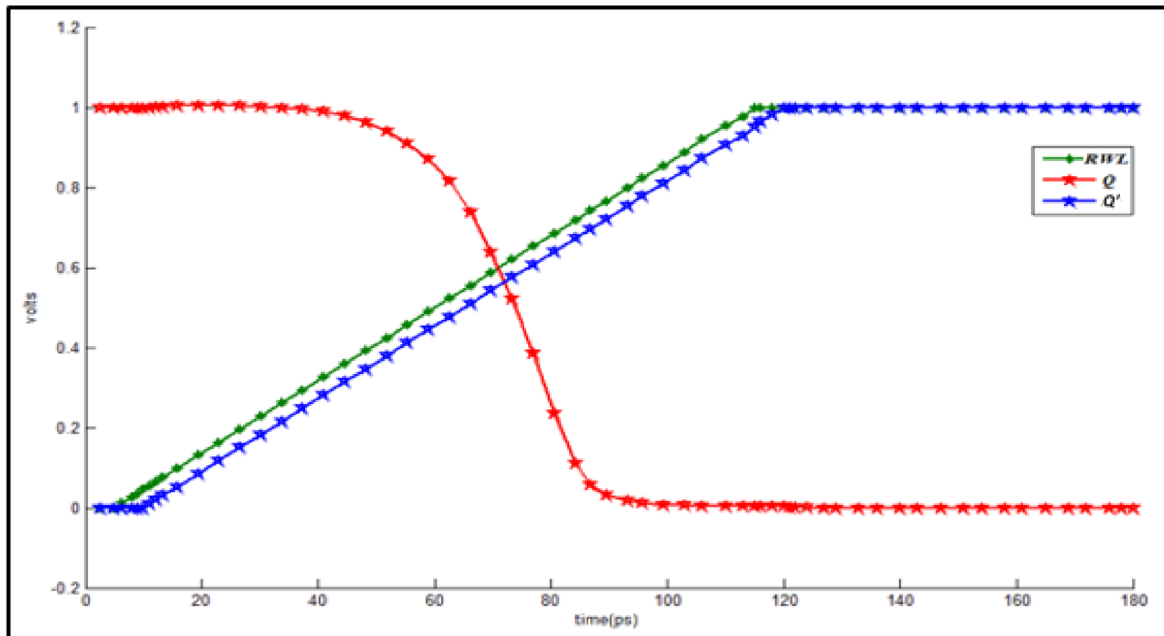


Figure 10: Read “0” operation.

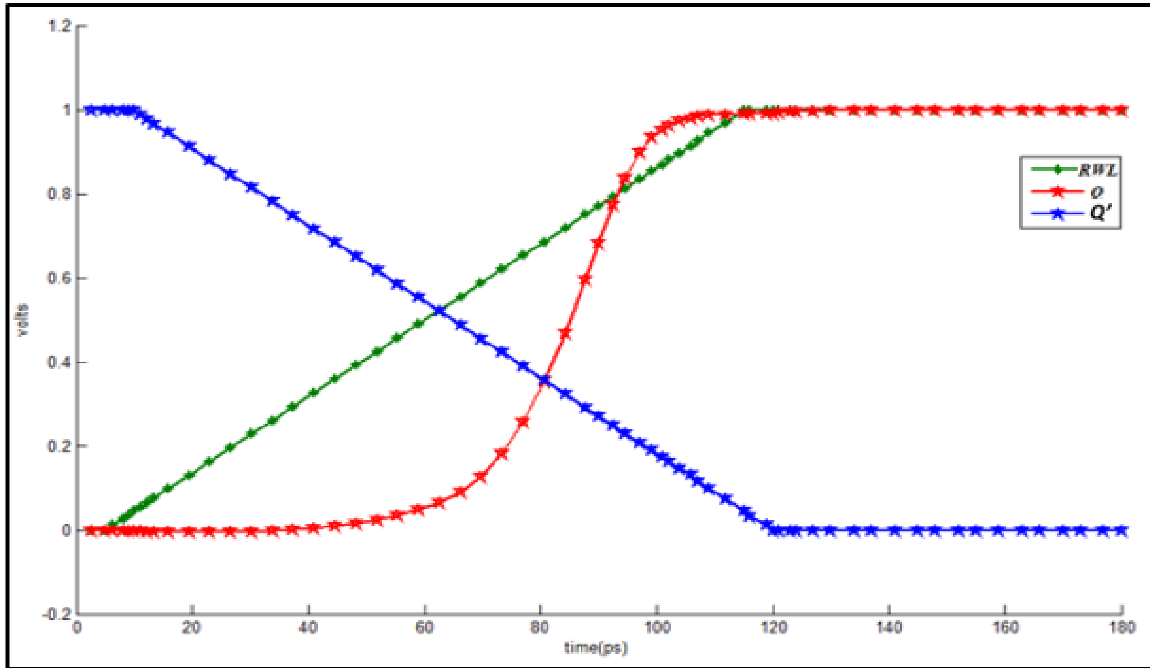


Figure 11: Read "1" operation.

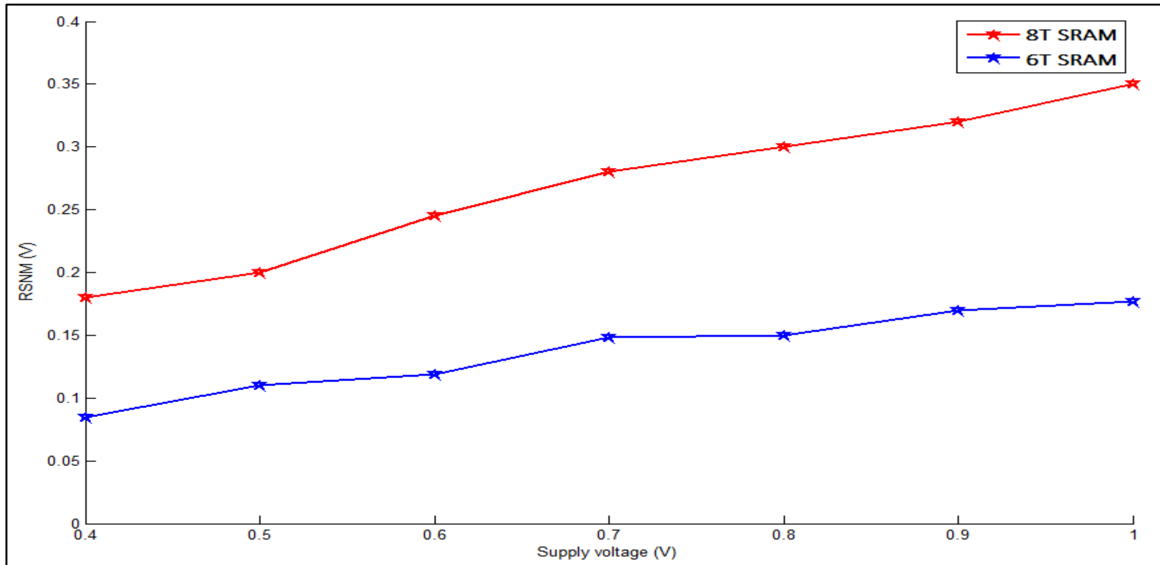


Figure 12: Variation of RSNM with supply voltage for 8T and 6T SRAM.

3.3 Hold Operation of the Proposed 8T SRAM

The 8T SRAM will be in the hold mode when WWL, RWL, WBL and RBL are deactivated. In this mode, the logic will be preserved between the cross coupled inverters.

CHAPTER 4

ANALYSIS OF POWER AND AREA OVERHEADS OF THE PROPOSED 8T SRAM

To provide a clear picture of the prospects of the proposed 8T SRAM cell, we have compared the power consumption and area overheads with the other existing SRAM designs.

4.1 Power Consumption of the Proposed 8T SRAM

In the previous works, different SRAM designs are implemented using different technology nodes from 40nm to 65nm. For fair comparison of power consumption, we have simulated all the SRAM circuits using 45nm technology node. Table 4 provides the data regarding the total power consumption (read and write operation combined) in different SRAM cells (6T to 10T) including our proposed new 8T SRAM design. The analysis is done in 45nm technology with 1V supply voltage. In this analysis we considered only the power consumed by the cell itself. We did not add the power consumption of the pre-charging circuits in conventional 6T, 7T, 8T and 9T SRAM cells that require pre-charging of the bit-lines during the read operation. Therefore, the actual power consumption during the read operation of these 6T, 7T, 8T and 9T SRAM cells would more than what is shown in Table 4. This indicates that our proposed new 8T SRAM cell will be significantly more energy efficient than all these previous designs both at the individual cell level as well as at the overall memory system level. We are currently working to implement a large memory system array using the proposed new 8T SRAM cell. Due to space limitation we cannot add the system level analysis in this paper.

Table 4: Power consumption analysis of single memory cell in 45nm technology with the supply voltage of 1V.

Design	Write 0 Power (nW)	Write 1 Power (nW)	Read 0 Power (nW)	Read 1 Power (nW)
Conventional 6T cell[1]	16.87	16.87	4.37	61.96
Single bit-line 7T cell[6]	15.08	14.62	4.37	65.46
8T cell[3]	18.02	18.47	8.75	30.28
Dual port 8T cell[2]	10.17	483.51	3.61	27.11
Single Ended 8T cell[5]	18.71	10.54	8.751	2.52
Proposed 8T cell	18.02	18.02	1.82	3.27
Conventional 9T cell[4]	78.63	75.28	96.24	9.66
9T SF-SRAM [3]	64.03	20.7	0.96	57580
Single Ended 10T cell[5]	87.18	150	17.17	590

4.2 Area Overhead of the Proposed 8T SRAM

For the calculation of the area overheads, we have performed the layout of the proposed 8T SRAM using 45nm technology data in Cadence. Figure 13 shows the layout of proposed 8T SRAM.

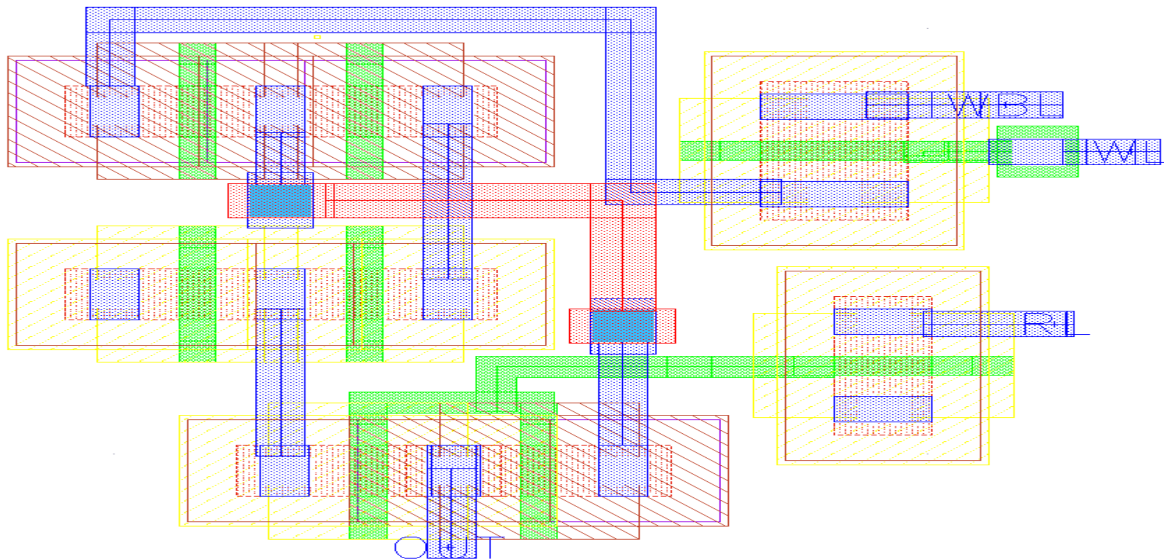


Figure 13: Layout of proposed 8T SRAM in 45nm technology node.

Table 5 provides a comparative analysis of the area overheads of different SRAM cells. We have implemented the conventional 6T SRAM cell using the 45nm technology node as well. It is observed that the area overhead of our proposed 8T SRAM increases by only 10% compared to the conventional 6T SRAM cell even with the additional transistors and wiring required for the proposed 8T SRAM design. This is due to the fact that conventional 6T SRAM cannot be implemented by minimum width transistors due to its ratioed design. But for the proposed 8T SRAM design we can use minimum width transistor for the whole circuit. We did not implement the layout of the existing 8T and 9T SRAM cells. However, from published literature [3] we can see that for 40nm technology node the area overheads of existing 8T and 9T cells are slightly less than our proposed 8T cell. We can anticipate that at 45nm technology node existing 8T cell would consume the same area as our design and the existing 9T cell would consume slightly higher area for the same technology node. Even with the same or slightly higher area overheads, our proposed design will be more attractive due to its other positive aspects and advantages as described in this paper.

Table 5: Single memory cell area of different SRAM designs.

Design	Area (μm^2)	Technology (nm)
Conventional 6T SRAM	0.986	45
8T SRAM[3]	0.8875	40
9T SRAM[3]	1.058	40
Proposed 8T SRAM	1.092	45

CHAPTER 5

STABILTY ANALYSIS OF THE PROPOSED 8T SRAM

Two of the most critical reliability and robustness metrics of SRAM are read stability and write ability. The write margin or the write ability is the minimum voltage on the BL to flip the data at the storage nodes (Q and Q'). The write margin increases with the increase of the sizes of the pull-up and access transistors (M4 and M6). Therefore, higher pull-up ration (PR) leads to higher write margin[9]. The read margin characterizes the stability of SRAM cell. It determines SRAM read stability as a function of V_{TH} and VDD variations. The read margin increases with the increase of the sizes of pull-down and access transistors (M1 and M5). Therefore, higher cell ratio (CR) leads to higher read margin[9].

5.1 Static Noise Margin Method

The ability to retain data in the cross coupled inverters of the SRAM is expressed as the static noise margin (SNM). It is the amount of noise voltage that would flip the data stored at the nodes Q and Q'[9]. SNM is dependent on VDD, CR and PR.The data retention voltage (DRV) is the minimum VDD required to retain the data at the storage nodes (Q and Q') in the hold/standby/idle mode when there is no read or write operation. The write-trip point is the maximum voltage on the BL, which flips the stored data. As the value of the write-trip point is decreased, it becomes more difficult to write in the cell[11]. The write trip current (WTI) is defined as the current margin of the cell, which changes the data stored at the storage node. WTI is inversely proportional to the write-trip point. Therefore, lower value of WTI allows easier write in the SRAM cell[11]. With the reduction ofthe supply voltage (VDD) the read operation becomes destructive. At low VDD the cell is highly prone to read upset. To minimize the power consumption of the SRAM cell it is recommended to scale down VDD,

which lowersthe robustness and the speed of the SRAM cell[14].SNM degrades with the increase of temperature. The write time of the SRAM cell also decreases with the increase oftemperature[12]. Another critical factor that determines the SNM in the SRAM cell is the V_{TH} of the transistors. To improve SNM the V_{TH} of the transistors should be increased. However, higher V_{TH}makes the SRAM very rigid in terms of operation and change of memory state.

Stability of the cell is a major concern while designing a new SRAM cell. Stability refers to the immunity of a cell against the noise to retain the data at the storage Q and Q'. It quantifies the maximum amount of the noise voltage SRAM cell can withstand without flipping the data at Q and Q'. SNM is extracted from the VTC of the two cross coupled inverters in the memory cell[10]. These cross coupled inverters are in positive feedback. VTC of one of the inverters in the feedback loop is superimposed to the inverse VTC of other inverter in loop. The resulting plot is known as the butterfly curve. SNM of the memory cell is then extracted by placing the largest possible square in the butterfly curve as shown in Figure 14. For SRAM reliability analysis three different SNM figures are relevant. These are Hold Static Noise Margin (HSNM), Write Static Noise Margin (WSNM) and Read Static Noise Margin (RSNM).Figure 14 shows the HSNM of the proposed 8T SRAM for 1V supply voltage.During the hold mode, the WWL and RWL are deactivated and the access transistors are turned off. The data is retained at the storage nodes Q and Q'. HSNM refers the stability of the cell during this holdstate.

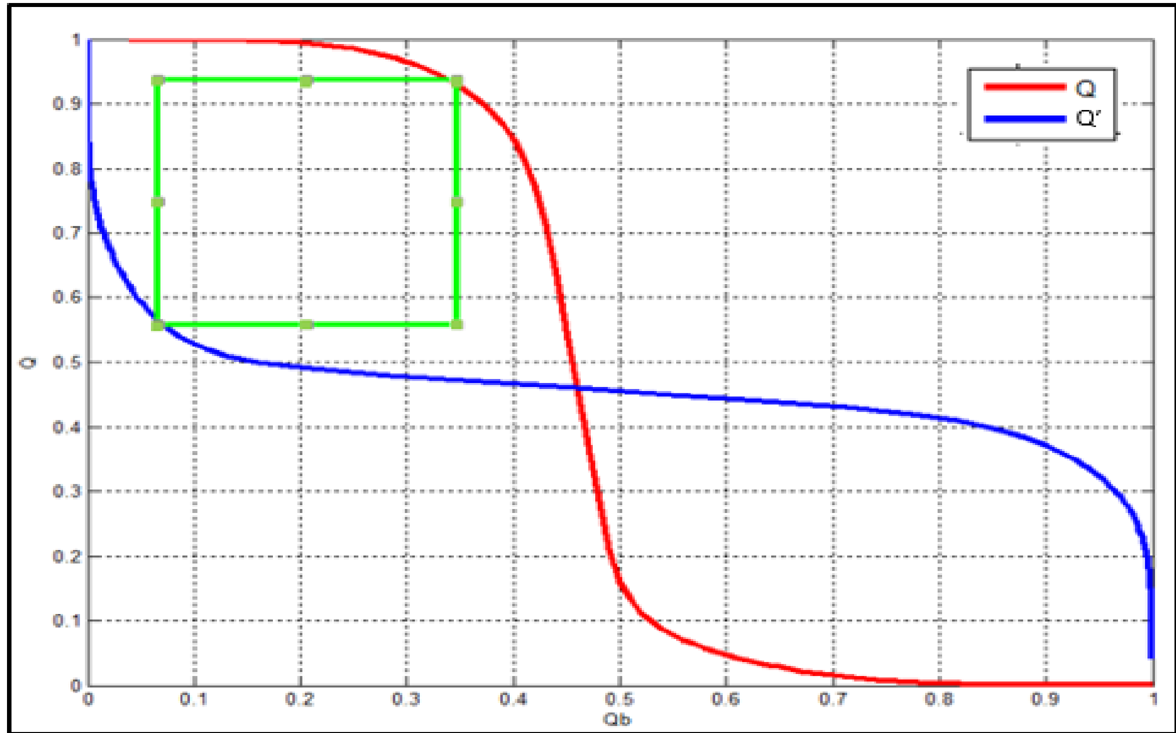


Figure 14: HSNM of the proposed 8T SRAM for 1V supply voltage.

In the 6T SRAM cell, RSNM degrades with the scaling down of VDD. By activating the RWL, RSNM can be extracted from the butterfly curve of the cross-coupled inverters similar to the HSNM. If the external DC noise is greater in magnitude than the SNM, the logic stored in the cell will change. Figure 15 shows the RSNM of the proposed 8T SRAM for 1V supply voltage. The RSNM of the proposed 8T SRAM is high because of the following reasons: (i) RBL is not precharged during the read operation and therefore there is no voltage available on RBL to destroy the data at the node Q' during the read operation; (ii) the inverter (M7-M8) isolates node Q' from the RBL and prevents any leakages from RBL from disturbing the data at Q'; and (iii) the read circuit is separated from the write circuit during the read operation. In contrast, the standard 6T SRAM is highly susceptible to noise because the bit-lines are precharged during the read operation and there is no isolation as in the proposed 8T SRAM

cell. Very careful selection of the CR and PR values is required to prevent read upset in the 6T SRAM. The required CR and PR values in this case represent the worst case scenario for the cell in terms of performance and reliability.

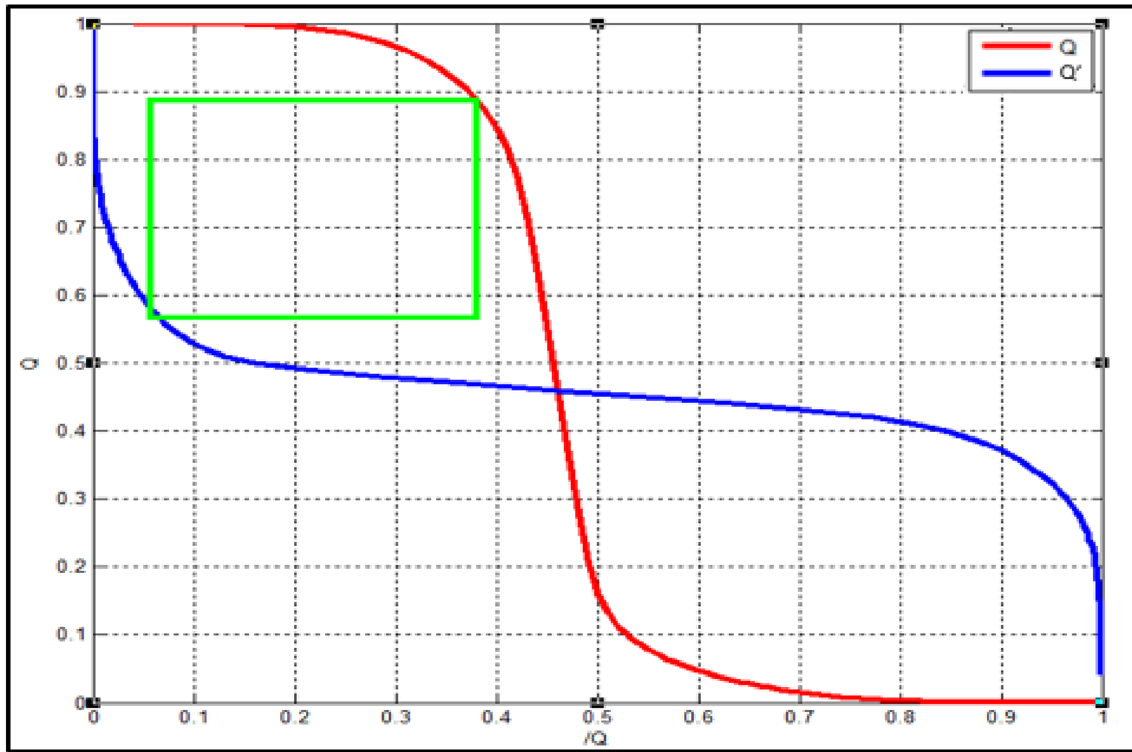


Figure 15: RSNM of the proposed 8T SRAM for 1V supply voltage.

Figure 16 shows the WSNM of the proposed 8T SRAM with 1V supply voltage.WSNM indicates the write ability of the cell. It is the minimum WBL voltage that flips the data at the storage node of the cell. In the proposed 8T SRAM design, the write circuit is separated from the read circuit, because each of these two circuits is activated independently by WWL and RWL respectively. The WWL and RWL are not activated together. Therefore, WSNM of the proposed 8T SRAM design is very high.

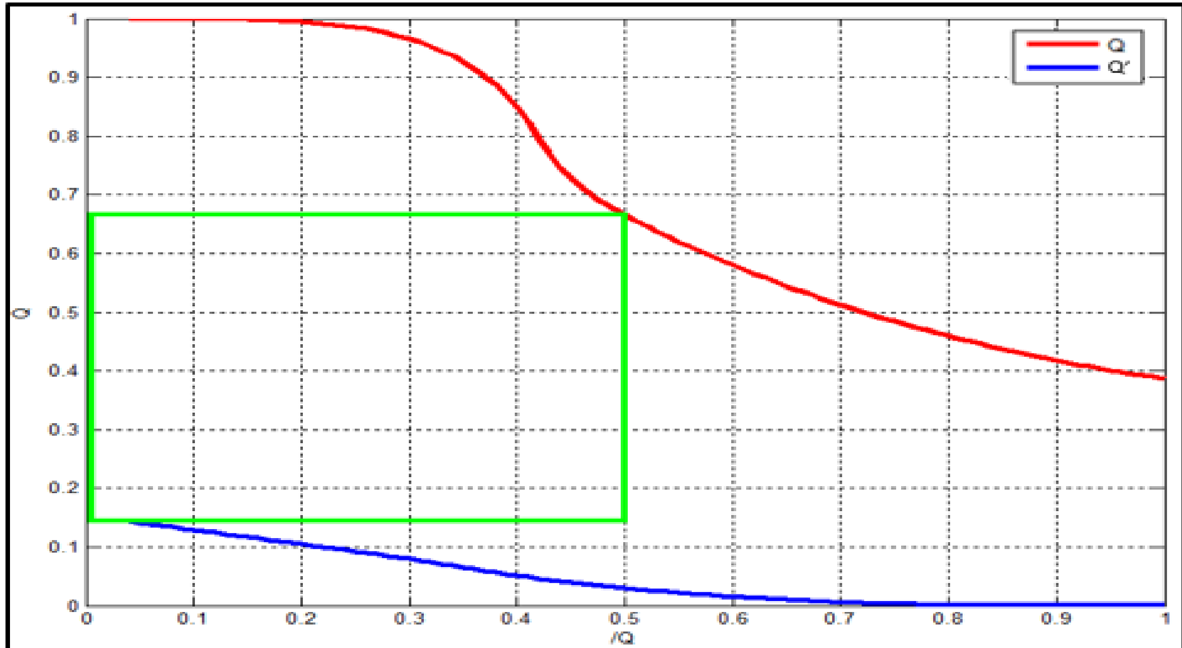


Figure 16: WSNM of the proposed 8T SRAM for 1V supply voltage.

5.2 N-curve Method

This approach is use to determine the read stability as well as to measure the write ability. N-curve illustrate the stability of SRAM cell in terms of current. Following setup is made to carry on the analysis. The proposed design is initially set to hold the "0". DC noise source (I_{in}) is connected to Q' of the proposed 8T SRAM cell. Both bit-lines WBL and RBL are clamped to VDD. Then a DC sweep is performed on Q' to get the current waveform through I_{in}. This current curve crosses zero at A, B and C as shown in Figure 17. The part between C and B represents write ability. The voltage difference between C and B is defined as write trip voltage (WTV). It is thevoltage required to change the data of cell. The negative peak current between C and B is the write trip current (WTI). It is the current margin of the cell which changes the data stored at the storage node. Similarly, the part between A and B represents read stability. Static voltage noise margin (SVNM) is the voltage difference between A and B.

It is the maximum tolerable DC noise voltage before flipping the content of the cell. The current peak between A and B is the Static current noise margin (SINM). It is the maximum current which can be injected in SRAM cell without flipping the data of cell. Table 6 provides the N-curve parametric details of the proposed 8T SRAM cell [15].

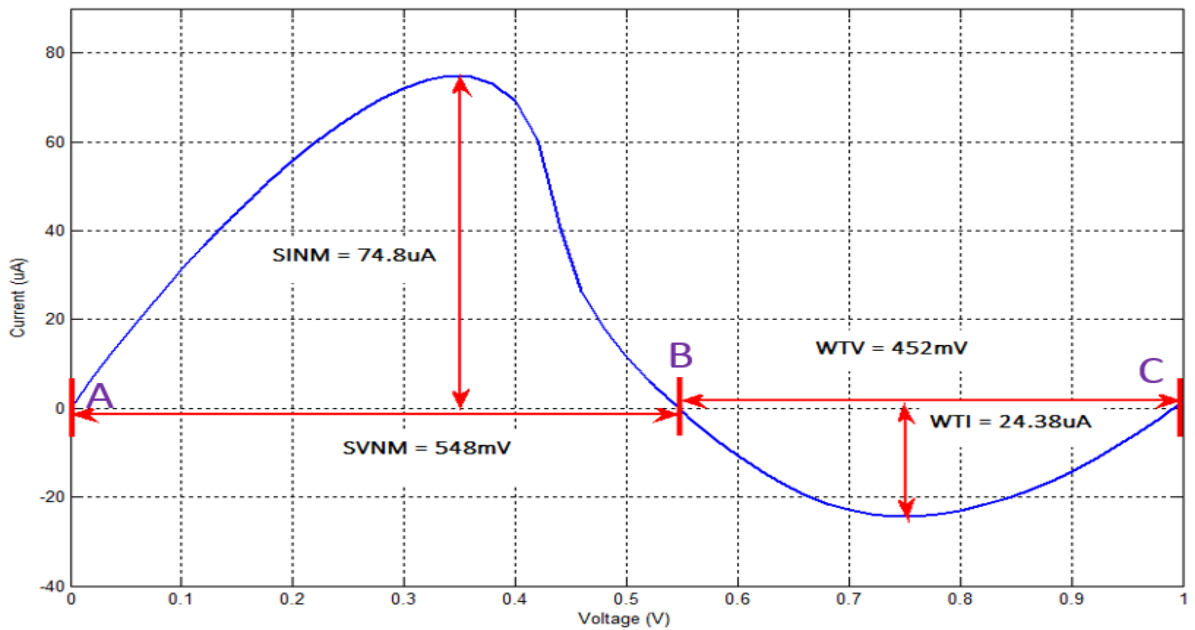


Figure 17: N curve of proposed 8T SRAM.

Table 6: N-curve parameters of the proposed 8T SRAM cell.

N curve metrics	Proposed 8T SRAM
SVNM (mV)	548
SINM (µA)	74.8
WTV (mV)	452
WTI (µA)	24.38

5.3 Bit-line Voltage

Another static method used to evaluate the write margin of SRAM cell is BL voltage, as shown in Figure 18[16]. In this method the proposed 8T SRAM cell is configured for write "1" operation. WBL is connected to the storage node holding "1". During the analysis WBL is swept from VDD to 0 during DC simulation. In this method the write margin of SRAM cell is the value of WBL voltage at which the data flip at storage nodes. High WBL voltage is preferred to ease the write operation. Hence, implying larger write margin. Table 7 provides write ability comparison between the standard 6T and the proposed 8T SRAM.

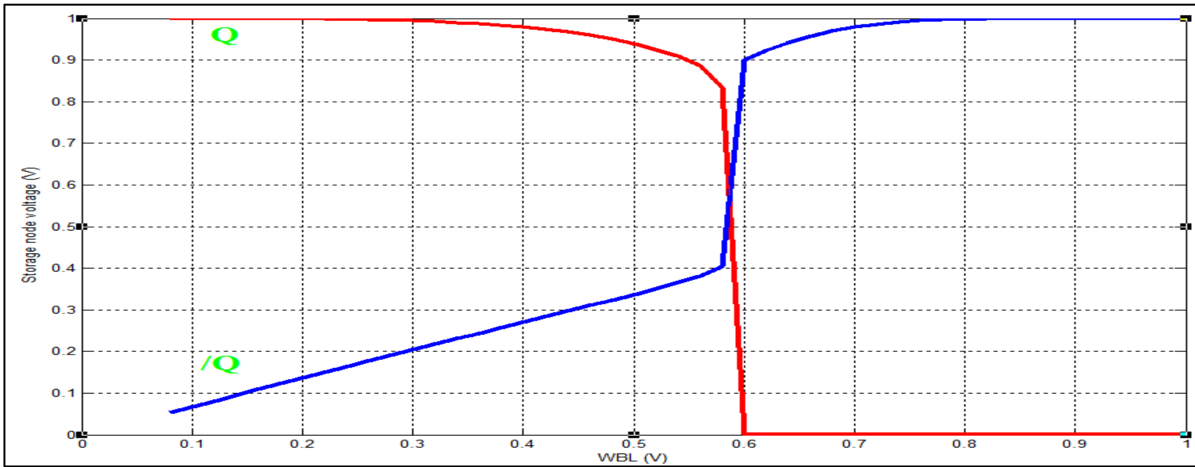


Figure 18: Write ability of the proposed 8T SRAM using voltage at WBL method for 1V supply voltage.

Table 7: Write ability analysis results for the conventional 6T and the proposed 8T SRAM.

Write ability parameter	6T SRAM [16] (V)	Proposed 8T SRAM (V)	Percentage write ability improvement in proposed 8T SRAM. (%)
WSNM	0.390	0.5	28.21
Voltage at the BL	0.287	0.587	150

CHAPTER 6

ANALYSIS OF PROCESS AND PARAMETRIC VARIATION IN THE PROPOSED 8T SRAM

With the shrinking of technologies supply, process and parametric variations impose significantly more prominent impact on the performance and reliability of the SRAM circuits. Increasing process variations lead to higher failure probability and lower yield in SRAM design. Supply variation due to internal and external causes is a very critical factor. Figure 19 shows the variation of the WSNM with the supply voltage in the proposed 8T SRAM and compares it with that of the conventional 6T SRAM. The random dopant fluctuation is one of the primary reasons of memory failure. The inter-die and intra-die variations lead to threshold voltage (V_{th}) mismatch among nearby transistors. Memory dies with low V_{th} have greater probability of read and hold time failures. On the other hand, dies with high V_{th}will have higher probability of failure during the write operation[10]-[13]. Therefore, for memory design it is very important to know these process corners to secure optimum performance and reliability.Figure 20 shows RSNM analysis of the proposed 8T SRAM and Figure 21 shows RSNM analysis of the conventional 6T SRAM at various process corners.Table 8 provides the numerical comparison of RSNM in the proposed 8T and the conventional 6T SRAMs. It can be observed that in the proposed 8T SRAM, the RSNM values are higher at every process corners.

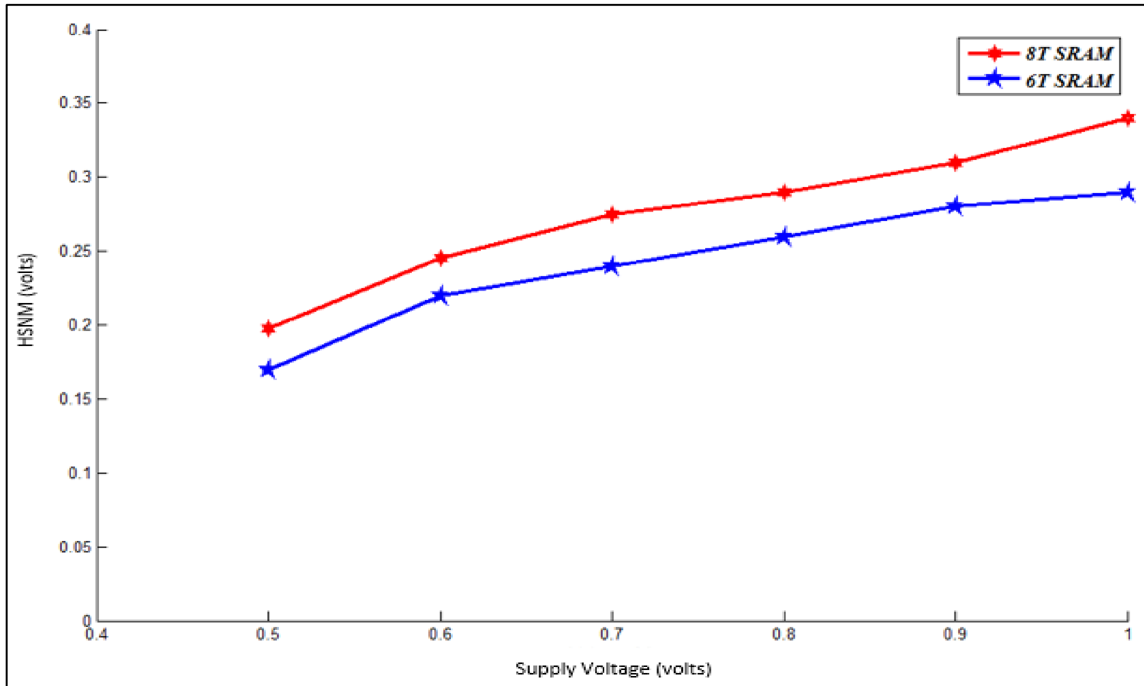


Figure 19: Variation of WSNM with supply voltage for 8T and 6T SRAM.

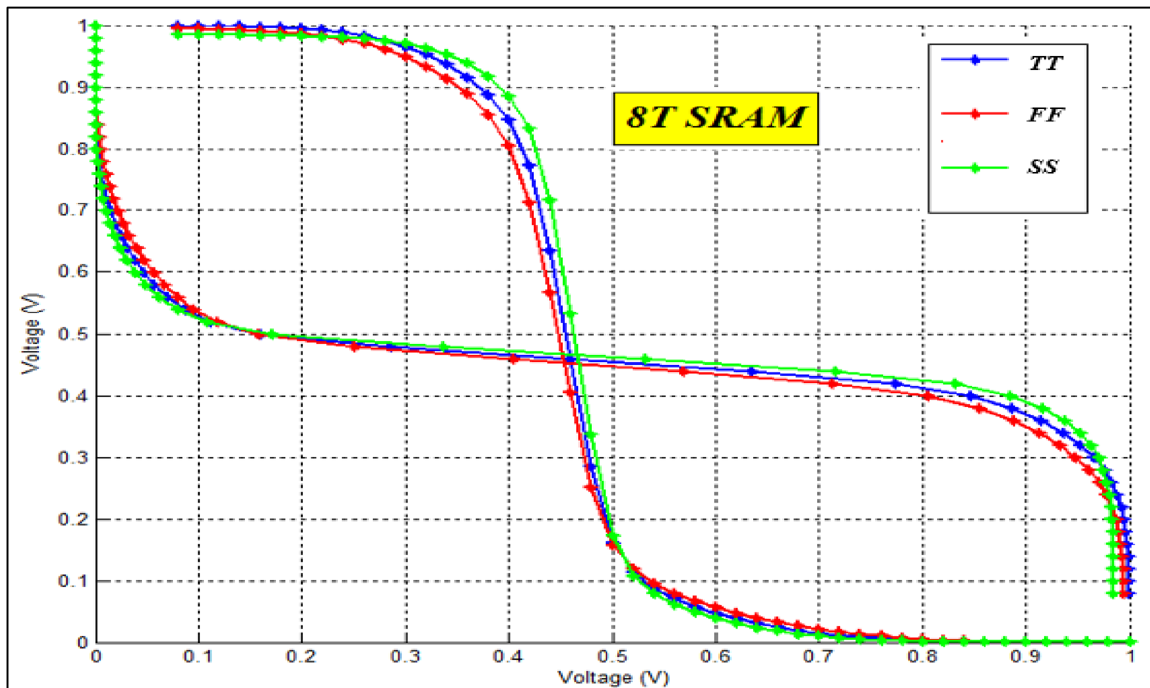


Figure 20: Stability analysis of 8T SRAM at different process corners.

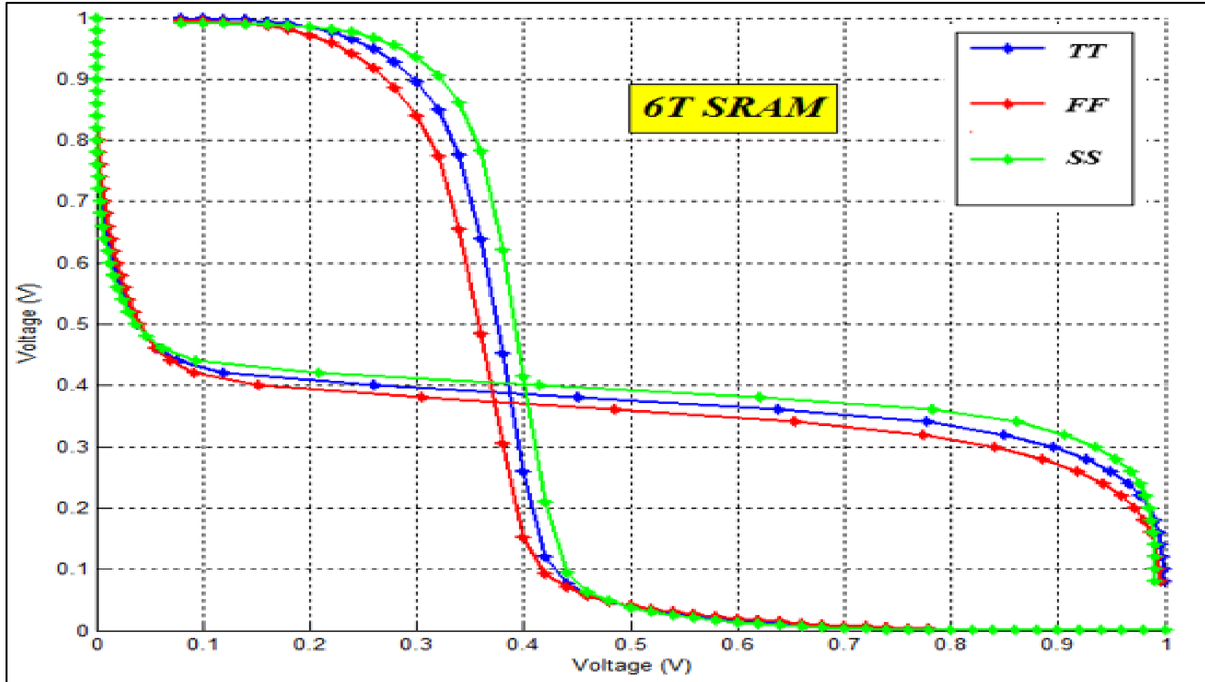


Figure 21: Stability analysis of 6T SRAM at different process corners.

Table 8: RSNM of 6T and 8T SRAM at different process corners.

Design	Corners	TT	FF	SS
6T SRAM	RSNM	0.291	0.280	0.301
8T SRAM	RSNM	0.349	0.344	0.356

Another critical parameter is the temperature, which affects the SNM of SRAM circuits. Figure 22 shows the variation of the SNM values with temperature in the proposed 8T and the conventional 6T SRAMs. It is observed that the stability of the SRAM degrades with the increase of temperature for both 8T and 6T designs. However, the stability of our proposed 8T SRAM is higher than the conventional 6T SRAM at any temperature.

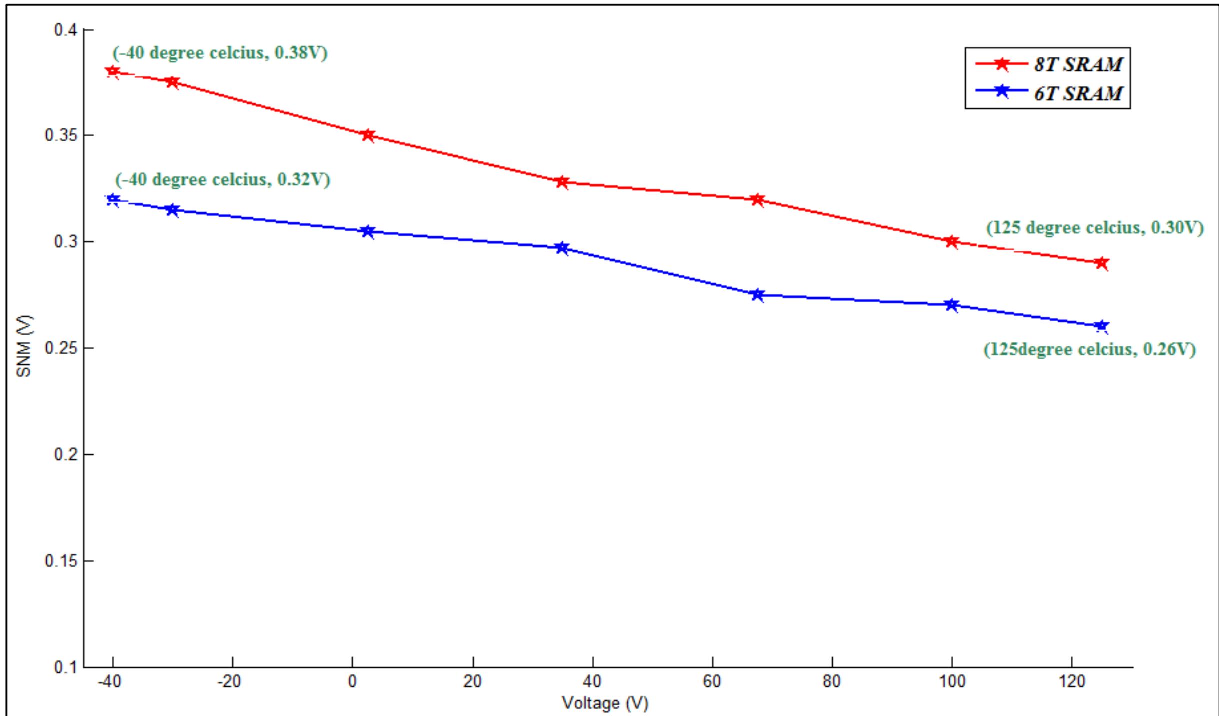


Figure 22: Variation of Stability of 6T and 8T SRAM with temperature.

CHAPTER 7

MONTE CARLO ANALYSIS

Monte Carlo analysis using statistical models (process and mismatch variation) are carried to attain satisfactory SNM with variation in Vth. Figures show the result of Monte Carlo loops where the Vtn and Vtp of all devices are varied. A 3σ tolerance is sufficient for mismatch in SRAM cell. Analysis was carried on 1000 samples points.

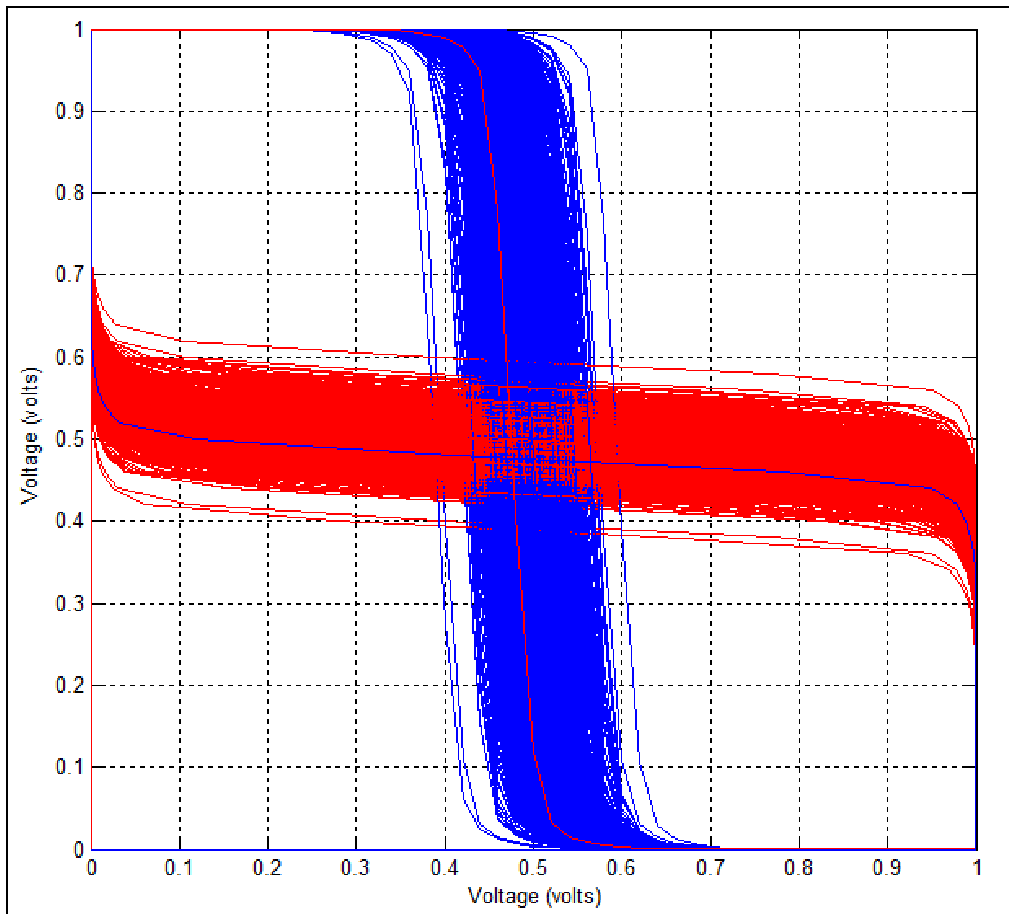


Figure 23: Variation Monte carlo analysis result for Vth variation in Pull down transistors in hold mode.

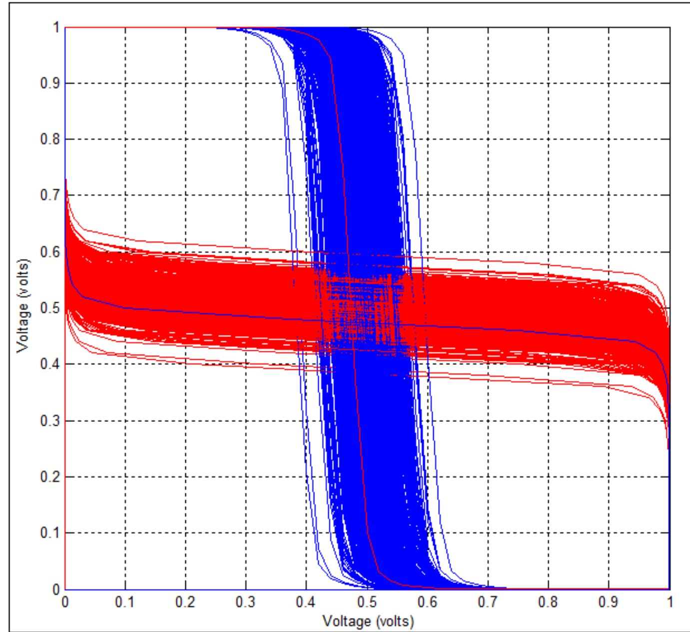


Figure 24: Variation Monte carlo analysis result for Vth variation in Pull up transistors hold mode.

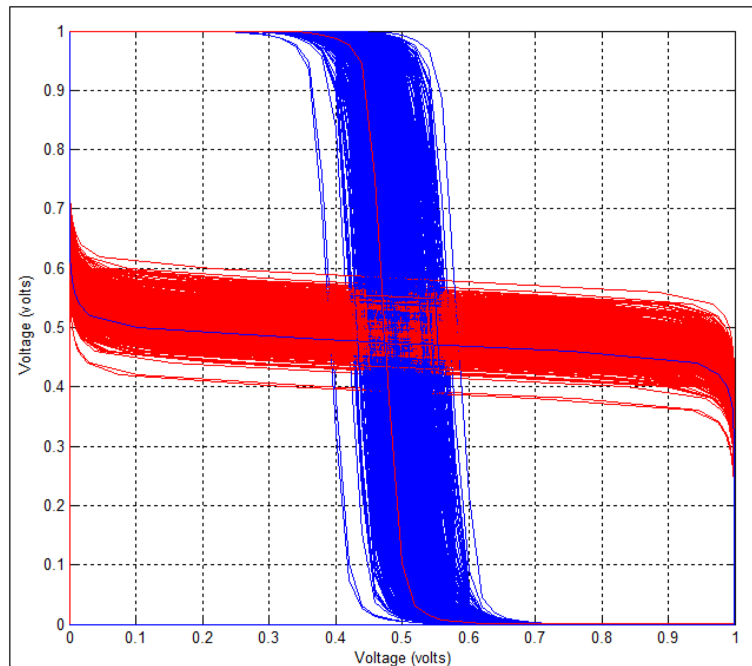


Figure 25: Variation Monte carlo analysis result for Vth variation in access transistors read mode.

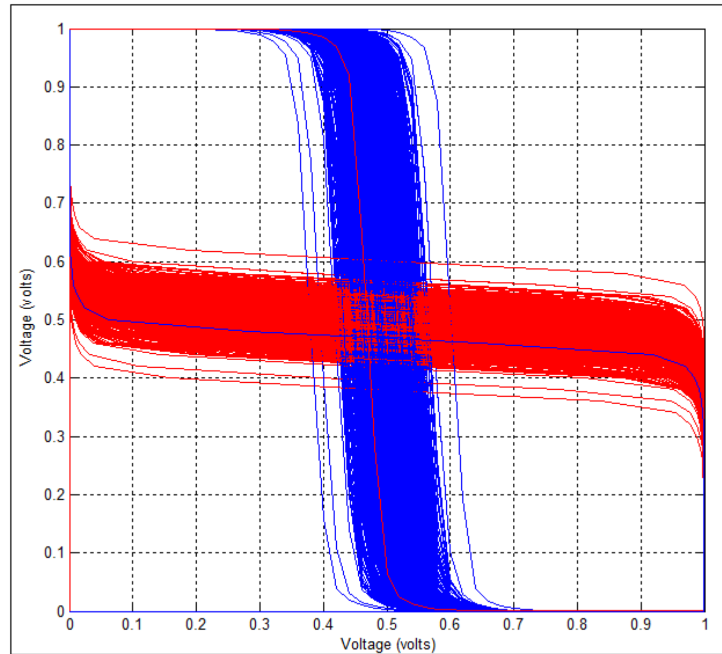


Figure 26: Variation Monte carlo analysis result for Vth variation in Pull down transistors read mode.

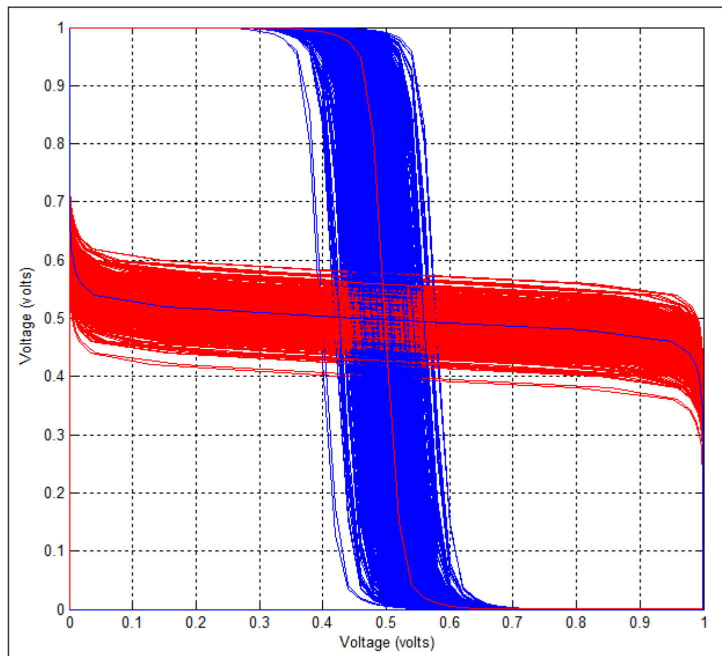


Figure 27: Variation Monte carlo analysis result for Vth variation in Pull up transistors read mode.

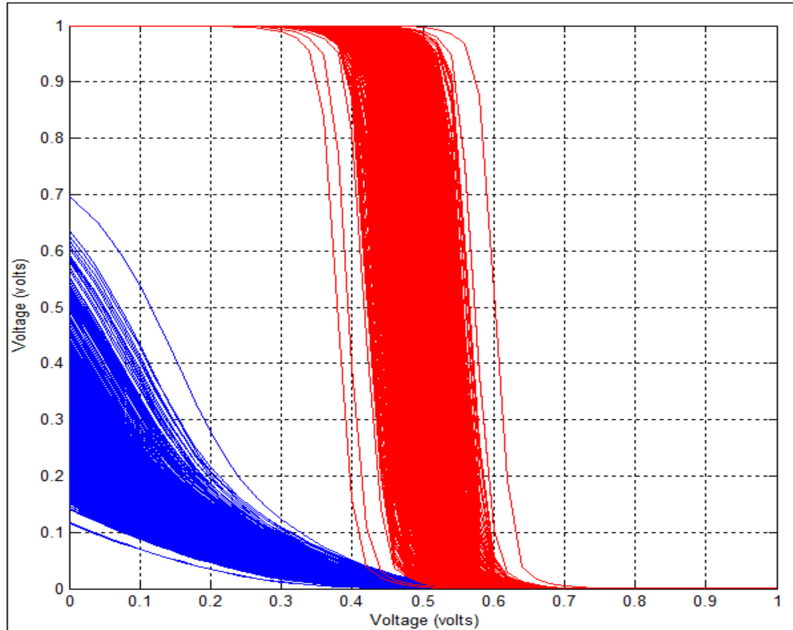


Figure 28: Variation Monte carlo analysis result for Vth variation in Pull down transistors write mode.

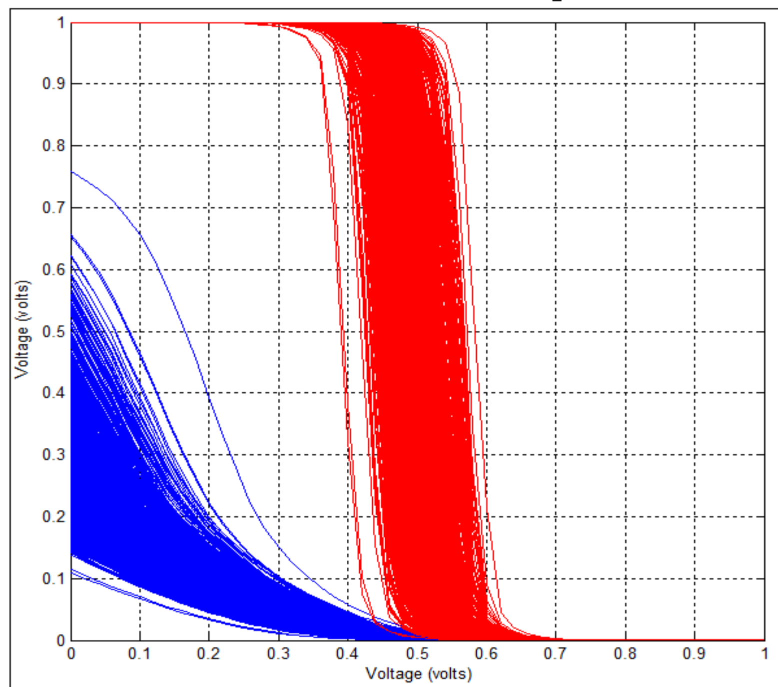


Figure 29: Variation Monte carlo analysis result for Vth variation in access transistors write mode.

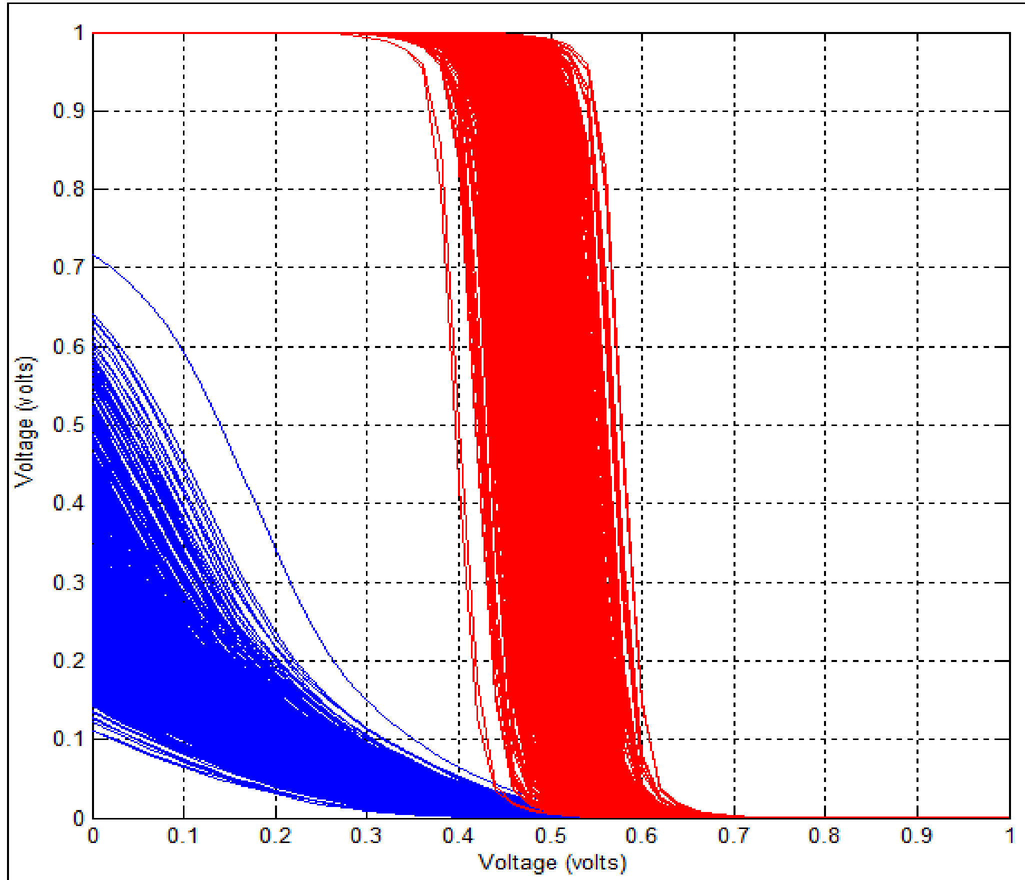


Figure 30: Variation Monte carlo analysis result for Vth variation in Pull up transistors write mode.

Table 9: Monte Carlo analysis for 8T SRAM for hold, read and write mode.

Static Noise Margin Vth Variation	RSNM (V)	HSNM (V)	WSNM (V)
Access Transistors	0.43	-	0.28
Pull Down Transistors	0.39	0.40	0.34
Pull Up Transistors	0.41	0.43	0.35

CHAPTER8

CONCLUSION

The analysis of 8T SRAM is done in 45nm technology. Comparison was done with various existing SRAM design with the proposed 8T SRAM design in terms of structural design, read and write operations along with total power consumption of each design during read "0 and 1" and write "0 and 1" operations respectively. Moreover, comparison was done between the conventional 6T SRAM design and the proposed 8T SRAM design in terms of static and dynamic analysis to determine the write ability of the SRAM cells. The proposed design have 28.21% write ability improvement in WSNM, 43.75% write ability improvement in voltage at WL method and 150% write ability improvement in voltage at BL method. The area of the proposed 8T SRAM is 9.72% more than the conventional 6T SRAM.

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