NANOSCALE NONVOLATILE MEMORY CIRCUIT DESIGN USING EMERGING SPIN TRANSFER TORQUE MAGNETIC RANDOM ACCESS MEMORY

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NANOSCALE NONVOLATILE MEMORY CIRCUIT DESIGN USING EMERGING STT-MRAM

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ABSTRACT

The spin transfer torque magnetic random access memory (STT-MRAM) is suitable for embedded and second level cache memories in the mobile CPUs. STT-MRAM is a highly potential nonvolatile memory (NVM) technology. There has been a growing demand to improve the efficiency and reliability of the NVM circuits and architectures. we present a modified STT-MRAM cell design, where each cell is comprised of one magnetic tunneling junction (MTJ) device and a regular access transistor. We provide analysis of device, circuit and memory architecture level issues of STT-MRAM. The Modified 1M1T STT-MRAM bit cell circuit offers simpler and more area- and power- efficient design compared to the existing STT-MRAM cell design. Some device-circuit co-design issues are investigated to demonstrate ways to reduce delay in MRAM circuits based on MTJ. An 8x8 conventional MRAM array is implemented using the existing 2M2T cell and the Modified 1M1T cell to perform a comparative analysis at the architecture level. The non-volatile nature of the proposed STT-MRAM is verified through SPICE simulation. The circuit implementations and simulations are performed for 45nm technology node.

As the transistor scales down it is prone to subthreshold leakage, gate-dielectric leakage, Short channel effect and drain induced barrier lowering. Now alternative of Access transistor is needed. We are using FinFET as access transistor in the STT-MRAM bit cell. FinFET based bit cell is designed to get an advantage of scaling down. Analysis is done and proven that the power consumption, standalone leakage current is less when compared to NMOS based STT-MRAM

bit cell. Also determined FinFET based bit cell produces less access time to access the logic value from MTJ.

Now, Industry is looking to have computational and storage capability together and that can be achieved through STT-MRAM. Addition to that there is a possibility to reduce power consumption and leakage more. So replacing FinFET technology with Carbon Nano Tube Field Effect Transistor (CNTFET) is required. As the conventional STT-MRAM requires certain current to reverse the magnetization of MTJ and one CNTFET alone cannot produce sufficient current required to store the logic value into MTJ. So new Bit cell is proposed using 3 CNTFET and 1 MTJ, this bit cell is capable of storing 3 logic values at a time that is capable of doing computation and act as AND gate. Also it utilizes less power to be in active region.

Sensing of any memory system is one of the main challenge in industry to get better performance with less resources. Conventional Sense Amplifier (SA) used to sense the value from SRAM, DRAM memory system is also used to sense the STT-MRAM memory. But use of conventional SA is prone to some error. Modified Sense Amplifier is designed to overcome the error produced from the conventional SA. It is compared with all the existing SA to get the performance details of the modified SA.

Index Terms— Spin Transfer Torque Magnetic Random Access Memory (STT-MRAM), Magnetic Tunneling Junction (MTJ) Device, Tunnel Magneto Resistance (TMR), and Nonvolatile Memory (NVM).

APPROVAL PAGE

The faculty listed below, appointed by the Dean of the School of Computing and Engineering have examined a thesis titled "Nanoscale Nonvolatile Memory Circuit Design using Emerging STT-MRAM" presented by Lohith Kumar Vemula, candidate for the Master of Science degree, and certify that in their opinion it is worthy of acceptance.

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CONTENTS

Contents……………………………………………………………………………..Page

ABSTRACT iii

LIST OF ILLUSTRATIONS x

LIST OF TABLES xiv

ACKNOWLEDGEMENTS xv

1.INTRODUCTION 1

1.1. TRENDS IN MEMORY TECHNOLOGIES 1

1.2. PARAMETERS OF MEMORY SYSTEM 2

1.3. INDUSTRY UPDATE 4

1.4. WHY TO CHOOSE STT-MRAM 5

2.PLANAR NMOS BASED STT-MRAM BIT CELL ANALYSIS AND CIRCUIT DESIGNING 8

2.1. INTRODUCTION 8

2.1.1. MTJ and its Operation 8

2.1.2. Single bit STT-MRAM 10

2.2. PROPOSED SIMPLIFIED STT-MRAM CELL DESIGN 12

2.2.1. Writing Operation of the Proposed STT-MRAM Cell 14

2.2.2. Reading Operation of the Proposed STT-MRAM Cell 15

2.2.3. Nonvolatile Feature of the Proposed STT-MRAM Cell 16

2.2.4. Temperature Dependence of the STT-MRAM Cell 17

2.2.5. Comparison of the Proposed and Existing STT-MRAM Cells 18

2.3. STT-MRAM DELAY REDUCTION BY DEVICE (MTJ) AND CIRCUIT CO-DESIGN 20

2.3.1. Optimization of MTJ Device Level Magnetization Property to Reduce Delay 20

2.3.2. Circuit Level Implementation of STT-MRAM to Reduce Delay 20

2.4. IMPLEMENTATION OF AN 8X8 RAM ARCHITECTURE USING THE EXISTING AND PROPOSED STT-MRAM 23

2.4.1. Conventional Architecture 25

2.4.2. Proposed Architecture 25

2.4.3. Analysis of the Impact of Threshold Voltage Variation of the Access Transistor on the Proposed STT-MRAM Cell... 27

2.5. CONCLUSION AND FUTURE WORK 30

3.PERFORMANCE IMPROVEMENT USING FINFET BASED STT-MRAM CIRCUIT DESIGN 34

3.1. INTRODUCTION 34

3.1.1. Disadvantages to use MOS based Access Transistor... 34

3.1.2. Advantages of FinFET technology over MOS Transistor.................................... 35

3.1.3. Comparison of FinFET based cell with existing models 35

3.2. FINFET BASED BIT CELL.. 35

3.2.1. Writing Operation of bit Cell 35

3.2.2. Reading Operation of STT-MRAM bit cell 37

3.3. PERFORMANCE PARAMETERS OF FINFET BASED STT-MRAM BIT CELL SIMULATIONS.. 39

3.3.1. Delay Variation of FinFET based STT-MRAM bit cell. With respect to number of Fins of FinFET.. 39

3.3.2. Power consumption with respect toNumber of Fins of FinFET based STT-MRAM bit cell 40

3.3.3. Leakage Power variation in FinFET based STT-MRAM bit cell with respect to number of Fins of FinFET 41
3.3.4. Delay variation with respect to process Technology of FinFET 42
3.3.5. Delay of bit cell variation with respect to Temperature Dependence at different voltage levels of high performance model of FinFET. 43
3.3.6. Delay of bit cell variation with respect to Temperature Dependence at different voltage levels of Low performance model of FinFET... 44
3.3.7. Delay of bit cell in different Process Voltage Temperature conditions 45
3.3.8. Power Utilized by STT-MRAM in different PVT conditions.............................. 46
3.3.9. Leakage Power Variation of FinFET based STT-MRAM bit cell with respect to temperature and voltage change 47
3.3.10. Delay variation in PVT conditions with the variation of number of fins of FinFET of a STT-MRAM bit cell. 48
3.4. CONCLUSION AND FUTURE WORK 49
4.LOGIC-IN-MEMORY USING CNT-FET BASED STT-MRAM BIT CELL AND OPTIMIZATION 50
4.1. PROPOSED BIT CELL 50
4.2. WRITING OPERATION OF CNTFET BASED STT-MRAM BIT CELL. 51
4.3. READING OPERATION OF CNTFET BASED STT-MRAM BIT CELL. 51
4.4. SIMULATION OF BIT CELL. 52
4.5. DELAY PERFORMANCE PARAMETER SIMULATION 53
4.6. ADVANTAGES AND DISADVANTAGES OF CNTFET BASED STT- MRAM BIT CELL... 53
4.7. CONCLUSION AND FUTURE WORK 54

5.ERROR FREE SENSE AMPLIFIER DESIGN FOR STT-MRAM NONVOLATILE MEMORY 55
5.1. INTRODUCTION 55
5.1.1. MTJ operation 55
5.1.2. Single bit STT-MRAM 56
5.1.3. Sense amplifier 57
5.2. EXISTING DESIGNS 58
5.2.1. Precharge Sense Amplifier Without Activation Signal 58
5.2.2. Pre-Charge Sense Amplifier by Using Activation Signal 62
5.3. PROPOSED SENSE AMPLIFIER 63
5.4. CONCLUSION AND FUTURE WORK 66
REFERENCES 67
VITA 72

LIST OF ILLUSTRATIONS

Figure Page

1. Performance parameters comparison[18]... 3
2. Toshiba architecture on memory hierarchy... 4
3. Attributes of STT-MRAM.. 6
4. STT-MRAM memory placement with respect to other Non-Volatile memories[19]........... 7
5. Direction of electrons in the pinned and free layers, which represents the mode of operation and bit stored in MTJ: (a) parallel mode of MTJ (bit “0”) and (b) anti parallel mode of MTJ (bit “1”).. 9
6. Single bit STT-MRAM including a MTJ and an access transistor (sense amplifier is not shown) [3].. 11
7. One-bit cell STT-MRAM circuit with one MTJ, one access transistor (45nm), one BL, one WL, one source-line and the state signal (the state signal is to observe the switching mechanisms of MTJ whether it is a parallel or an anti-parallel). MTJ offers spin transfer torque technique with in-plane anisotropy. 11
8. Schematic circuit of (a) one of the existing MRAM bit cell [2] and (b) the proposed STT-MRAM bit cell. 13
9. CIRCUIT simulation of STT-MRAM bit cell when a deactivating signal (WL=0) is applied at the access transistor. 14
10. CIRCUIT simulation of STT-MRAM bit cell when an activating signal (WL=1) is applied at the access transistor. 15
11. The non-volatile characteristics of STT-MRAM circuit. SPICE simulation of STT-MRAM bit cell when a deactivating signal is applied at WL. The outputs represent BL, WL and state signals of STT-MRAM bit cell. 17

12. Temperature dependence of MTJ for the input of Figure 6. 18
13. Simulation of STT-MRAM magnetization property along x, y and z axis when (a) I_E/I_S=8, (b) I_E/I_S=4, (c) I_E/I_S=1.3.. 22
14. The output state of the STT-MRAM device and circuit co-design approach. High W/L ratio of the access transistor reduces the delay in the demagnetizing of the MTJ....................... 24
15. Conventional STT-MRAM system architecture/array block diagram, where each cell is represented by 2 MTJs and 2 access transistors [2]. 25
16. Proposed architecture showing bit cell.. 26
17. Monte Carlo Simulation of V_{th} with 0 fail points and 50 pass points for 1000 bins........... 28
18. Monte Carlo simulation that is STT-MRAM is holding for 1000 points............................ 29
19. Conventional STT-MRAM system 8x8 architecture/array, where each cell is represented by two MTJs and two access transistors [2]... 31
20. Proposed STT-MRAM system 8x8 architecture/array, where each cell has one MTJ and one pass transistor (45nm). 32
21. Plots of Values stored in eight MTJs of the proposed Architecture.................................. 33
22. FinFET based STT-MRAM Bit Cell.. 37
23. CIRCUIT simulation of STT-MRAM bit cell when an activating signal (WL=0.7V) is applied at the access transistor. 38
24. Delay Variation of FinFET based STT-MRAM bit cell with respect to number of Fins of FinFET.. 40
25. Power consumption variation of FinFET based STT-MRAM bit cell with respect to number of Fins of FinFET 41
26. Leakage Power Variation of FinFET based STT-MRAM bit cell with respect to number of Fins of FinFET 42

27. Delay with respect to FinFET Technology Node 43
28. Temperature Dependence with respective to Delay at different Voltage levels with high performance model of FinFET 44
29. Temperature Dependence with respective to Delay at different Voltage levels with low performance model 45
30. Delay of STT-MRAM with FinFET Access Transistor in PVT conditions 46
31. Power Utilized by STT-MRAM in different PVT conditions 47
32. Leakage Power Variation of FinFET based STT-MRAM bit cell with respect to temperature and voltage change 48
33. Delay Variation with respect to Voltage and Temperature Variation for High and Low performance devices for different number of Fins 49
34. CNTFET access Transistor based STT-MRAM bit cell. 51
35. Simulation of CNTFET based STT-MRAM bit cell. 52
36. Delay variation of STT-MRAM bit cell. 53
37. Spin orientation of electrons both in the pinned and free layers, which represents the mode of operation and bit stored in MTJ (a) parallel mode of MTJ (bit "1") (b) anti parallel mode of MTJ (bit "0"). 57
38. STT-MRAM bit cell including a MTJ and an access transistor. (a) 3D model MRAM (sense amplifier is not shown) [1], (b) circuit representation of MRAM with the sense amplifier. 59
39. A precharge sense amplifier of STT-MRAM in 45 nm technology without the activating signal. This sense amplifier circuit allows low sense margin and the parallel read-write capability [24]. 60
40. Output waveforms of pre-charge sense amplifier circuit of Figure 39. 61

41. Pre-charge sense amplifier circuit by using the activating signal [9]................................. 64

42. Output waveform of the pre-charge sense amplifier by using the activation signal. 64

43. Proposed sense amplifier circuit.. 65

44. Output waveforms of the proposed pre-charge sense amplifier... 65

LIST OF TABLES

Table Page

1. Industry prototype specifications available in the market. 5
2. Comparison between the existing and proposed MRAM nonvolatile memory bit cell. 19
3. State of art of STT MRAM circuit and architecture. 19
4. Power and performance comparison of memory arrays implemented with the proposed and conventional MRAM cells 27
5. Distribution of points in Monte Carlo simulation 29
6. Comparison of Existing FinFET Technologies with our Design 36
7. Comparison of the existing sense amplifiers of STT-MRAMs.. 58
8. Comparison of the proposed sense amplifier of STT-MRAM with the existing sense amplifiers. 66

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CHAPTER 1

INTRODUCTION

1.1.TRENDS IN MEMORY TECHNOLOGIES

Memories broadly divided into two types. Volatile Memory and on the other hand Non Volatile Memory. Volatile-Memory (VM) is the storage which erases the data when system is powered off or interrupted. Non-Volatile Memory (NVM) is the storage which remains the data even when system is powered off or interrupted. Examples of Volatile memory are SRAM and DRAM. These are the basic volatile memories that are in market. DRAM is again sub divided into embedded and standalone devices. These volatile memories are used to design the maximum part of the memory hierarchy. Examples are computing units, register files, L1 cache and L2 cache.

Non Volatile Memories are sub divided into three types according to the ITRS 2015 report. Base line NVM is the storage that readily available in the market to store the logic values into it. Examples of baseline NVM's are Flash Memories (NAND and NOR). Applications of baseline NVM are Main memory and storage memory. Prototypical models are the storage that we have just a prototype but not available in the market. They going to be in the market in very few years from now. Examples are Fe RAM, PCM, MRAM and STT-MRAM. Now market is used to replace all the volatile memories with NVM to gain certain advantages over them. Third type NVM are Emerging Research Devices (ERD). These are at a stage of research and they don't have any prototypical model up to now. Examples are Ferro Electric Memory (FeFET, FTJ), ReRAM (Electrochemical Metallization bridge, Metal oxide – bipolar Filamentary, Metal

oxide- unipolar filamentary, metal oxide – bipolar non filamentary), Mott memory, Carbon Memory, Macromolecular memory.

1.2.PARAMETERS OF MEMORY SYSTEM

There are six parameters for designing optimal memory design. We compare all the memory systems with these parameters. Parameters are as follows.

1. Leakage
2. Density
3. Retention time
4. Endurance
5. Performance
6. Dynamic Energy

1. Leakage: For any optimal design Leakage should be low. Since memories are the one which have to be in standalone for long time. This leakage causes more power utilization of the memory system. Any memory system design should be capable of low leakage.
2. Density: Optimal design is capable of high storage at lesser area. Bit cell size should be much smaller when compared to existing memories. Designing should be capable of storing huge data in lesser area.
3. Retention time: Retention time is the time taken by the memory unit to with stand the data when system is powered off. Ideally Retention time should be high and memory should be capable of holding data in huge time.
4. Endurance: Endurance is parameter that describes how many times we can write and read the data from memory unit. Ideally Memory system should be capable of unlimited endurance.

5. Performance: Ideal memory system should have a high speed i.e., high access time which results in usage of memory in computational designs.
6. Dynamic Energy: However, the standalone power is important, at the same time dynamic power utilization also place an important role. It is nothing but switching power. Ideally Memory system should be capable of low dynamic energy.

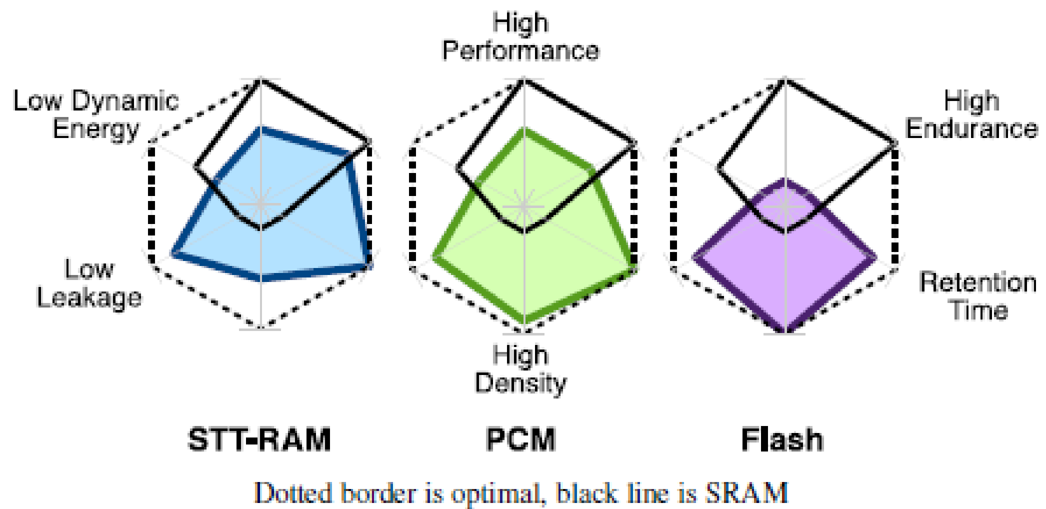


Figure 1: Performance parameters comparison[18].

In Figure 1 performance parameters are discussed. Here dotted line represents the optimal design. Black solid line represents the SRAM behavior. Blue, green and pink represents the STT-MRAM, PCM and Flash Performance respectively. From the figure we can conclude that the Flash memory is better in density but not good at performance when compared with all other Non-Volatile memories that we are comparing. Also not good at Endurance and dynamic energy utilization. PCM is better than Flash memory but not good than the SRAM memory and other NVM's. PCM is better in Retention time than SRAM but not than of Flash Memory. Leakage is far better than SRAM. STT-MRAM is better in all other aspects but still need to have a better device for performance when compared to SRAM. If we can reach the performance of SRAM

then we can replace the memory with NVM which gives the additional advantages over the existing memories.

1.3.INDUSTRY UPDATE

New architecture proposed by Toshiba in December 2013 which includes tables in storage that contains certain input combinations. Improves power consumption and speed. Cycles needed to solve equation decreased from 408 to 44. IBM implementing the Nanostructure of MRAM cell using domain wall mechanism. China Academia researchers implementing to increase the number of bits per cell.

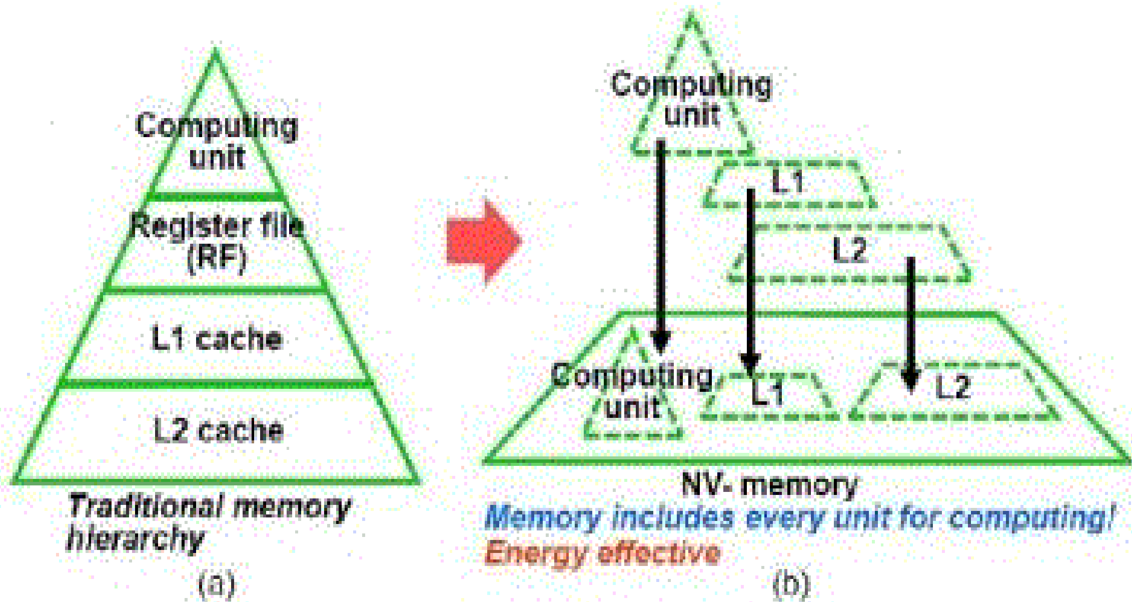


Figure 2: Toshiba architecture on memory hierarchy

Figure 2 represents the Toshiba new architecture that discussed before and which have huge advantage over the traditional hierarchy.

Table 1: Industry prototype specifications available in the market.

Industry	Memory size	Vol	Wright/read cycle	Power dissipation
Everspin	1MB	1.8 V	50ns	0.6W
Aeroflex	16MB	0-4V	45ns	4W
Freescale	16MB	2.2V	35ns	0.6W

Table 1 gives the information of the industries who have prototype now in the market and also the specifications of Memory System they are using now. The other companies working on STT-MRAM Grandis, Qualcomm, Russian Nano-Technology Corp., Avalanche Technology, Crocus Technology, Spin Transfer Technologies.

1.4.WHY TO CHOOSE STT-MRAM

Main problem with the existing memory technologies is due to the limitations of scaling down. SRAM cannot be scale down due to its electrical and physical limits. DRAM cannot scale down because of its capacitor usage. Scaling down can lose its property. Flash cannot be scale down because of its charge retention property. So, we need an alternative that can replace these memories but should have all the attributes of existing memory technologies. As we know that the existing memory technologies all depends on the electron movement. As per the limitations we are exploring a possibility with the rotation of electron to store the logic value. So, STT-MRAM have a property of all attributes from existing memory technologies and also store depends on the magnetic field i.e., electron orientation. It takes the advantage of speed property from SRAM Memory. As the speed of STT-MRAM memory is very comparable with the SRAM memory and can be discussed in the later section. It takes an advantage of density and Power consumption parameter from DRAM memory. Non-Volatile property and also density property is taken from Flash Memory. Additional STT-MRAM have the practically highly endurance and

high retention time. It is capable of replacing L2 cache of memory hierarchy. Now it is capable of replacing secondary memory. There is a need in concentrate on the performance parameters of the Memory system that can give the better advantage over the existing memory technologies like delay, leakage power and power utilization. This whole project is mainly depend on the respective parameters simulation for bit cell and find the optimized value of the design for the memory system. Figure 3 represents the attributes distribution from the existing memory technologies to the STT- MRAM memory system.

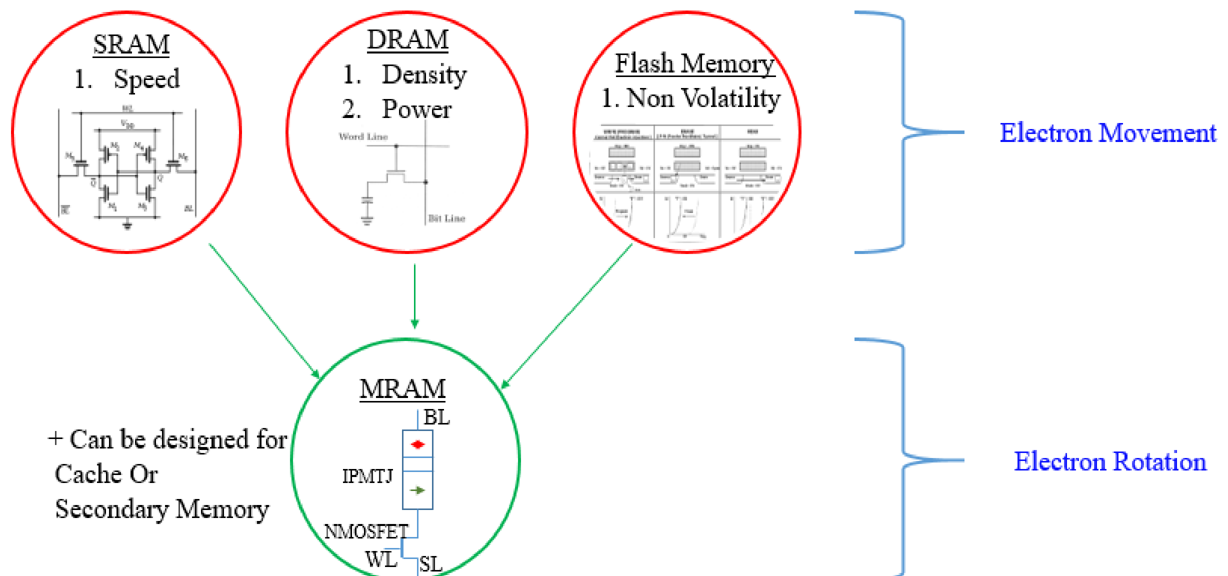


Figure 3: Attributes of STT-MRAM

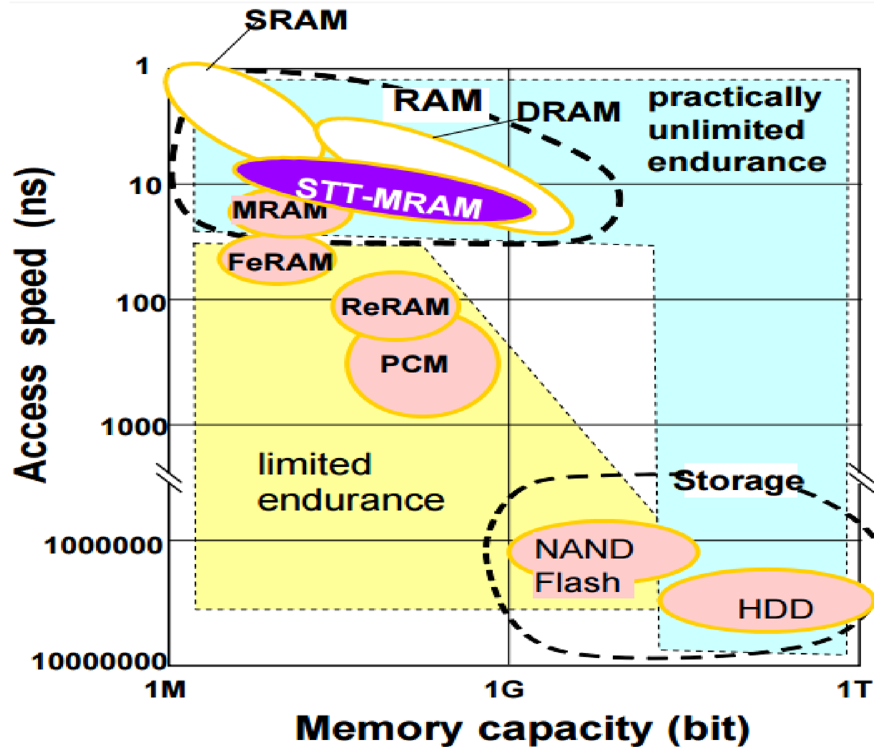


Figure 4: STT-MRAM memory placement with respect to other Non-Volatile memories[19].

Figure 4 represents the placement of STT-MRAM with all other Non-Volatile Memories with respect to Access Time. Flash memory have a worst access time behavior with respect to all other memory technologies. So we need an alternative of Non-Volatile memory that can be comparable to SRAM Access time. STT-MRAM have better properties than other Non-Volatile memories and will be the best in all other Non-Volatile memories.

CHAPTER 2

PLANAR NMOS BASED STT-MRAM BIT CELL ANALYSIS AND CIRCUIT DESIGNING

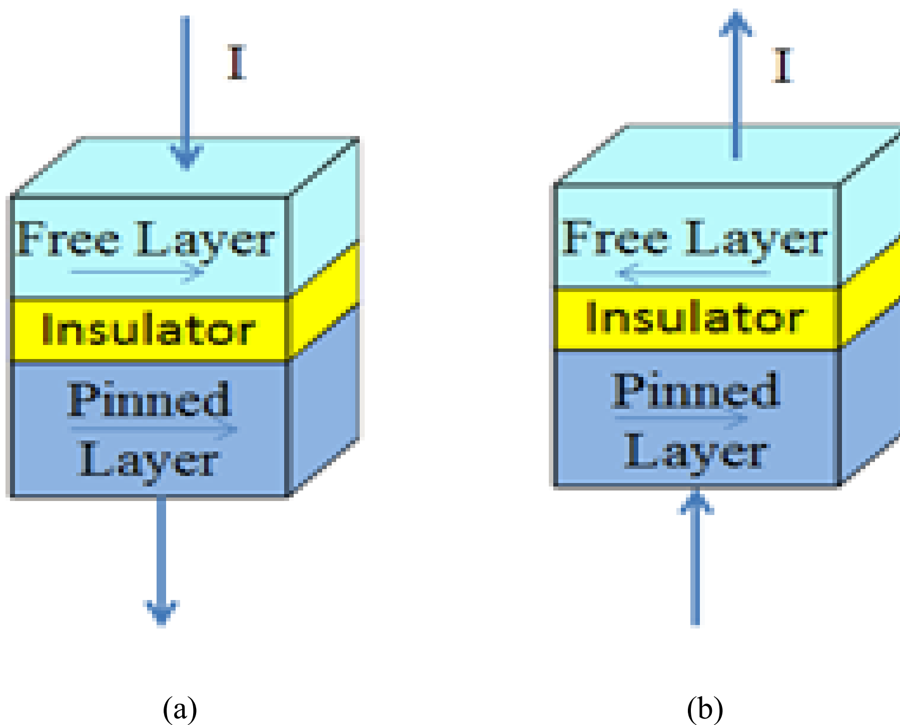
2.1.INTRODUCTION

Magnetic Random Access Memory (MRAM) is a revolutionary technological alternative to SRAM, which is volatile in nature. Due to the advancement of the spintronic technology, magnetic memory devices based on Spin Transfer Torque (STT) MRAM technology are becoming more feasible and attractive to replace the conventional SRAM for Cache and other emerging memory applications. MRAM has some significant advantages, such as, nonvolatile memory property, read and write access speed of 2-10 nanoseconds (ns) for single MRAM-cell, high retention time, unlimited endurance and compatibility to CMOS process. Access speed of 30ns has already been demonstrated in on-chip implementation of MRAM. In this paper, we propose a new simplified single-bit STT-MRAM cell design. We formally name this cell as 1T1M MRAM Cell. We have performed comparative analysis of the proposed and existing STT-MRAM cell designs. We have also investigated some implementation issues of the proposed STT-MRAM and demonstrated an 8x8 MARM array architecture using the proposed cell to compare its benefits with respect to the existing MRAM cell. We also compared different architectures for MRAM memory. Before introducing the new design and related work, it would be relevant to provide a brief overview of the relevant technologies and concepts.

2.1.1. MTJ and its Operation

MRAM is based on magnetic tunneling junction (MTJ) device. Instead of using electric charge to store the data, magnetic storage phenomenon is used in MTJ [1] device. Figure 5 shows the mode of operation of MTJ, which has three layers – a pinned and a free layers separated by an insulator or thin dielectric tunnel barrier (made of MgO). The pinned and the

free layers are made of ferromagnetic materials like Fe, Co and CoFeB. The electron spin direction in the pinned or fixed layer does not change, while the electron spin of the free magnetic layer changes its direction depending on the biasing. The free layer is responsible for the spin polarized current, which depends on the direction of the electrons in the free layer with respect to the pinned layer. Based on the relative electron directions the junction achieves low and high resistance that defines the parallel and antiparallel configuration of the STT-MRAM [1]. In the writing cycle of the STT-MRAM, the energy dissipation of the MTJ can be decreased by having a smaller hysteresis loop during the change in the electron spin direction. For lower hysteresis loop ferromagnetic materials with low coericivity should be used as the free material [4].



(a) (b)

Figure 5 : Direction of electrons in the pinned and free layers, which represents the mode of operation and bit stored in MTJ: (a) parallel mode of MTJ (bit “0”) and (b) anti parallel mode of MTJ (bit “1”).

2.1.2. Single bit STT-MRAM

MTJ cannot be used as a standalone device in the RAM circuit. It always requires an access transistor. Figure 6 shows the layout of a single bit STT-MRAM cell including a MTJ and an access transistor. This layout provides an idea about the size of a 45nm diameter MTJ relative to a conventional MOSFET of 45nm channel length. Figure 7 shows the schematic of a basic single-bit STT-MRAM cell comprising an MTJ and an access transistor. MTJ is the basic building block of STT-MRAM bit cell. The bidirectional signal is given to one end of the MTJ (M1) through the bit line (BL). The other end of the MTJ is connected to the access-transistor (N1) drain. The word line (WL) is connected to the gate terminal of N1. The other terminal of the access transistor is connected to the source-line, which is always connected to the ground. The state or the internal signal of the MRAM can be parallel or anti parallel and will be delivered through the bit line. Here, we are showing the pull-up resistor (R1) to monitor its switching. This pull-up resistor doesn't affect the area and power of the bit-cell. It is just included in the model to monitor the state of MTJ and verify the model while designing MTJ. MTJ is modeled with the resistance based on the brinkman-model [17], which uses the spin transfer torque technique for an in plane anisotropy. With a tunnel oxide thickness of 0.85nm, the MTJ will have a Tunnel Magneto Resistance of 0.99 under initial neutral or zero bias condition, when the MTJ is in a parallel state. Magneto resistance is the ratio of the parallel resistance and the total resistance.

It is anticipated that the direction of the electrons changes according to the generated current because of the spinning. Spin polarized current is the result of Spin transfer torque at the junction and responsible for switching of data in storage layer. Scalability and low-power consumption are the major advantages of STT memory [8]. Scalability issue is resolved by reducing the writing current value. In the large scale memory design, the tunneling oxide gets

damaged because of the high current density. For computation, STT-MRAM requires a high writing energy for a flip flop device operation [8].

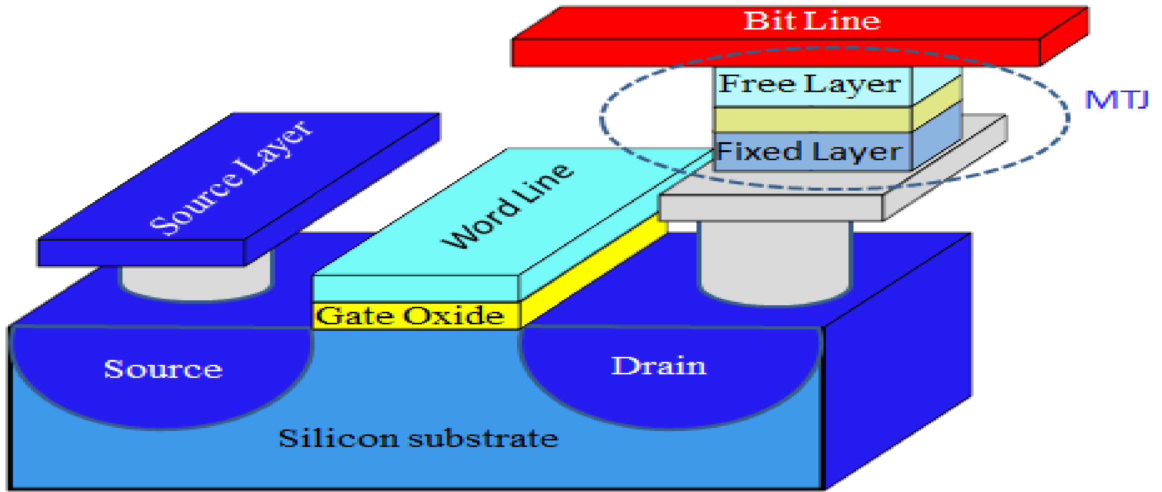


Figure 6: Single bit STT-MRAM including a MTJ and an access transistor (sense amplifier is not shown) [3].

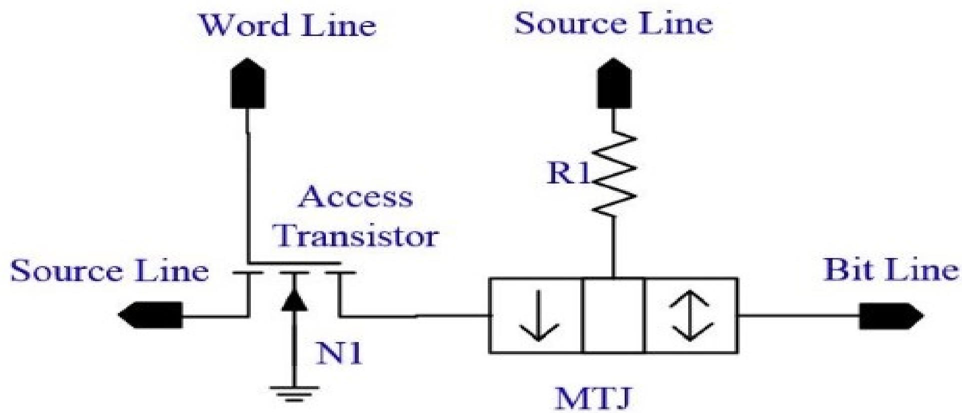


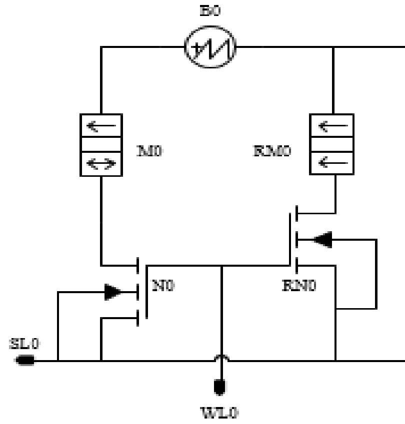
Figure 7: One-bit cell STT-MRAM circuit with one MTJ, one access transistor (45nm), one BL, one WL, one source-line and the state signal (the state signal is to observe the switching mechanisms of MTJ whether it is a parallel or an anti-parallel). MTJ offers spin transfer torque technique with in-plane anisotropy.

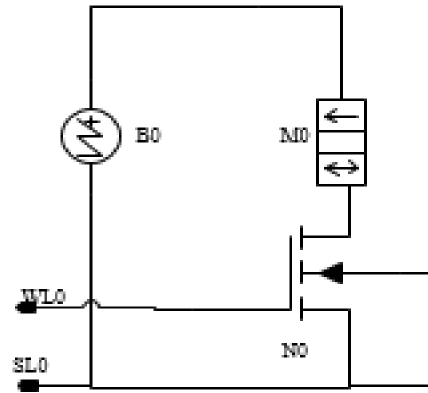
The rest of the paper is organized as follows. Section 2.2 introduces our proposed STT-

MRAM cell and investigates the prospects and constraints of the proposed design with respect to the existing technology. Section 2.3 discusses some device and circuit level issues of the proposed STT-MRAM. Section 2.4 demonstrates an 8x8 MRAM architectures using proposed and existing MRAM cell designs. Finally, 2.5 concludes the paper with a brief overview of our ongoing and future work.

2.2. PROPOSED SIMPLIFIED STT-MRAM CELL DESIGN

Over the last few years several STT-MRAM cell designs have been proposed [2], [11], [14]-[16]. STT-MRAM cells' sizes are in general larger than the flash and DRAM cells, because in each MRAM cell 1 or 2 additional MOSFET transistors are needed to access the MTJ, which leads to the increase in the size. The density of STT-MRAM depends on the MTJ and access transistor's technology node. To ensure higher switching speed (in the range of 10ns) the access transistor should be able to provide higher current (in the range of 100μA) [12]. Therefore, the size (W/L ratio) of the access transistor should be big enough to allow this huge current. Additionally, the higher number of interconnects and contacts between the MTJ and access transistor increases the manufacturing complexity, cell area and cost [11]. Since this is a new and emerging area, there are many challenges and huge opportunities for the improvements of every possible aspect of MRAM design from individual cell to large MRAM architecture and memory systems that would be utilizing MRAM cells as the fundamental building blocks. There is also another growing demand to introduce efficient circuits and architectures to compete with the existing nonvolatile memory (NVM) technologies. Due to the nonvolatile nature of MRAM cell, there is an enormous potential for this new memory technology in the fastest growing NVM industry.





(a)	(b)
1. 2 MTJ/cell	1.1 MTJ/cell
2. 2 Access Transistor /cell	2. 1 Access Transistor/ cell
3. More Area	3. Less Area
4. Complex reading mechanism	4. Simple reading mechanism
5.Implemented in 130nm-65nm technology nodes	6. implementing in 45nm technology node

Figure 8: Schematic circuit of (a) one of the existing MRAM bit cell [2] and (b) the proposed STT-MRAM bit cell.

Among the existing MRAM cell designs, the 2M2T STT-MRAM cell of [2] is widely referenced and verified through some prototype implementations. Each MRAM bit cell proposed in [2] has 2 MTJs and 2 access transistors. In this paper, we proposed a 1M1T STT-MRAM cell design and compared it with the previously validated and implemented 2M2T cell design of [2]. At the architecture level, we have used the modified array architecture, which minimizes the number of access transistors. In Figure 8b we have shown our proposed 1M1T STT-MRAM cell design and compared it with the existing 2M2T MRAM cell design (Figure 8a) [2]. Existing architectures use the conventional sense amplifier, which need an additional

MTJ and a transistor per bit-cell.

2.2.1. Writing Operation of the Proposed STT-MRAM Cell

The MTJ's state will remain as it is irrespective of the state of the bit line (BL) if the write line signal WL=0. When the write line is activated (WL=1) and a positive pulse is applied at the bit line (BL), the MTJ switches from parallel state to antiparallel state. With WL=1, a negative pulse at BL switches the state of MTJ from the antiparallel state to the parallel state. When an intermediate (between positive and negative) pulse is applied at BL, MTJ holds the previous state.

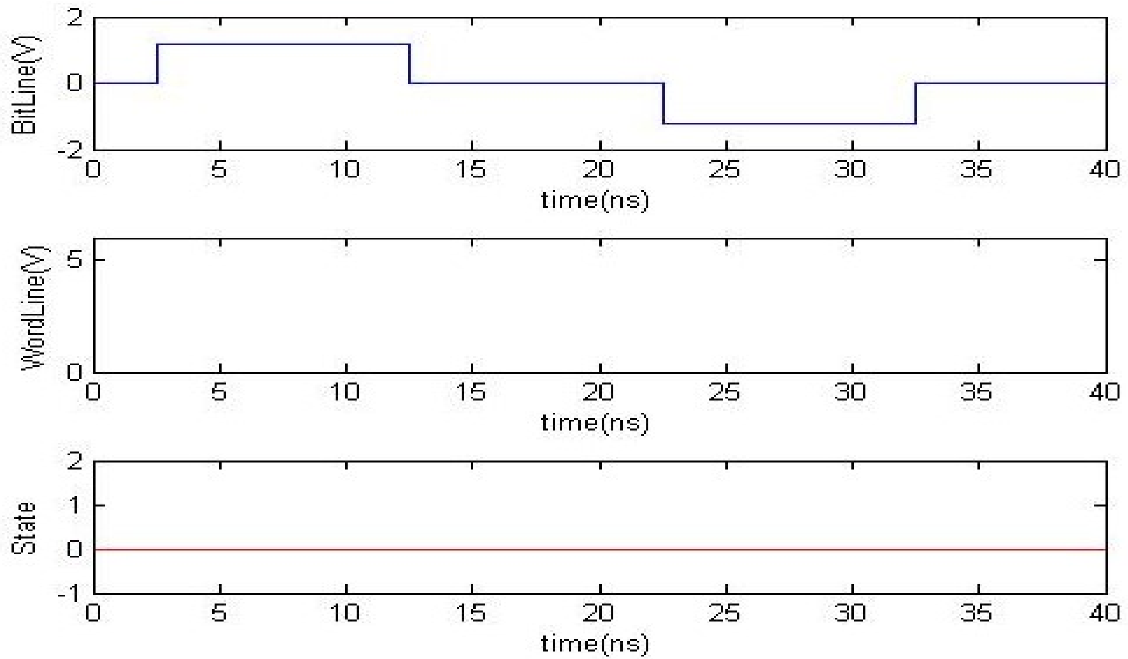


Figure 9: CIRCUIT simulation of STT-MRAM bit cell when a deactivating signal (WL=0) is applied at the access transistor.

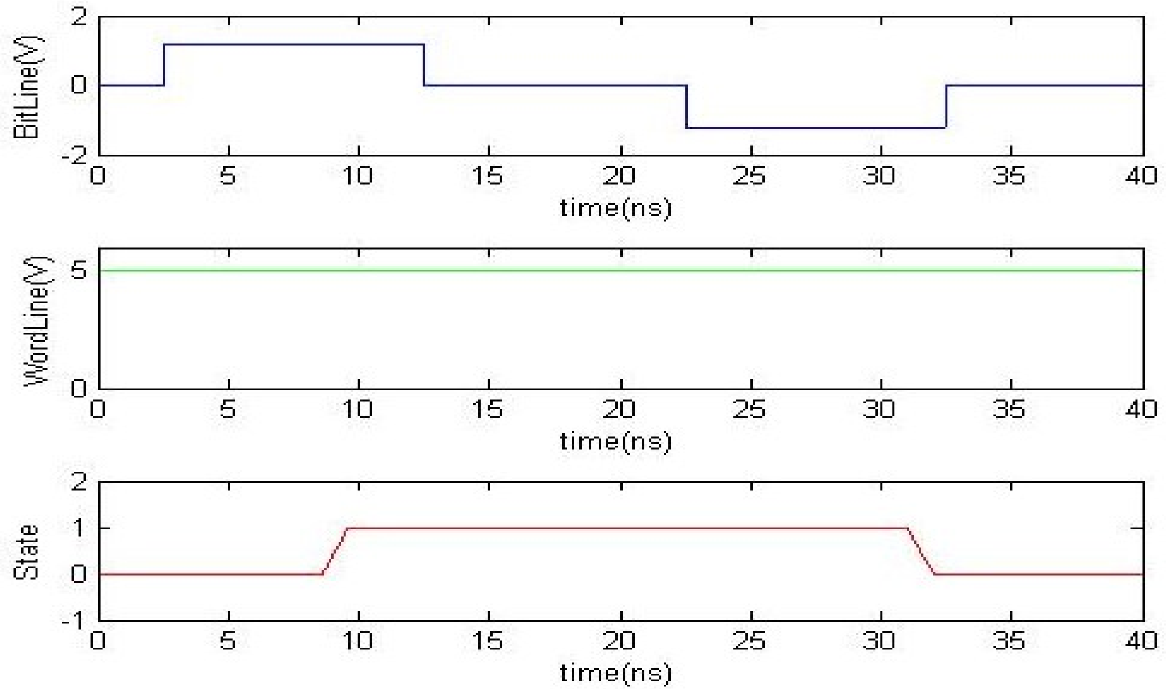


Figure 10: CIRCUIT simulation of STT-MRAM bit cell when an activating signal (WL=1) is applied at the access transistor.

2.2.2. Reading Operation of the Proposed STT-MRAM Cell

During the reading operation, a small pulse is applied at the BL when the pass transistor gets activated and the current of pinned layer is available at the bit-line, which can be used to recognize the state of the MTJ. Reading pulse is applied at the gate of the pass transistor. Sense margin is not comparable with the logic levels (1/0). An additional amplifier circuit is used to make a reliable reading output. Write and read operations are controlled separately by the access transistor and pass transistor.

For the verification of the operation of MRAM cell, we have performed simulation of the circuit using Cadence Spectra. For the simulation the 45nm process development kit (PDK) from Cadence is used for the transistor model and Verilog-A model of [13] is used for the MTJ. The access transistor is in OFF state when a deactivating signal (WL=0) is applied at the gate terminal of the access transistor as shown in Figure 9. For the MTJ to be activated its pinned

layer has to be connected to the source line of the access transistor, which is connected to the ground. If the access transistor is OFF, the MTJ cannot get sufficient energy to spin the electrons in the free layer irrespective of the state of the bit-line. In this condition, the STT-MRAM bit-cell cannot read or write a new value through the bit-line. The state of MTJ will be in hold mode.

When a positive pulse (1.2V) is applied to the access transistor (WL=1) the bit-cell is activated and ready for read/write operations. Without any voltage applied at the bit-line the STT-MRAM is initially in parallel state. When a positive pulse of 1.2V is applied to the bit-line (BL=1), the free layer of the MTJ gets sufficient energy to spin the electrons in the opposite direction of the pinned layer electrons' direction. At this stage, the STT-MRAM switches from parallel state ("0" bit) to anti-parallel state ("1" bit). Figure 10 shows the writing and reading operation of STT-MRAM when the access transistor is at ON state.

2.2.3. Nonvolatile Feature of the Proposed STT-MRAM Cell

Storing a value in the STT-MRAM depends on the electron rotation rather than the electron movement. After providing sufficient energy (either 1.2V or -1.2 V) to the electrons in the free layer of the MTJ the rotations (parallel or anti-parallel) of the electrons with respect to the pinned layer will remain unchanged until we apply an opposite voltage (either -1.2V or 1.2V) to change the electrons rotation. This feature ensures the nonvolatile nature of STT-MRAM cell. Figure 11 demonstrates this nonvolatile feature. Figure 11 shows the hold state of the STT-MRAM. In this state it retains the previous state value. This is done by deactivating (WL=0) the access transistor, when the BL value has no effect on the state of the cell.

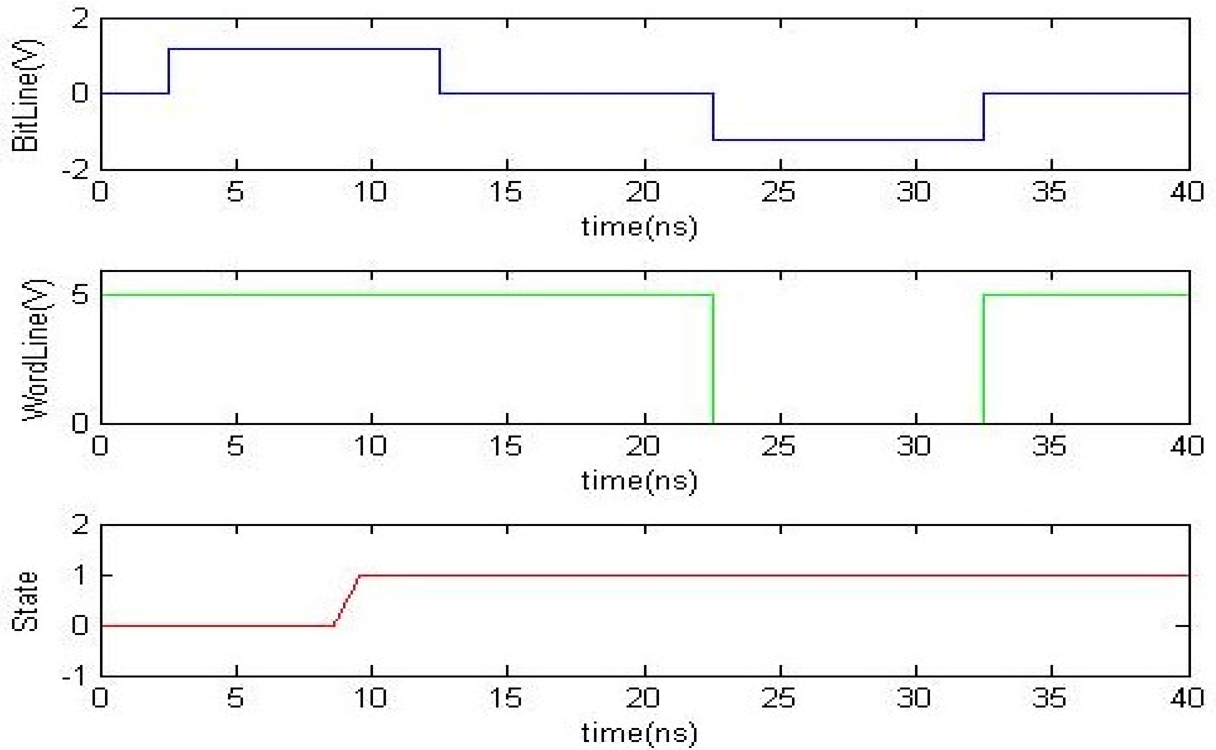


Figure 11: The non-volatile characteristics of STT-MRAM circuit. SPICE simulation of STT-MRAM bit cell when a deactivating signal is applied at WL. The outputs represent BL, WL and state signals of STT-MRAM bit cell.

2.2.4. Temperature Dependence of the STT-MRAM Cell

MTJ requires certain amount of energy to be either in the parallel or in the antiparallel state. The temperature of STT-MRAM changes according to the operating states of the MTJ. Figure 12 shows the change of temperature during the parallel and anti-parallel states of the STT-MRAM for the input signals of Figure 10. The dependence of the physical and performance parameters of the STT-MRAM on temperature is not a simple issue. This requires in-depth analysis. There are many other issues that need to be investigated. Since the focus of this paper is to present the concept of a new STT-MRAM cell design and provide some preliminary validation, we did not include further analysis on these issues. Besides, space

limitation prevents us from including more contents into a single paper. Our future work will address many of these issues.

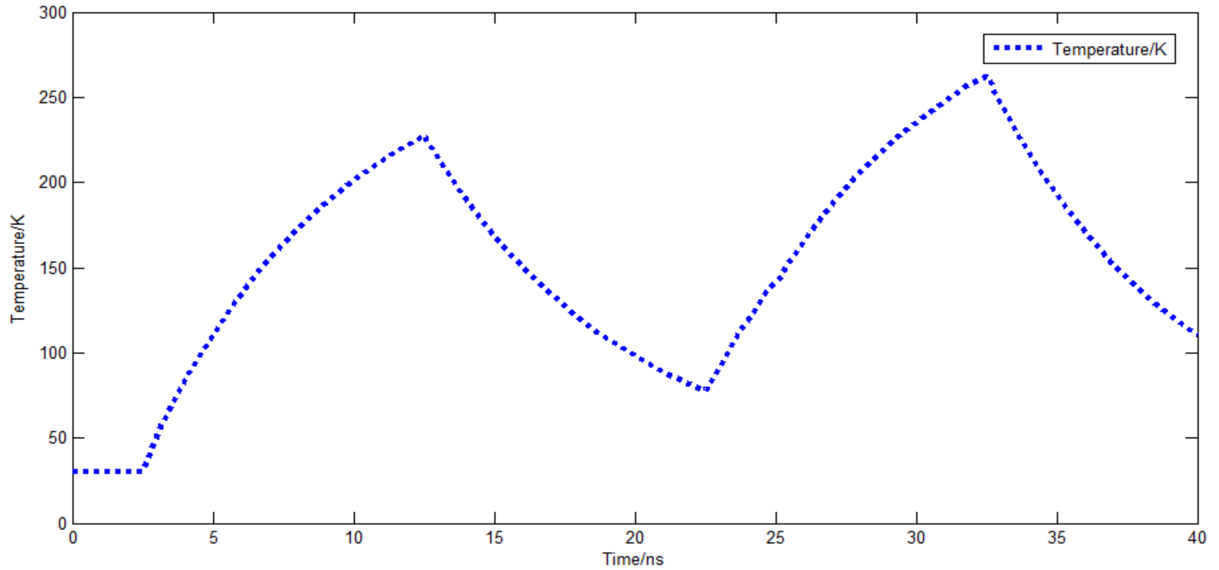


Figure 12: Temperature dependence of MTJ for the input of Figure 10.

2.2.5. Comparison of the Proposed and Existing STT-MRAM Cells

The 2M2T MRAM cell proposed in [2] is considered as one of the standard designs. The other proposed designs of [11] and [14] -[16] are claimed to be 1M1T designs, which implies that these cell designs would require only 1 MTJ and 1 access transistor. However, this claim has not been validated, and a closer look at these designs reveals that each of these cells actually requires 1 additional MTJ and 1 additional access transistor. Therefore, these designs are not truly 1M1T as it is claimed. All the previous MRAM cells are demonstrated for 90nm to 130nm technology generations. Here, we have introduced the new design for 45nm technology generation. For MRAM cell design, 45nm is the most recent trend. Table 2 provides detail comparison of our proposed 1M1T STT-MRAM cell design with respect to the other existing designs. Although each of the previously proposed designs are based on different technology nodes and operation mechanisms, for reasonable comparison we have implemented the

previous designs using 45nm technology node.

Table 2: Comparison between the existing and proposed MRAM nonvolatile memory bit cell.

	Current (uA)	Voltage (V)	Time (ns)	Energy (pJ)	Power (pW)
2M2T[14]	270.544	1.2	10.2	3.30	33
2M2T[2]	760.434	1.2	3.99	3.641	36.41
1M1T	283.18	1.2	7.7	2.6	26

Scaling down the existing designs leads to increase in overall delay of the circuit. Huge amount of current is required to write into STT-MRAM. So we need large access transistor to provide the large writing current that results in the increase of total cell area. Table 3 represents the state-of-the-art of the scaling of STT-MRAM in different architectures.

Table 3: State of art of STT MRAM circuit and architecture.

Architecture BitCell Type	CMOS Node (nm)	Cell	Delay (ns)	Write Energy (pJ)	Critical Current (uA)
Conventional Array with stretched write cycles(SWC)[14]	45	1M2T	10.2	3.3048	270.54
Multicontext [15]	90	2M2T	4	4.4	200
Cross-point [11]	65	2M2T	1.2	0.9	100
Conventional[2]	65	2M2T	9	1.5	200

2.3.STT-MRAM DELAY REDUCTION BY DEVICE (MTJ) AND CIRCUIT CO-DESIGN

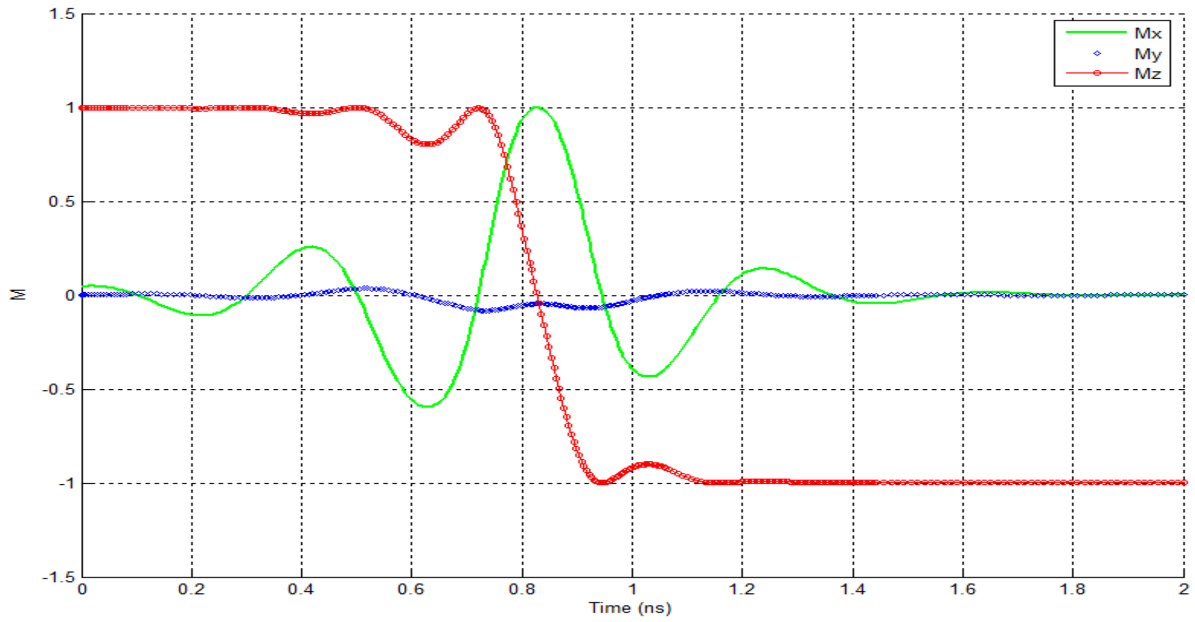
2.3.1. Optimization of MTJ Device Level Magnetization Property to Reduce Delay

Delay of the STT-MRAM cell can be reduced by increasing the ratio of the switching current and the critical switching current (I_E/I_S). Critical switching current (I_S) is the good spin value of the MTJ. Usage of MgO as the tunnel oxide in MTJ instead of $AlOx_3$ reduces critical switching current density by 3-4 times. Critical switching current is fixed for a particular technology. Switching current (I_E) is the current passing through the STT-MRAM cell at any instance. With the increase of the switching current of the MTJ, it takes less time to have the magnetization reversal in the device. Magnetization reversal is the stage where the electrons in the free layer lose their stability and are ready to rotate accordingly. Delay is the time measured at which magnetic reversal takes place. The magnetization reversal property is simulated in MATLAB. Magnetization (M) is observed in all directions (m_x, m_y, m_z). Here, m_z is considered as the indication of the magnetization reversal property. Figure 13 shows the magnetization (M) characteristics of the MTJ as a function of the time (t). The switching and critical switching current ratio (I_E/I_S) of MTJ is used as a parameter. Figure 13a shows M-t characteristics when $I_E/I_S=8$. Figure 13b shows M-t characteristics when $I_E/I_S=4$. Figure 13c shows M-t characteristics when $I_E/I_S=1.3$. By comparing the three plots of Figure 13 it is concluded that Mz shifts from positive to negative magnetization (demagnetization) value when I_E/I_S is higher. Therefore, $I_E/I_S=8$ offers faster demagnetization than $I_E/I_S=4$ and $I_E/I_S=1.3$.

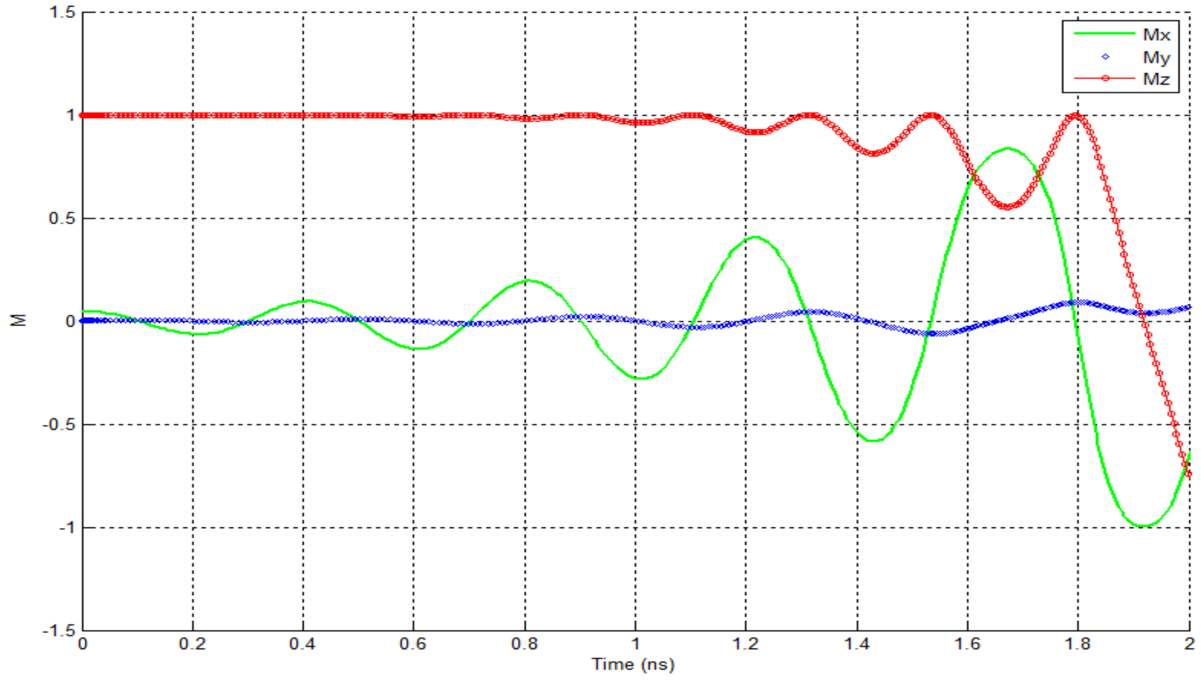
2.3.2. Circuit Level Implementation of STT-MRAM to Reduce Delay

Since the critical switching current (I_S) is fixed for a particular technology, the only parameter that can be optimized to reduce the delay in STT-MRAM cell is the switching current (I_E). As mentioned earlier, the delay of the STT-MRAM circuit is reduced when I_E increases. Size of the access transistor will have direct impact on the value of I_E. The delay of the cell will

decrease if the size (W/L ratio) of the access transistor is increased, because larger access transistor can provide higher I_E and larger I_E/I_S ratio in the MTJ. Therefore, at the circuit level simulation and optimization the W/L ratio of the access transistor shows a proportional dependency on I_E/I_S. We have performed the circuit level simulation of one bit STT-MRAM cell with an access transistor of 45nm technology node. The simulation is shown in Figure 14.



(a)



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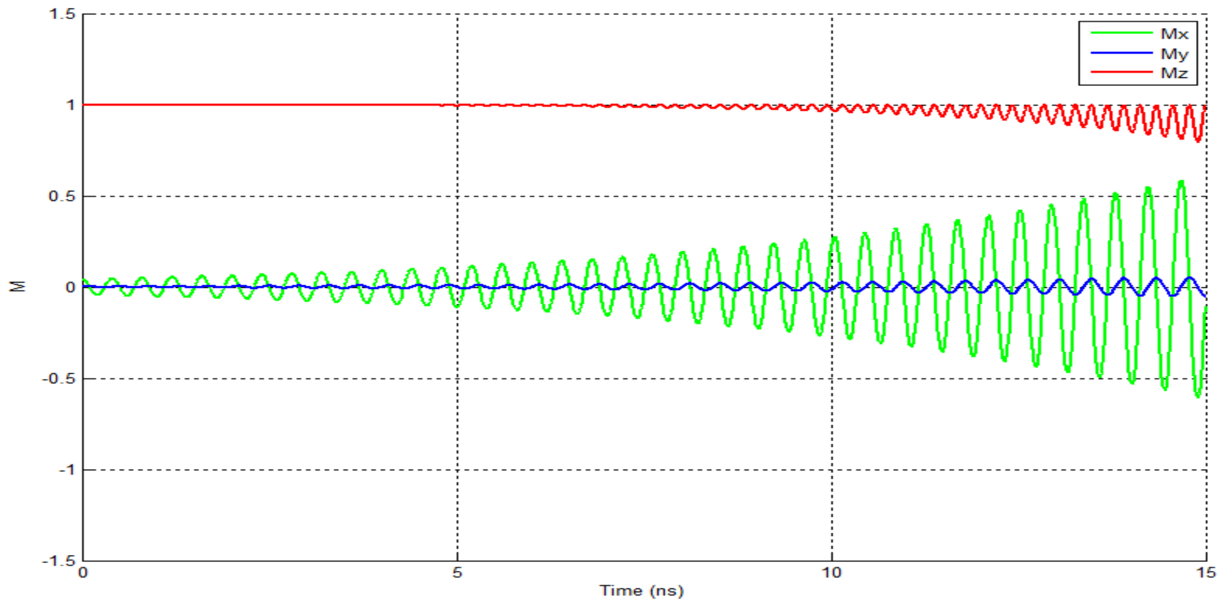


(c)

Figure 13: Simulation of STT-MRAM magnetization property along x, y and z axis when (a) I_E/I_S=8, (b) I_E/I_S=4, (c) I_E/I_S=1.3.

Figure 14 shows how MTJ device level delay optimization is implemented in STT-MRAM

circuit level design. This is a device-circuit co-design approach, where any parametric optimization in the MTJ device directly reflects in the STT-MRAM circuit level performance. To decrease the delay (time taken to demagnetize the STT-MRAM to write a new state into it) of the STT-MRAM, W/L ratio of the access transistor should be increased. Delay can also be reduced by introducing different bit structure, which consumes more area that is discussed in [5] and [8]. Usage of FinFET can also be a solution to decrease delay, which is discussed in [6]. Figure 14 compares the delays for different sizes of the access transistor. State1 represents W/L=150 with a delay of 1ns. State2 represents W/L = 30 with a delay of 1.291ns. State3 represents W/L = 15 with a delay of 1.67ns. State4 represents W/L = 7.5 with a delay of 2.431ns. State5 represents W/L = 2.5 with a delay of 6.08ns.

2.4. IMPLEMENTATION OF AN 8X8 RAM ARCHITECTURE USING THE EXISTING AND PROPOSED STT-MRAM

To validate our proposed STT-MRAM cell design and investigate its prospects and constraints we have implemented an 8x8 RAM array using the conventional 2M2T MRAM cell and our proposed 1M1T MRAM cell.

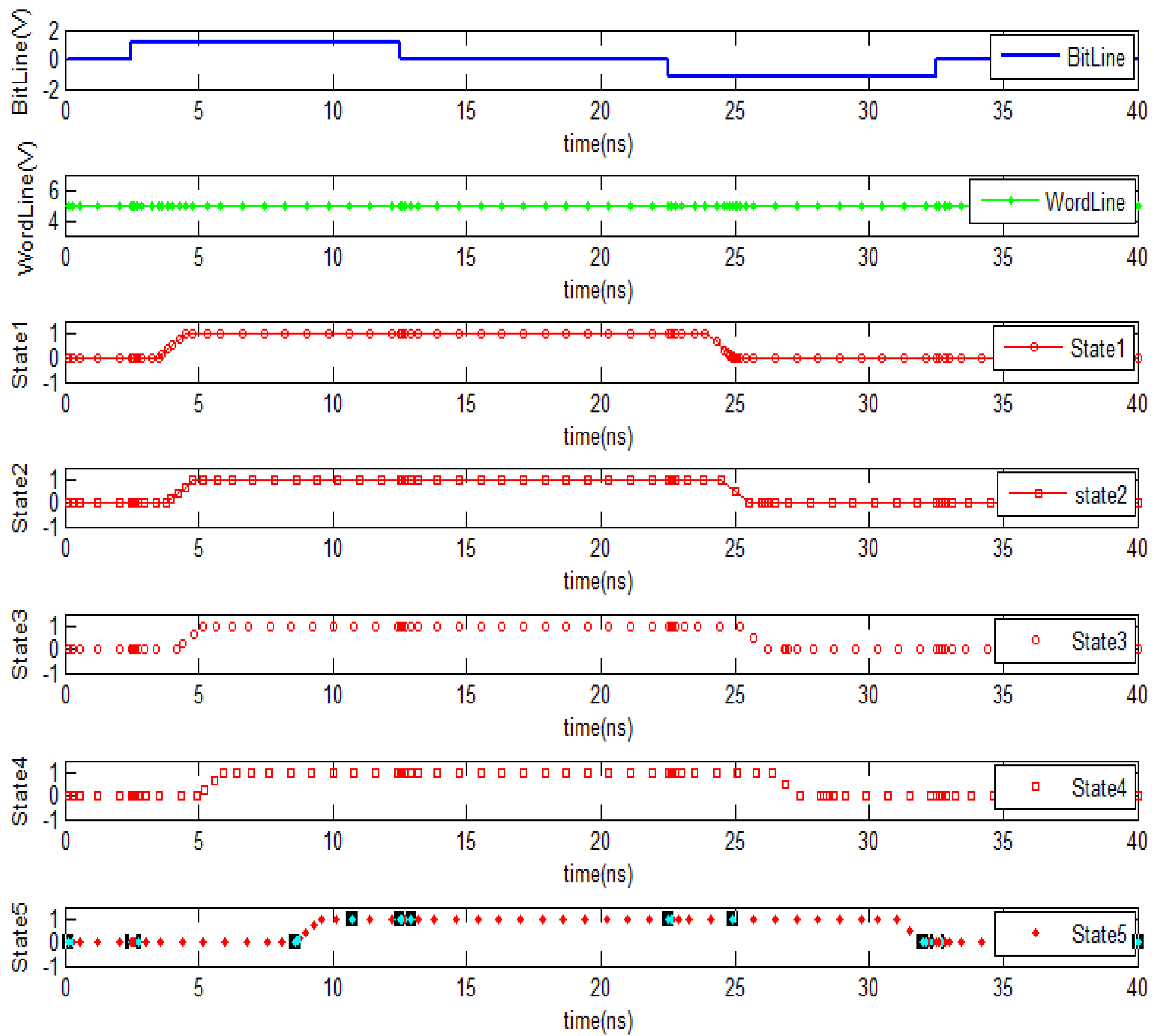


Figure 14: The output state of the STT-MRAM device and circuit co-design approach. High W/L ratio of the access transistor reduces the delay in the demagnetizing of the MTJ.

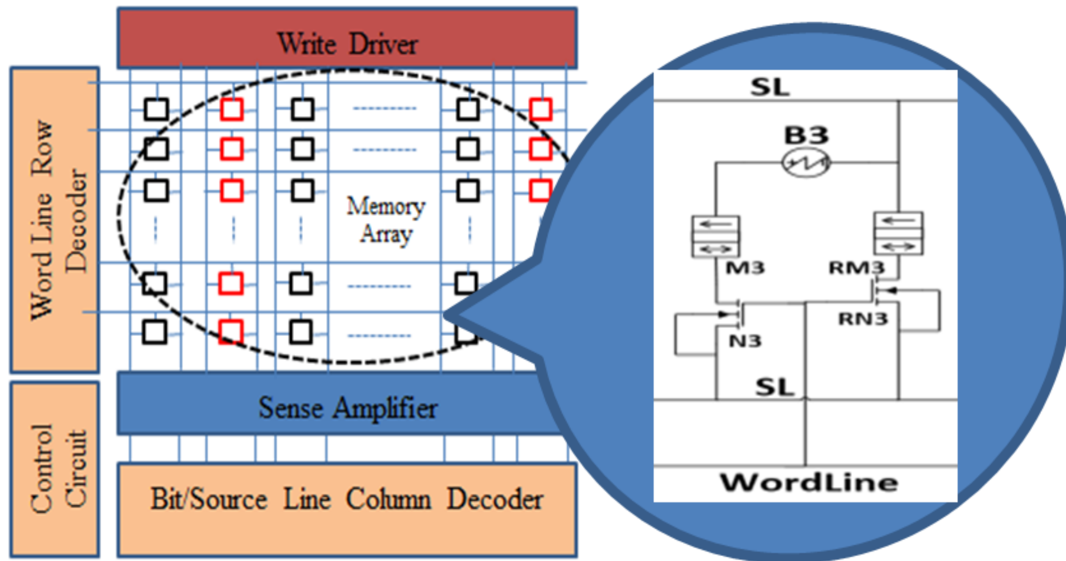


Figure 15: Conventional STT-MRAM system architecture/array block diagram, where each cell is represented by 2 MTJs and 2 access transistors [2].

2.4.1. Conventional Architecture

Figure 15 shows the conventional STT-MRAM system architecture/array block diagram, where each bit cell is selected by the row and column decoders. Figure 19 shows the circuit implementation of the 8x8 MRAM array using conventional cell. In each cell, one of the two MTJs is used as the reference to sense the value stored in the other MTJ. The existing MRAM designs propose to use the regular sense amplifier used in basic SRAM and DRAM memory applications. The standard sense amplifiers have some limitations in terms of the usage in MRAM array. There are some power related issues as well in the current MRAM design. Low power issues of the existing STT-MRAM circuit design is discussed in [10].

2.4.2. Proposed Architecture

Figure 16 shows STT-MRAM architecture/array block diagram for the proposed cell. Figure 20 shows the circuit implementation of 8x8 STT-MRAM array using our proposed cell. Each STT-MRAM bit cell has one access transistor, which is active when the corresponding

word line is active. Here, the write signal (WL) is connected to the gate terminals of all the access transistors in a word. When a write signal is active the whole word is activated and the row and column decoders select the specific bit cell within that word. To change the state of a specific MTJ in the STT-MRAM array either a -1.2 V or a +1.2 V is applied at the bit line. With +1.2 V, the state of MTJ changes from parallel to anti-parallel and with -1.2 V, it changes from anti-parallel to parallel state.parallel to parallel state.

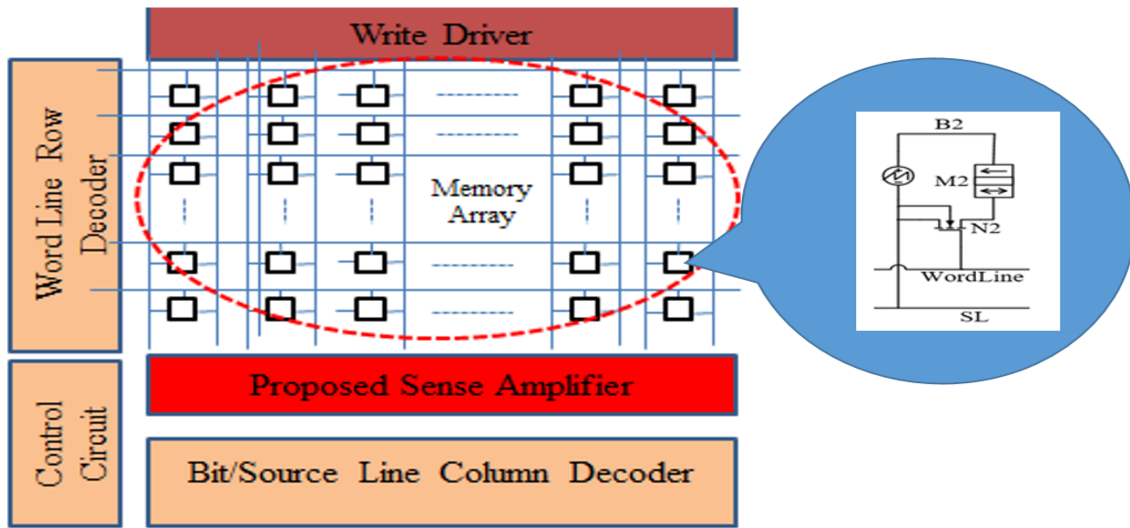


Figure 16: Proposed architecture showing bit cell.

In our proposed architecture the reference MTJ of the 2M2T MRAM cell is eliminated from the cell. Additionally, the number of access transistor per cell in our proposed design is one (1) as opposed to two (2) access transistors per cell in the design of Figure 15. The elimination of 1 MTJ and 1 access transistor from the proposed cell makes each individual cell and the overall architecture significantly simpler and energy efficient, and it can be implemented in less area. Roughly, we can estimate that 50% of the area of the chip can be saved by using our proposed cell. Elimination of 1 MTJ and 1 access transistor per cell will also provide significant reduction of leakage leading huge savings in overall power consumption.

Figure 21 represents the output of bits (B0-B8) for the proposed architecture. Outputs are

taken from the sense amplifier connected to the pass transistor logic at the bit line. This simulation is executed to show that our proposed Array is accessible to read and write operations. In this simulation WL0 signal is given a pulse input with a pulse-width and period of 40ns and 80ns respectively. B0 signal is also given a pulse input with 10ns pulse-width, 20ns period, and +1.2V as high input and -1.2V as low input. The delay of B0 is 0ns. B1-B7 signals are have delays in the increment of 10ns. WL1-WL7 is deactivated (0V). Output is plotted from the sense amplifiers connected to the bit-lines (B0-B7).

Table 4: Power and performance comparison of memory arrays implemented with the proposed and conventional MRAM cells

	Power (nW)	Delay (ns)
Conventional Array	2.33	510.72
Proposed Array	1.664	492
Improved percentage	28.755%	3.67%

Table 4 compares the proposed array architecture with respect to the conventional array architecture in terms of power and delay. Delay and power is calculated using Cadence Spectre simulation tool. Our proposed array architecture reduces overall power by 28% with respect to the conventional array architecture. Delay of the proposed array architecture is reduced by 3.67%. As mentioned earlier, we anticipate close to 50% saving in area. However, without the actual layout it would not be possible to quantify the area saving.

2.4.3. Analysis of the Impact of Threshold Voltage Variation of the Access Transistor on the Proposed STT-MRAM Cell

Figure 17 represents Monte Carlo simulation of the variation of V_{th} in the access transistor.

This variation leads to the shift of the operating region of the access transistor, which affects the write and read operating of the MTJ. The simulation is performed by activating W0 and deactivating all other word lines (W1-W7) in the proposed array architecture of Figure 20. The bit-line (B0) is given a sequence of signal as in Figure 21. The variation of V_{th} in the access transistor (N_0) and its effect is observed through Monte Carlo simulation using ADE-XL simulator. The variation is taken from the technology file provided to the simulator. Latin hypercube sampling method is chosen to do the simulation due to its faster ability. The input for this simulation is the number of points (N), which we selected to be 1000. Number of points is the samples between the ranges of V_{th} variation. Mu is the mean of the analysis and here it is 237.931 mV, which represents the maximum number of pass points at that sample. Pass points are the yield of the analysis. In our simulation, yield is 100%. The term *sd* is the standard deviation of the analysis and here it is 10.46 mV. Standard deviation shows the number of points towards the mean. When *sd* tends to zero more points are towards the mean. Figure 18 shows the output of the bit-cell in the proposed array with the variation of V_{th} of the access transistor. Table 5 gives the information of distribution of the number of points.

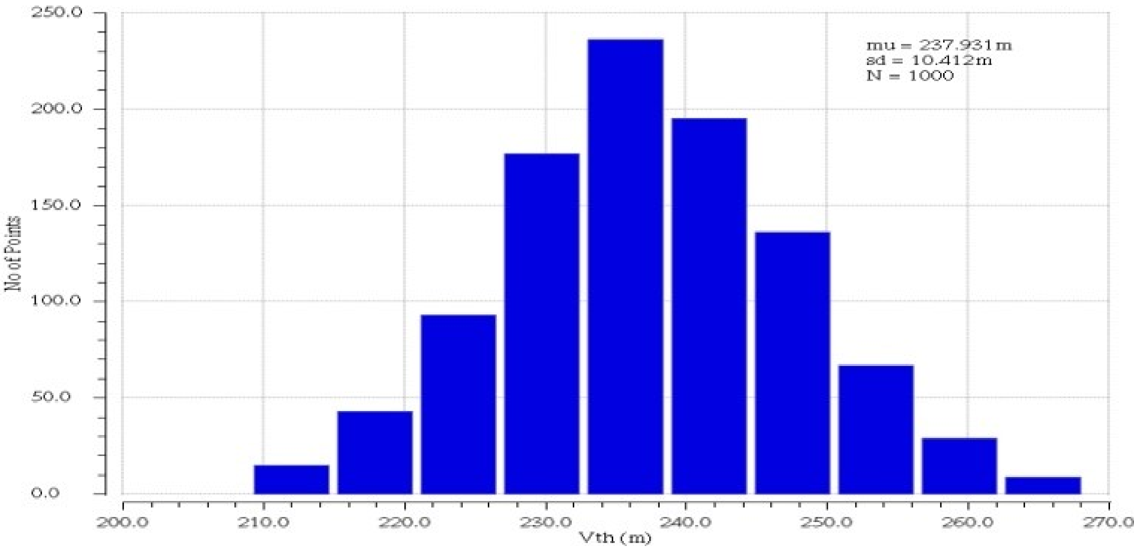


Figure 17: Monte Carlo Simulation of V_{th} with 0 fail points and 50 pass points for 1000 bins.

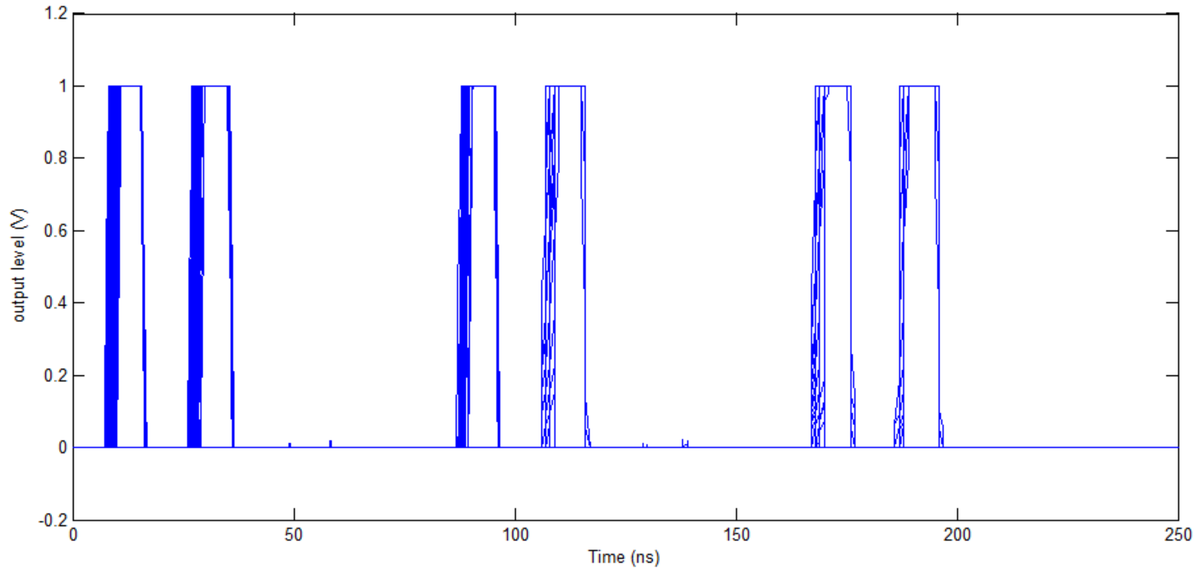


Figure 18: Monte Carlo simulation that is STT-MRAM is holding for 1000 points.

Table 5: Distribution of points in Monte Carlo simulation

V_{th} of the access transistor (mV)	Number of Points
209.64	15
215.57	43
221.50	93
227.41	177
233.33	236
239.26	195
245.18	136
251.1	67
257.02	29
262.94	9
Total points	1000

2.5.CONCLUSION AND FUTURE WORK

In this paper, a new STT-MRAM cell has been proposed, which contains 1 MTJ and 1 access transistor. The proposed 1M1T MRAM cell and the corresponding array architecture would be simpler and more area- and power- efficient than the existing 2M2T MRAM cell and its corresponding array architecture. In this paper, the main focus is to proof the concept of a new STT-MRAM cell. In our future work, we will focus on quantifying the advantages of the new MRAM cell in terms of power, area and circuit implementation._The proposed STT-MRAM circuit and architecture are implemented in 45nm technology node. All the prior work on MRAM cells were based on 130 to 65nm nodes. The power consumption, delay and area of the proposed 1M1T are expected to be significantly lower than that 2M2T due to lower number of MTJ and access transistors. For the first time, we demonstrated the implementation of an 8x8 STT-MRAM array architecture using the proposed 1M1T and existing 2M2T MRAM cells. For fair comparison, we implemented both architectures using same technology node. In addition, this paper discusses some circuit and architecture co-design issues and impacts of process and parametric variation. Our future work involves Ultra-Low-Power MRAM design in sub-nm technology (20 to 10nm).

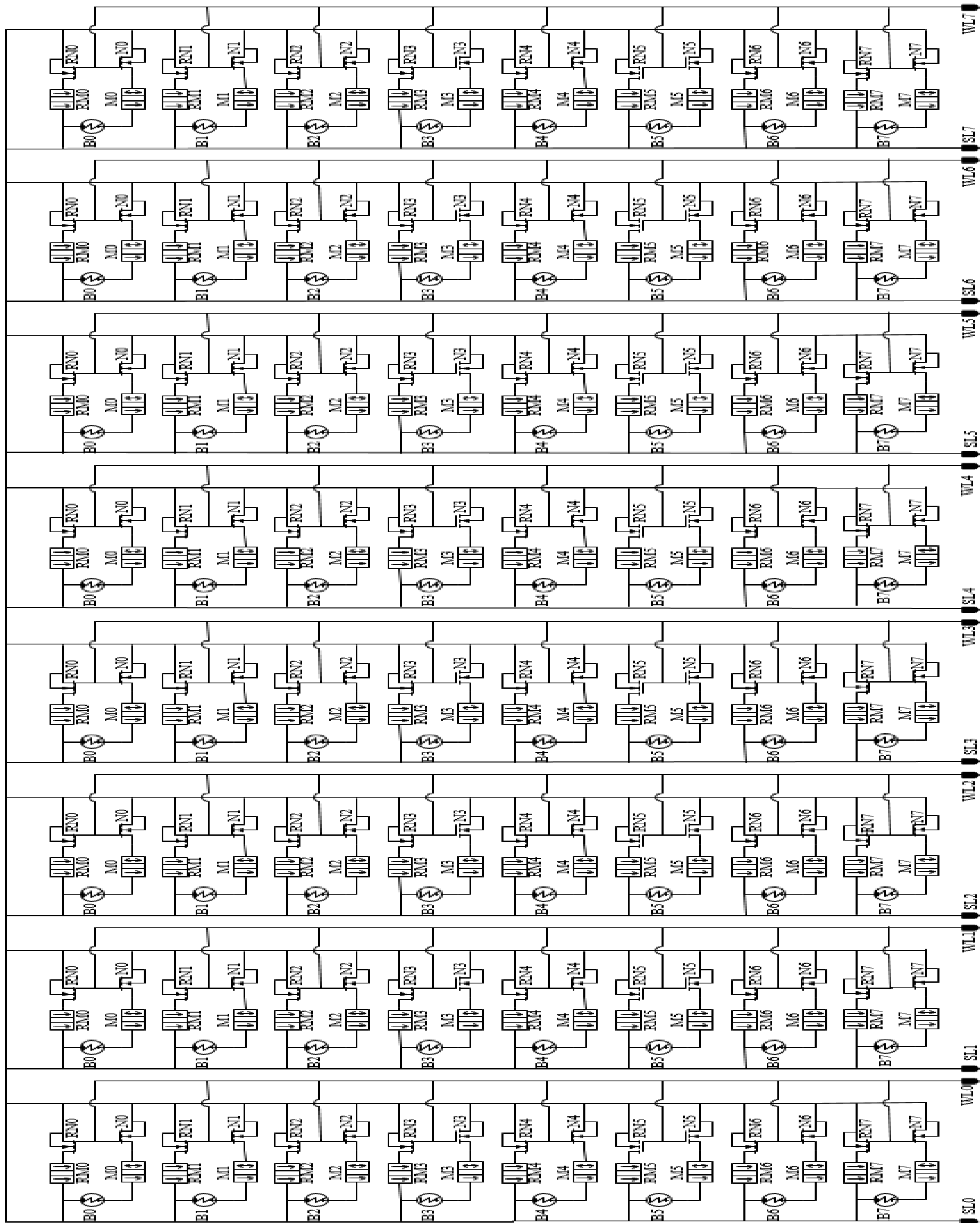


Figure 19: Conventional STT-MRAM system 8x8 architecture/array, where each cell is represented by two MTJs and two access transistors [2].

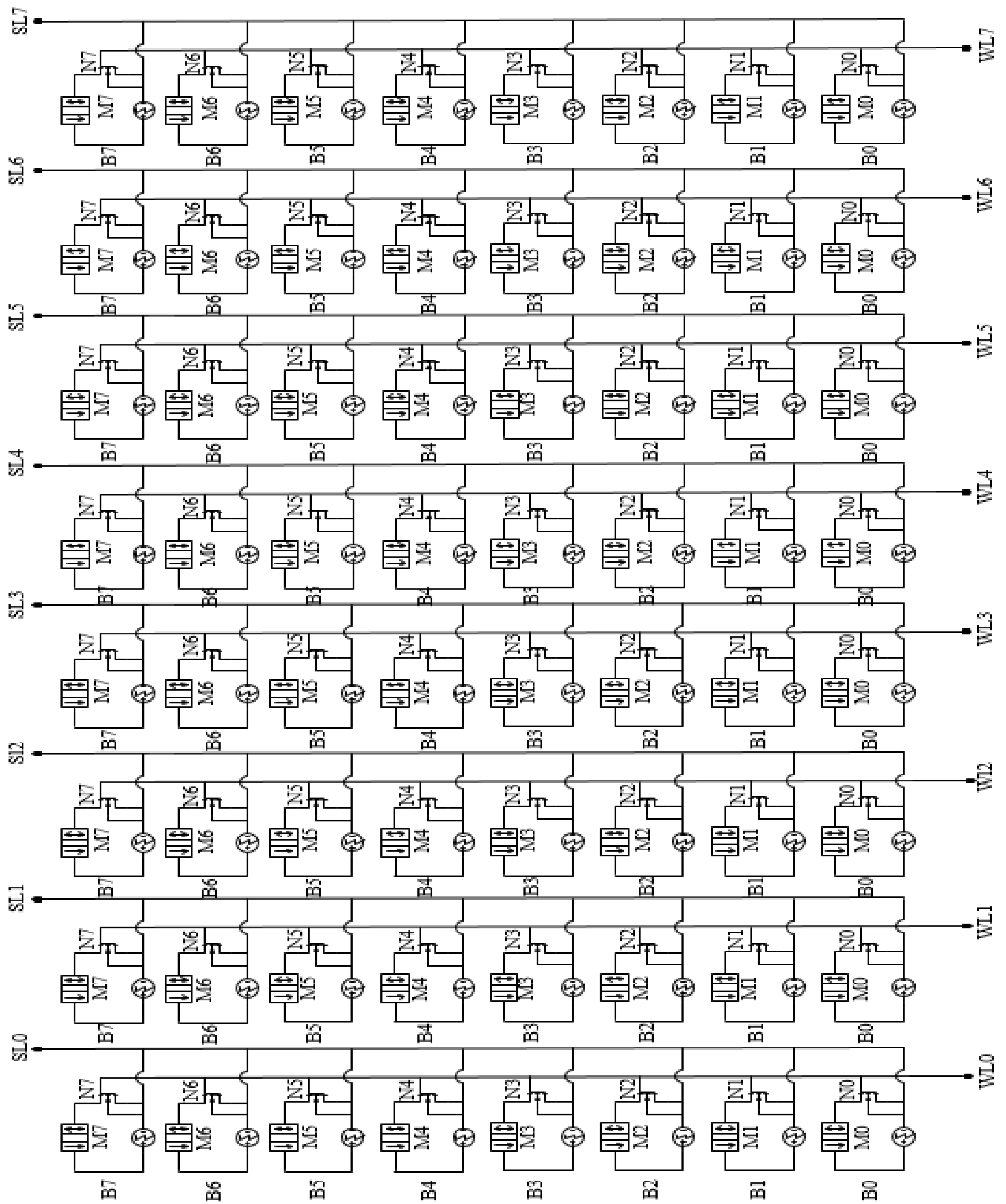


Figure 20: Proposed STT-MRAM system 8x8 architecture/array, where each cell has one MTJ and one pass transistor (45nm).

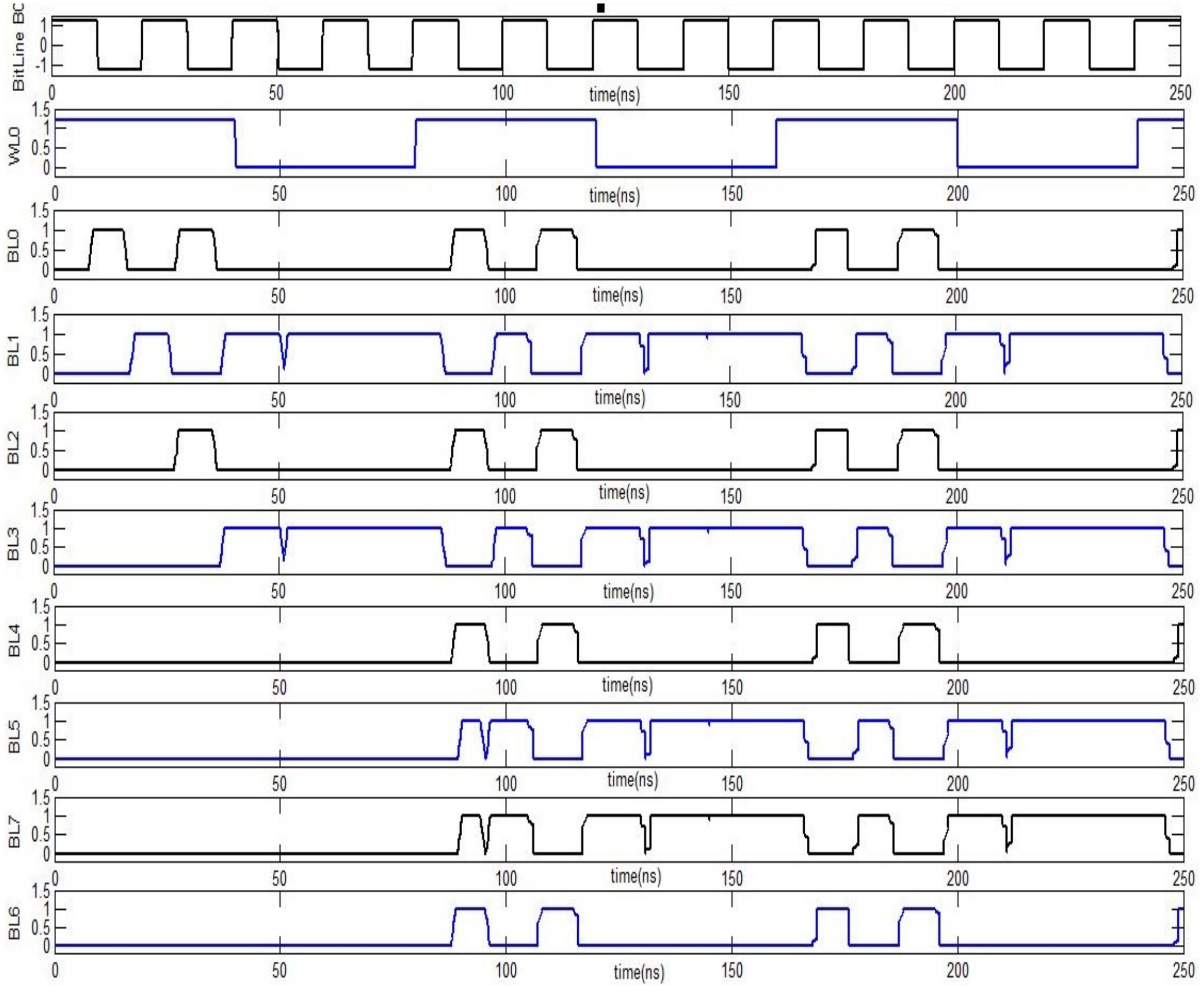


Figure 21: Plots of Values stored in eight MTJs of the proposed Architecture

As of now all the current research works on MRAM including our work use the standard sense amplifiers of the basic memory applications to demonstrate MRAM memory arrays. However, based on our preliminary study, we anticipate that standard sense amplifiers would not be very efficient for MRAM arrays. We are currently working to design a new type of sensing amplifier for our proposed and other MRAM cells and memory architectures to improve the performance and reliability of MRAM. Some neural applications need parallel reading and writing of the memory. The proposed cell and the architecture can be configured to perform simultaneous read and write using the sense amplifier under investigation

CHAPTER 3

PERFORMANCE IMPROVEMENT USING FINFET BASED STT-MRAM CIRCUIT DESIGN

As the transistor scales down, it is prone to subthreshold leakage, gate-dielectric leakage, Short channel effect and drain induced barrier lowering. Now alternative of Access transistor is needed. We are using FinFET as access transistor in the STT-MRAM bit cell. FinFET based bit cell is designed to get an advantage of scaling down. Analysis is done and proven that the power consumption, standalone leakage current is less when compared to NMOS based STT-MRAM bit cell. Also determined FinFET based bit cell produces less access time to access the logic value from MTJ.

3.1.INTRODUCTION

Switch mechanism of access transistor in a STT-MRAM bit cell should be much effective to easily scale down and have a better control over MTJ to store respective logic value into it. As due to the electrical and physical limitation of a transistor it is necessary to go beyond NMOS technology. Standalone power is a crucial parameter of any L2 cache of Traditional Memory Hierarchy. As per the design, it should be capable of having less leakage in subthreshold region. That is if you are scaling down the access transistor of STT-MRAM bit cell, then there is prone to current between the source terminal and the drain terminal of the access transistor.

3.1.1. Disadvantages to use MOS based Access Transistor

Subthreshold Leakage, Gate-Dielectric Leakage, SCE (Short Channel Effect), DIBL (Drain Induced Barrier Lowering) of a transistor is limited to scale down the size of any transistor. Alternate device is FinFET technology.

3.1.2. Advantages of FinFET technology over MOS Transistor

It reduces the effects of all disadvantages of MOS scale down and also having Higher ON current, Denser Layout than the transistor

3.1.3. Comparison of FinFET based cell with existing models

In Literature there are two existing designs working with FinFET based STT-MRAM bit cell for better performance and to reduce the access time. In [29] they discuss the read failure and write failure aspects of the design. They used ASU-PTM model with 32nm technology node. In [30] they concentrated on write current, cell area and sub array performance parameters. Our design discusses cell area using CACTI 6.5 model. Our design concentrates on the performance parameters like delay, Leakage and power consumption of bit cell with one FinFET and One MTJ based bit cell. Detailed comparison on what we are working is shown in Table 6.

3.2.FINFET BASED BIT CELL

STT-MRAM bit cell consists of two basic components, one is Magnetic Tunnel Junction (MTJ) and other is access Transistor. Access Transistor here is N-FinFET. Gate terminal is connected to Word Line. Source of the FinFET is connected to Source Line of Memory System. Drain terminal is connected to Pinned layer of MTJ and Fixed Layer terminal of MTJ is connected to Bit Line.

3.2.1. Writing Operation of bit Cell

Writing Logic Zeros into MTJ mainly depends on Bit Line and Source Line values. Bit Line is given Bit line(BL) is Given with high value and source line (SL) is given with Low value to write logic 0 into MTJ (Parallel) provided Write Line is Activated. Bit line(BL) is given with

Low value and Source line(SL) is given with High value to write Logic 1 into MTJ (Anti-Parallel) provided Write Line is Activated. Figure 22 shows the FinFET based bit cell with its associated Lines that are connected to it.

Table 6: Comparison of Existing FinFET Technologies with our Design

Parameters	[29]	[30]	Our design
Technology node	32nm	32nm	7nm
Model	ASU-PTM	ASU-PTM with BSIM capacitance model	ASU-PTM
Read Failure	Yes		
Write failure	Yes		
Write current		Yes	
Cell Area		Yes	yes
Sub array performance		Yes	
Delay performance			Yes
Leakage power			Yes
Power Consumption			Yes

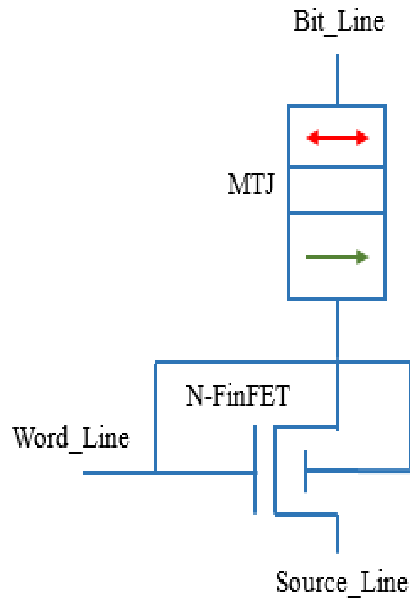


Figure 22: FinFET based STT-MRAM Bit Cell

3.2.2. Reading Operation of STT-MRAM bit cell

Sense amplifier plays a main role in sensing the data in any memory system. I am using error free sense amplifier which is modified version of the conventional sense amplifier. Figure

23 is the simulation of the bit cell sense from the sense amplifier connected to the bit cell provided the Word Line is activated.

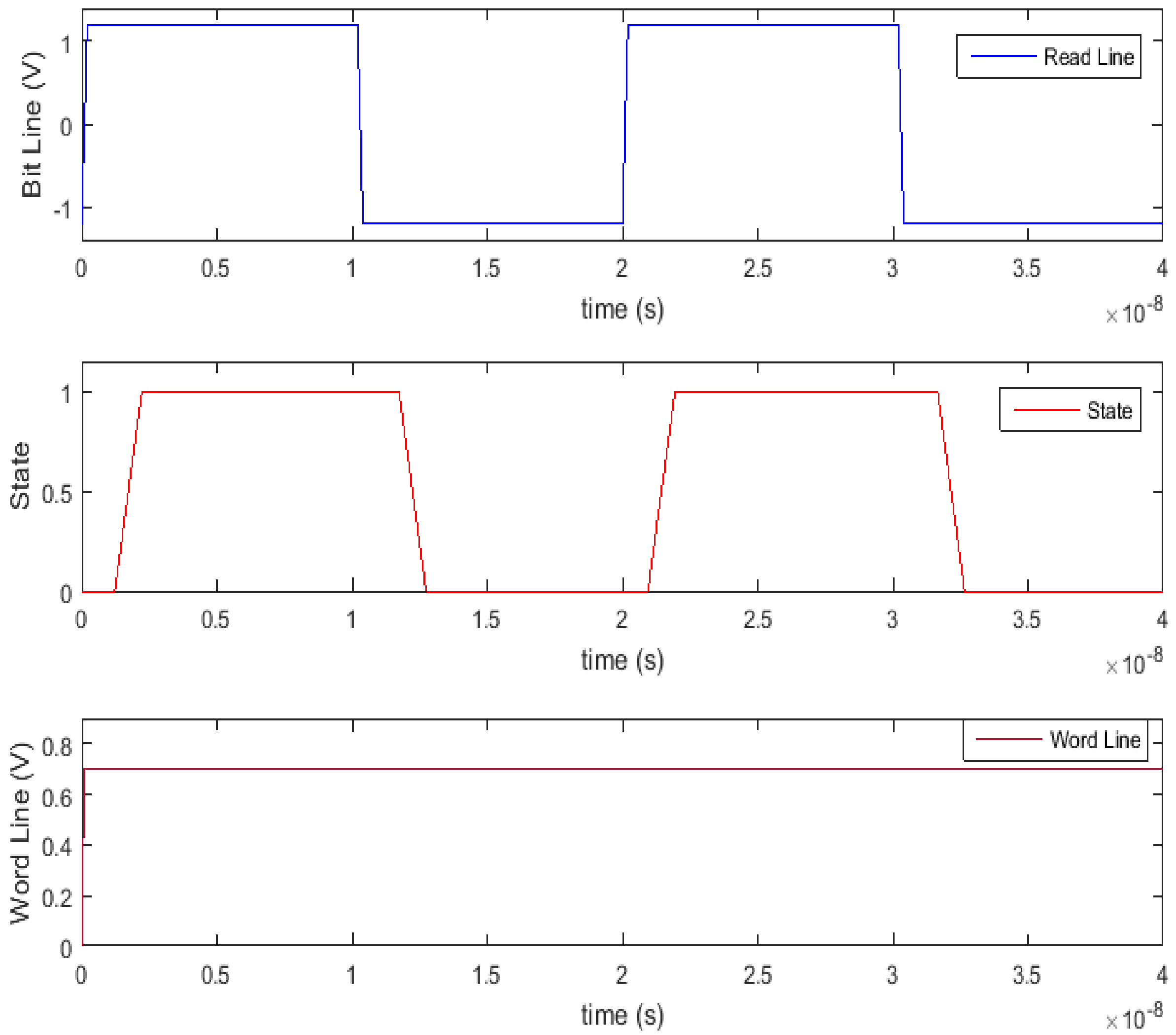


Figure 23: CIRCUIT simulation of STT-MRAM bit cell when an activating signal (WL=0.7V) is applied at the access transistor.

3.3. PERFORMANCE PARAMETERS OF FINFET BASED STT-MRAM BIT CELL SIMULATIONS

Performance parameters that we are discussing in this session is delay, power consumption, Leakage power utilization, Delay and power in PVT conditions. Temperature dependence and showing the thermal instability of the bit cell.

3.3.1. Delay Variation of FinFET based STT-MRAM bit cell. With respect to number of Fins of FinFET.

Delay of bit cell constitutes the access speed of the memory system that we need to take care of. We have to choose a bit cell which can have a less delay value. We can change the delay value with the variation of number of Fins. As we can change current by varying number of Fins which is used to get sufficient amount of current to MTJ to store respective logic value into it. Figure 24 is the simulation of Delay parameter in terms of number of fins of the FinFET. When the number of fins on FinFET increases, delay of the bit cell also increases. Here we can observe delay of bit cell is almost constant after certain number of fins. We choose the minimum number of fins where delay is constant for rest of the simulation of FinFET based STT-MRAM bit cell. Points are extracted from ADE XL Simulator of cadence and plotted accordingly.

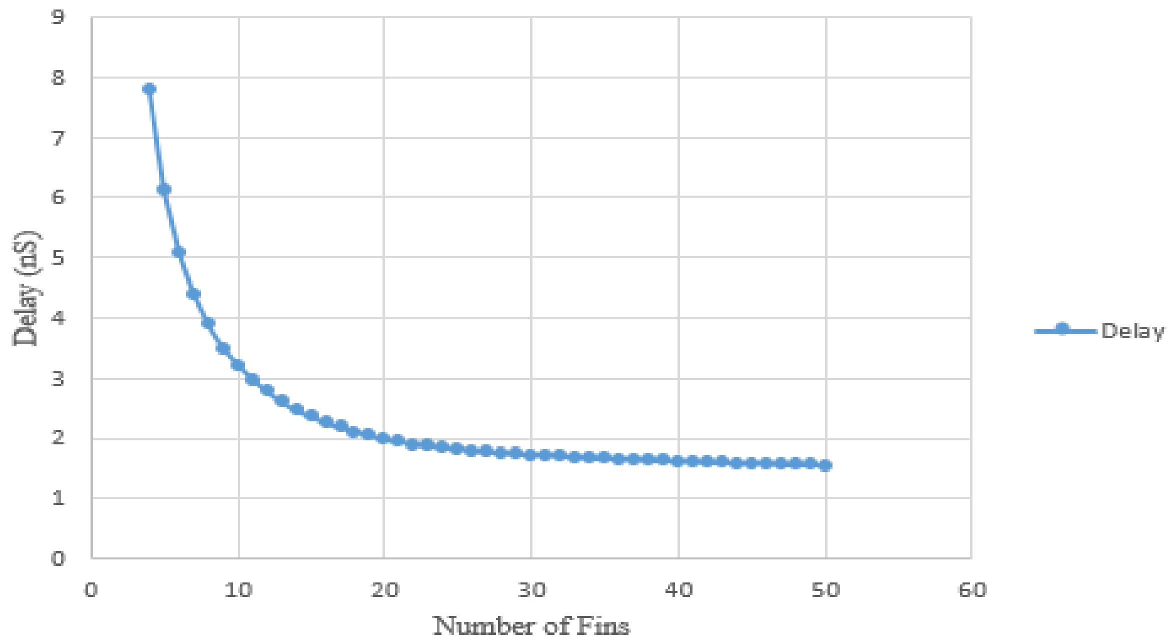


Figure 24: Delay Variation of FinFET based STT-MRAM bit cell with respect to number of Fins of FinFET

3.3.2. Power consumption with respect toNumber of Fins of FinFET based STT-MRAM bit cell

Power of FinFET based STT-MRAM bit cell depends on the current in the bit cell. As we know the current changes when the number of fins of a FinFET varies. Power consumption samples are extracted in ADEXL simulator of Cadence and plotted accordingly. Figure 25 gives the power consumption variation with respect to number of Fins of FinFET technology of FinFET based STT- MRAM bit cell. As we observed that the number of fins increases, power consumption also increases. Here graphs indicate that power consumption is linearly increasing up to 30 fins and then gradually increases after 30 fins of FinFET. This analysis is done to find the optimized value for number of fins based on low power consumption. This analysis is done while writing a logic value in to it. Power consumed by bit cell is calculated accordingly.

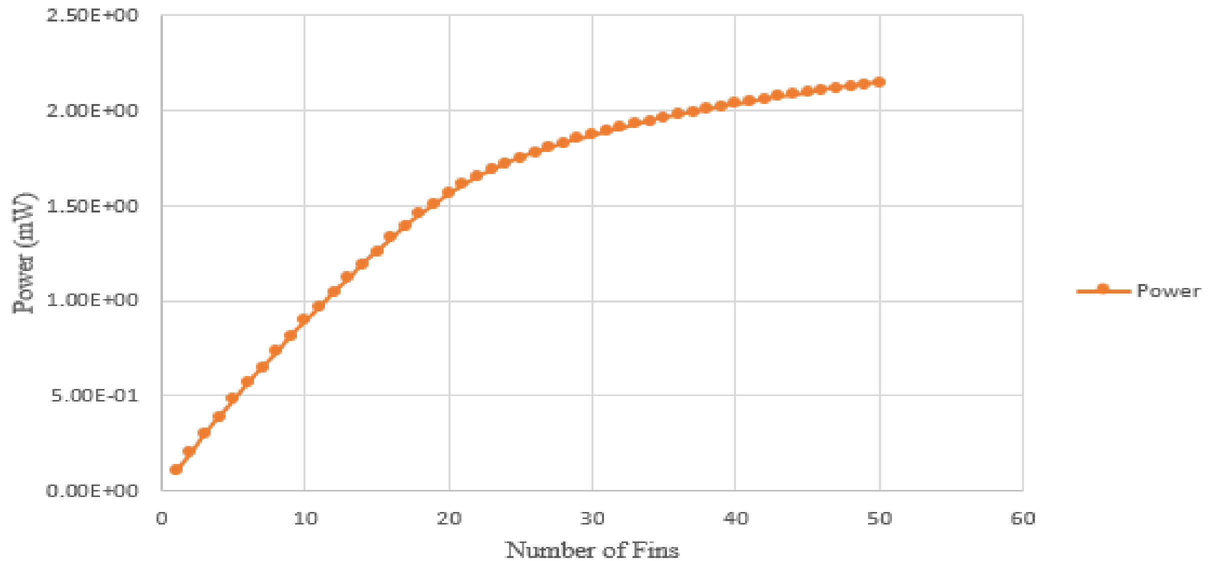


Figure 25: Power consumption variation of FinFET based STT-MRAM bit cell with respect to number of Fins of FinFET

3.3.3. Leakage Power variation in FinFET based STT-MRAM bit cell with respect to number of Fins of FinFET

As Leakage power is atmost important to know the standalone power utilization of any bit cell as this is the basic building block of memory unit. The analysis is done and points are extracted from ADE XL simulator of cadence and plotted graph. Figure 26 represents the simulation of Leakage power consumption of bit cell with respect to the number of fins of FinFET. There is abnormal behavior that we can observe at 20 fins of FinFET. At 30 fins it is observed that with less leakage power and constant for rest profile. So we choose 30 fins for FinFET to do all the simulations of logic value storage in memory system. This simulation is done with Low performance FinFET device model of ASU PTM model with 7nm technology node.

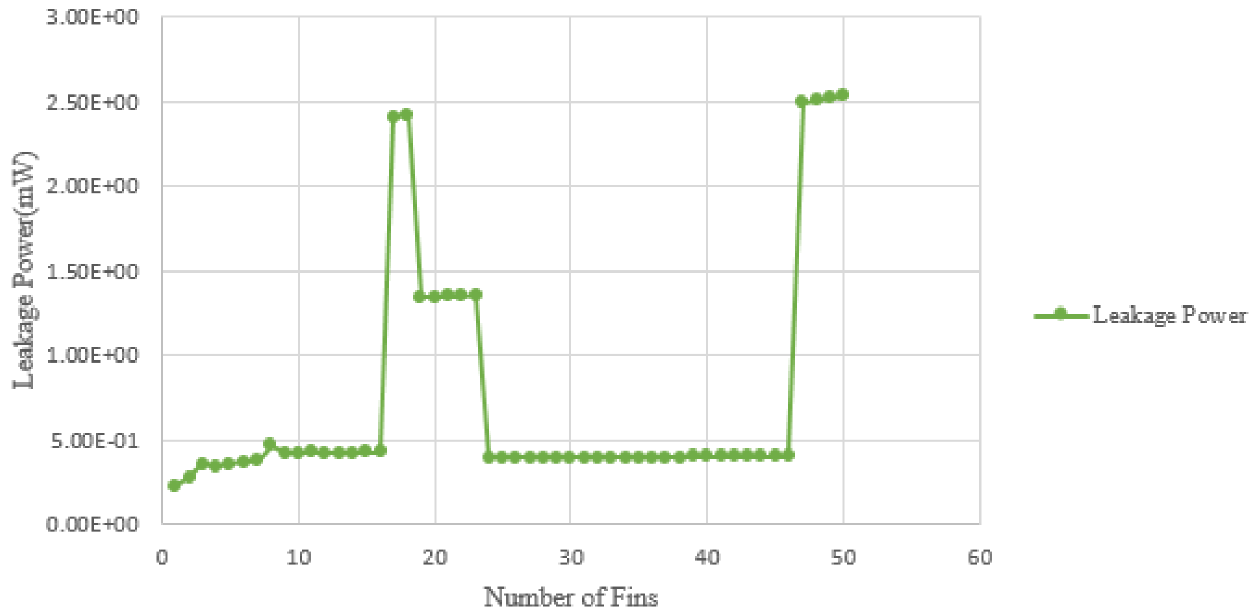


Figure 26: Leakage Power Variation of FinFET based STT-MRAM bit cell with respect to number of Fins of FinFET

3.3.4. Delay variation with respect to process Technology of FinFET

It is necessary to do analysis of delay variation of FinFET based STT-MRAM bit cell with all the technology nodes. Figure 27 represents the simulation of the delay of bit cell with respect to the technology node variation. Blue line represents low performance device of ASU-PTM model of FinFET and orange solid line represents the low performance device of ASU-PTM model of FinFET. Dotted line represents the optimal behavior of delay variation. We observed that the technology node decreases, delay also decreases respectively. This is the state of technology node variation with delay of FinFET based STT-MRAM bit cell. Points are extracted from ADEXL simulator in cadence and plotted graph.

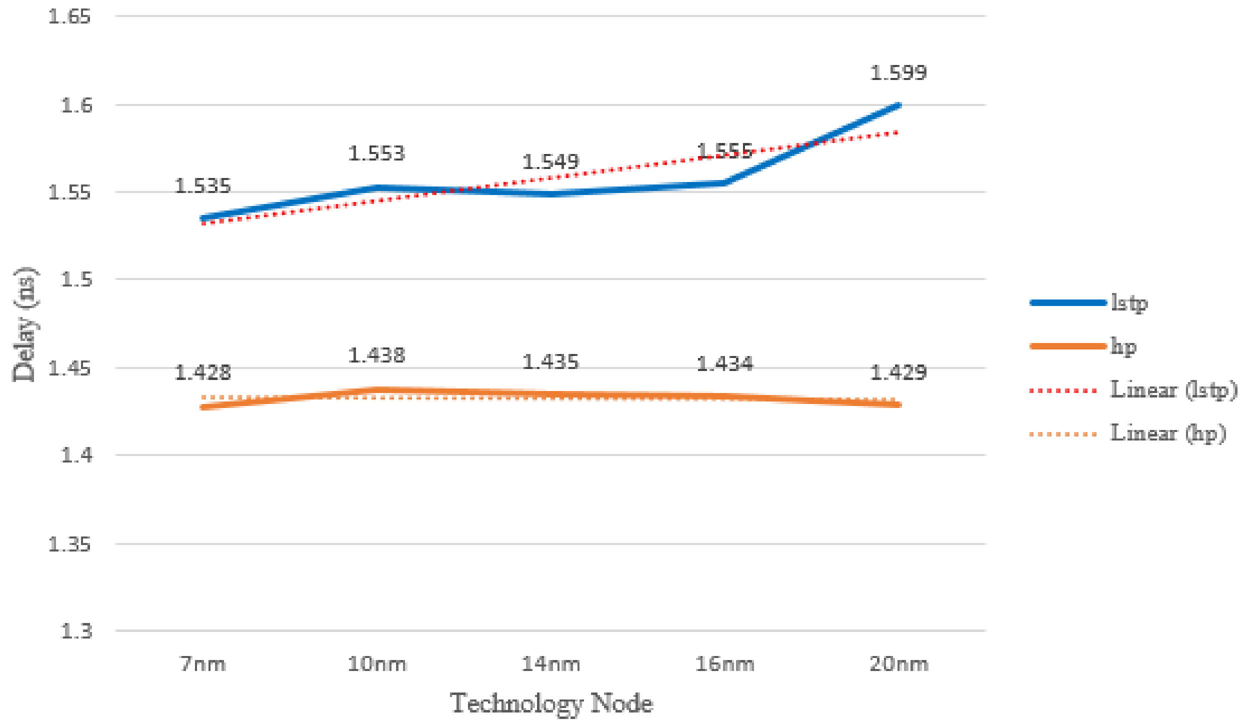


Figure 27: Delay with respect to FinFET Technology Node

3.3.5. Delay of bit cell variation with respect to Temperature Dependence at different voltage levels of high performance model of FinFET.

Our design should work at any temperature, so simulation of delay with respect to temperature is more important to do delay variation. Figure 28 represents the simulation of Delay of high performance FinFET based STT-MRAM bit cell with respect to the temperature. It is observed that at different voltages, delay is varying with respect to temperature. As we know that at high temperatures In-Plane Magnetic Anisotropy based MTJ have thermal instability and decreases its delay. As the temperature increases, electrons in free layer takes less time to demagnetize and rotate the orientation of the electrons accordingly. So delay of the FinFET based STT-MRAM bit cell decreases accordingly. Model is taken from ASU-PTM in 7nm technology node and with high performance. Points are extracted from cadence ADEXL

simulator and plotted accordingly. Blue line indicated the profile at 0.5 V. Orange, gray and yellow lines represents the profile at 0.7V, 0.9V and 1V respectively. There is no much variation in all the profiles from 0.7V to 1V voltage supply to FinFET of bit cell. Temperature that we are doing simulations are at -40 ºC, 27 ºC and 125 ºC.

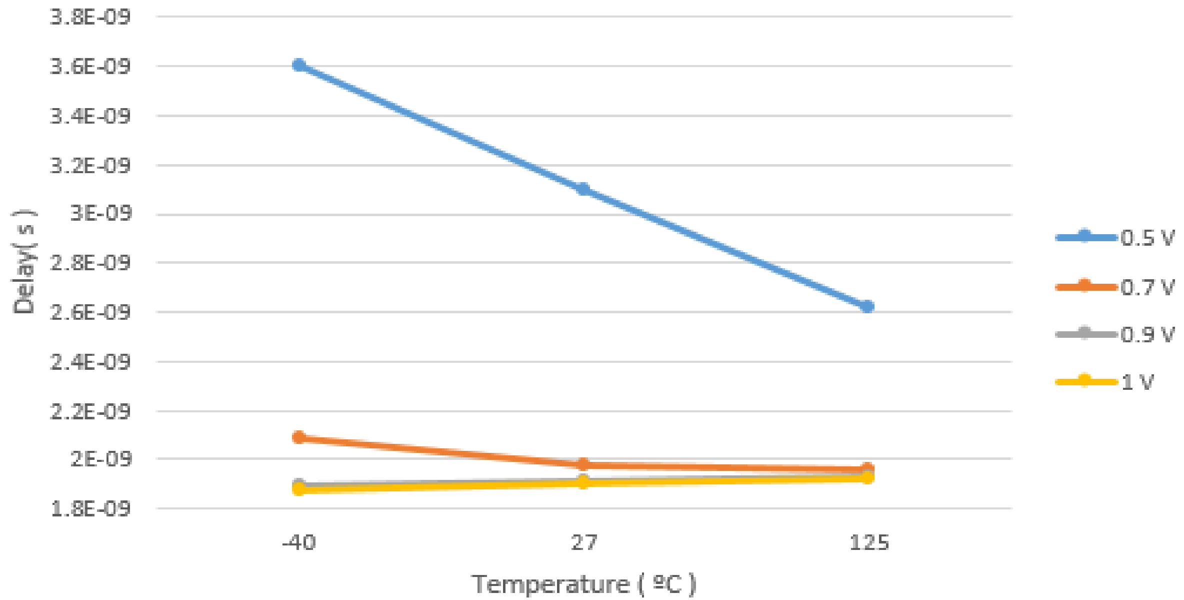


Figure 28: Temperature Dependence with respective to Delay at different Voltage levels with high performance model of FinFET

3.3.6. Delay of bit cell variation with respect to Temperature Dependence at different voltage levels of Low performance model of FinFET.

Our design should work at any temperature, so simulation of delay with respect to temperature is more important to do delay variation. Figure 29 represents the simulation of Delay of Low performance FinFET based STT-MRAM bit cell with respect to the temperature. It is observed that at different voltages, delay is varying with respect to temperature. As we know that at high temperatures In-Plane Magnetic Anisotropy based MTJ have thermal instability and decreases its delay. As the temperature increases, electrons in free layer takes less time to

demagnetize and rotate the orientation of the electrons accordingly. So delay of the FinFET based STT-MRAM bit cell decreases accordingly. 0.5V profile in graph shows the instability behavior of MTJ. Model is taken from ASU-PTM in 7nm technology node and with high performance. Points are extracted from cadence ADEXL simulator and plotted accordingly. Blue line indicated the profile at 0.5 V. Orange, gray and yellow lines represents the profile at 0.7V, 0.9V and 1V respectively. There is no much variation in all the profiles from 0.7V to 1V voltage supply to FinFET of bit cell. Temperature that we are doing simulations are at -40 ºC, 27 ºC and 125 ºC.

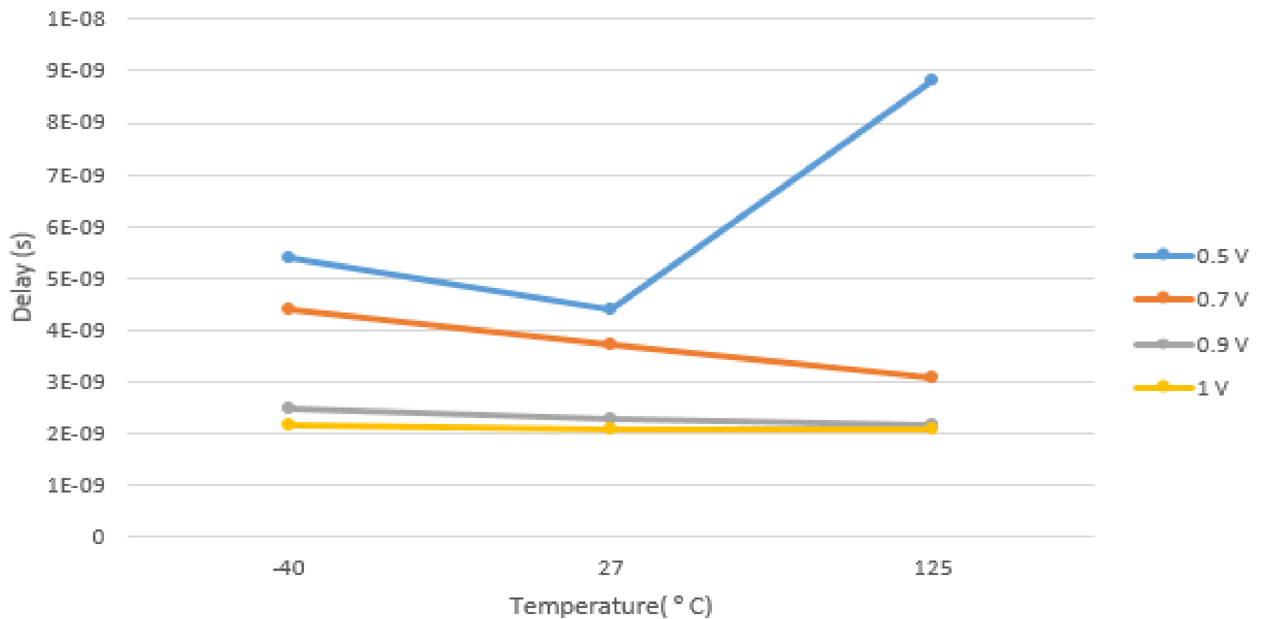


Figure 29: Temperature Dependence with respective to Delay at different Voltage levels with low performance model

3.3.7. Delay of bit cell in different Process Voltage Temperature conditions

Overall Delay performance of FinFET based STT-MRAM bit cell in PVT conditions is plotted in and shown variation in Figure 30. This profile is simulated using ADEXL simulator in cadence. Model of FinFET is taken from ASU-PTM models in 7nm technology node. It is

observed that the delay is decreased gradually as the voltage increased. Also delay decreases as the temperature increases. Delay decrease as the performance model is increasing(High Performance),

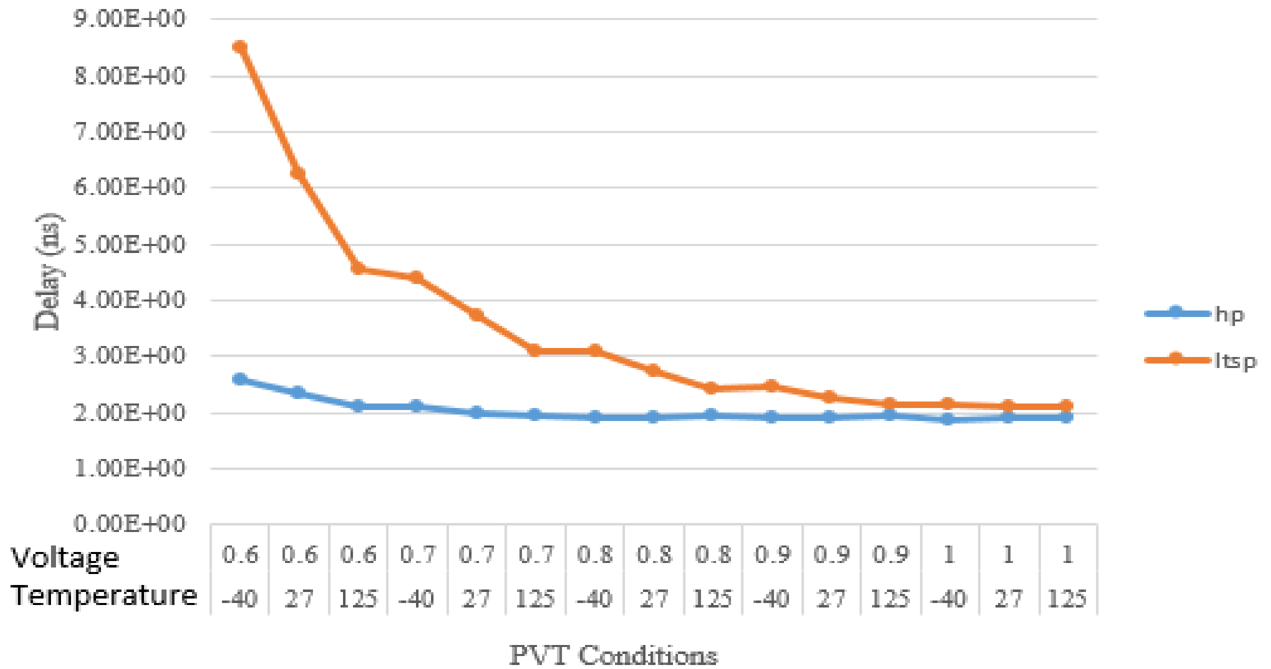


Figure 30: Delay of STT-MRAM with FinFET Access Transistor in PVT conditions

3.3.8. Power Utilized by STT-MRAM in different PVT conditions

Overall power consumption of FinFET based STT-MRAM bit cell in PVT conditions is plotted in and shown variation in Figure 31. This profile is simulated using ADEXL simulator in cadence. Model of FinFET is taken from ASU-PTM models in 7nm technology node. It is observed that the power is increasing gradually as the voltage increased. Also power consumption increases as the temperature increases. Power consumption decrease as the performance model is decreasing.

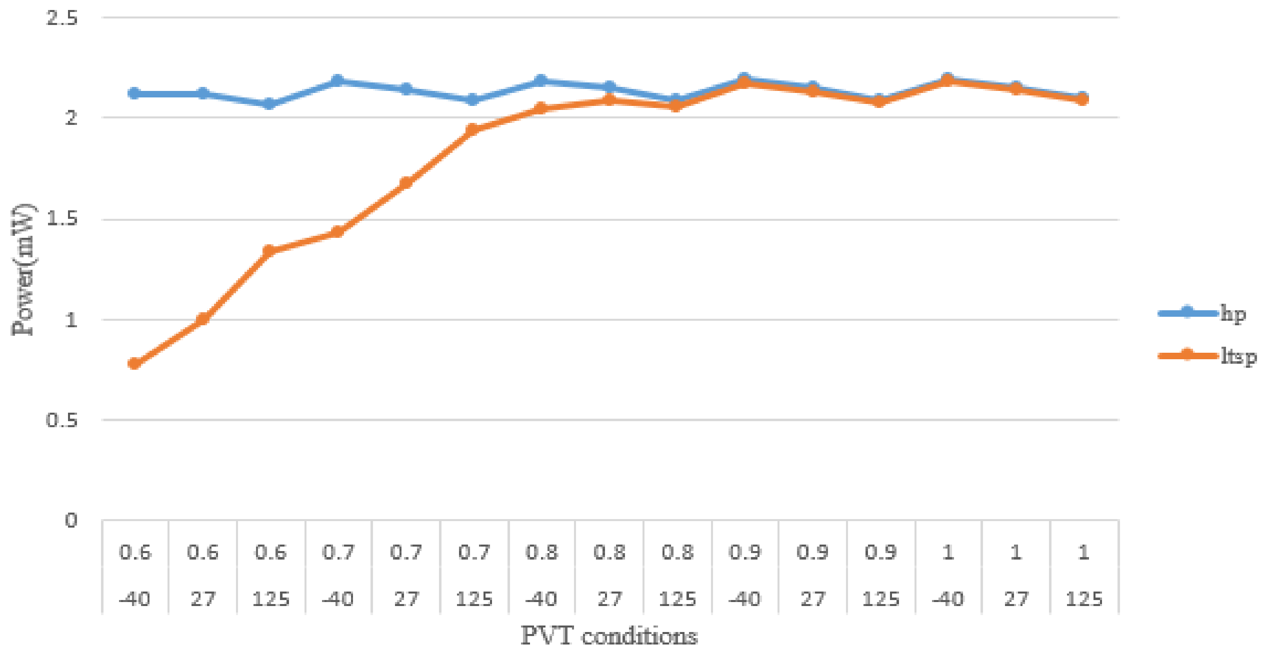


Figure 31: Power Utilized by STT-MRAM in different PVT conditions

3.3.9. Leakage Power Variation of FinFET based STT-MRAM bit cell with respect to temperature and voltage change

As per the standalone power consumption, leakage power plays an important role and simulation is done with the variation of a leakage power consumption in different PVT conditions. Points are extracted from ADEXL simulator of cadence and plotted accordingly. High performance and low performance models of FinFET is using and voltages from 0.6V to 1V. As the temperature increases provided voltage constant then leakage power increases. Leakage power increases for high performance devices when compared to low performance device model. There is abnormal behavior on leakage power when temperature is constant and voltage varies. Figure 32 shows the simulation of STT-MRAM bit cell for leakage power in PVT Conditions. Blue line represents high performance device profile and orange line represents the low performance device model simulation. FinFET model is taken from ASU-PTM in 7nm technology node.

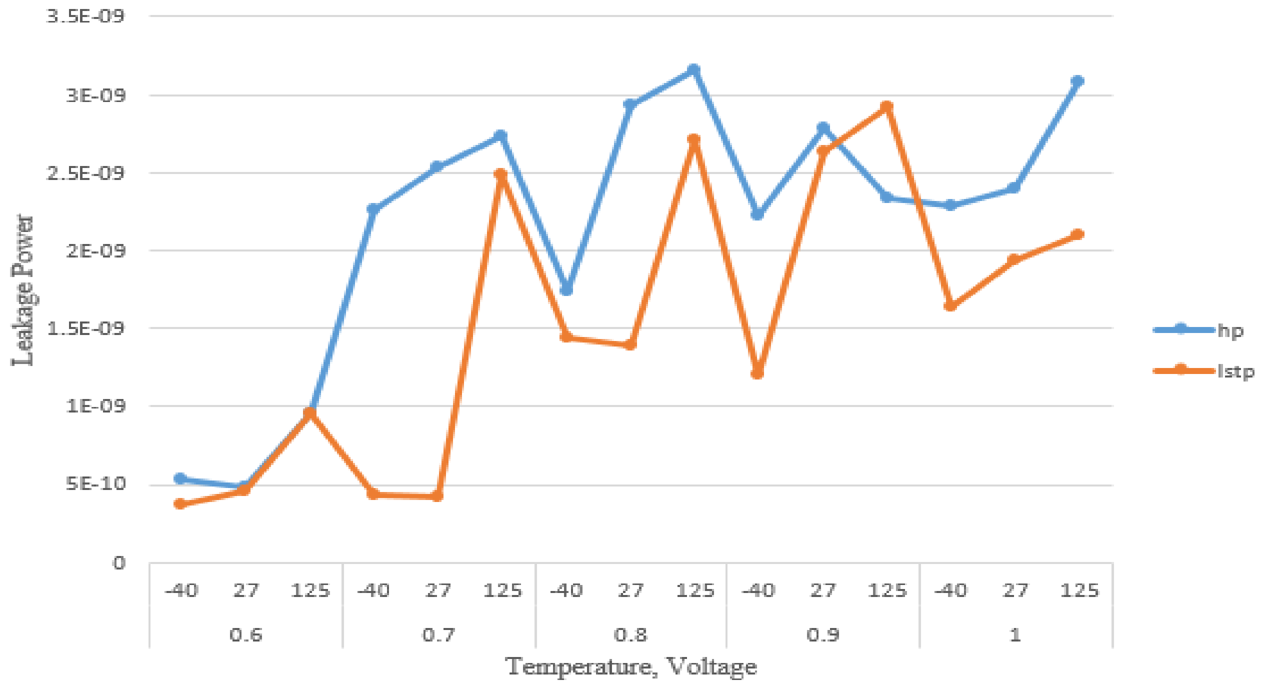


Figure 32:Leakage Power Variation of FinFET based STT-MRAM bit cell with respect to temperature and voltage change

3.3.10. Delay variation in PVT conditions with the variation of number of fins of FinFET of a STT-MRAM bit cell.

Figure 33 represents the simulation of STT-MRAM bit cell delay variation with respect to PVT Conditions along with the variation of number of Fins of FinFET of STT-MRAM bit cell. The variation of Fins is analyzed from 20 Fins to 50 Fins. FinFET model we are using are high performance and low performance. Temperature variation is -40 ºC to 125 ºC. Voltage variation is 0.6 V to 1V. Points are extracted from ADEXL simulator of cadence and plotted accordingly. We can observe that the delay decreases as the temperature increase as we know that the demagnetization of electrons takes in little time at high temperature that results in less delay of the bit cell. Delay decreases as number of Fins of FinFET increases. Delay decreases as

we vary the model from high performance to low performance model with same attributes. Models are taken from ASU-PTM with 7nm technology node.

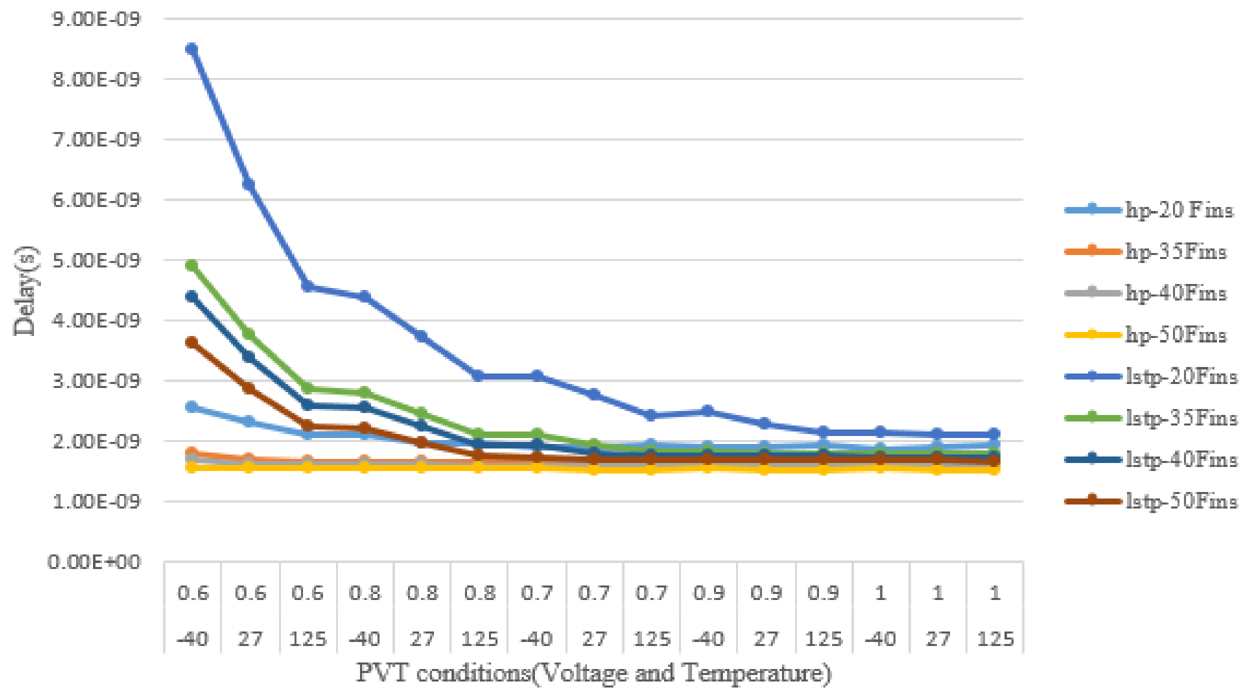


Figure 33: Delay Variation with respect to Voltage and Temperature Variation for High and Low performance devices for different number of Fins

3.4. CONCLUSION AND FUTURE WORK

We simulated the performance characteristics of FinFET based STT-MRAM bit cell i.e., delay variation, power consumption, Leakage power analysis. This Simulations are also done in PVT conditions to optimized the design to the desired values. Later we need to concentrate on the architectural issues of the FinFET based STT-MRAM based bit cell memory system design.

CHAPTER 4

LOGIC-IN-MEMORY USING CNT-FET BASED STT-MRAM BIT CELL AND OPTIMIZATION

The advantages of CNTFET over MOSFET is as follows. The effect of temperature on threshold voltage of CNTFET is negligibly small. The high threshold voltage can be achieved at low chiral vector pair. The threshold voltage increases with decreasing channel length in CNTFET devices, this is quite contrary to the well-known short channel effect. At below 10 nm channel length the threshold voltage is increased rapidly in case of CNTFET device whereas in case of MOSFET device the threshold voltage decreases drastically below 10 nm channel length. The CNTFET devices are advantageous over MOSFETs due to their reduced quantum capacitance, as the value of quantum capacitance is an increasing issue in MOSFETs that leads to an increased propagation delay and hence leads to performance degradation.

4.1.PROPOSED BIT CELL

As per the conventional design there is only one access transistor in logic bit cell. When we are designing CNTFET based STT-MRAM bit cell using conventional bit cell, CNTFET doesn't provide sufficient amount of energy to store a logic value into MTJ. But to use an advantage of CNTFET and used to store the logic value it is necessary to see an alternative. There is mechanism keeping CNTFETS in parallel and can provide a sufficient amount of energy into MTJ to store a logic value into it. So here is a proposed bit cell using CNTFET access transistor which have an additional advantage over the conventional STT-MRAM bit cell. Figure 34 represents the bit cell of STT-MRAM where CNTFET is access transistor.

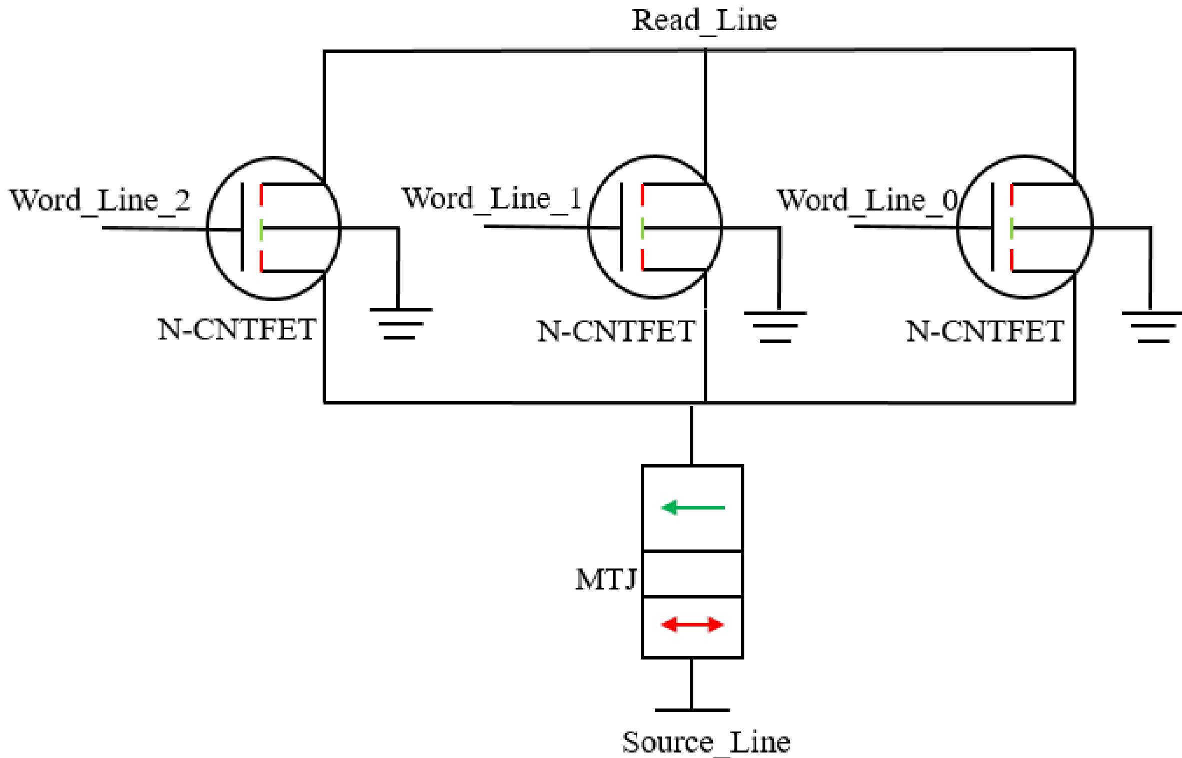


Figure 34: CNTFET access Transistor based STT-MRAM bit cell.

4.2.WRITING OPERATION OF CNTFET BASED STT-MRAM BIT CELL.

In order to write 1, Read_Line should be given as Low Voltage, Source_Line is given with High Voltage and Write_Line [0:2] should be given with 0.4 V that is MTJ free layer is Antiparallel with Fixed Layer. In order to write 0, Read_Line should be given as High Voltage, Source_Line is given with Low Voltage and Write_Line [0:2] should be given with 0.4 V that is MTJ Free Layer is Parallel with Fixed Layer.

4.3.READING OPERATION OF CNTFET BASED STT-MRAM BIT CELL.

Less than the operated value is given to Read_Line and connected to conventional sense amplifier and give the word line [0:2] as high value and then the sense amplifier gives the logic stored in the MTJ.

4.4.SIMULATION OF BIT CELL.

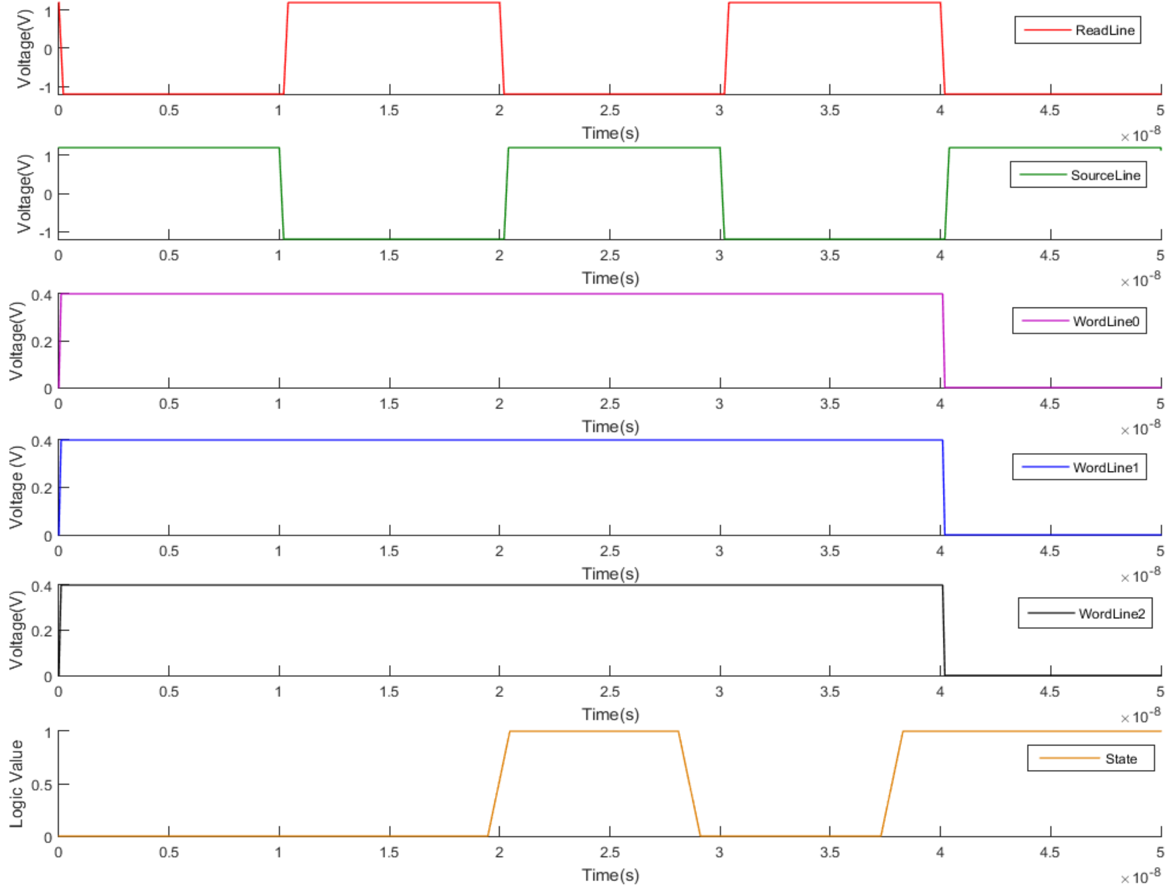


Figure 35: Simulation of CNTFET based STT-MRAM bit cell.

Simulation is done in cadence ADE environment in normal corner with 32nm channel length. There is more delay than the FinFET model but there is advantage of Power utilization and area consideration. FinFET uses 30 Fins as nominal which is more area than CNTFET. When their word line is inactive i.e., Word_Line [0:2] has low value then MTJ contains the previous value that can be observed at 38ns in State signal beside CNTFET utilizes only 0.4 V to Switch-ON but FinFET utilizes 0.7 V. **Figure 35** represents the cadence simulation of STT-MRAM bit cell to store the logic value into MTJ.

4.5.DELAY PERFORMANCE PARAMETER SIMULATION

Delay performance is simulated in cadence ADEXL Simulator and points are extracted and plotted accordingly. Asper the simulation it is observed that the delay is abnormal until the length of channel is 32nm and there after it is constant and there is less variation. This analysis is done to choose the channel length accordingly.

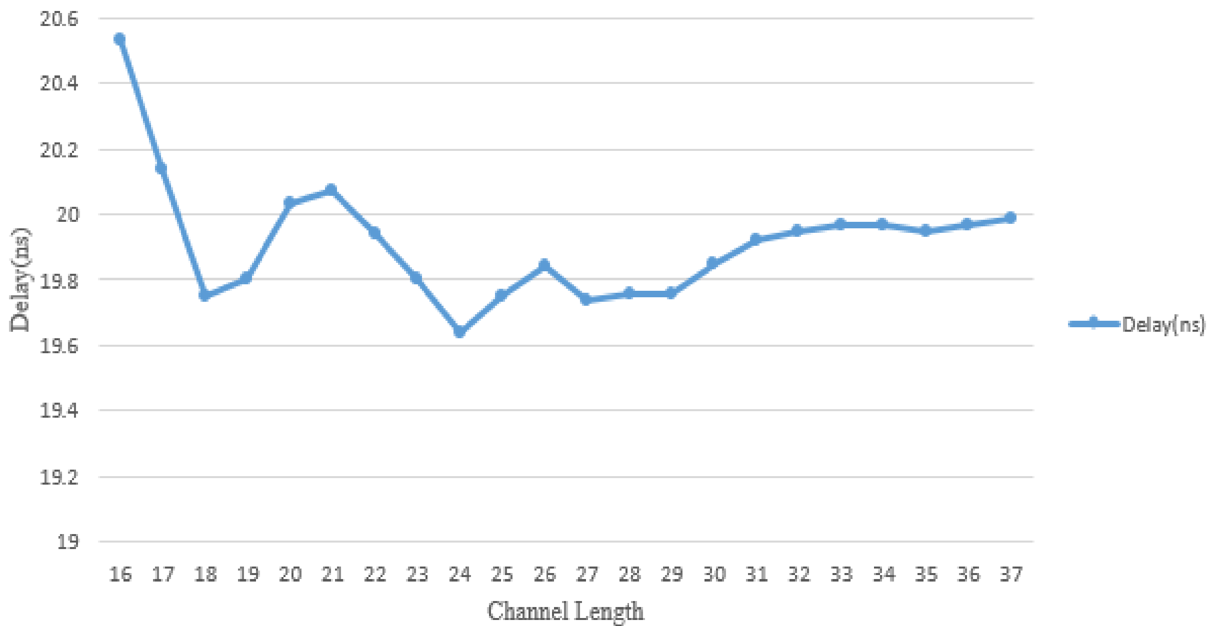


Figure 36: Delay variation of STT-MRAM bit cell.

4.6.ADVANTAGES AND DISADVANTAGES OF CNTFET BASED STT- MRAM BIT CELL.

Logic in Memory, as this bit cell consists of three access transistor, it is capable of storing more logic values and can be store according to the logic that we did in the bit cell. The demonstrated bit cell can be used as AND gate and can be used to store 8 logic values into it. Area is less when compared to FinFET or planar NMOS based bit cell as due to its nanoscale. It

uses only 0.4 V in order to activate the access transistor to store the logic value into the MTJ. Disadvantage is its ACCESS time.

4.7.CONCLUSION AND FUTURE WORK

Bit cell using CNTFET s demonstrated and stated its advantages and disadvantages. We need to do more analysis to integrate the bit cell in Memory system.

CHAPTER 5

ERROR FREE SENSE AMPLIFIER DESIGN FOR STT-MRAM NONVOLATILE MEMORY

The spin transfer torque magnetic random access (STT-MRAM) is suitable for embedded memories and also for the second level cache memory in the mobile CPU's. The most capable NVM component is STT-MRAM, which enhances the performance by 3.3 nS access time. It has strong radiation hardness, higher integrity and maximum endurance compared to SRAM. The power consumption of STT-MRAM is decreased by an order of magnitude by reducing the writing current. In this article, a new error free sense amplifier circuit is proposed. The detail analysis of the sense amplifier circuit is provided here. Finally, the performance of the proposed the sense amplifier is compared with existing sense amplifiers.

Index Terms: Clamped BL sense amplifier, Fore-Placed sense amplifier, MTJ

5.1.INTRODUCTION

Magnetic Random Access Memory (MRAM) is an alternative to SRAM for the Cache memory design because of its non-volatile nature. The access speed of single MRAM bit cell is 2-10 nS. While 30 ns access speed is achieved for the on-chip application. Recent researches in the spintronic are disclosing a diversity of magnetic memory devices, which have the non-volatility (NV). STT-MRAM has couple of advantages i.e. non-volatility, fast read speed and write speed, high retention time, unlimited endurance, and compatible with CMOS.

5.1.1. MTJ operation

Instead of using the electric charge to carry the data, the magnetic storage phenomenon is used in the magnetic tunneling junction (MTJ) [1]. Figure 37 shows the mode of operation of

MTJ, which has three layers. The electron spin of the pinned or fixed layer (e.g. Fe, Co, CoFeB) doesn't change. But the electron spin of the free magnetic layer (e.g. Fe, Co, CoFeB) changes depending on the applied voltage. The free layer is responsible for the spin polarized current by offering a resistance. Spin Polarized current is formed due to the change of the direction of electrons in the free layer in accordance with the pinned layer. The thin dielectric tunnel barrier (i.e. MgO) is used as an insulation. MTJ offers low and high resistances which define the parallel and antiparallel states of STT-MRAM [1].

In the writing cycle, MTJ dissipates less energy because it uses the electron spin direction property to store a data. While, conventional memories i.e. SRAM, DRAM, Flash use the electron momentum property to store a data. Therefore, the electron spin based memory consumes less power than the electron momentum based memory. To achieve the low hysteresis loop, a ferromagnetic material with low coericivity is used as the free layer [4].

5.1.2. Single bit STT-MRAM

Figure 38 shows the single bit cell STT-MRAM including a MTJ and an access transistor. It is anticipated that the direction of electrons changes according to the current generation because of the spinning. The scalability and less power consumption are benefits of STT-MRAM [8]. The switching in the data storage layer occurs through the spin polarized current with the spin transfer torque (STT) across the junction. However, the scalability issue is resolved though reducing the writing current value. In the large scale memory design, the tunneling oxide gets damaged because of the high current density. For computation, STT-MRAM requires a high writing energy to establish a flip flop device [8].

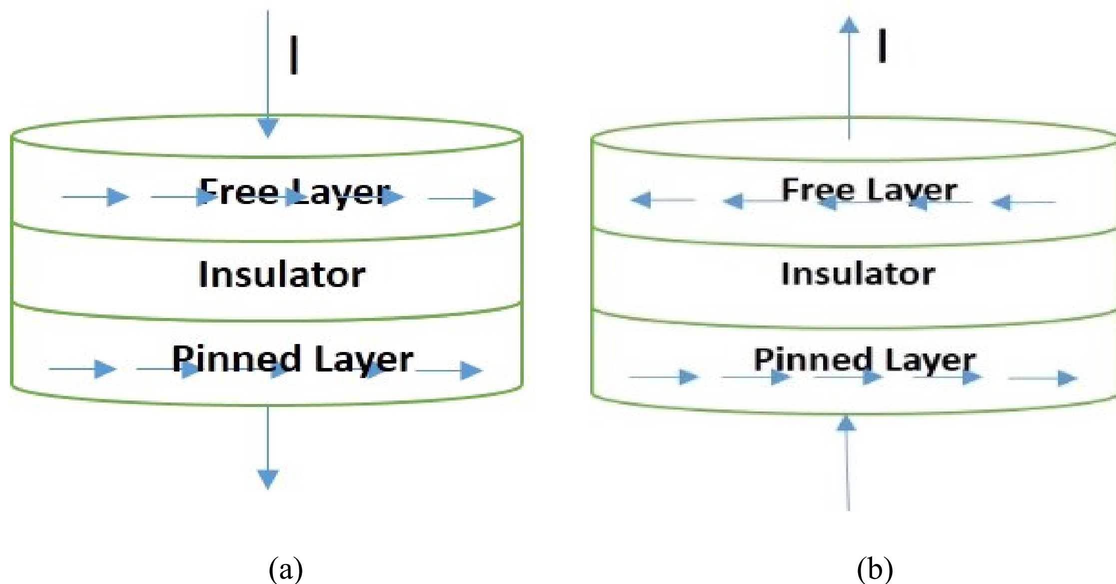


Figure 37: Spin orientation of electrons both in the pinned and free layers, which represents the mode of operation and bit stored in MTJ (a) parallel mode of MTJ (bit "1") (b) anti parallel mode of MTJ (bit "0").

5.1.3. Sense amplifier

To read the state of MTJ a sense amplifier is required. The sense amplifier should have high sense margin, reliability and simple implementation. It senses the current on the pinned layer and amplifies to the desired level.

The state of art of the current STT-MRAM sense amplifier are summarized in Table 7. The sensing circuit of MRAM is very crucial. There are several sense amplifiers are reported to read MRAM. The Clamped bit-line sense amplifier (BLSA) requires large difference in current value to compare but the delay is more [25]. The power consumption of The Current-mode sense amplifier is lower than the clamped BLSA [26]. The Fore-placed sense amplifier requires more transistors for normal operation [27].

Table 7: Comparison of the existing sense amplifiers of STT-MRAMs.

Sense amplifier	Power Consumption (mW)	No. of transistors	Reliability	Technolog y Feature (nm)	Parallel Reading and writing
Clamped BLSA [25]	0.2006	10	Medium	180	No
Current Mode sense amplifier [26]	0.1756	8	High	180	No
Fore-placed sense amplifier [27]	Low	9	High	180	No

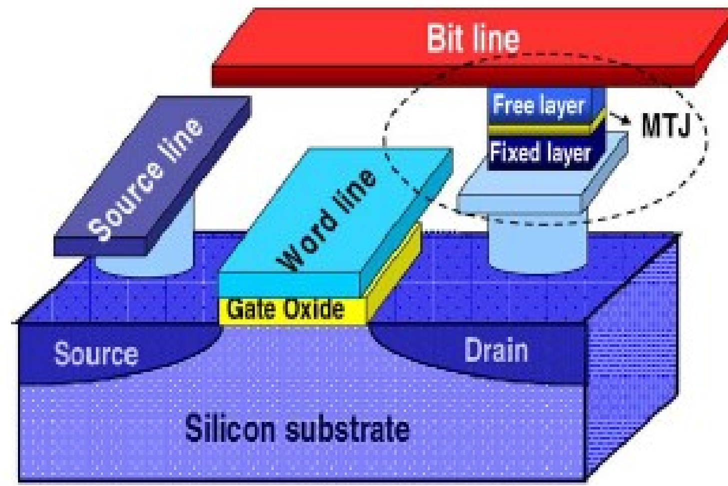
5.2. EXISTING DESIGNS

Figure 39 shows the sense amplifier, which do not have the activation signal and Figure 40 shows the corresponding output waveform. Figure 41 show the sense amplifier, which has the activation signal and Figure 42 shows the corresponding output waveform. Figure 43 explains the new proposed sensing amplifier for STT-MRAM reading mechanism and Figure 44 shows the corresponding output waveform. The compact model of MTJ from [23] is used in this paper for simulations.

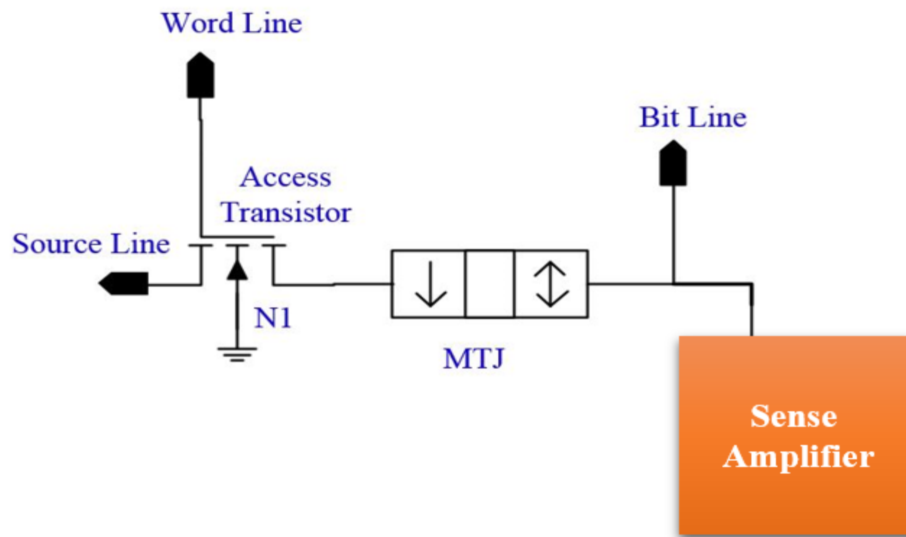
5.2.1. Precharge Sense Amplifier Without Activation Signal

Figure 39 shows the sense amplifier circuit with two back to back inverters which allows comparison between the reference current and MTJ current. There is an error in the output and sense margin is acceptable. The resistance of the reference MTJ is set to compare the equivalent resistance of the resistance of MTJ at the parallel and antiparallel state. This circuit is reliable but the initial state of the output shows wrong value because both Q_m and Q_m' are charged

to high through PMOS transistors of the pre-charge circuit. The supply voltage of the circuit Vdd=1.2 V. After pre-charging (PCL= 0 V) both output lines Qm and Qm’ will be 1.



(a)



(b)

Figure 38: STT-MRAM bit cell including a MTJ and an access transistor. (a) 3D model MRAM (sense amplifier is not shown) [1], (b) circuit representation of MRAM with the sense amplifier.

The reference MTJ is connected with 0V. Two precharge PMOS transistors increases Qm and Qm' pull up to Vdd and trigger the sense amplifier circuit. When PCL= 0V, P1 and P2 make the output lines to Vdd - Vth and reduce the sense margin. Still the sense margin is acceptable. The access transistor can be shared between the bit cell MTJ and reference cell MTJ. By this way the area is reduced without losing any performance.

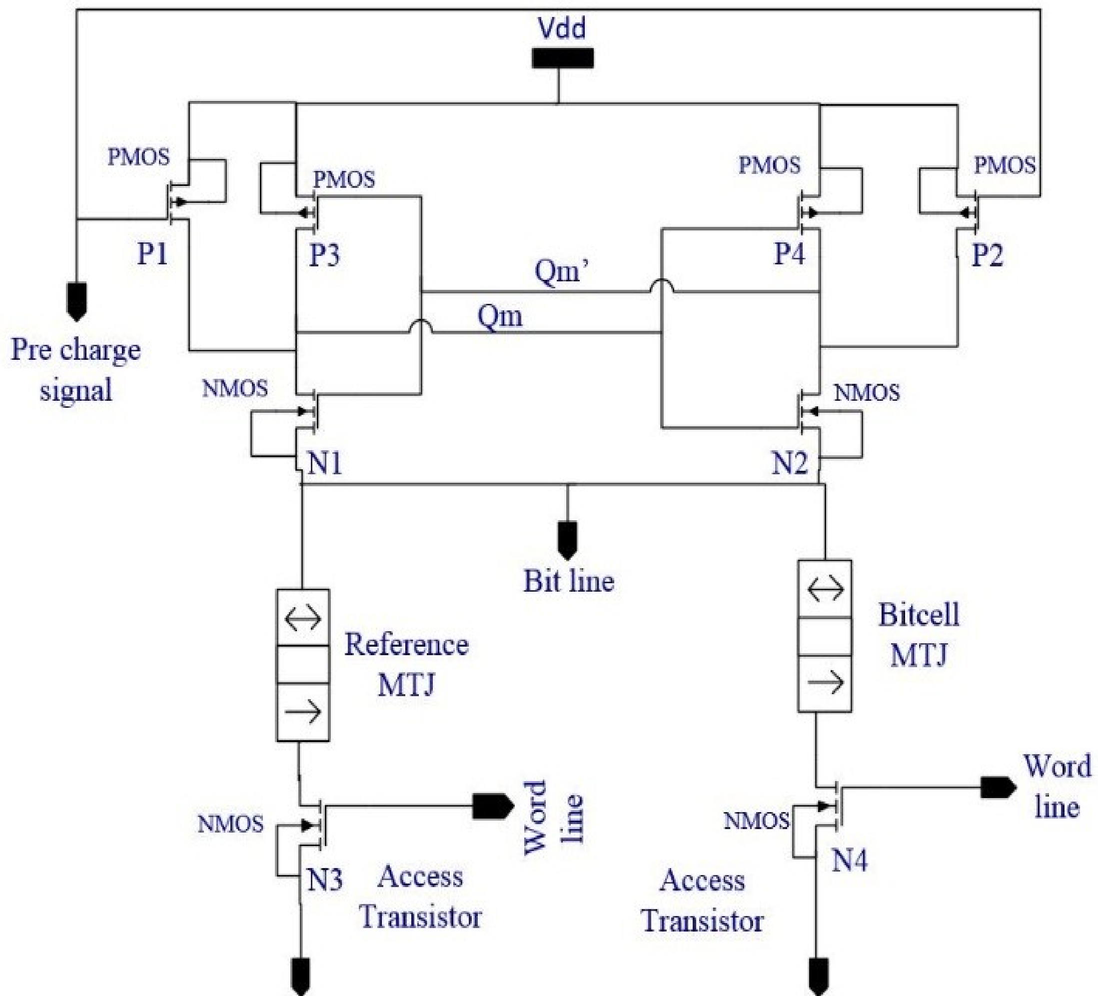


Figure 39: A precharge sense amplifier of STT-MRAM in 45 nm technology without the activating signal. This sense amplifier circuit allows low sense margin and the parallel read-write capability [24].

The back to back inverters is reliable because it's sense margin is higher than the capacitor and pass transistor logic sense amplifier. The sense margin of the back to back inverters is 1.194 V, which is close to the high logic level (1.2V). While the sense margins of the capacitor and pass transistor logic sense amplifiers are 0.0244 V and 0.1597 V respectively.

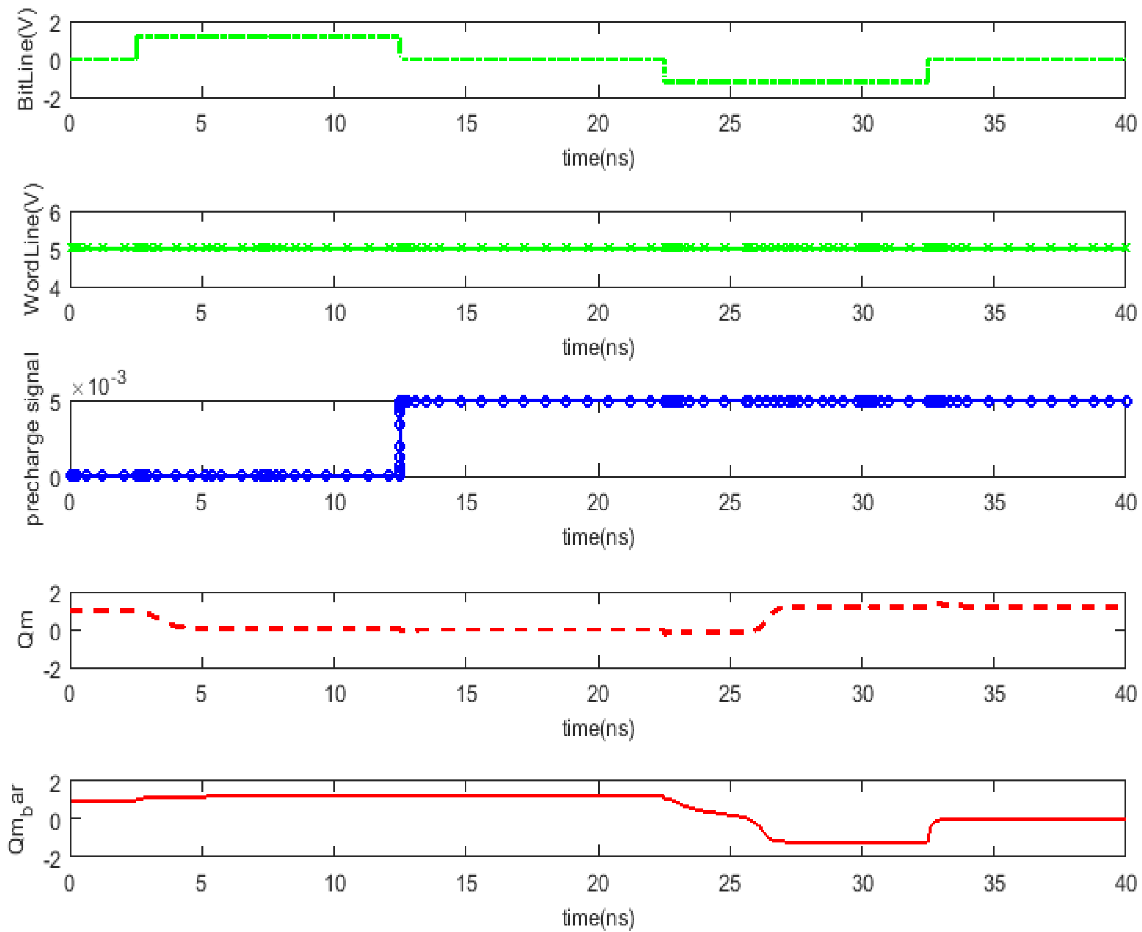


Figure 40: Output waveforms of pre-charge sense amplifier circuit of Figure 39.

Figure 40 shows the output waveforms of the precharge sense amplifier without any activation signal. Initially, PCL= 0V is applied, which activates the P1 and P2 and charges Qm and Qm' to +1.2 V as power supply with drop (vdd-vth) in it. Usually, PCL= 0 V for 1-2 nS. But

PCL= 0 V for 12 nS for better understanding. When PCL=1.2 V, P1 and P2 are turned off and disconnected from the sense amplifier. Although PCL= 0 V triggers the circuit, PCL=1.2 V starts the correct write. /read operation of STT-MRAM circuit. When, BL= +1.2 V, the state of MTJ changes from the parallel state to anti parallel state, which leads to Qm=0 and Qm'=1. While BL= -1.2 V, the state of MTJ changes from the anti-parallel state to parallel state writing, which leads to Qm=1 and Qm'=0. So, in the anti-parallel state, Qm=0 and Qm'=1 while in the parallel state writing, Qm=1 and Qm'=0. This circuit allows the read and write operation in parallel. The access transistor size (W/L) determines the sense margin of the circuit.

5.2.2. Pre-Charge Sense Amplifier by Using Activation Signal

Figure 41 shows the pre-charge sense amplifier circuit by using the activating signal, which separates the sense amplifier circuit and writing circuit. When RL is low, N3 and N4 transistors are off, then the sense amplifier is unable to read MTJ state but write operation is allowed. When RL is high, N3 and N4 transistors are on, then the sense amplifier reads MTJ state. The reference bit cell is modeled in such way that it's resistance is equal to the average resistance of the parallel and antiparallel state. The area is reduced by using only one access transistor, which is shared between the reference cell and bit cell. This circuit is more reliable than the capacitor and pass transistor logic and precharge sense amplifier without activation signal sense amplifiers. But the output Qm and Qm' at PCL= 0 V is erroneous.

Figure 42 represents output waveforms of the pre-charge sense amplifier, which utilizes the activation signal. The operation is similar to the the pre-charge sense amplifier.

5.3.PROPOSED SENSE AMPLIFIER

Figure 43 shows the proposed sense amplifier circuit, which initializes STT-MRAM correctly. Therefore, no error at the output with improved sense margin. when PCL=0, P3 and N3 are on, then Qm goes to high and Qm’ goes to low. An additional inverter is needed to activate N3, which replaces PMOS of the existing pre-charge sense amplifiers.

Figure 44 shows output waveforms of the proposed sense amplifier that is more reliable and easy to implement. The proposed sense amplifier allows both the simultaneous and separate write and read operation. So, control on the sense amplifier is more with reduced power consumption. When both RL and WL are high, the reading and writing operation are done simultaneously. Initially, Qm and Qm’ are at high and low respectively. When WL is activated, the output Qm’ holds the value according to BL input. When, BL= +1.2 V, the state of MTJ changes from the parallel state to anti parallel state, which leads to Qm=0 and Qm’=1. While BL= -1.2 V, the state of MTJ changes from the anti-parallel state to parallel state writing, which leads to Qm=1 and Qm’=0. So, in the anti-parallel state, Qm=0 and Qm’=1 while in the parallel state writing, Qm=1 and Qm’=0. Table 8 shows the comparison of the proposed sense amplifier of STT-MRAM with the existing sense amplifiers.

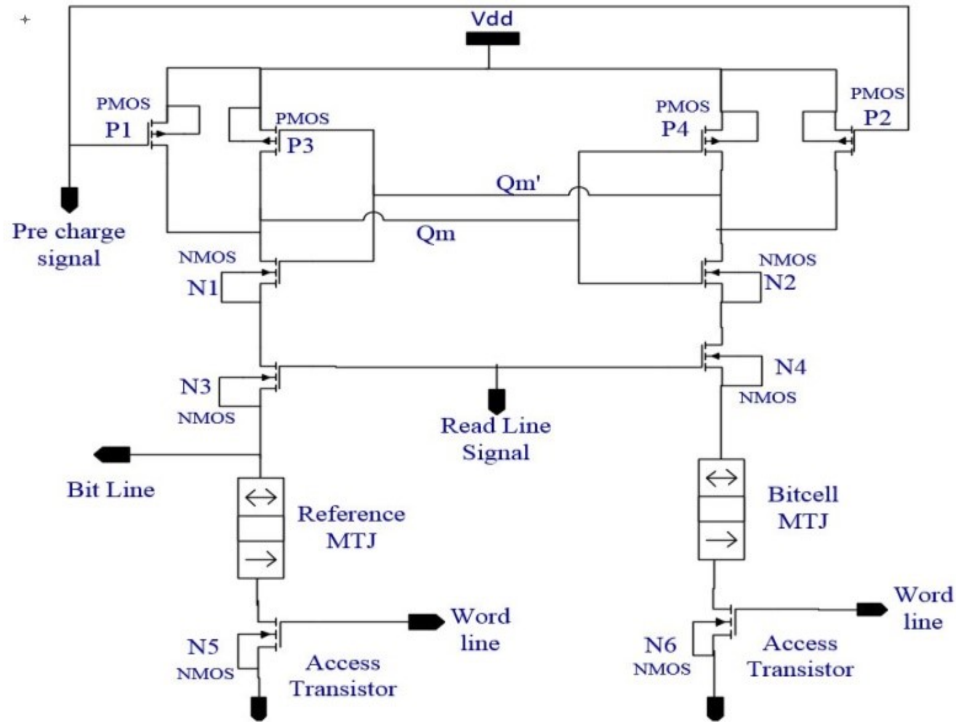


Figure 41: Pre-charge sense amplifier circuit by using the activating signal [9].

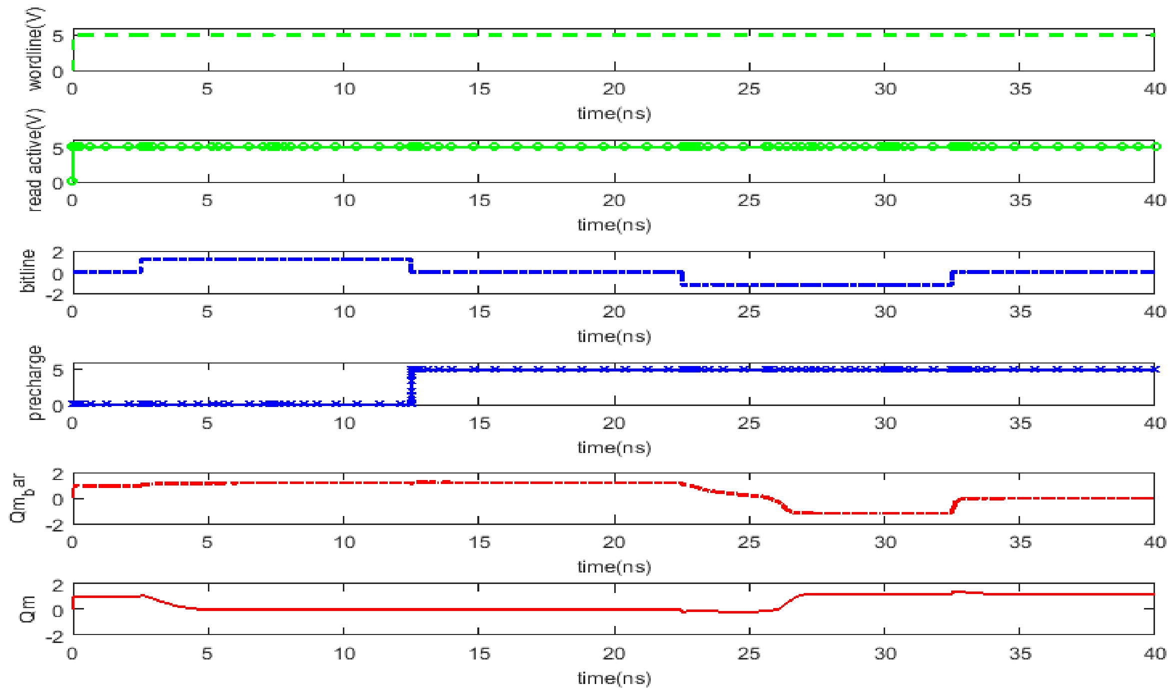


Figure 42: Output waveform of the pre-charge sense amplifier by using the activation signal.

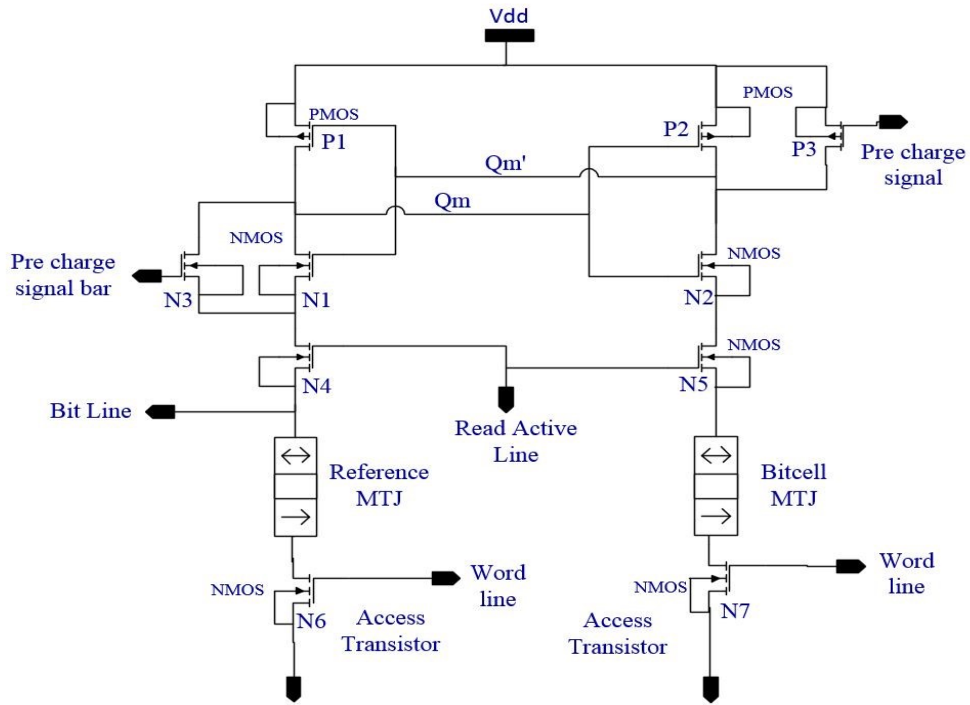


Figure 43: Proposed sense amplifier circuit

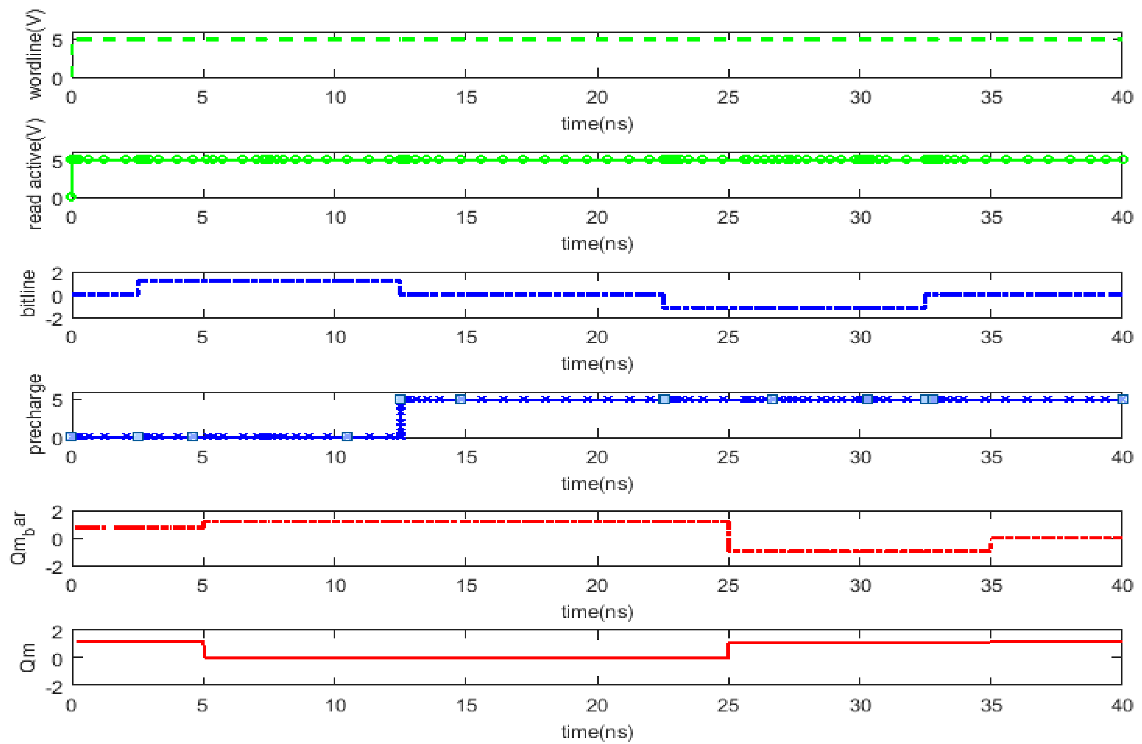


Figure 44: Output waveforms of the proposed pre-charge sense amplifier.

Table 8: Comparison of the proposed sense amplifier of STT-MRAM with the existing sense amplifiers.

Sense amplifier	Sense margin	No. of transistors	Technology Feature (nm)	1st error output	Reliability	Parallel Writing & Reading
Pre charge sense amplifier without activating signal [24]	1.194	6	45	yes	low	yes
Pre charge sense amplifier with activation signal [28]	1.199	8	45	yes	low	Depends on activation signal
Proposed pre charge sense amplifier	1.144	8	45	no	high	Depends on activation signal

5.4.CONCLUSION AND FUTURE WORK

A novel sense amplifier is proposed and analyzed in details by SPICE simulation. The comparison of the proposed sense amplifier with existing sense amplifiers shows that the proposed sense amplifier outperforms existing sense amplifiers in the error correction. The proposed sense amplifier gives no error signal at the beginning while the existing sense amplifiers give error signal when they trigger. To gain the error free sense amplifier we had to trade-off with the sense margin and the number of transistors (Table 8). Our future work involves ultra-low power STT-MRAM sense amplifier design.

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