ULTRA LOW POWER SUBTHRESHOLD DEVICE DESIGN USING NEW ION IMPLANTATION PROFILE

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by

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ABSTRACT

One of the important aspects of integrated circuit design is doping profile of a transistor along its length, width and depth. Devices for super-threshold circuit usually employ halo and retrograde doping profiles in the channel to eliminate many unwanted effects like DIBL, short channel effect, threshold variation etc. These effects are always become a serious issue whenever circuit operates at higher supply voltage. Subthreshold circuit operates at lower supply voltage and these kind of effects will not be a serious issue. Since subthreshold circuit will operate at much lower supply voltage then devices for subthreshold circuit does not require halo and retrograde doping profiles. This will reduce the number of steps in the fabrication process, the parasitic capacitance and the substrate noise dramatically.

This dissertation introduces four new doping profiles for devices to be used in the ultra-low-power subthreshold circuits. The proposed scheme addresses doping variations along all the dimensions (length, width and depth) of the device. Therefore, the approaches are three dimensional (3D) in nature. This new doping scheme proposes to employ Gaussian distribution of doping concentration along the length of the channel with highest concentration at the middle of the channel. The doping concentration across the depth of the device from the channel region towards the bulk of the device can follow one of the following four distributions: (a) exponentially decreasing, (b) Gaussian, (c) low to high, and (d) uniform doping. The proposed doping scheme keeps the doping concentration along the width of the device uniform. Therefore, under this scheme we achieve four sets of new 3D doping profiles. This dissertation also introduces a new comprehensive doping scheme for the transistors in subthreshold circuits. The proposed doping scheme would bring doping changes in the source and drain areas along with the substrate and channel region of the transistors. The proposed doping scheme is characterized by the absence of halos at the source and drain end. We propose a Gaussian doping distribution inside the source, drain region and a low-high-low distribution across the depth of the transistor from the channel surface towards the body region. It also has a low-high-low doping distribution along the length of the transistor below the channel region.

Results show that a device optimized with proposed doping profiles would offer higher ON current in the subthreshold region than a device with the conventional halo and retrograde doping profiles. Among the four 3D doping profiles for subthreshold device some has better ON current than others. Based on specific requirements one of these four doping profiles can be adopted for different ultra-low-power applications. Our analysis shows better subthreshold swing can be achieved using new doping profile based subthreshold design. Results also show that the optimized

device with the proposed comprehensive doping profile would provide higher ON current (I_{on}) at smaller body bias condition. The analysis is performed by changing the doping profile, body bias and (V_{gs}) to observe the off-state current (I_{off}), threshold voltage variation, magnitude of I_{on}/I_{off} ratio, transconductance and the output conductance with the proposed doping profiles.

APPROVAL PAGE

The faculty listed below, appointed by the Dean of the School of School of Graduate Studies have examined a dissertation titled "Ultra Low Power Sub-Threshold Device Design Using New Ion Implantation Profile," presented by Munem Hossain, candidate for the Doctor of Philosophy degree, and certify that in their opinion it is worthy of acceptance.

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LIST OF ABBREVIATIONS

LAC	Lateral Asymmetric Channel
DSM	Deep Sub Micron
HD	Halo Doping
DH	Double Halo Doping
UD	Uniform Doping
RCP	Retrograde Channel Profile
SSR	Super Steep Retrograde
SSRW	Super Steep Retrograde Well
LDD	Lightly Doped Drain
DG	Double Gate
MOS	Metal Oxide Semiconductor
CMOS	Complementary Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
TFET	Tunneling Field Effect Transistor
BTBT	Band to Band Tunneling
SOC	System on Chip
SOI	Silicon on Insulator
ULP	Ultra Low Power
DIBL	Drain Induced Barrier Lowering

GIDL	Gate Induced Drain Leakage
SCE	Short Channel Effect
GD	Gaussian Distribution
PUN	Pull Up Network
PDN	Pill Down Network
TCAD	Technology Computer Aided Design
GCDMDG	Graded Channel Dual Material Double Gate
RFID	Radio Frequency Identification
IOT	Internet of Things

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CHAPTER 1

INTRODUCTION

1.1 Motivation

One of the important aspects of integrated circuit design is the doping profile of a transistor along its length, width and depth. Devices for super-threshold circuit usually employ halo and retrograde doping profiles in the channel to eliminate many unwanted effects. Devices for subthreshold circuits do not require halo and retrograde doping profiles like conventional super-threshold devices. This will reduce the number of steps in the fabrication process, the parasitic capacitance, and the substrate noise dramatically in the subthreshold devices. The proposed doping scheme would bring changes in doping properties along the length (X direction) and depth (Y direction) of the device and keep the doping concentration along the width constant. The doping profile in X direction is kept somewhat constant in most of the previous designs and only the Y direction doping profiles have been varied. We propose a three-dimensional doping scheme, where doping profiles would be varied in both directions. We propose to adopt Gaussian distribution of doping density in the X direction and four different doping profiles in the Y directions for subthreshold devices. Based on the proposal we would get four possible combinations of two-dimensional doping profiles. Superposition of two 2D doping profiles in X and Y directions would lead to a 3D doping profile for the device under each combination. In this dissertation we will focus on the following four combinations of 3D doping profiles: (i) Gaussian distribution of doping profiles

in both X and Y direction, (ii) Gaussian distribution in X and exponentially decreasing in Y direction, (iii) Gaussian distribution in X and low-to-high distribution in Y direction, and (iv) Gaussian distribution in X and uniform distribution in Y direction. For all four combinations we assume the doping density along the width of the device is uniform. It is anticipated that each combination will have certain prospects and constrains for different applications of subthreshold circuits. In this dissertation, we plan to show that for a particular technology generation, lower power and higher performance can be achieved in the subthreshold region by redesigning the devices specifically for subthreshold operation.

1.2 Background

Device, circuit, architecture, and system level requirements for ultra-low-power subthreshold circuits (that would be operated below the threshold voltage) are often different from the conventional super-threshold circuits (that are operated above the threshold voltage). Also, the requirements would be different for digital, analog, and mixed signal applications [1], [2]. One of the important aspects of the design is the doping profile along the length, width, and depth of a transistor. Deeply scaled analog CMOS device design for system-on-chip (SOC) applications is very challenging because of the conflicting requirements of the analog and digital circuits [3], [4]. Also, aggressive scaling of power supply is preferred in digital logic circuits, but this leads to degraded signal range and lower design margins for analog circuits [5]. It is observed that with lateral asymmetric channel (LAC) doping the total gate capacitance of a transistor is reduced by almost 10% in the saturation region at 100nm technology node compared to the conventional MOSFETS [6], [7]. Transistor capacitances have significant influences on its RF performance. Furthermore, in the subthreshold region, the transistor input capacitance is less than that of strong inversion operation. The transistor input capacitance in subthreshold is a combination of intrinsic

capacitance, depletion capacitance, parasitic capacitance and fringing capacitances of a transistor. In contrast, the input capacitance in strong inversion operation is dominated by the oxide capacitance. Due to the smaller capacitance and lower supply voltage (maximum limit is the threshold voltage of the transistor) digital subthreshold circuits consume significantly less power than their strong inversion counterpart at a particular frequency of operation. In [8], the electron velocity overshoot phenomenon in the inversion layer is experimentally investigated for a novel thin film silicon-on-insulator (SOI) test device with channel lengths down to 0.08μm. The test SOI structure used LAC doping profile [9]. The high field drift velocity of the inversion carriers is measured. Simulation results show that very uniform carrier density and drift velocity can be achieved with LAC profile in SOI device.

Short-channel devices are usually optimized for super-threshold circuits to ensure higher mobility, lower drain-induced barrier lowering (DIBL), reduced leakage, and minimal threshold voltage roll-off. However, a transistor optimized for super-threshold circuit may not be optimal for the subthreshold region where effects like DIBL, threshold voltage roll-off, and electron/hole tunneling are much less significant [10]. As a consequence, high doping, traditionally used in the super-threshold device to overcome the short-channel effect (SCE) will not be critical for subthreshold operation [11]. In super-threshold device, the main functions of halo and retrograde doping [12], [13] are to reduce DIBL, prevent body punch through, and control the threshold voltage of the device independent of its subthreshold slope. Since DIBL, body punch through and threshold voltage variation are not severe in the subthreshold device due to lower supply voltage, the halo and retrograde doping is not required for such design. High to low doping profile has been proposed for subthreshold operation in [10]. For subthreshold circuit operation lower subthreshold swing and internal device capacitances are critical. However, existing doping profiles do not offer

any means to address these critical needs. Also the operating current of subthreshold device is the subthreshold leakage current of the conventional device. Because of the low voltage and leakage current based operation subthreshold circuits will not operate at very high frequency.

1.3 Problem Statement

This dissertation introduces four new doping profiles for devices to be used in the ultra-low-power subthreshold circuits. The proposed scheme addresses doping variations along all the dimensions (length, width and depth) of the device. Therefore, the approaches are three dimensional (3D) in nature. This new doping scheme proposes to employ Gaussian distribution of doping concentration along the length of the channel with highest concentration at the middle of the channel. The doping concentration across the depth of the device from the channel region towards the bulk of the device can follow one of the following four distributions: (a) exponentially decreasing, (b) Gaussian, (c) low to high, and (d) uniform doping. The proposed doping scheme keeps the doping concentration along the width of the device uniform. Therefore, under this scheme we achieve four sets of new 3D doping profiles. The doping concentration across the depth of the device is exponentially decreasing means channel surface has highest concentration of dopant distribution and bulk is contained with less dopant distribution. The Gaussian distribution across the depth of the device turn the device into low dopant distribution at the top and bottom surface whereas middle surface is filled with more dopant distribution. Similarly, low to high distribution is somewhat opposites of exponentially decreasing distribution with very small distribution of dopant at the top surface and high distribution underneath the bulk. Finally, uniform distribution specify the equally distributed dopant inside the device from top surface to the bottom surface.

This dissertation also introduces a new comprehensive doping scheme for the transistors in subthreshold circuits. The proposed doping scheme would bring doping changes in the source and drain areas along with the substrate and channel regions of the transistors. The proposed doping scheme is characterized by the absence of halos at the source and drain ends. We propose a Gaussian doping distribution inside the source and drain regions, and a low-high-low distribution across the depth of the transistor from the channel surface towards the body region. It also has a low-high-low doping distribution along the length of the transistor below the channel region.

1.4 Contribution of the Dissertation

In this dissertation four different subthreshold doping profile and one comprehensive doping profile has been proposed and mathematically solved for subthreshold application. The main four subthreshold doping profiles are composed of X dimension and Y dimension varying dopant distribution. This new doping scheme proposes to employ Gaussian distribution of doping concentration along the X dimension (length of the channel) with highest concentration at the middle of the channel. The doping concentration across the Y dimension (depth of the device) from the channel region towards the bulk of the device can follow one of the following four distributions: (a) exponentially decreasing, (b) Gaussian, (c) low to high, and (d) uniform doping. Results show that a device optimized with any of the four proposed doping profiles would offer higher ON current in the subthreshold region than a device with the conventional halo and retrograde doping profiles. Among the four 3D doping profiles for the subthreshold device some has better ON current than the others. Based on specific requirements one of these four doping profiles can be adopted for different ultra-low-power applications. Threshold voltage modelling has been performed and a comparative analysis is presented between super-threshold and sub-threshold devices threshold voltages. We have also analyzed the subthreshold swing characteristics

of the device with the proposed doping profiles. Our analysis shows that better subthreshold swing can be achieved using our new doping profile based subthreshold design.

In comprehensive doping scheme a Gaussian doping distribution inside the source and drain regions, and a low-high-low distribution across the depth of the transistor from the channel surface towards the body region. It also has a low-high-low doping distribution along the length of the transistor below the channel region. We simulated this comprehensive doping scheme using COMSOL Multiphysics simulation tools. Results show that the optimized device with the proposed doping profiles would provide higher ON current (I_{on}) at smaller body bias condition. The analysis is performed by changing the doping profile, the body bias, and the gate-source voltage (V_{gs}) to observe the off-state current (I_{off}), threshold voltage variation, magnitude of I_{on}/I_{off} ratio, transconductance, and the output conductance with the proposed doping profiles.

1.5 Organization of the Dissertation

In chapter 1 we have discussed the background of the proposed doing profile. We explained our proposed doping profile and summarizes the contribution of whole work. In chapter 2 we have explained the theory behind the MOS subthreshold device, different power issue, different leakage currents and other details. In chapter 3 we have shown our detail analysis of four different doping profile by solving all the proposed doping profile equations. In chapter 4 we shown threshold voltage and subthreshold swing modelling of the one of the proposed doping profile. In chapter 5 we simulated comprehensive doping profile using COMSOL Multiphysics simulation tools and analyzed and compared our results with existing work published recently. Finally, chapter 6 we have concluded our all work and analysis with some future work for further continuation of this research.

CHAPTER 2

SUBTHRESHOLD BACKGROUND

This chapter begins with an introduction to subthreshold circuits. It then explains the behavior of a transistor in the subthreshold region of operation. The difference between power, energy and frequency of operation in subthreshold and super-threshold circuits is explained. In this chapter, we provide the fundamental aspects of subthreshold design for ultra-low power circuits [36]. A description of subthreshold circuit properties as given here will be helpful to illustrate our proposed methods in this dissertation. This chapter introduces the problem of power consumption in modern deep sub-micron devices. Subsequently, a description of a transistor's leakage mechanisms is given, and the obstacle to technology scaling, by exponential leakage power increases, is exposed. Later, the paradigms of subthreshold design at several levels of hierarchy are presented. First, the characteristics and behavior of MOS transistors in the subthreshold region are described to comprehend subthreshold logic. In addition, the properties and evolution of subthreshold designs, including the state-of-the-art are presented. Then, the challenges of process variations and its impact on circuit behavior are addressed with an emphasis on research in the subthreshold regime. Lastly, considerations for construct a subthreshold optimized transistor are discussed.

2.1 MOSFET Basic

In this dissertation, the object of discussion, analysis, and optimization is the Metal-Oxide-Semiconductor Field-Effect (MOSFET) transistor. Such a transistor is the dominant device in integrated circuits such as processors and memories. The transistor's current is transported by electrons in n-channel devices (nMOS) or by holes in p-channel devices (pMOS). A basic nMOS channel structure is depicted in Figure 1, the substrate (bulk or body) is composed of p-type silicon in which two heavily doped n-type silicon regions, the drain and the source, are formed. Typically, the gate consists of heavily doped or silicide polysilicon, and is separated from the substrate by a thin silicon dioxide film, the gate oxide. The main device parameters are gate oxide insulator thickness (T_{ox}), physical gate length (L_g), channel doping concentration (N_{ch}), source/drain junction depth (Y_j), and transistor width (W).

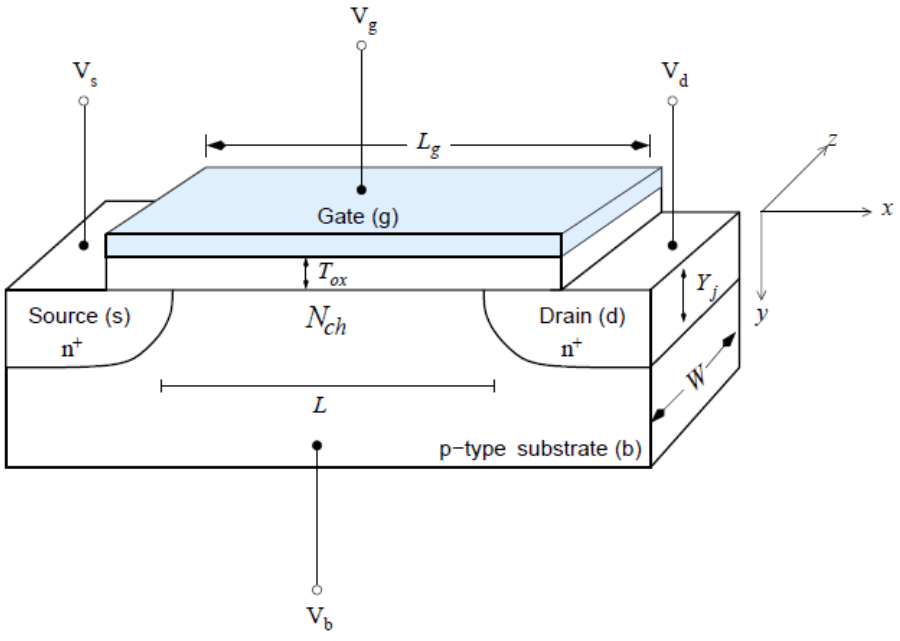


Figure 1: Device structure of an n-channel MOSFET [37]

With shrinking technology sizes, energy efficiency has become a critical aspect of designing digital circuits. Traditionally, voltage scaling, a mechanism in which the supply voltage is varying and the threshold voltage is constant, has been an effective solution in meeting stringent energy requirements. However, voltage scaling does come at a cost of reduction in performance. The limits of voltage scaling, and therefore energy minimization, can be explored by operating a circuit at subthreshold [38]. In subthreshold circuits, the supply voltage is reduced well below the threshold voltage of a transistor. Due to the quadratic reduction in power with respect to the supply voltage, subthreshold circuits are classified as ultra-low power circuits. Specifically in application areas where performance can be sacrificed for low power, subthreshold circuits are an ideal fit. Some of the applications include devices such as hearing aids [39], wrist watches [40], radio frequency identification (RFID), sensor nodes and battery operated devices such as cellular phones. One of the major areas where subthreshold design can be used.

Subthreshold logic operates completely in the subthreshold region. The drain on and off currents are composed entirely of subthreshold leakage. Therefore, the logic assumes a power supply voltage that is less than the threshold voltage, $V_{dd} < V_{th}$. Since the leakage current is orders of magnitude lower than the drain strong inversion current and since the power supply is reduced, subthreshold logic dissipates ultra-low-power. Due to the small drive leakage current, the subthreshold logic only fits in designs, where the performance is considerably poor, and not the main concern.

Subthreshold logic shares important properties with traditional strong inversion CMOS logic.

a) High Noise Margins: The output swing goes from V_{dd} to ground (GND).

b) Low Output Impedance: In the steady state, a low impedance path to either V_{dd} or GND exists.

In addition, subthreshold logic has a number of advantages over its strong inversion counterpart.

a) Lower Power Consumption: At the same frequency, subthreshold circuits consume orders of magnitude less power than strong inversion circuits [41].

b) Higher Gain: The exponential relationship between Isub and Vgs leads to a high transconductance [42].

c) Better Noise Margins: I_{sub} readily becomes independent of V_{ds}. This near ideal current source characteristic improves the noise margin of the logic gates [43].

A notable difference between strong inversion CMOS logic and subthreshold circuits is their robustness. Strong inversion logic will always work, given that the appropriate complementary Pull-Up Network (PUN) and Pull-Down Network (PDN) are implemented, even if the transistors are erroneously sized. In subthreshold circuits, transistor sizing impacts the functionality of CMOS circuits due to low supply voltages [44]. For example, consider a simple inverter, operating in the subthreshold region. Subthreshold I_{off} leakage always flow through a large pMOS device (which forms the PUN) to a certain extent where, a smaller nMOS (which forms the PDN) cannot pull down the voltage at the output to a full logic 0 level, and vice versa. This problem is augmented by the effect of the process variations.

2.2 Origin of Subthreshold Circuit Design

The MOS (Metal Oxide Semiconductor) transistor conducts current, majority carriers, through an inverted channel between the source and drain caused by a nominal voltage applied to

the gate. When a low voltage is applied to the gate, majority carriers in the substrate are repelled from the surface directly below the gate. Then, a depletion charge of immobile atoms forms a depletion region beneath the gate. The minority carriers in the depletion layer are made to move by diffusion and induce a drain current by applying a voltage between the drain and source in the MOS device. This weak inversion current was considered to be insignificantly small and ignored in digital circuit design until the recent decade. The early exploration of subthreshold design was focused on analog circuits such as amplitude detector, quartz ring oscillator, bandpass amplifier, and transconductance amplifier [45]. In the past years, subthreshold digital CMOS designs have been implemented for biomedical devices, FFT processors, and SRAMs [46-51]. This unintended discovery provides an opportunity for meeting the demands of extreme energy efficient systems.

2.3 Subthreshold Current

The region of operation of a transistor depends on the supply voltage at which it operates. As the supply voltage is reduced, the region of operation shifts from strong inversion to moderate inversion and finally to weak inversion. The strong inversion region, also known as the super-threshold regime, is characterized by large current drives and a supply voltage substantially above V_{th}, the threshold voltage of the transistor. The moderate inversion has lower current drives as compared to the super-threshold regime and an operating voltage near to the V_{th}. The weak inversion region, also known as the subthreshold regime, is characterized by small current drives and a supply voltage below V_{th}. The behavior of the transistor in the subthreshold and super-threshold regions is shown in equations (2.1) and (2.2) [38]

$$I_{on-sub} = \frac{W}{L_{eff}} \mu_{eff} C_{ox} (m-1) V_T^2 \exp\left(\frac{V_{gs} - V_{th}}{m V_T}\right)\left(1 - \exp\left(\frac{-V_{ds}}{V_T}\right)\right) \tag{2.1}$$

where W is the width of the transistor, L_{eff} is the effective length, μ_{eff} is the effective mobility, C_{ox} is the oxide capacitance, m is the subthreshold slope factor and $V_T = (KT/q)$.

$$I_{on-super} = \frac{g_{msat}}{1 + R_s g_{msat}} (V_{dd} - V_{th} - V_{PO}) \tag{2.2}$$

where g_{msat} is the saturation transconductance, R_s is the source resistance and V_{PO} is the pinch off voltage.

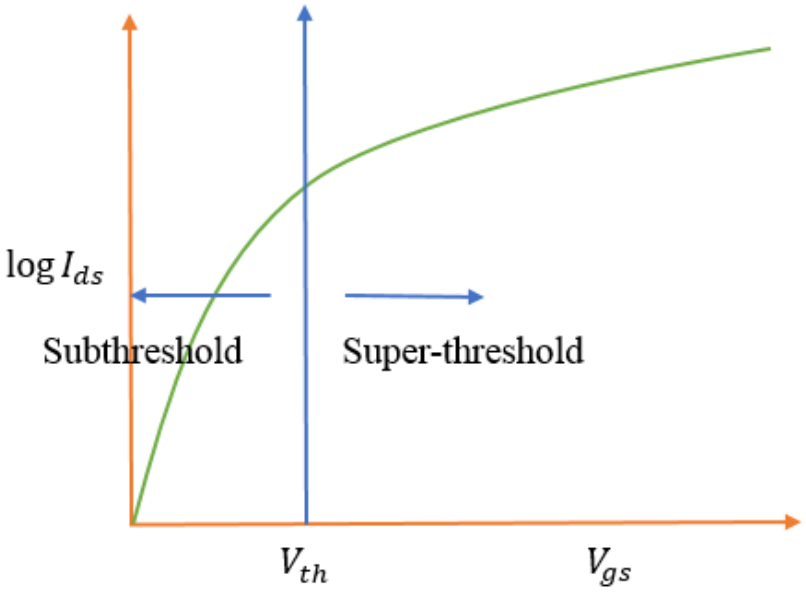


Figure 2: Transistor current characteristics.

The subthreshold and super-threshold regions of operation are highlighted in Figure 2. In the super-threshold region, the current is fairly linear in nature. The transistor current I_{on} in the subthreshold regime is exponentially dependent on V_{th} and supply voltage due to which power, delay and current matching between two transistors is also exponentially dependent on V_{th} and V_{dd}. This exponential dependence is a key challenge in designing circuits in subthreshold. Some of the parameters that are affected by this challenge are process variations, noise margins, soft errors and

output voltage swings. Therefore, when designing energy optimal subthreshold circuits, these parameters play an important role. The current in the subthreshold region, also known as leakage current, is considered to be undesirable when operating the transistor in the super-threshold region. However, this current is quintessential as far as subthreshold operation is concerned. Leakage current is utilized by subthreshold circuits as their conduction current.

2.4 Power, Energy and Frequency

The total power in a CMOS circuit is given by equation (2.3)

$$P_{Total} = P_{dynamic} + P_{static} = \frac{1}{2} C_L V_{dd}^2 \alpha f + I_{sc} V_{dd} + I_{static} V_{dd} \quad (2.3)$$

where C_L is the load capacitance, f is the frequency of operation, I_{SC} is the short circuit current and α is the activity factor. As can be seen from Equation (2.3) the total power consists of two major components: dynamic power and leakage power. Both these components reduce in magnitude as the supply voltage reduces.

The dynamic power consumption is due to the charging and discharging of the load capacitance and the short circuit current. A short circuit current flows when the pull up and pull down networks in a CMOS circuit are simultaneously on and a direct path exists between the supply line and ground. Dynamic power is directly proportional to the square of the supply voltage. Therefore, dynamic power reduces in a quadratic manner when the supply voltage is reduced. Leakage power is dependent on the leakage current flowing in the CMOS circuit.

At super-threshold, the charging (or discharging) current is greater than the leakage current. Hence, dynamic power dominates over leakage power in super-threshold. At subthreshold, supply voltage is lower than the threshold voltage of the transistor. Due to its quadratic relation with

supply voltage, dynamic power reduces drastically in subthreshold. Also, leakage current is regarded as the conduction current in subthreshold. Therefore, leakage power dominates than dynamic power in the subthreshold region of operation.

Energy is one of the important design metrics in digital circuits. The energy estimation in these circuits is given by Equation (2.4)

$$E_{Total} = E_{dynamic} + E_{static} = \frac{1}{2} C_L V_{dd}^2 \alpha + I_{static} V_{dd} t_p \tag{2.4}$$

where C_L is the load capacitance, t_p is the circuit delay and α is the activity factor. The important observation in Equation (2.4) is the dependence of leakage energy on delay t_p. Since t_p is high in subthreshold, the leakage energy is greater than the dynamic energy. As the supply voltage is increased, the delay and hence the leakage energy, reduces. Therefore, at super-threshold the dynamic energy is the more dominant of the two. Short circuit energy is negligible at subthreshold and can be ignored [38].

2.5 Minimum Energy Operation

Since energy minimization is the enabling factor for subthreshold design, identifying the operating voltage range for the optimal energy forms the design basis. Two commonly used terms in subthreshold design are V_{min}, the voltage at which the energy of the circuit is minimum and $V_{dd,limit}$, the lowest supply voltage at which the circuit can be operated. In most cases the V_{min} is greater than $V_{dd,limit}$. V_{min} denotes the ideal supply voltage at which the circuit should be operated. Stacking of transistors raises the $V_{dd,limit}$ of a circuit well above that of a simple inverter. The location of the energy minimum of any circuit is a compromise between the dynamic and leakage energies. The point of intersection of the dynamic and leakage energy curves is defined as the

minimum energy point of the circuit. The activity factor, α, V_{th}, L_{eff}, sub-V_{th} slope and I_{on} are interdependent and should be considered for determining the minimum energy point of any design.

The minimum energy operation point (E_{min}) for a digital circuit means that the circuit consumes less Energy per cycle than any other point in the parameter space. Among the different parameters, power supply voltage (V_{dd}) and device threshold voltage (V_{th}) are mainly considered for the minimum energy point. The energy and delay contours for a ring oscillator circuit with varying V_{dd} and V_{th} show that E_{min} occurs in the subthreshold region [52]. For given V_{dd} and V_{th}, the minimum energy point for a circuit is determined by the relationship between energy and latency. As V_{dd} scales down, dynamic energy is quadratically reduced, while the delay of a circuit exponentially increases at supply voltages below V_{th}. The increased delay induces an exponential increase of leakage energy. The minimum energy point occurs where the magnitudes of dynamic energy and leakage energy are equal. The switching activity of a circuit affects its minimum energy point. When the dynamic energy is decreased by reducing switching events, the leakage energy remains constant with switching activity. Thus, the leakage energy contributes substantially more to the total energy of a circuit. In that case, the minimum energy point occurs at higher supply voltages compared to higher activity circuits. Adversely, higher switching circuits move the minimum energy point to lower supply voltages to suppress the dynamic energy. There are two representative minimum energy models in the literature. First, when the operating frequency and technology of a subthreshold circuit are given, the minimum energy model is derived to obtain the closed forms for optimal V_{dd} and V_{th}, respectively [53]. This model uses fitting parameters normalized to a characteristic inverter for the given technology, where the minimum sized inverter, for simplicity, is a good choice. All other gates are normalized with respect to the inverter.

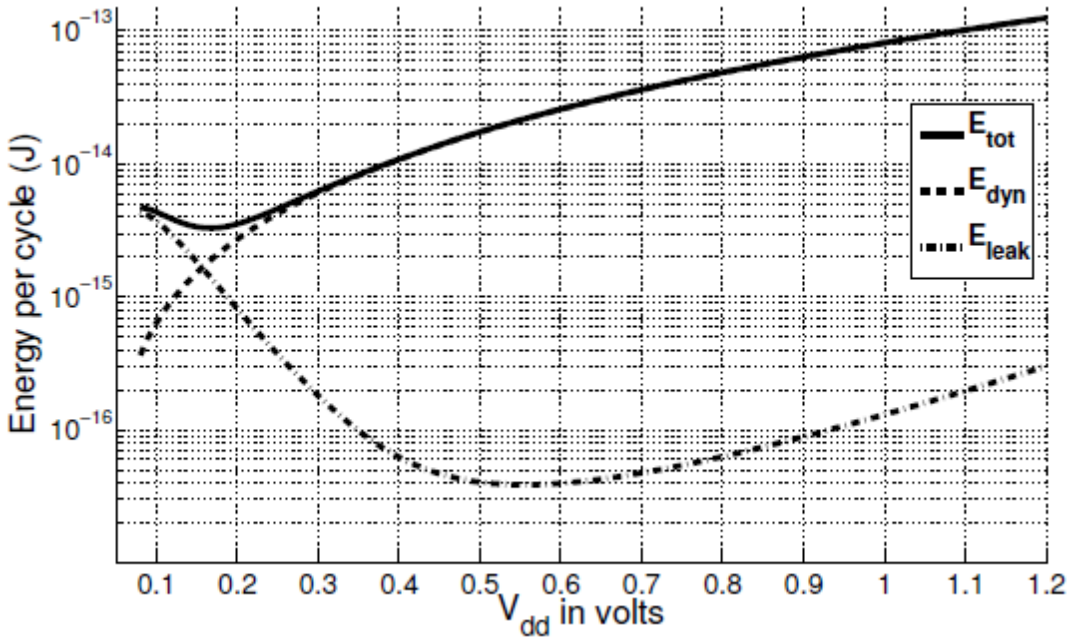


Figure 3: Energy per cycle for an 8-bit ripple carry adder through HSPICE [54] simulation in PTM *90 nm* CMOS, $E_{min} = 3.29\ fJ$ at $V_{dd} = 0.17\ V$ ($V_{th,pmos} = -0.21\ V$ and $V_{th,nmos} = 0.29\ V$).

2.6 Leakage Mechanism

Static power is dissipated during the idle time, that is, when no transition or switching activity occurs. As the transistor threshold voltage, channel length, and gate oxide thickness are reduced in deep submicron (DSM) regimes, the static power dissipation becomes a challenging obstacle for the development of modern ICs. Consequently, the identification of the different leakage components is pivotal for the analysis and design of low-power applications. Figure 4 [55] denotes the seven transistor intrinsic leakage mechanisms in short channel devices.

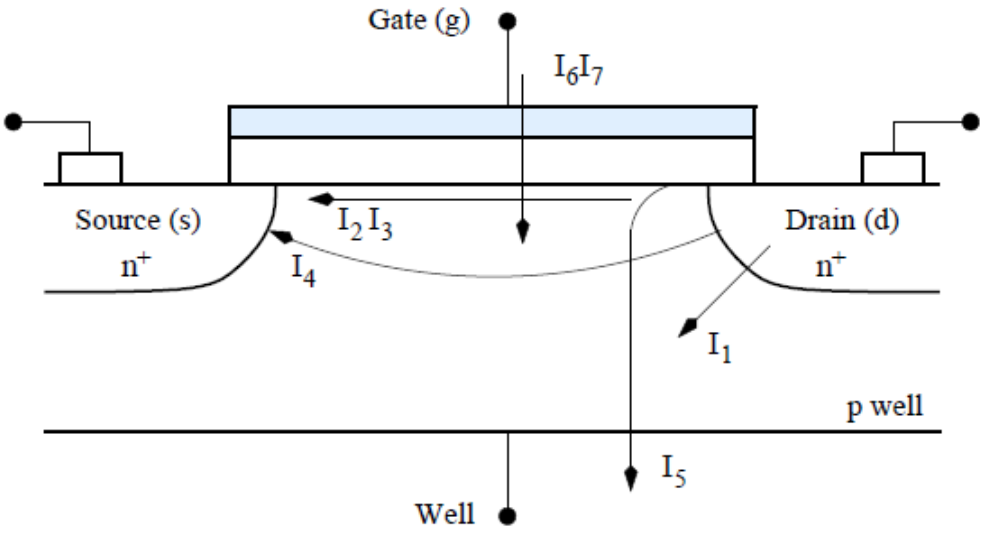


Figure 4: Short-channel transistor mechanisms: (I_1), reverse biased p-n junction; (I_2), subthreshold or weak inversion; (I_3), drain-induced barrier lowering; (I_4), punch-through; (I_5), gate-induced drain leakage; (I_6), gate oxide tunneling; and (I_7), hot-carrier injection.

I_1 is the reverse bias p-n junction leakage. Drain-to-substrate and source-to- substrate junctions are normally reverse biased, occasioning a p-n junction leakage current. It has two components: i) the minority carrier diffusion/drift near the edge of the depletion region, and ii) the electron-hole pair generation in the depletion region of the reverse biased junction. If both the n- and p-regions are heavily doped, which is the case of an advanced MOS, to mitigate short-channel effects, Band-to- Band Tunneling (BTBT) can also be present. The effect dominates the p-n junction leakage component. IBTBT occurs when a high electric field ($> 10^6 V/cm$), across the reverse biased junction, leads to electrons from the valence band of the p-side to migrate to the conduction band of the n-side, as denoted in Figure 5 [56].

I_2 is the weak inversion or subthreshold conduction current between the source and drain. It occurs when the gate voltage is below the threshold voltage ($V_g < V_{th}$). Recently, this current dominates device off-state leakage mechanisms due to the low V_{th} values of transistors [57]. This

weak inversion current is the drive current in the subthreshold regime. Consequently, this leakage component is looked at the next section.

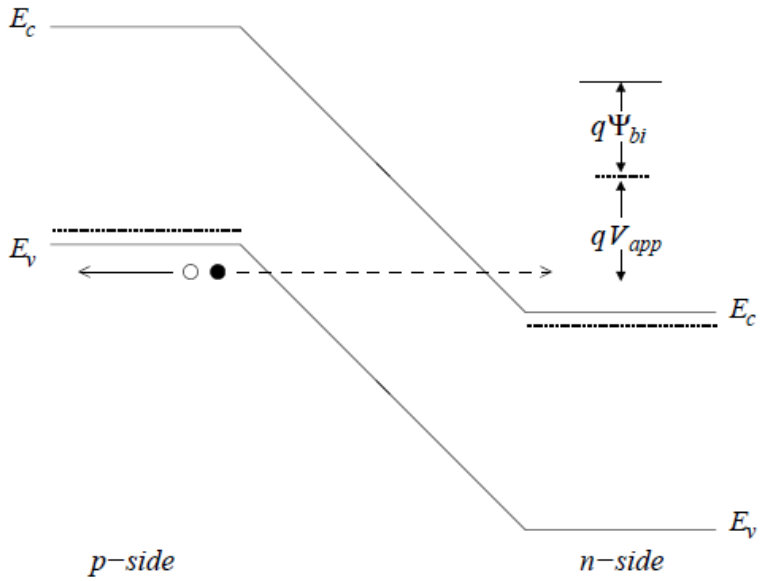


Figure 5: Band-to-band tunneling in an nMOS: valence band electron tunneling from the valence band of the p-side to the conduction band of the n-side; the total voltage drop across the junction, the reverse bias voltage and the built-in voltage is greater than the energy-band gap, ($V_{app} + \psi_{bi} > E_g$).

I_3 is the Drain-Induced Barrier Lowering (DIBL). It occurs when a high drain voltage is applied to a short-channel device, and thus, the potential (voltage) barrier (to the electrons for an nMOS) at the surface between the source and drain is lowered. For example, consider the potential energy barrier at the surface between the drain and source, depicted in Figure 6 [58]. At the off condition, this potential prevents the flow of electrons between the terminals. However, as the drain voltage is increased, the potential barrier is reduced in short-channel devices. In this way, the higher the drain voltage applied to a short channel device, the lower the barrier height is, and

thus, the source injects carriers into the channel surface without the control gate voltage playing a role [58].

I_4 is the channel punch-through. At even higher drain voltages and channel length reductions, the drain and source depletion regions approach each other and eventually merge in the deep substrate. As a result, the gate totally loses control over the channel, and the flow of the drain current becomes independent of the control voltage [58].

I_5 represents the Gate-Induced Drain Leakage (GIDL). It is the result of the influence of high electric fields on the gate-drain overlap region. Consequently, the depletion width of the drain to substrate p-n junction is thinned out [58]. Carriers are generated in the substrate and drain from the direct band-to-band tunneling, trap-assisted tunneling, or a combination of thermal emission and tunneling [57]. Oxide thickness (T_{ox}) reductions and higher supply voltages lead to a higher potential between the gate and the drain, which in turn, enhances the electric field dependent GIDL.

I_6 refers to oxide leakage tunneling. The continuous reduction of the oxide thickness leads to an increase in the field across Tox. The high electric field results in the tunneling of electrons from the inverted substrate-to-gate and also from the gate-to-substrate through T_{ox}. This current flow is known as oxide leakage tunneling. The direct tunneling of electrons is signified in Figure 7.

I_7 is the gate current due to hot carrier injection. If a region with a high electric field is located near the Si-SiO2 interface (as it occurs in the pinch-off condition), some of the electrons or holes can gain sufficient energy from the field to cross the interface potential barrier and enter the oxide layer. This phenomenon, called a hot-carrier injection, is represented in Figure 7 [58].

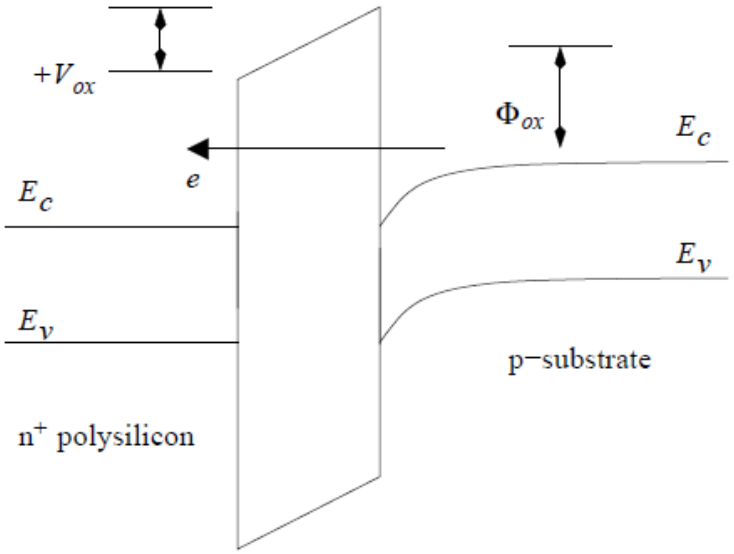


Figure 6: Tunneling of electrons: direct tunneling occurs when the potential drop across the gate oxide is lower than the barrier height of the tunneling electron ($V_{ox} < \varphi_{ox}$).

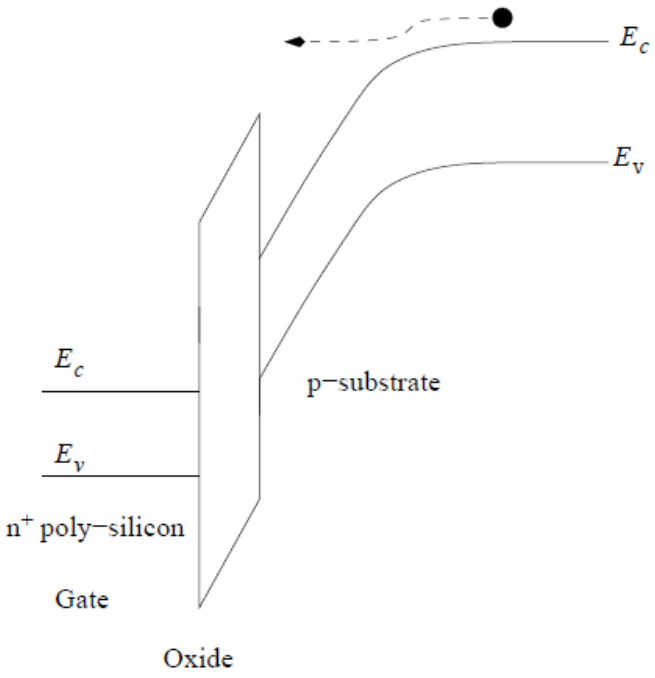


Figure 7: Injection of hot electrons from the substrate to the oxide.

2.7 Conclusion

This chapter describes some issues in reducing power consumption in scaled devices. A MOS's intrinsic leakage mechanisms are explained. The three more contributive leakage components in DSM technologies are subthreshold, oxide tunneling, and reverse bias p-n junction BTBT. Subthreshold leakage is the drive current in the subthreshold regime. In addition, the characteristics of MOS transistors in the subthreshold region are examined with respect to the strong inversion regime, including current flow mechanism, intrinsic capacitances, and the exponential relation between the gate voltage and drain current. Then, the paradigms of subthreshold logic are outlined. Subthreshold logic and strong inversion CMOS logic share several properties such as high noise margins, and low output impedance with improved features in power consumption and gain. Beginning with the analog field, it was not until the late 1990s that subthreshold circuits attracted attention in the digital domain; since then, several subthreshold systems have been implemented with standard DSM technologies. Later, process variations and their impact on circuit behavior are presented. The three essential parameters to account for variations are: oxide thickness, channel length, and channel doping concentration. Variability is one of the most challenging obstacles in recent technologies, and is accentuated in subthreshold designs. Finally, an optimized transistor structure for subthreshold operation is discussed, as a promising construction block in terms of simplified fabrication processes, faster operation, and lower power consumption.

CHAPTER 3

IMPLANTATION PROFILES

Devices for super-threshold circuit usually employ halo and retrograde doping profiles in the channel to eliminate many unwanted effects. Devices for subthreshold circuits do not require halo and retrograde doping profiles. This will reduce the number of steps in the fabrication process, the parasitic capacitance, and the substrate noise dramatically. This chapter introduces four new doping profiles for devices to be used in the ultra-low-power subthreshold circuits. The proposed scheme addresses doping variations along all the dimensions (length, width and depth) of the device. Therefore, the approaches are three dimensional (3D) in nature. This new doping scheme proposes to employ Gaussian distribution of doping concentration along the length of the channel with highest concentration at the middle of the channel. The doping concentration across the depth of the device from the channel region towards the bulk of the device can follow one of the following four distributions: (a) exponentially decreasing, (b) Gaussian, (c) low to high, and (d) uniform doping. The proposed doping scheme keeps the doping concentration along the width of the device uniform. Therefore, under this scheme we achieve four sets of new 3D doping profiles. Results show that a device optimized with any of the four proposed doping profiles would offer higher ON current in the subthreshold region than a device with the conventional halo and retrograde doping profiles. Among the four 3D doping profiles for the subthreshold device some

has better ON current than the others. Based on specific requirements one of these four doping profiles can be adopted for different ultra-low-power applications.

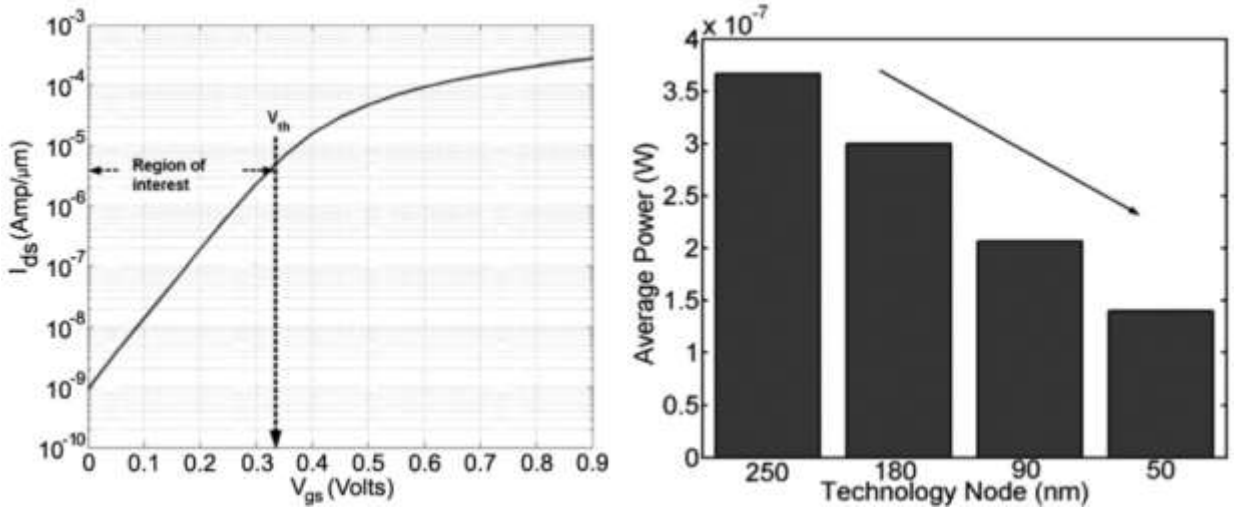
3.1 Introduction

Device, circuit, architecture, and system level requirements for ultra-low-power subthreshold circuits (that would be operated below the threshold voltage) are often different from the conventional super-threshold circuits (that are operated above the threshold voltage). Also, the requirements would be different for digital, analog, and mixed signal applications [1], [2]. One of the important aspects of the design is the doping profile along the length, width, and depth of a transistor. Deeply scaled analog CMOS device design for system-on-chip (SOC) applications is very challenging because of the conflicting requirements of the analog and digital circuits [3], [4]. Also, aggressive scaling of power supply is preferred in digital logic circuits, but this leads to degraded signal range and lower design margins for analog circuits [5]. It is observed that with lateral asymmetric channel (LAC) doping the total gate capacitance of a transistor is reduced by almost 10% in the saturation region at 100nm technology node compared to the conventional MOSFETS [6], [7]. Transistor capacitances have significant influences on its RF performance. Furthermore, in the subthreshold region, the transistor input capacitance is less than that of strong inversion operation. The transistor input capacitance in subthreshold is a combination of intrinsic capacitance, depletion capacitance, parasitic capacitance and fringing capacitances of a transistor. In contrast, the input capacitance in strong inversion operation is dominated by the oxide capacitance. Due to the smaller capacitance and lower supply voltage (maximum limit is the threshold voltage of the transistor) digital subthreshold circuits consume significantly less power than their strong inversion counterpart at a particular frequency of operation. In [8], the electron velocity overshoot phenomenon in the inversion layer is experimentally investigated for a novel

thin film silicon-on-insulator (SOI) test device with channel lengths down to 0.08μm. The test SOI structure used LAC doping profile [9]. The high field drift velocity of the inversion carriers is measured. Simulation results show that very uniform carrier density and drift velocity can be achieved with LAC profile in SOI device.

Short-channel devices are usually optimized for super-threshold circuits to ensure higher mobility, lower drain-induced barrier lowering (DIBL), reduced leakage, and minimal threshold voltage roll-off. However, a transistor optimized for super-threshold circuit may not be optimal for the subthreshold region where effects like DIBL, threshold voltage roll-off, and electron/hole tunneling are much less significant [10]. As a consequence, high doping, traditionally used in the super-threshold device to overcome the short-channel effect (SCE) will not be critical for subthreshold operation [11]. In super-threshold device, the main functions of halo and retrograde doping [12], [13] are to reduce DIBL, prevent body punch through, and control the threshold voltage of the device independent of its subthreshold slope. Since DIBL, body punch through and threshold voltage variation are not severe in the subthreshold device due to lower supply voltage, the halo and retrograde doping is not required for such design. High to low doping profile has been proposed for subthreshold operation in [10]. For subthreshold circuit operation lower subthreshold swing and internal device capacitances are critical. However, existing doping profiles do not offer any means to address these critical needs. Also the operating current of subthreshold device is the subthreshold leakage current of the conventional device. Because of the low voltage and leakage current based operation subthreshold circuits will not operate at very high frequency. Figure 8(a) shows the region of operation of the subthreshold logic circuits. Power consumption is becoming a critical issue in super-threshold device. Technology scaling results in reduction of the total power consumption in super-threshold domain. Figure 8(b) shows how technology scaling can reduce the

total average power consumption of an inverter (driving an identical inverter), all operating at the same frequency [10]. Dramatic reduction of average power consumption is also possible in the subthreshold circuits with technology scaling.



(a) (b)

Figure 8: (a) Subthreshold logic region of operation and (b) average power consumption of different technology nodes [10].

We are currently exploring a set of new doping profiles for devices to be used in the subthreshold circuits. Here, we have outlined the general principle of this new doping scheme. We have presented the outline of four possible combinations of doping profiles along the three dimensions of the device for the subthreshold circuits. This four new doping profile is characterized by Gaussian distribution along the X-direction (along the channel length) and exponentially decreasing, Gaussian, low-to-high or uniform doping concentration along the Y-direction (towards the depth) of the device.

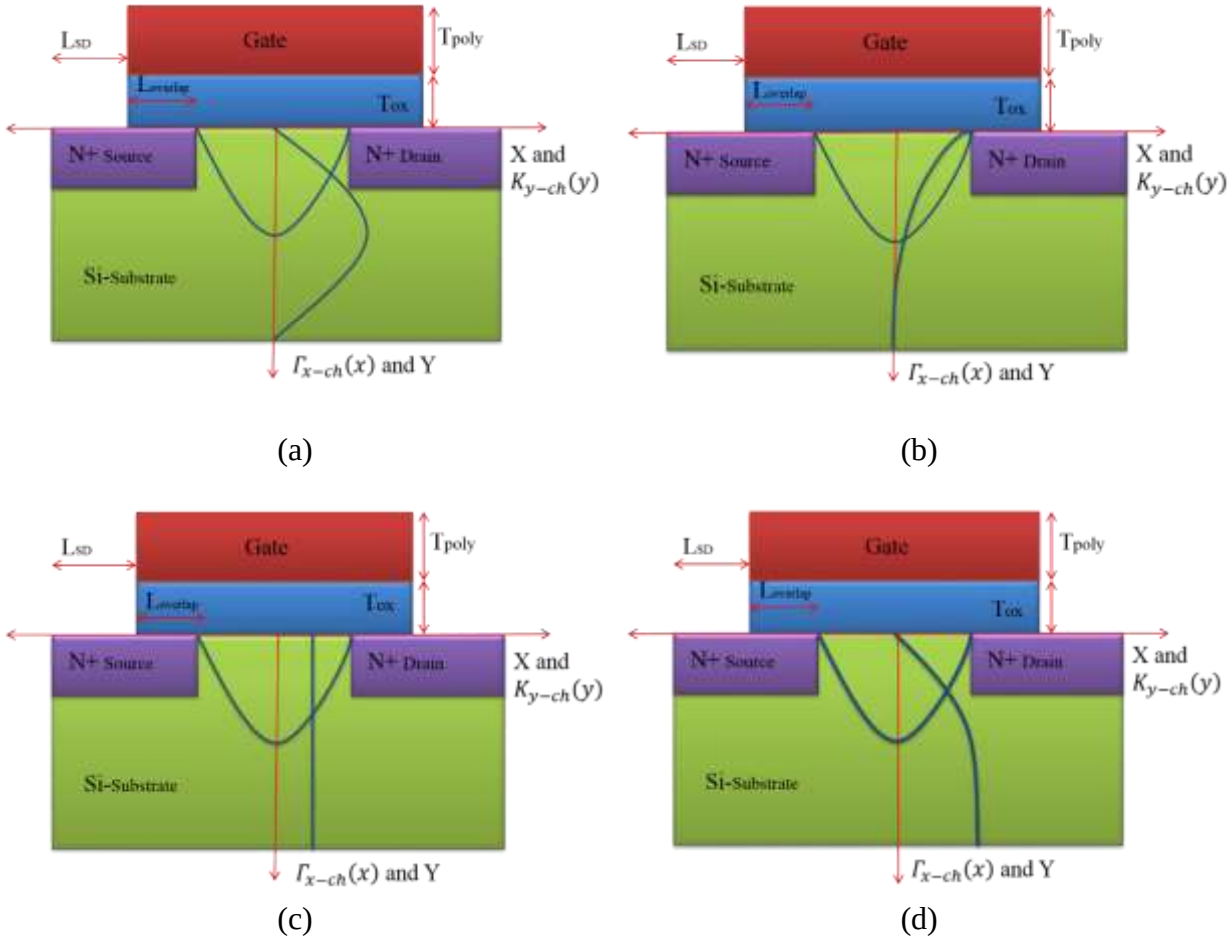


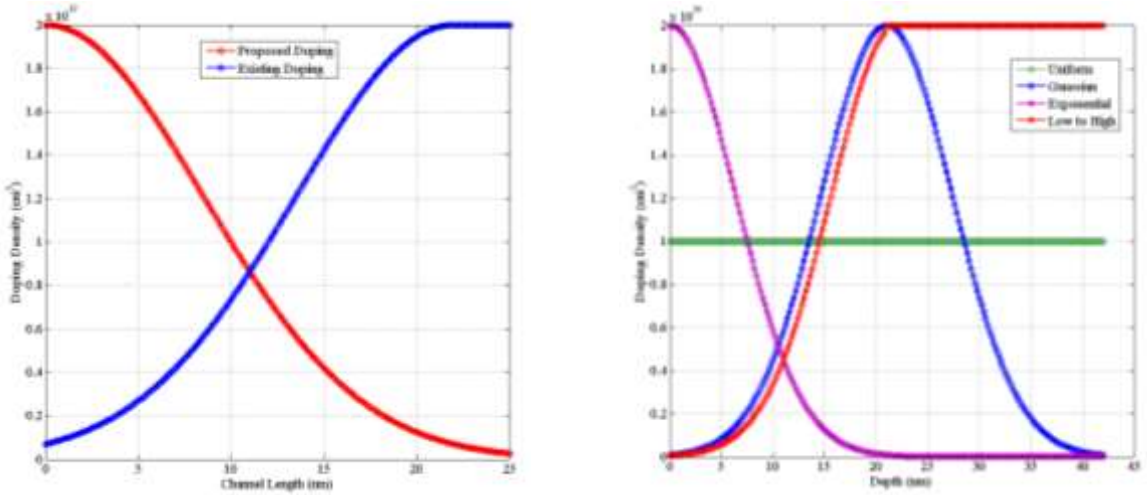
Figure 9: (a) X-direction Gaussian and Y-direction Gaussian doping, (b) X-direction Gaussian and Y-direction Exponentially decreasing doping (c) X-direction Gaussian and Y-direction uniform doping, and (d) X-direction Gaussian and Y-direction low-to-high doping.

3.2 Proposed Doping Scheme for Subthreshold Device

The proposed doping scheme would bring changes in doping properties along the length (X direction) and depth (Y direction) of the device and keep the doping concentration along the width constant. The doping profile in X direction is kept somewhat constant in most of the previous designs and only the Y direction doping profiles have been varied. We propose a three-dimensional doping scheme, where doping profiles would be varied in both directions. We propose to adopt Gaussian distribution of doping density in the X direction and one of the four different doping

profiles in the Y directions for subthreshold devices. Based on the proposal we would get four possible combinations of two-dimensional doping profiles illustrated in Figure 9. Superposition of two 2D doping profiles in X and Y directions would lead to a 3D doping profile for the device under each combination. In this chapter we will focus on the following four combinations of 3D doping profiles: (i) Gaussian distribution of doping profiles in both X and Y direction, (ii) Gaussian distribution in X and exponentially decreasing in Y direction, (iii) Gaussian distribution in X and low-to-high distribution in Y direction, and (iv) Gaussian distribution in X and uniform distribution in Y direction. For all four combinations we assume the doping density along the width of the device is uniform. It is anticipated that each combination will have certain prospects and constrains for different applications of subthreshold circuits. In this project, we plan to show that for a particular technology generation, lower power and higher performance can be achieved in the subthreshold region by redesigning the devices specifically for subthreshold operation.

Conventional super-threshold devices use combination of halo or retrograde doping along the channel and uniform or high-to-low doping along the depth of the channel. In this dissertation we have applied the proposed four doping profiles in the super-threshold device as well to perform a comparative analysis of the performance both in the super- and sub-threshold devices with the proposed doping scheme. Each of these four doping combinations opens the door for a new class of subthreshold devices optimized for specific set of ultra-low-power applications in analog, digital and mixed signal domains. Our future work will present detail comparative analysis of various performance parameters of the doping profiles of Figure 9a to Figure 9d in a more comprehensive form along with the validation using device level simulation tools like TCAD and test data if possible. Here we concentrate on the analytical proof and qualitative analysis of proposed doping.



(a) (b)

Figure 10: (a) Doping distribution along X-dimension – from the middle of the channel to drain (source) end and (b) all four doping distribution along Y-direction from the top surface of the channel towards the bottom surface of the substrate. In (a) red is for the proposed doping profile for subthreshold device and blue is of conventional device.

3.3 Mathematical Modelling and Analysis

A technique based on the subthreshold current–voltage (I-V) characteristics to extract 2-D doping profiles is proposed in [14]. Here we propose a new doping profile for subthreshold device operation using similar approach. We modeled MOSFET subthreshold current based on the proposed doping profile. The formulation of the model is shown for NMOS transistor and can be easily applied to PMOS transistor. Device structure with Gaussian shaped channel doping along the X dimension (length of the channel) has been considered as shown in Figure 10a. In conventional super-threshold device the doping concentration at the middle of the device is the lowest and at the source (drain) ends it is the highest (blue line) and it will lead to form an inverse Gaussian shape dopant distribution. In our proposed scheme for subthreshold device (red line), the middle of the channel has highest doping concentration and the drain (source) end has the lowest.

The variation of doping concentration from the middle towards the both ends is of Gaussian shape under our proposed scheme. And the proposed doping profile (red line) is exactly the inverse of the existing doping profile (blue line). The reason behind selecting the inverse model of X dimension doping profile has been discussed earlier. Across the vertical middle line of the device the doping is symmetrical. In this dissertation, for the Y direction (along the depth of the device) we consider the variation of doping concentration as depicted in Figure 10b, where the four different Y dimension doping density from the channel surface towards the body of the device are shown. The 2D Gaussian doping profile in the channel can be represented as in (3.1) [14].

$$N_{cheff}(x,y) = A_p \Gamma_{x-ch}(x) K_{y-ch}(y) + N_{sub} \tag{3.1}$$

$$\Gamma_{x-ch}(x) = exp^{\left(\frac{-(x)^2}{\sigma 1^2_{x-ch}}\right)}, \qquad -\frac{L_{eff}}{2} \leq x \leq +\frac{L_{eff}}{2} \tag{3.2}$$

$$\Gamma_{x-ch}(x) = exp^{\left(\frac{-(x-\beta_{ch})^2}{\sigma 1^2_{x-ch}}\right)}, \qquad 0 \leq x \leq \beta_{ch} \tag{3.3}$$

Equations (3.2) and (3.3) represents X dimension doping distribution for subthreshold and super-threshold device operation. For subthreshold device, the X dimension has high doping at the center of the channel and falls off towards the source or drain junction as in (3.2). For super-threshold the X dimension has low doping at the center of the channel and increase towards the source or drain junction as depicted in (3.3). L_{eff} is the effective length of the channel and β_{ch} controls the position of the effective doping along the channel. Here (3.4) illustrates the Gaussian Y dimension (from the channel surface towards the body) doping profile for the subthreshold device. Gaussian doping profile along Y-dimension is realized by lower doping in the channel area followed by exponentially increase towards the bulk and reaches to a peak value at $y = \alpha_{ch}$. After peak the doping will exponentially decrease and reaches to steady state at $y \leq 2\alpha_{ch}$. Parameter

α_{ch} controls the position and $\sigma 1_{y-ch}$ controls the variance of gaussian doping profile along y-dimension. Since the doping distribution is getting low inside lower end of the bulk that will lead to reduce the capacitance of the bottom junction and reduces substrate noise effects and parasitic latch-up problems. And strong doping between channel area and lower end of the bulk will help to form the channel very fast at lower threshold voltage.

$$K_{y-ch}(y) = exp^{\left(\frac{-(y-\alpha_{ch})^2}{\sigma 1^2_{y-ch}}\right)}, \quad 0 \le y \le 2\alpha_{ch} \tag{3.4}$$

Equation (3.5) illustrates the exponentially decreasing Y dimension (from the channel surface towards the body) doping profile for the subthreshold device.

$$K_{y-ch}(y) = exp^{\left(\frac{-(y-\alpha_{ch})^2}{\sigma 1^2_{y-ch}}\right)}, \alpha_{ch} = 0, 0 \le y \le d \tag{3.5}$$

Here d is the depth of the device (measured from the channel surface to the bottom surface of the substrate). The parameter α_{ch} controls the position and $\sigma 1_{y-ch}$ controls the variance of exponentially decreasing doping profile along Y-direction. Here $\alpha_{ch} = 0$ means that the variation of doping concentration starts from the surface of the channel. Since the doping at lower end is low this will also lead to the reduced capacitance at the bottom junction, lower substrate noise and lower parasitic latch-up problems.

$$K_{y-ch}(y) = exp^{\left(\frac{-(y-\alpha_{ch})^2}{\sigma 1^2_{y-ch}}\right)}, \sigma 1_{y-ch} = c, 0 \le y \le d_1 \tag{3.6(a)}$$

$$= exp^{\left(\frac{-(y-\alpha_{ch})^2}{\sigma 1^2_{y-ch}}\right)}, \sigma 1_{y-ch} = \infty, d_1 \le y \le d_2 \tag{3.6(b)}$$

Equation 3.6 (a) and (b) shows the low to high doping distribution along the Y-direction of the device. Low-to high doping profile along y-dimension is realized by the low doping at the

beginning of the channel and high doping beneath the channel. Where d_1 and d_2 is the length from gate oxide to a fixed point inside substrate. Since the doping density is low-to-high d_1 set the final boundary of low doping density from top surface of the channel. d_2 set the final boundary of higher doping where low doping density has stopped at d_1. Parameter α_{ch} controls the position and $\sigma 1_{y-ch}$(constant) controls the variance of uniform doping profile along Y-dimension. $\sigma 1_{y-ch} = \infty$ will ensure that channel doping has constant high doping in the y direction for $d_1 \leq y \leq d_2$. Higher doping concentration in the channel reduce depletion width and short channel effect. Since in this proposed doping short channel effect is minimum but high doping inside channel even help more to reduce this kind of effect. However, the low-high profile does not require any special sputtering or ion-implant steps (as it is required for halo/retrograde doping) and hence, significantly reduces the process complexity and cost.

$$K_{y-ch}(y) = exp^{\left(\frac{-(y-\alpha_{ch})^2}{\sigma 1_{y-ch}^2}\right)}, \sigma 1_{y-ch} = \infty, 0 \leq y \leq d \tag{3.7}$$

Uniform doping profile in (3.7) along y-dimension is realized by the constant doping from channel surface to underneath the channel. $\sigma 1_{y-ch} = \infty$ will ensure that channel doping has no variation in the y direction for $0 \leq y \leq d$. To suppress short-channel effects such as DIBL and threshold voltage roll-off, extremely high levels of channel doping are required for super-threshold device, but these results in increased leakage and degraded electron mobility. Since subthreshold circuit has minimum short channel effect which will require low level of uniform channel doping that will lead to reduce leakage power and degraded mobility.

In subthreshold operation the bias voltage is less than that of super-threshold operation. Therefore, the doping profile for subthreshold operation has to be optimized for low bias voltage. The subthreshold current flowing through the transistor can be given by (3.8) [15].

$$I_{sub} = \frac{w_{eff}}{L_{eff}} \mu \sqrt{\frac{q\varepsilon_{si}N_{cheff}}{2\phi_s}} v_T^2 \times exp\left(\frac{V_{gs} - V_{th}}{mv_T}\right)\left(1 - exp\left(\frac{-V_{ds}}{v_T}\right)\right) \quad (3.8)$$

In (8), Ncheff is the effective channel doping, Φs is the surface potential, m is the body effect and v_T is the thermal voltage. Different parameters in the above model depend on the effective channel doping. The effective channel doping can be calculated by (3.9), where Δ_{ch} is the area of the channel region that under the influence of the gate. The X and Y directional doping profiles in (3.9) would be calculated using (3.2) to (3.7) depending on the type of doping profile has chosen.

$$N_{cheff} = \frac{A_p}{\Delta_{ch}} \int_{x=-\frac{L_{eff}}{2}}^{x=+\frac{L_{eff}}{2}} \Gamma_{x-ch}(x)dx \int_{y=0}^{y=2\alpha_a} K_{y-ch}(y)\, dy + N_{sub} \quad (9)$$

In subthreshold operation the current flowing from the drain to source of transistor is known as the subthreshold current. Using charge sharing model the threshold voltage [16], [17] can be expressed as:

$$V_t = V_{FB} + \Phi_s + \gamma\sqrt{\Phi_{s0} - V_{bs}}\left(1 - \lambda\frac{X_d}{L_{eff}}\right) \quad 3.10(a)$$

$$X_d = \sqrt{\frac{2\varepsilon_{Si}}{qN_{cheff}}}\sqrt{\Phi_{s0} - V_{bs}} \quad 3.10(b)$$

Where V_{FB} is the flat band voltage, Φ_{s0} is the zero bias surface potential, γ is the body factor, X_d is the depletion layer thickness, λ is a fitting parameter (~1) [16], [17]. Φ_s of short channel devices from its zero bias value due to short channel effect like DIBL and Vth roll off. The inverse subthreshold slope (S) for the short channel device, considering the penetration of the drain-induced electric field in the center of the channel is given by [17]

$$S = \ln(10)\frac{kT}{q}\left(\frac{1}{\lambda} + \frac{C_d}{C_{ox}}\right) \qquad 3.11(a)$$

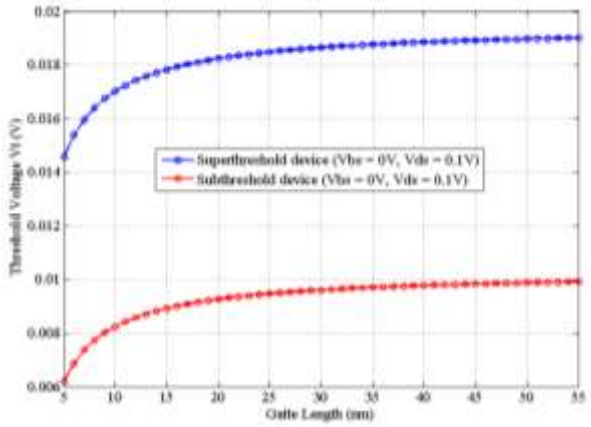
$$\lambda \approx 1 - 2\exp\left(-\frac{L_{eff}}{2l}\right) \qquad 3.11(b)$$

$$l = \sqrt{\frac{\varepsilon_{Si} t_{ox} X_d}{\varepsilon_{ox}}} \qquad 3.11(c)$$

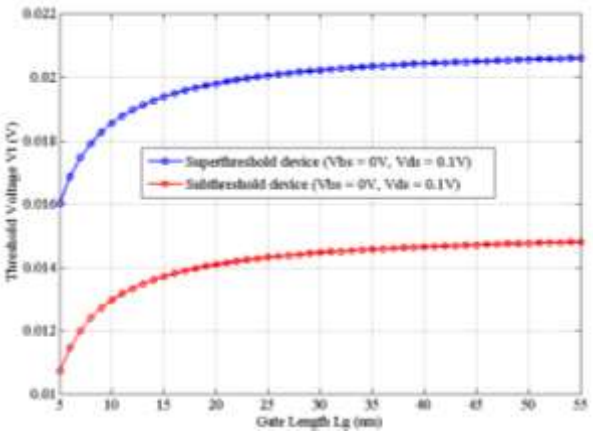
C_d and C_{ox} are the depletion and oxide capacitance of the device. The influence of the short channel effect on the subthreshold swing is determined by factor λ. l is the characteristics length, ε_{Si} and ε_{ox} are the permittivity of the silicon and silicon oxide, t_{ox} is the oxide capacitance and X_d is the depletion width.

In the rest of this section we have analyzed the performance of the proposed four doping profiles for the subthreshold device compared to a super-threshold device. A super-threshold device is a device that is operated (ON state) with a voltage above the threshold voltage of a conventional MOSFET. In Figure 8a the threshold voltage V_{th}*~0.3V* under which the device is considered OFF. On the other hand the operating region of a subthreshold device is complete moved to the subthreshold region (*0V* to *0.3V* in the case of Figure 8a). Within that subthreshold region the subthreshold device must have distinguishable OFF and ON states. Therefore, our area of interest in Figure 8a is the subthreshold region, where a voltage very close to *0V* will be considered as the OFF state and a voltage close to Vth would be considered as the ON state. A steeper subthreshold slope translates to higher I_{on}/I_{off} ratio within this region of interest in Figure 8a. In our analysis all the simulations are done for the voltage range 0V to 0.3V (from Figure 1a we see that assumed threshold voltage V_{th}*~0.3V*). In all the simulations below we define a device as a super-threshold device if it uses the conventional halo and retrograde doping profile and it is

optimized for the operation in the linear and saturation regions (above V_{th}~*0.3V*) of a MOSFET. Here we have tried to demonstrate that if the operation of this super-threshold device is shifted to its subthreshold region (below V_{th}~*0.3V* range) without changing the doping profile, the current it can deliver would be significantly less than a device optimized for the operation in the subthreshold region. Here, the device optimized for the subthreshold region operation is defined as a subthreshold device. Figure 13 to Figure 18 show that the current for the voltage range *0V* to V_{th}~*0.3V* provided by a super-threshold device is less than a subthreshold device using our proposed doping profiles.



(a)



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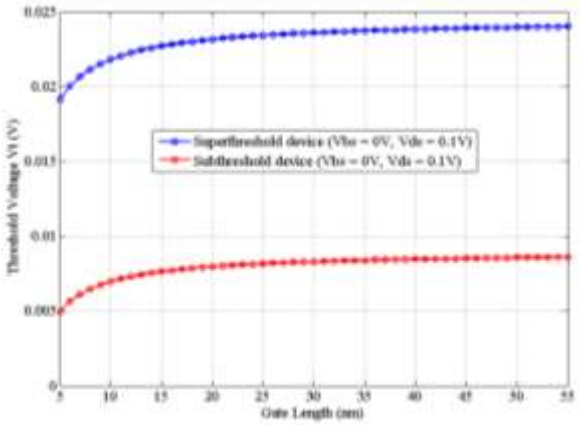

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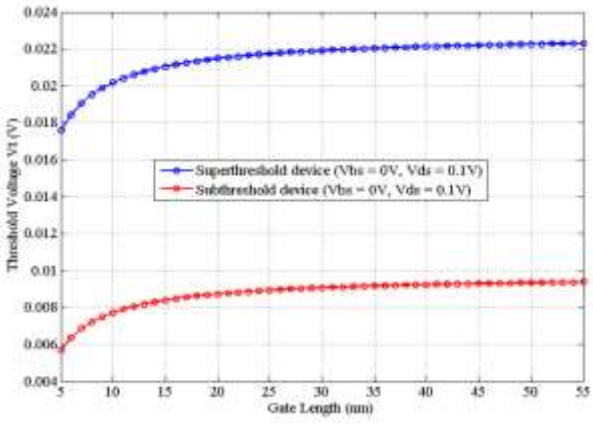
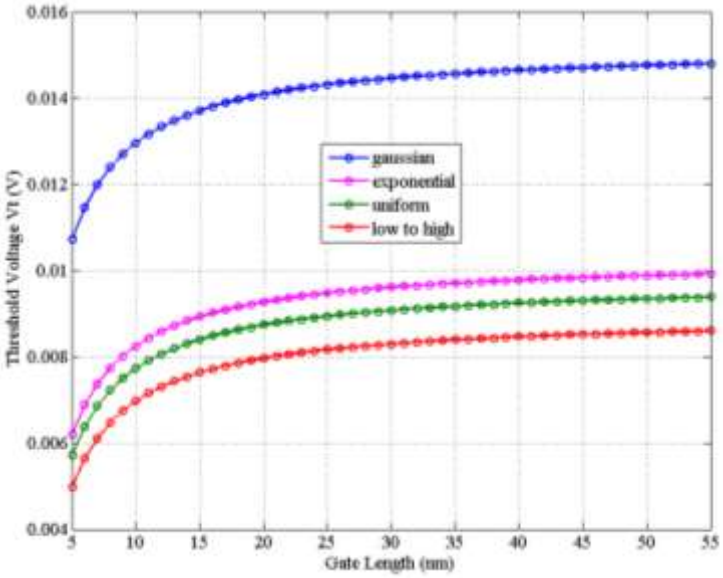
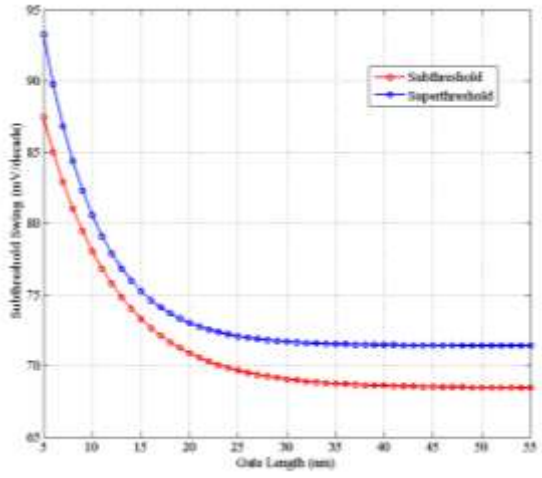


(d)

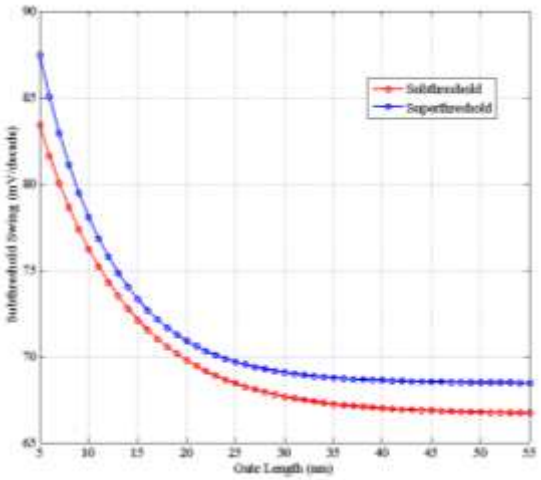


(e)

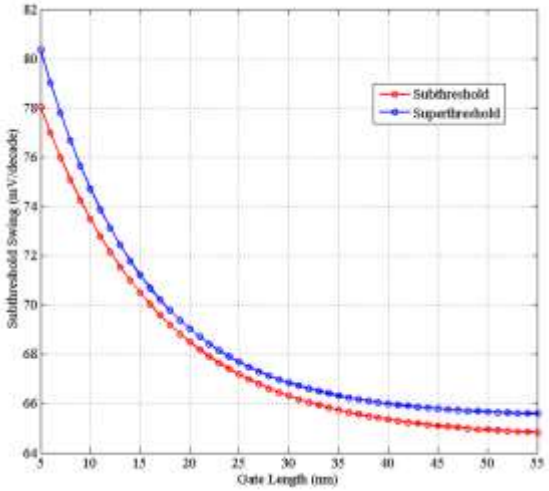
Figure 11: Threshold voltage variation with gate length: (a) exponentially decreasing doping profile, (b) Gaussian doping profile, (c) low to high doping profile (d) uniform doping profile and (e) combined threshold voltage versus gate length for subthreshold device. Where $N_{SD} = 1.7 \times 10^{19}$ and $N_{sub} = 1.0 \times 10^{15}$.



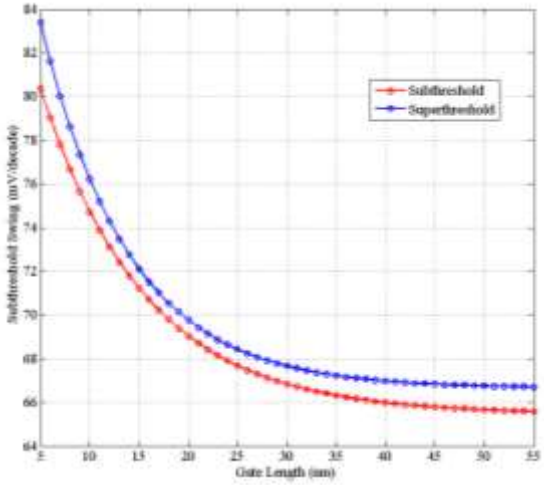
(a)



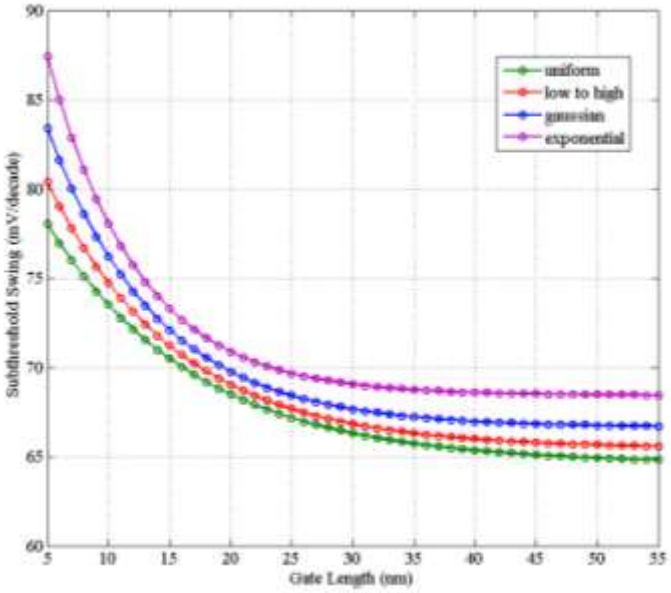
(b)



(c)



(d)



(e)

Figure 12: SS variation with gate length for subthreshold and super-threshold device: (a) exponentially decreasing doping profile, (b) Gaussian doping profile, (c) low to high doping profile (d) uniform doping profile and (e) combined SS versus gate length for subthreshold device at constant I_{off} = *1nA/μm*. Where L_{eff} = *50 nm*, W_{eff} = *1μm*, doping density at source and drain region $N_{SD} = 1.7 \times 10^{19}$, t_{ox} = *1nm*, *T = 300 K*, $\sigma 1_{y-ch} = 21\ nm$ $\sigma 1_{x-ch} = 10\ nm$ and V_{dd} = *0.2 V*.

Figure 11 shows how threshold voltage varies with the change of the gate length. Super-threshold device shows higher threshold voltage as compared to the subthreshold device for all the proposed doping profiles. Therefore, the proposed doping profile for the subthreshold device improves (lowers) the threshold voltage that would lead to higher ON current and faster transition to the ON state. From Figure 11 it can be observed that with the decrease of channel length the threshold voltage also decreases for both super-threshold and subthreshold devices. Figure 12 shows the subthreshold swing versus gate length plot for different doping profiles. This figure provides an insight of the subthreshold swing of a device with the proposed doping. Figure 13 shows the I_{on} versus V_{ds} plot for four different doping profiles for the super-threshold and the subthreshold devices. For all four cases the subthreshold device shows higher ON current compared to the super-threshold device. Among the four doping profiles uniform doping profile gives the highest ON current and exponentially decreasing doping profile gives the lowest ON current for both the super-threshold and subthreshold devices.

Table 1: Intrinsic Delay of Gate Length *50 nm*

Parameter / ***Doping Profile***	***Subthreshold Device***	***Super-threshold Device***
Exponentially Decreasing	*0.209 ps*	*0.310 ps*
Gaussian	*0.104 ps*	*0.155 ps*
Low to High	*0.097 ps*	*0.014 ps*
Uniform	*0.00194 ps*	*0.00282 ps*

Table 2: R_{eff} and C_{eff} Sub Components of Delay Value

Parameter / ***Doping Profile***	***Subthreshold Device R_{eff}***	***Subthreshold Device C_{eff}***
Exponentially Decreasing	*≥99.99%*	*≤ 0.01%*
Gaussian	*≥99.98%*	*≤ 0.02%*
Low to High	*≥99.96%*	*≤ 0.04%*
Uniform	*≥99.999%*	*≤ 0.001%*

Table 3: Tabulated I_{on} at constant I_{off} =1nA/μm

Parameter / ***Doping Profile***	***Subthreshold Device I_{on} (A/μm)***	***Super-threshold Device I_{on} (A/μm)***
Exponentially Decreasing	7.4×10^{-6}	5.0×10^{-6}
Gaussian	1.48×10^{-5}	1.0×10^{-5}
Low to High	1.6×10^{-5}	1.1×10^{-5}
Uniform	8×10^{-4}	5.5×10^{-4}

Table 1 provides the comparison of the intrinsic delay of the device for all the proposed doping profiles. It is observed that for all cases the subthreshold device has lower delay than the super-threshold device. Among the four options the uniform doping profile gives the lowest delay and exponentially decreasing doping profile gives the highest delay. Table 2 shows the contribution of R_{eff} and C_{eff} subcomponent of intrinsic delay value. Intrinsic delay value of the proposed doping profile based device have been calculated using the equation below.

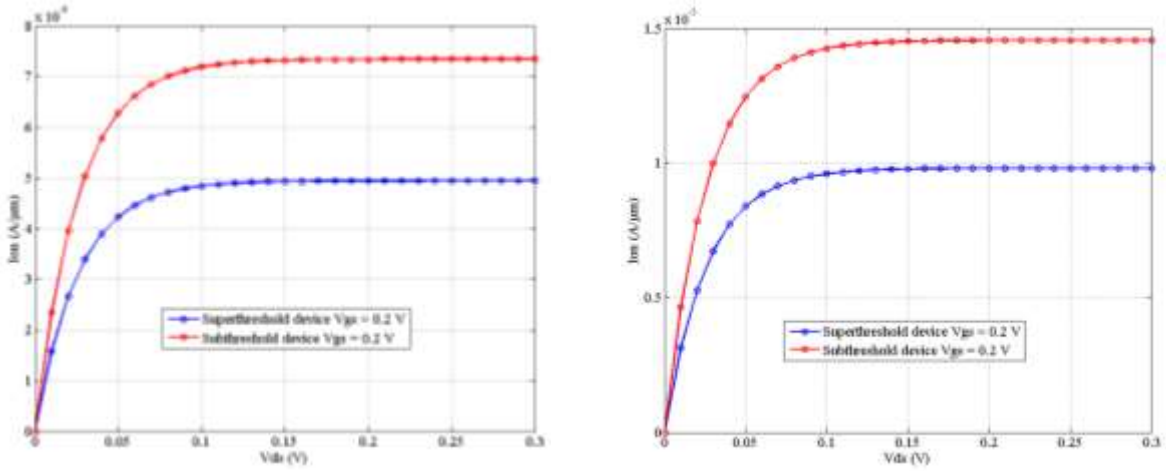
$$Intrinsic\ delay = \frac{Maximum\ gate\ capacitance\ \times V_{dd}}{Maximum\ saturation\ current}$$

The gate delay (or propagation delay) is divided into two terms: the intrinsic gate delay and the (external) gate load delay. The intrinsic gate delay depends on the physical characteristics of the MOSFET transistors. The load delay includes the slowing effect of the load on the gate propagation delay. Therefore, the intrinsic gate delay equals the propagation delay under zero load condition. Already from the *0.25μm* technology generation, the interconnect delay began to surpass the intrinsic gate delay. It is clear that, for state-of-the-art technologies, the gate delay is no longer the limiting factor for the circuit speed. Only, when a spacer with an optimized dielectric constant is used, the intrinsic gate delay shows a relatively strong dependency on the gate capacitance rather than on the drive current. Total effective capacitance C_{eff} is consist of depletion capacitance C_{dep} and the inner fringe capacitance C_{if}. In our proposed subthreshold device structure, there is no double halo doping to reduce the impact of inner fringe capacitance. But for the super-threshold device the inner fringe capacitance value will be comparatively higher than the subththreshold device. So the capacitive dependence of intrinsic delay is higher in the super-threshold device compared to the subthreshold device. Even though the capacitance impacts are small the C_{dep} part contributes more compared to C_{if} part in intrinsic delay calculation.

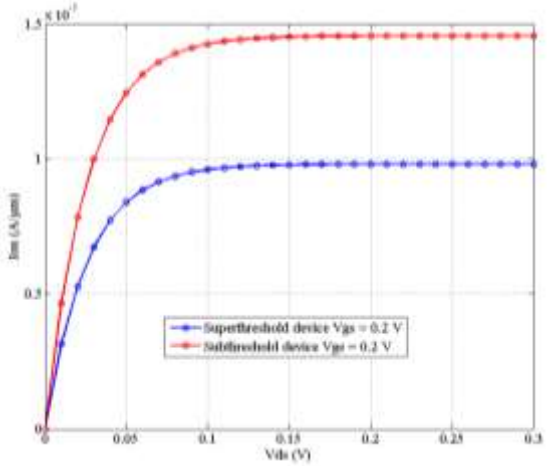
In Table 3 we have tabulated the subthreshold and super-threshold Ion value at a constant $I_{off} = 1nA/\mu m$. For the same I_{off}, the better the subthreshold slope the better is the device. In Figure 12, we have plotted the subthreshold slope for both the subthreshold device and the super-threshold device. From Figure 12 it is evident that the subthreshold slope of the devices using the proposed doping profiles is always better than the super-threshold device and hence it will deliver more I_{on}. Since our interest is in the region below the threshold voltage, we are not interested in the exact value of the threshold voltage, as long as we meet a predefined I_{off}. The work function of both the subthreshold and the super-threshold devices has been adjusted so that it gives an $I_{off} = 1nA/\mu m$.

In all of our simulations the same gate work function has been used and henceforth I_{off} will remain constant. It should also be noted that as the reverse bias increases, I_{off} decreases (due to increasing V_{th}). As a result, the peak doping concentration A_p has to be commensurately lowered to ensure I_{off} = *1nA/µm*. A peak doping concentration of $A_p = 2\times10^{19}\ cm^{-3}$ and $N_{sub} = 10.4\times10^{13}$ gives an I_{off} = *1nA/µm*. Finally, it is evident that our doping profiles offer a fundamental improvement in Ion at constant I_{off}.

In this design we applied the same four doping profiles in the Y dimension (towards the depth) of the device for both the super-threshold and subthreshold operations for better comparison in each case of the four different profiles. In the X direction (along channel length), for super-threshold operation high-doped double halo effect at the source and drain ends has been considered and peak doping is varied. In case of the subthreshold device operation there is no high-doped double halo doping. Only the peak doping is varied and low doping is present at the source and drain ends. Figure 14 shows the variation of I_{on} with the variation of the peak doping density (A_p) in the super- and sub-threshold devices for the four proposed doping combinations.



(a) (b)



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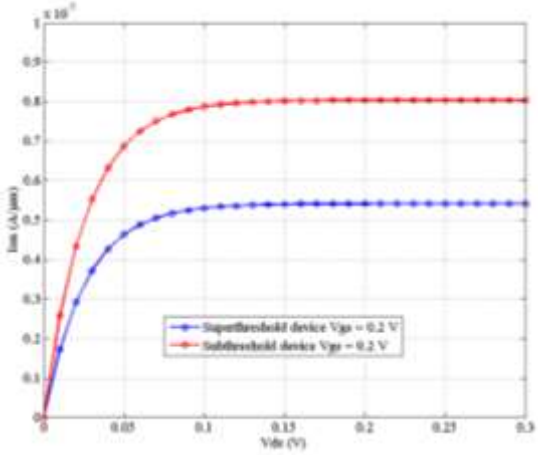

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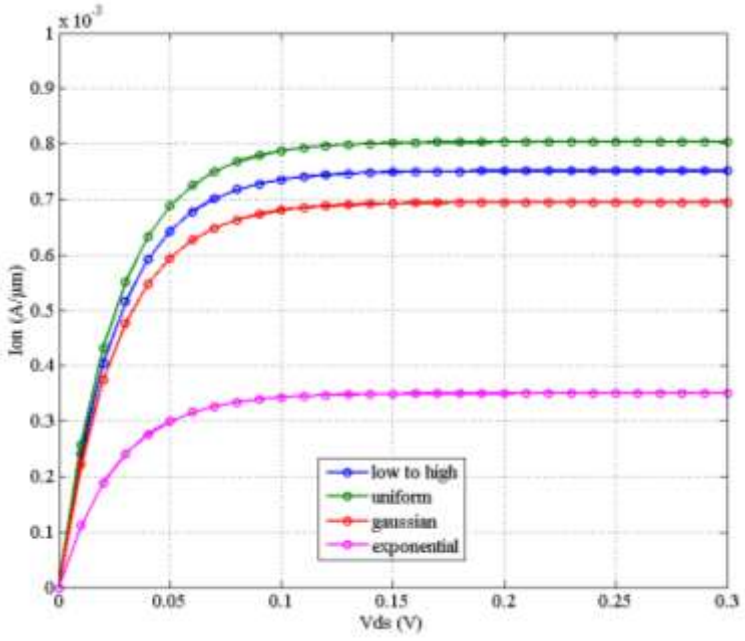


(e)

Figure 13: I_{on} variation with V_{ds} for subthreshold and super-threshold device: (a) exponentially decreasing doping profile, (b) Gaussian doping profile, (c) low to high doping profile (d) uniform doping profile and (e) combined I_{on} variation with V_{ds} for subthreshold device at constant I_{off} = $1nA/\mu m$. Where $L_{eff} = 50\ nm$, $W_{eff} = 1\mu m$, doping density at source and drain region $N_{SD} = 1.7 \times 10^{19}$, $t_{ox} = 1nm$, $T = 300\ K$, $\sigma 1_{y-ch} = 21\ nm$ $\sigma 1_{x-ch} = 10\ nm$ and $V_{dd} = 0.2\ V$.

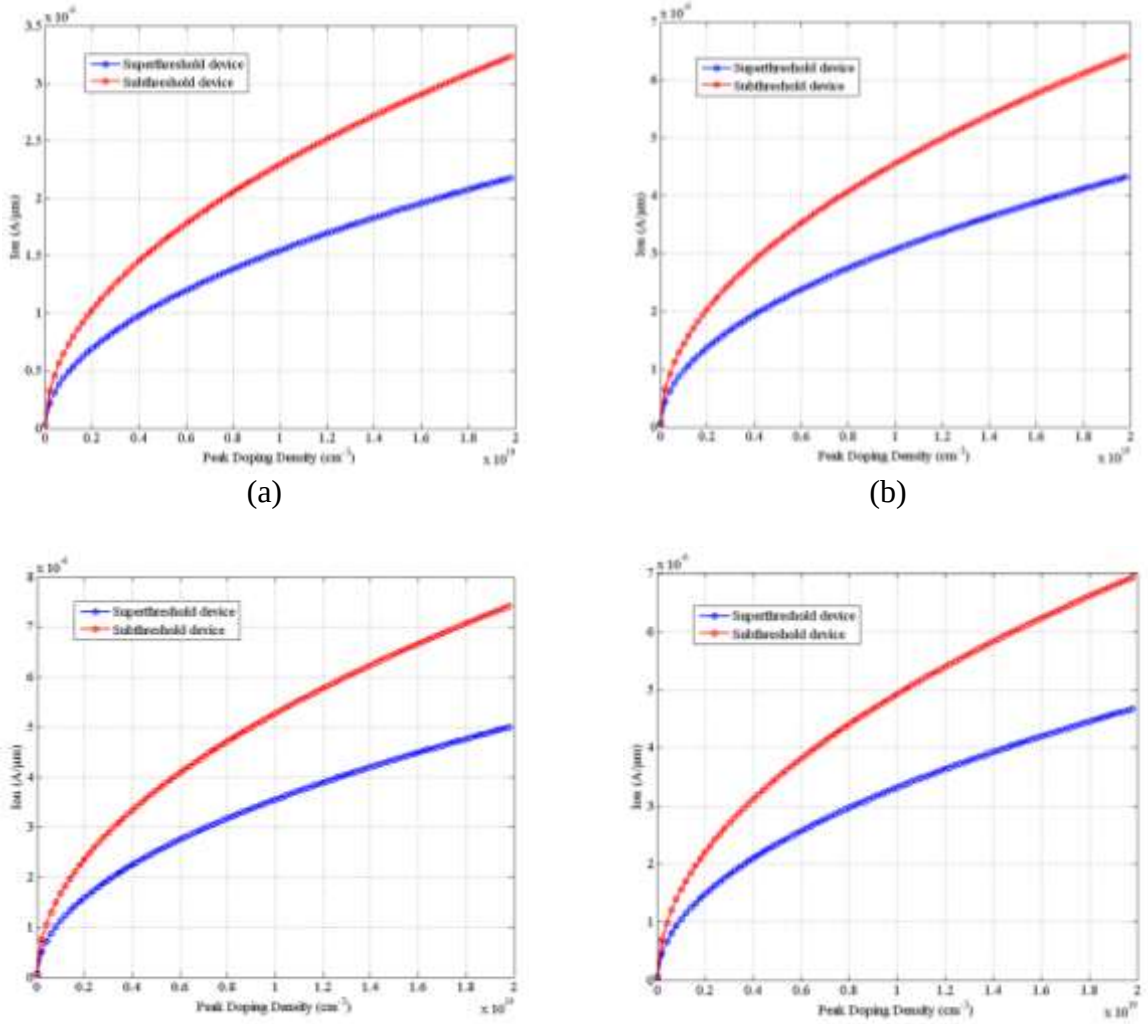


Figure 14: I_{on}-Peak doping density for super- and sub-threshold device: (a) exponentially decreasing doping profile, (b) Gaussian doping profile, (c) low to high doping profile and (d) uniform doping profile at constant $I_{off} = 1nA/\mu m$. Where $L_{eff} = 50\ nm$, $W_{eff} = 1\mu m$, doping density at source and drain region $N_{SD} = 1.7 \times 10^{19}$, $t_{ox} = 1nm$, $T = 300\ K$, $\sigma 1_{y-ch} = 21\ nm$ $\sigma 1_{x-ch} = 10\ nm$ and $V_{dd} = 0.2\ V$.

From Figure 14 it has been observed that as the peak doping decreases I_{on} decreases at the same time. The decreasing rate and magnitude of I_{on} for subthreshold device is smaller than the super-threshold device. Higher I_{on} for subthreshold device than super-threshold device makes the

circuit faster. Doping level of the channel is very critical as can be concluded from the Figure 14. As the doping density goes down and becomes close to zero, I_{on} is significantly reduced leading to very slow operation, and logic switching may not be possible at such low level of current. For standard device the peak doping has been chosen to be $A_p = 2 \times 10^{19}$. From Figure 14 it is observed that for each of the four doping profiles I_{on} is higher in the subthreshold device compared to the super-threshold device.

From the analysis of Figure 14 we can also observe among the four doping profiles which one offers better performance in cases of the super-threshold and the subthreshold circuits. For better understanding and easy interpretation we have produced the graphs of Figure 15 using the same data of Figure 14 to observe the variation of I_{on} with the peak doping density (A_p) for the four doping profiles for subthreshold devices. It is observed that I_{on} demonstrates the same trend for the four doping profiles for subthreshold devices. In subthreshold devices uniform doping in the Y direction provides highest I_{on} among the four doping options. With exponentially decreasing doping density in the Y direction I_{on} is the lowest among the four options.

From Figure 14 and Figure 15 it is observed that for all four doping options I_{on} in the subthreshold device is significantly higher than in the super-threshold device. This observation illustrates the suitability of the proposed doping scheme for the subthreshold device operation. Junction capacitance of the device is another important factor for both the super-threshold and the subthreshold devices. It has been noted that by decreasing the peak doping density the junction capacitance can be reduced. Since the subthreshold devices according to our proposed doping scheme would have low doping level at the source and drain junctions, the junction capacitance will be lower than the super-threshold device that has higher doping density at the source and drain ends.

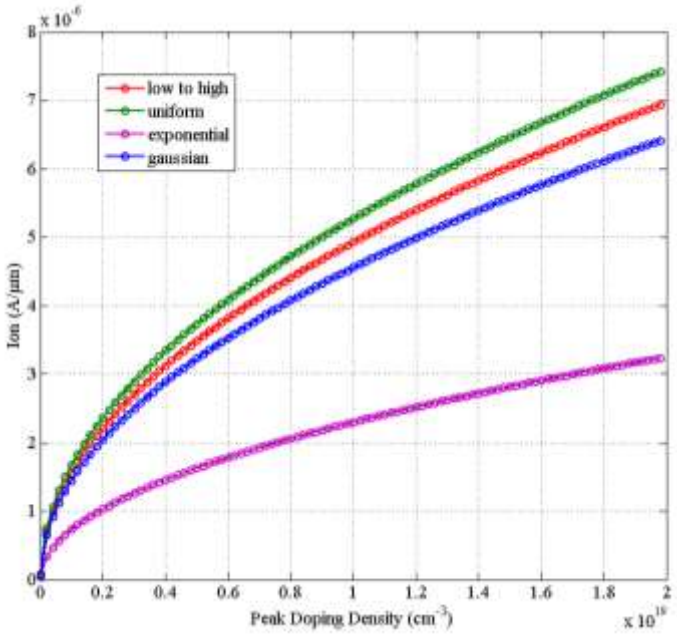


Figure 15: Combined Ion-peak doping density comparison for among four different doping profiles for subthreshold operation at constant $I_{off} = 1nA/\mu m$.

Gate bias voltage (V_{gs}) is another important factor for device performance. Figure 16 shows the variation of Ion with the variation of V_{gs}. Here, I_{on}- V_{gs} variation has been plotted for both super- and sub-threshold devices using the four proposed doping profiles for comparative and qualitative analysis. It has been observed that the optimized subthreshold device has higher Ion compared to the super-threshold device for the same bias voltage at the gate in all cases. From the data of Figure 16 we can derive the graph of Figure 17, which shows, I_{on}-V_{gs} plots for the subthreshold devices for the four doping profiles. Again it is observed that among the four doping profiles uniform doping in the Y direction provides the highest I_{on} and the exponentially decreasing doping profile provides the lowest I_{on} for a specific V_{gs}. In general, the I_{on} of the subthreshold device is much higher than in the super-threshold device for all doping profiles under investigation.

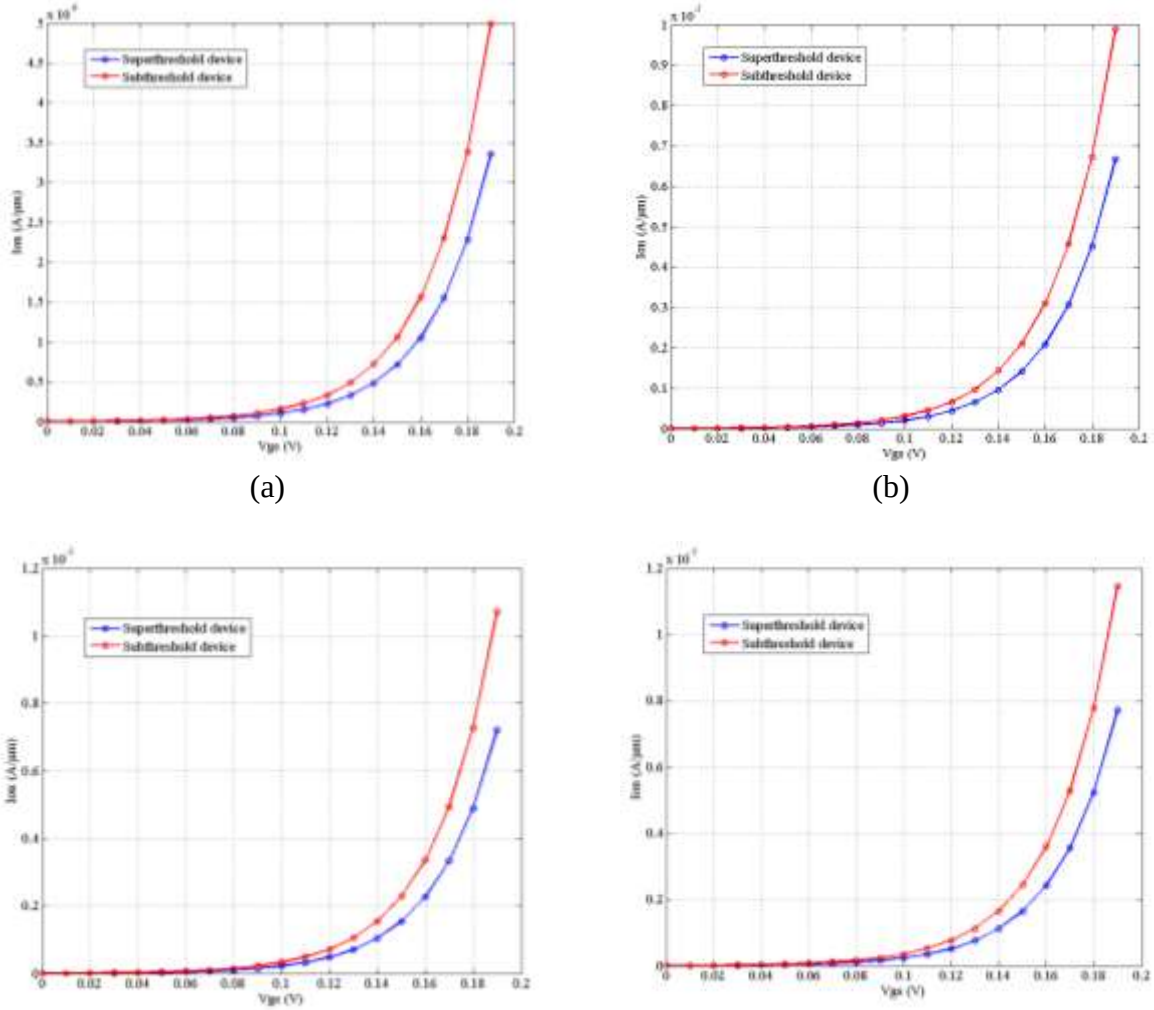


Figure 16: I_{on}-V_{gs} for superthreshold and subthreshold device. Figure (a) exponentially decreasing doping profile, (b) Gaussian doping profile, (c) low to high doping profile and (d) uniform doping profile at constant I_{off} = *1nA/μm*. Where L_{eff} = *50 nm*, W_{eff} = *1μm*, doping density at source and drain region $N_{SD} = 1.7 \times 10^{19}$, t_{ox} = *1nm*, *T = 300 K*, $\sigma 1_{y-ch} = 21\ nm$ $\sigma 1_{x-ch} = 10\ nm$ and V_{dd} = *0.2 V*.

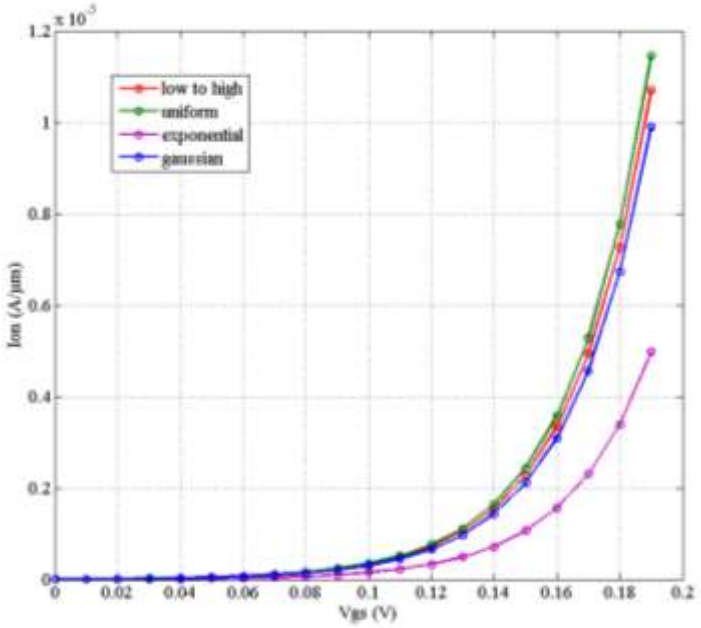
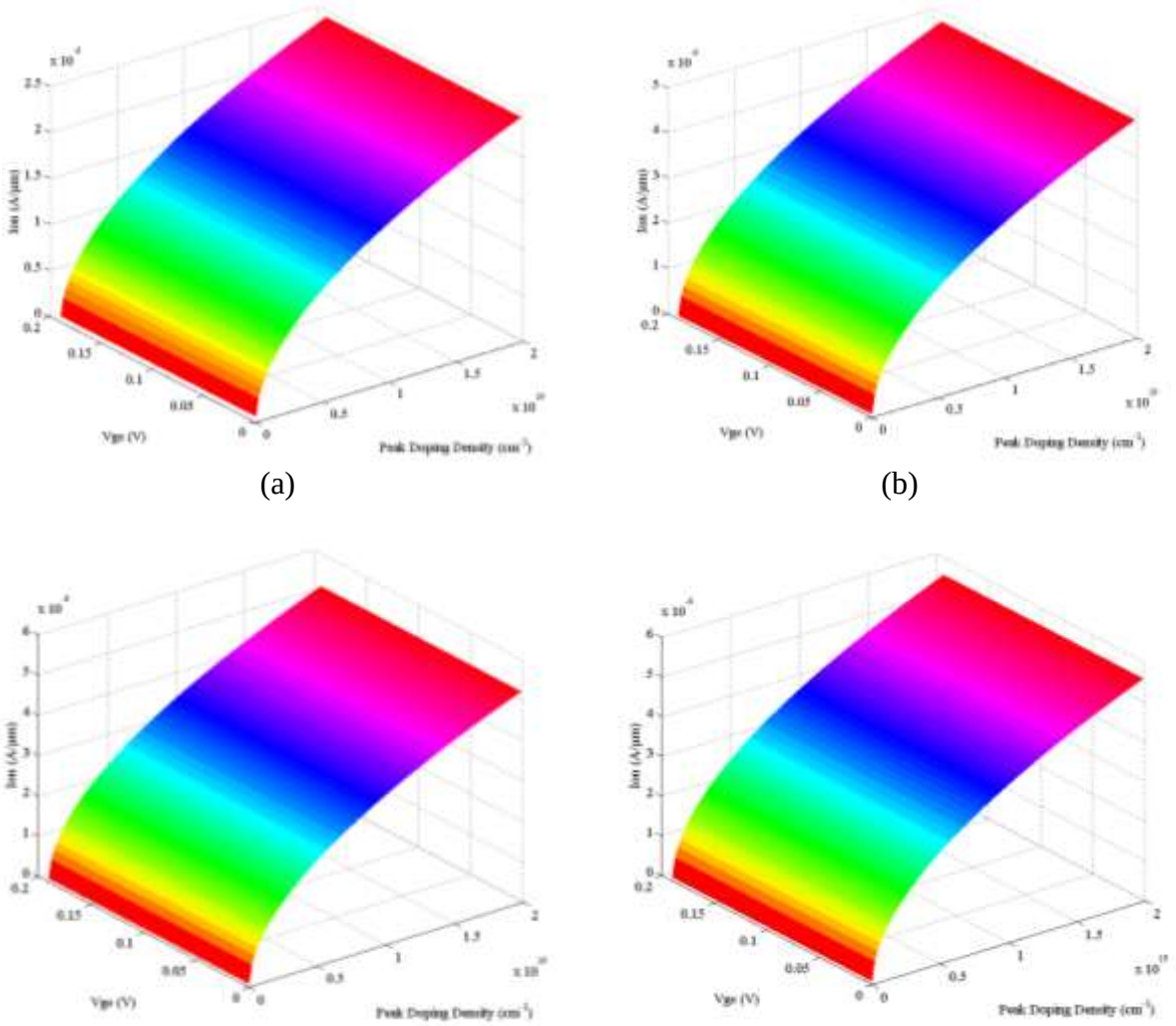


Figure 17: I_{on}-V_{gs} comparison among four different doping profile for subthreshold operation at constant $I_{off} = 1nA/\mu m$.

From Figure 13 to Figure 17 the impacts of the peak doping density (A_p) the gate bias voltage (V_{gs}) and V_{ds} on I_{on} have been analyzed for both super- and sub-threshold devices. We have identified these two key parameters (A_p and V_{gs}) to optimize the performance of the subthreshold circuits. To illustrate the prospects of the proposed doping scheme for the subthreshold circuits, we have analyzed the combined impacts of A_p and V_{gs} on I_{on} in the subthreshold device for the four different doping profiles. From the 3-D plot in Figure 18, which shows the combined impact of A_p and V_{gs} on I_{on}, the optimum value of I_{on} can be selected for a specific set of peak doping density and V_{gs}.



(a) (b)

(c) (d)

Figure 18-11: I_{on}-V_{gs}-peak doping density for subthreshold device. Figure (a) exponentially decreasing doping profile, (b) Gaussian doping profile, (c) low to high doping profile and (d) uniform doping profile.

3.4 Conclusion

In this chapter we have proposed a new doping scheme for the subthreshold device. The proposed scheme is characterized by Gaussian doping profile along the length of the channel (X direction) and four alternative doping profiles (exponentially decreasing, Gaussian, low-to-high, and uniform) across the depth of the device (Y direction). Therefore, under the proposed doping

scheme we get four doping combinations for the subthreshold device. In conventional super-threshold device halo and retrograde channel doping profile along the channel length and high-to-low or uniform doping profiles along the depth are usually used to eliminate short channel effects and other unwanted phenomenon [18], [19]. Since non-uniform doping profile is desired to provide better control on the electrical characteristics of the device, in previous work on the subthreshold design, transistors with the above-mentioned conventional doping were operated in the subthreshold region to implement the subthreshold logic [10]. The subthreshold devices operate at very low biasing voltage, which leads to minimal short channel effect. Therefore, high doping near source and drain as in conventional halo and retrograde doping scheme is not necessary for the subthreshold device. This high doping near source and drain will lead to higher junction capacitance, which is not desirable for ultra-low-power operation. Our proposed Gaussian distribution along the channel length would lead to a low doping level at the drain and source ends and it will lower the junction capacitance leading to faster speed and lower power consumption. Similarly, exponentially decreasing doping density towards the bottom surface of the device will lead to lower body capacitance. Other proposed doping profile also improve various other performance parameters. All four proposed doping profiles have been mathematically modeled and their prospects are analyzed. It is observed that the on current (I_{on}) of the subthreshold device with the proposed doping profiles is higher than in super-threshold device for specific values of the drain bias voltage, gate bias voltage and peak doping density.

Based on specific application requirements in ultra-low-power regime we may need different I_{on} (higher or lower). The proposed doping scheme provides four different options for the subthreshold circuit. Any one of the options might be the perfect choice for a specific low power application. We anticipate that with the current progresses in the fabrication process it would be

possible to incorporate the proposed doping profiles in the design of ultra-low-power circuits. This chapter presents a study of the doping profile optimization in the channel for subthreshold voltage operation. However, here we only show the variation of I_{on} with V_{gs}, V_{ds} and peak doping density. Also we have shown other factors like subthreshold swing, threshold voltage variation, intrinsic delay, R_{eff} and C_{eff} subcomponent of intrinsic delay and tabulated I_{on} value at constant I_{off} = $1nA/\mu m$. Here, we have explained the basic concept of the new doping scheme and analyzed the prospects of the new doping profiles for the subthreshold circuits. Our future work will cover all other factors and parameters that would impact the doping process and requirements in ultra-low-power subthreshold circuits.

CHAPTER 4

THRESHOLD VOLTAGE CALCULATION

One of the important aspects of integrated circuit design is the doping profile of a transistor along its length, width and depth. Devices for super-threshold circuits usually employ halo and retrograde doping profiles in the channel to eliminate many unwanted effects. Devices for subthreshold circuits do not require halo and retrograde doping profiles. This will reduce the number of steps in the fabrication process, parasitic capacitance and substrate noise dramatically. This chapter introduces one of the four doping profile for devices to be used in subthreshold circuits. The proposed scheme addresses doping variations along all the dimensions of the device. This new doping scheme proposes to employ Gaussian distribution of doping concentration along the length of the channel with highest concentration at the middle of the channel. The doping concentration across the depth of the device is exponentially decreasing with channel surface at the highest concentration. The proposed doping scheme keeps the doping concentration along the width of the device uniform. Results show that the optimized device with the proposed doping profile offers higher ON current in the subthreshold device. In this chapter, threshold voltage modelling has been performed and a comparative analysis is presented between super-threshold and sub-threshold devices threshold voltages. We have also analyzed the subthreshold swing characteristics of the device with the proposed doping profiles. Our analysis shows that better subthreshold swing can be achieved using our new doping profile based subthreshold design.

4.1 Introduction

Proper ion implantation or doping is one of the most critical design decisions for deeply scaled CMOS devices. For emerging system-on-chip (SOC) applications doping is very challenging due to the conflicting requirements of the analog and digital circuits. It is observed that with lateral asymmetric channel (LAC) doping the total gate capacitance of a transistor is reduced by almost 10% in the saturation region at 100nm technology node compared to the conventional MOSFETS [6], [7]. Transistor capacitances have significant influences on its RF performance. In [8], it is demonstrated that the electron velocity in the inversion layer of a novel thin film silicon-on-insulator (SOI) device is affected by doping profile. The test SOI structure used LAC doping profile. With the growing demand for ultra-low-power (ULP) circuits and systems, there is a critical need to engineer MOSFET devices to be operated in the sub-threshold region of the conventional devices. The existing doping schemes for devices that are being operated in the saturation region (significantly above the threshold voltage) may not be suitable for devices to be operated in the subthreshold region.

In conventional integrated circuits, short-channel devices are usually optimized for operation in super-threshold region to ensure higher mobility, lower drain-induced barrier lowering (DIBL), reduced leakage, and minimal threshold voltage roll-off. However, a transistor optimized for super-threshold circuit may not be optimal for the subthreshold region where effects like DIBL, threshold voltage roll-off and electron/hole tunneling are much less significant [10]. As a consequence, high doping traditionally used in super-threshold device to overcome the short-channel effect (SCE) will not be critical for subthreshold operation [11]. In super-threshold device, the main functions of halo and retrograde dopings are to reduce DIBL, prevent body punchthrough and control the threshold voltage of the device independent of its subthreshold slope. Since DIBL,

body punchthrough and threshold voltage variation are not severe in subthreshold device due to lower supply voltage, the halo and retrograde doping is not required for such designs. High to low doping profile [10] has been proposed for subthreshold operations. For subthreshold circuit operation lower subthreshold swing and internal device capacitances are critical. However, existing doping profiles do not offer any means to address these critical needs of ULP circuits.

An attempt has been made by our group to explore a set of new doping schemes for devices to be used in the subthreshold circuits. In [20-22], we have outlined the general principle of four new doping schemes. Each of these doping scheme involves determining two doping profiles for the X-direction (along the channel length) and Y-direction (across the depth) of the device. In these 3-dimensional schemes, we also prescribe a constant doping concentration across the width of the device at any depth. In [20-22], we have presented detail analysis of one doping scheme with Gaussian distributions of doping profile in both X and Y directions.

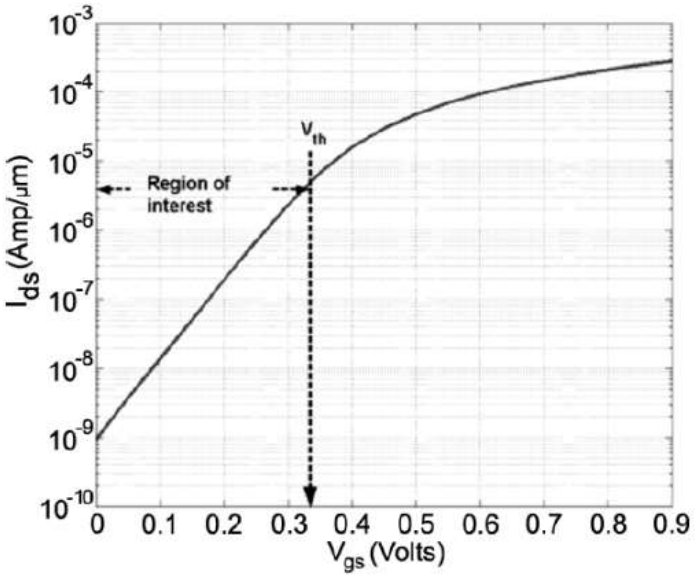


Figure 19: Subthreshold logic region of operation [10].

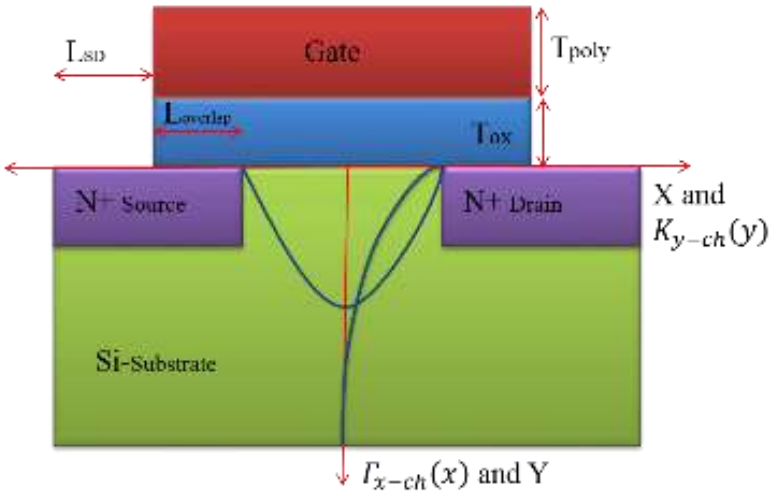


Figure 20: X-direction Gaussian and Y-direction Exponentially decreasing doping. Where, L_{eff} = 50 nm, $W_{eff} = 1\mu m$ and $t_{ox} = 1nm$.

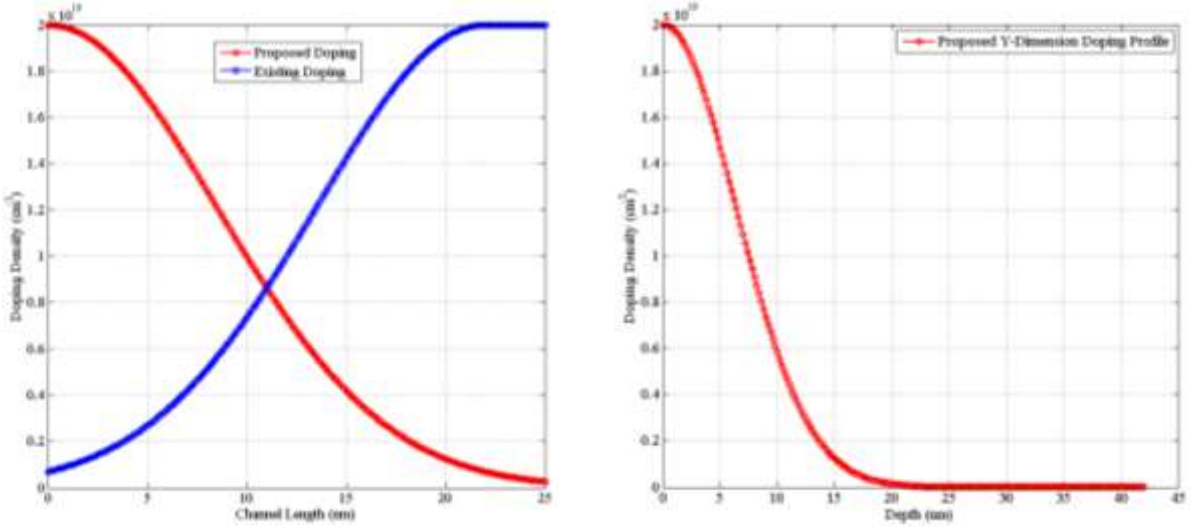
4.2 Subthreshold Doping Scheme

The focus of this chapter is to illustrate the doping scheme with two doping profiles illustrated in Figure 20. In this section, we have mathematically analyzed the proposed doping profiles in the X and Y direction for the subthreshold device operation. A super-threshold device is a device that is operated (ON state) with a voltage above the threshold voltage of a conventional MOSFET. In conventional circuit design, any device would be considered OFF if the gate voltage is under 0.3V for a device with a threshold voltage $V_{th} \sim 0.3V$ as shown in Figure 19. On the other hand the operating region of a subthreshold device would be completely moved to the subthreshold region (*0V* to *0.3V* in the case of Figure 19). Within that subthreshold region the subthreshold device must have distinguishable OFF and ON states. Therefore, our area of interest in Figure 19 is the subthreshold region, where a voltage very close to *0V* will be considered as the OFF state and a voltage close to V_{th} would be considered as the ON state. A steeper subthreshold slope translates to higher I_{ON}/I_{OFF} ratio within this region of interest in Figure 19. In our analysis all the

simulations are done for the voltage range *0V* to *0.3V* (from Figure 19 we see that the assumed threshold voltage for the device to be operated in the super-threshold region is V_{th}*~0.3V*). In all the simulations below we define a device as a super-threshold device if it uses the conventional halo and retrograde doping profile and it is optimized for the operation in the linear and saturation regions (above V_{th}*~0.3V*) of a MOSFET. Here we have tried to demonstrate that if the operation of this super-threshold device is shifted to its subthreshold region (below V_{th}*~0.3V* range) without changing the doping profile, the current it can deliver would be significantly less than a device optimized for the operation in the subthreshold region. Here, the device optimized for the subthreshold region operation is defined as a subthreshold device.

A technique based on the subthreshold current–voltage (I-V) characteristics to extract 2-D doping profiles is proposed in [14]. Here we propose new doping profiles for subthreshold device operation using similar approach. We modeled MOSFET subthreshold current based on the proposed doping profiles. The formulation of the model is shown for NMOS transistor and can be easily applied to PMOS transistor. Device structure with Gaussian shaped channel doping along the X dimension (length of the channel) has been considered as shown in Figure 21a. In conventional super-threshold device, the doping concentration at the middle of the device is the lowest and at the source and drain ends it is the highest (blue line). In our proposed scheme for subthreshold device (red line), the middle of the channel has highest doping concentration and the drain and source ends have the lowest. The variation of doping concentration from the middle towards the ends is of Gaussian shape under our proposed scheme. Across the vertical middle line of the device the doping is symmetrical. In this design, for the Y direction (along the depth of the device) we have consider the variation of doping concentration as depicted in Figure 21b, where

the doping density is exponentially decreasing from the channel surface towards the body of the device as shown in Figure 21b.

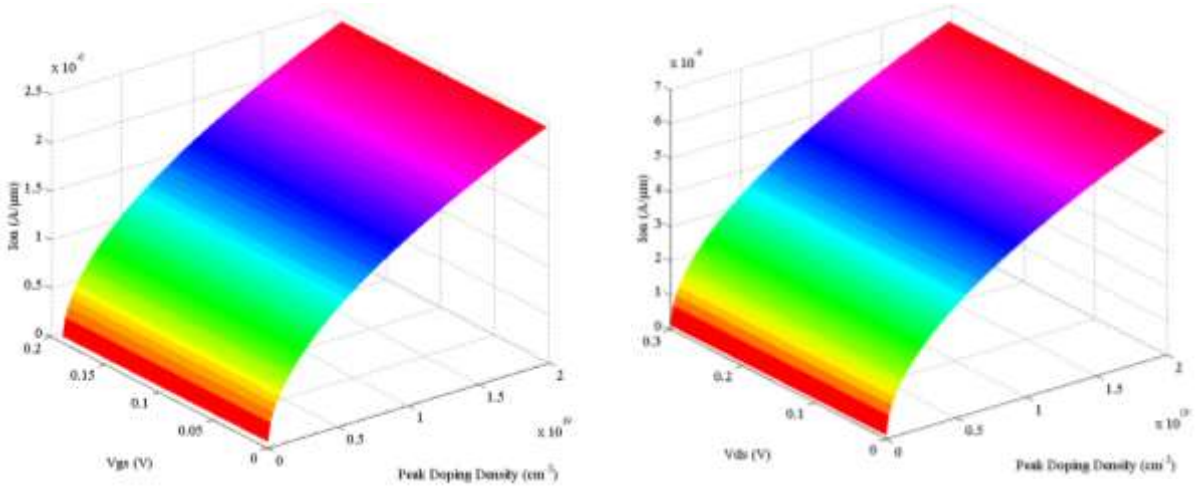


(a) (b)

Figure 21: (a) Doping distribution along X-dimension – from the middle of the channel to drain (source) end and (b) Doping distribution along Y-direction from the top surface of the channel towards the bottom surface of the substrate. Red is for the proposed doping profile for subthreshold device and blue is of conventional device**.**

In this design we kept the Y dimension doping profiles same for both super-threshold and subthreshold operation for better comparison. The 3-D plot in Figure 22 shows the changes of I_{on} with the variations of gate bias voltage and the peak doping density. Based on the 3-D plot of Figure 22, the optimum value of I_{on} can be found for a specific set of peak doping density and V_{gs} values. For the super-threshold operation high doped double halo effect has been considered and peak doping is varied. In case of subthreshold device operation there is no highly doped double halo doping at the source and drain ends [21]. Only the peak doping is varied and low doping is present at the source and drain ends. It has been found that as the peak doping decreases, I_{on} decreases at the same time. The decreasing rate and magnitude of I_{on} for the subthreshold device

is smaller than the super-threshold device. Higher I_{on} for the subthreshold device than the super-threshold device makes the circuit faster. Doping level of the channel is very critical as can be concluded from the Figure 22. As the doping density goes down and becomes close to zero, I_{on} is significantly reduced leading to very slow operation and logic switching may not be possible at such low level of current. With the decrease of peak doping the number of free charge carrier becomes very low in the channel areas, which eventually reduces the on current. However, due to the higher doping just below the gate area inversion layer forms very promptly to turn the device on. As a consequence of the abundance of electrons in the channel area higher on current with small V_{dd} *(0.3 V)*, is possible. For standard device the peak doping has been chosen to be $A_p = 2 \times 10^{19}$and the doping density at the source and drain regions is $N_{sd} = 2 \times 10^{19}$. Numerical simulation has been done at temperature *300K* for obtaining various parameters.



(a) (b)

Figure 22: I_{on}-V_{gs}-peak doping density for subthreshold device and I_{on}-V_{ds}-peak doping density for subthreshold device.

Figure 22 also shows the variation of I_{on} with the variation of V_{gs}. It has been found that the optimized subthreshold device has higher on current compared to super-threshold device for

the same bias voltage at the gate [21]. Junction capacitance of the subthreshold device is another important factor for both super-threshold and subthreshold devices. It has been predicted that by decreasing the peak doping the junction capacitance can be reduced. Because of low doping at the source and drain junctions of the proposed subthreshold device, the junction capacitance will be lower as well. Based on the 3-D plot of Figure 22, the optimum value of I_{on} can be found for a specific set of peak doping density and V_{ds} values. Subthreshold device shows higher ON current compared to the super-threshold device. Figure 23 shows the variation of the off current with variation of peak doping density. In Figure 23, off current is little higher for the subthreshold device compared to that of the super-threshold device. Since the off current is very low for both the cases, this will not affect the subthreshold circuit operation that much. Figure 24 shows how the threshold voltage will change with gate length at specific body bias and source-drain bias voltage. Random dopant fluctuation is another important factor for device performance, which depends on the vertical and horizontal electric field of the channel. Since the gate voltage and biasing voltage is very small, the impact of both electric fields will not be strong enough to cause random dopant fluctuation in the channel area.

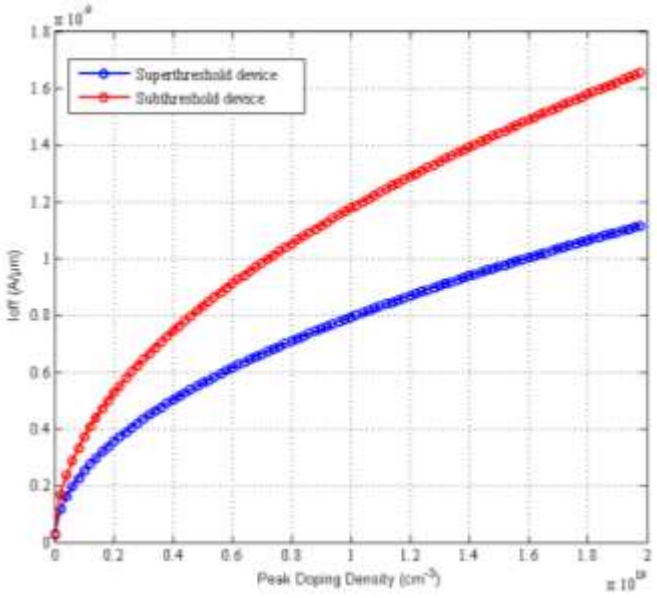


Figure 23: I_{off}-Peak doping density for super-threshold and subthreshold device.

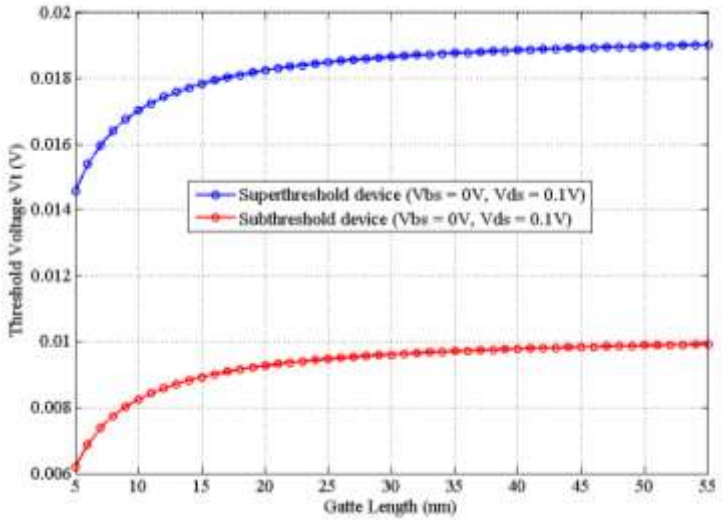


Figure 24: Threshold voltage variation with gate length.

4.3 Threshold Voltage Modelling

The current flowing from the drain to source of the transistor under the threshold voltage is known as the subthreshold current. For super-threshold device, this subthreshold current is considered as the undesired leakage, which is one of the most serious problems in current

nanoscale IC design. For subthreshold device this subthreshold current is the useful current. Due to the exponential dependence of the subthreshold conduction on the threshold voltage (see Figure 19) the variation of the threshold voltage is, therefore, a very critical factor in both conventional and subthreshold devices. In (4.1), V_{bi} is the source/drain built-in potential and N_{sd} is the doping concentration in the lightly doped region.

$$V_{bi} = \frac{kT}{q} \ln\left(\frac{N_{sd} N_{ch}}{n_i^2}\right) \tag{4.1}$$

In (4.2) and (4.3), Φ_{s0} is the surface potential and Φ_{01} is the short-channel surface potential. It is found that potential-barrier lowering is needed in addition to the charge-sharing effect since they describe different contributions to the observed SCE (V_t roll-off) [16].

$$\Phi_{s0} = 2\frac{kT}{q} \ln\left(\frac{N_{sub}}{n_i}\right) \tag{4.2}$$

$$\Phi_{01} = 2\frac{kT}{q} \ln\left(\frac{N_{ch}}{n_i}\right) \tag{4.3}$$

From the quasi 2D model [23] the surface potential Φ_S in short channel device is lowered by $\Delta\Phi_S$ due to source/drain fringing fields. And it is smaller than $2\Phi_B$ (bulk potential) at strong inversion condition. In (4.5), $\Delta\Phi_S$ is the function of the characteristics length l_α and α is the fitting parameter.

$$\Phi_s = \Phi_{s0} - \Delta\Phi_s = 2\Phi_B - \Delta\Phi_s \tag{4.4}$$

$$\Delta\Phi_s = (V_{bi} - \Phi_{s0} + 0.5V_{ds})\left(\frac{1}{\cosh\left(\frac{L_{eff}}{2l_\alpha}\right)}\right) \tag{4.5}$$

$$l_\alpha = \alpha(\Phi_{01} - V_{bs})^{0.25} \tag{4.6}$$

Using charge sharing model the threshold voltage can be expressed as in (15) [16-17].

$$V_t = V_{FB} + \Phi_s + \gamma\sqrt{\Phi_{s0} - V_{bs}}\left(1 - \lambda\frac{X_d}{L_{eff}}\right) \tag{4.7}$$

$$X_d = \sqrt{\frac{2\varepsilon_{Si}}{qN_{cheff}}}\sqrt{\Phi_{s0} - V_{bs}} \tag{4.8}$$

$$\gamma = \frac{\sqrt{2q\varepsilon_{Si}N_{sub}}}{C_{ox}} \tag{4.9}$$

Here V_{FB} is the flat band voltage, Φ_{s0} is the zero bias surface potential, γ is the body factor, X_d is the depletion layer thickness, and λ is a fitting parameter (~1) [16-17]. Φ_s of short channel devices from its zero bias value due to short channel effect like DIBL and V_{th} roll off.

Figure 25 shows how threshold voltage varies with the change of the gate length. Super threshold device shows higher threshold voltage as compared to the subthreshold device. Also comparison has been made for different body biases *(V_{bs} = 0, -0.5V)* for different types of device. Negative body bias improves the threshold voltage for both super-threshold and subthreshold device operation. In both cases, V_{ds} is kept constant to make fair comparison. Proposed doping profile for the subthreshold device improves the threshold voltage, which will lead the device to go to ON state even faster. Figure 26 shows the impact of the fitting parameter λ on the threshold voltage. At $\lambda = 0.1$ the threshold voltage is constant with the variation of the gate length, but for $\lambda = 1$ the threshold voltage significantly varies with the variation of the gate length. Higher λ reduces the threshold voltage in both the cases of super-threshold and subthreshold devices. Figure 27 shows the impact of oxide thickness on the threshold voltage variation. Under proposed doping profile and constant oxide thickness subthreshold device has lower threshold voltage than the super threshold device. Channel length below *25 nm* has more impact on threshold voltage for specific

oxide thickness. Figure 28 shows the impact of uniform substrate doping on the threshold voltage. Higher substrate doping increases the threshold voltage for both super threshold and subthreshold devices. Therefore, uniform substrate doping profile is one of the important performance parameters for tuning the desired threshold voltage for low power subthreshold circuit design.

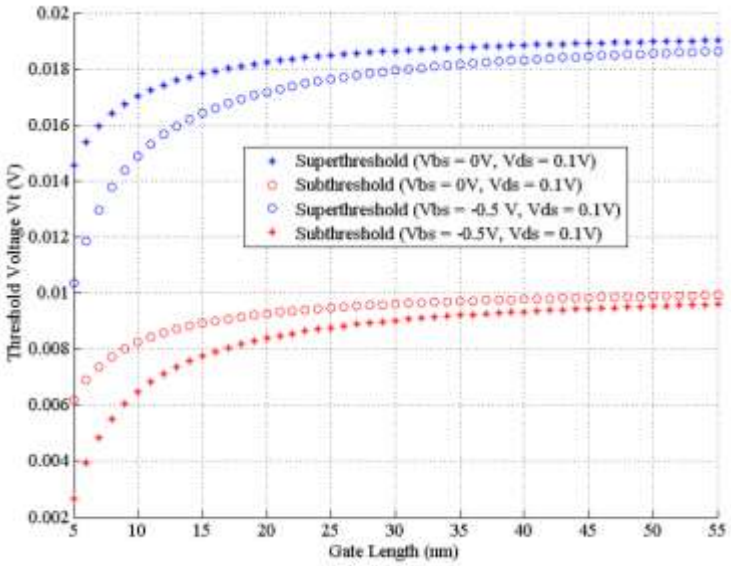


Figure 25: Threshold voltage variation with change of gate length at V_{ds} = *0.1V* and V_{bs} = *0, -0.5V*. Where L_{eff} = *50 nm*, W_{eff} = $1\mu m$, doping density at source and drain region $N_{SD} = 1.7 \times 10^{19}$, t_{ox} = *1nm*, *T = 300 K*.

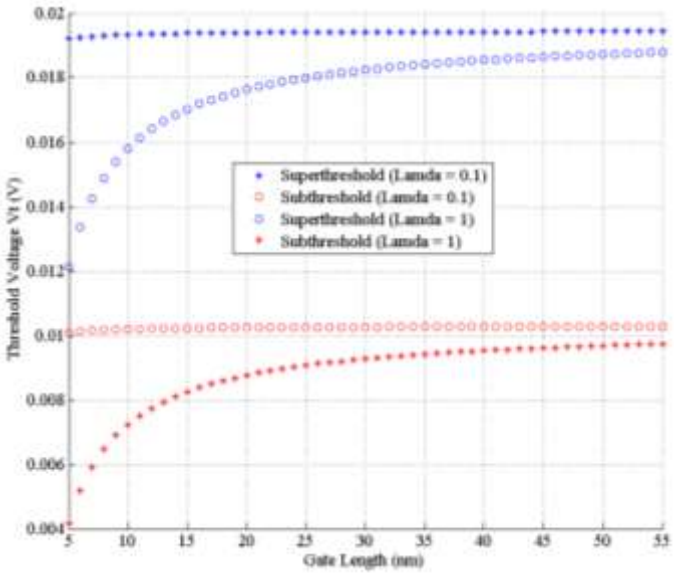


Figure 26: Threshold voltage variation with change of gate length at fitting parameter $\lambda = 0.1$ and 1. Where $L_{eff} = 50$ nm, $W_{eff} = 1\mu m$, doping density at source and drain region $N_{SD} = 1.7 \times 10^{19}$, $t_{ox} = 1nm$, $T = 300$ K, $V_{bs} = 0V$, and $V_{ds} = 0.1V$.

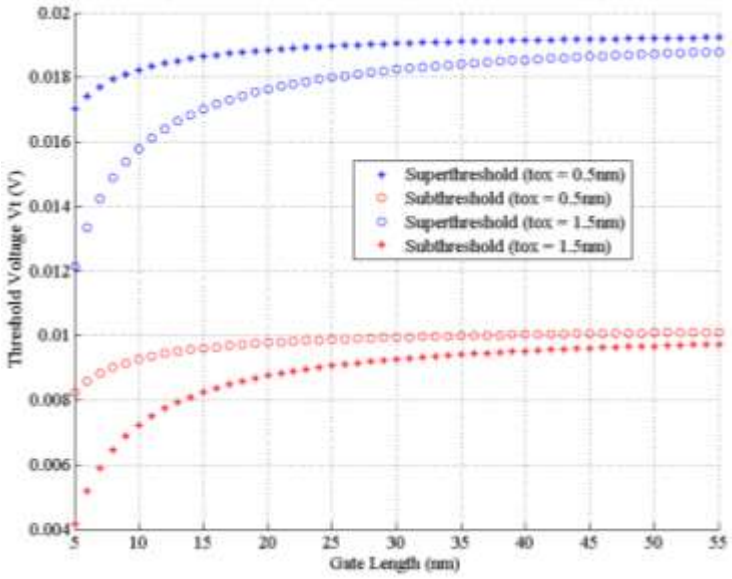


Figure 27: Threshold voltage variation with change of gate length at oxide thickness $t_{ox} = 0.5nm$ and 1.5 nm. Where $L_{eff} = 50$ nm, $W_{eff} = 1\mu m$, doping density at source and drain region $N_{SD} = 1.7 \times 10^{19}$, $t_{ox} = 1nm$, $T = 300$ K, $V_{bs} = 0V$, and $V_{ds} = 0.1V$.

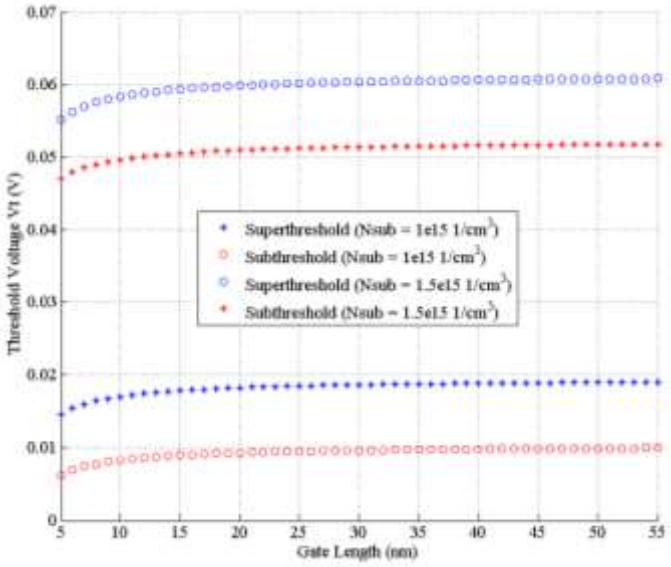


Figure 28: Threshold voltage variation with change of gate length at uniform substrate doping $N_{sub} = 1.0\times10^{15}\ cm^{-3}$ and $1.5\times10^{15}\ cm^{-3}$. Where $L_{eff} = 50\ nm$, $W_{eff} = 1\mu m$, doping density at source and drain region $N_{SD} = 1.7 \times 10^{19}$, $t_{ox} = 0.5nm, 1.5nm$, $T = 300\ K$, $V_{bs} = 0V$, and $V_{ds} = 0.1V$.

4.4 Analysis of Subthreshold Swing Characteristics

Subthreshold swing (S) is defined as the change in gate voltage required for a change in subthreshold current by one decade. Hence, subthreshold swing can be expressed as

$$S = \left(\frac{\partial log I_{sub}}{\partial V_{gs}}\right)^{-1} \tag{4.10}$$

The subthreshold swing (S) for the short channel device, considering the penetration of the drain induced electric field in the center of the channel is given by equation (4.11)

$$S = 2.3V_T\left(1 + \frac{11t_{ox}}{X_d}e^{-\frac{\pi L_{eff}}{(X_d+3t_{ox})}}\right) \tag{4.11}$$

where X_d is the depletion layer thickness, thermal voltage $V_T = kT/q$ *and the* body effect m is given by

$$m = 1 + \frac{3t_{ox}}{X_d} \tag{4.12}$$

Based on the proposed doping profile X_d has been determined and the oxide thickness of *1 nm* is considered to calculate the subthreshold swing for both subthreshold and super-threshold device.

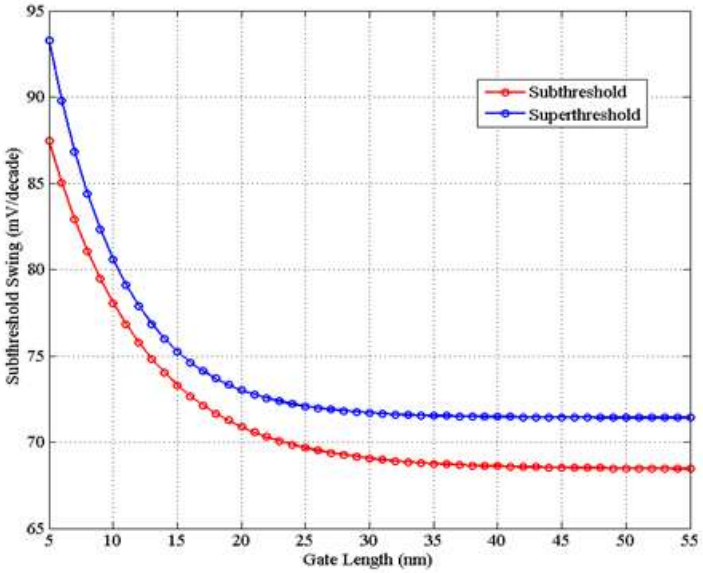


Figure 29: Subthreshold swing versus gate length for super-threshold and subthreshold device.

Figure 29 shows the subthreshold swing versus gate length for super-threshold and subthreshold device. It can be noted that as channel length falls, subthreshold swing start to increase for both subthreshold and super-threshold device. Above *15 nm* channel length subthreshold swing is minimum. Our analysis shows that better subthreshold swing can be achieved using our new doping profile. The subthreshold swing of the redesigned device is always better than the super-threshold device and hence it delivers more I_{on}. However, technology scaling

reaps the high benefits of oxide thickness scaling and channel length scaling. As the oxide is thinned, the gate control on the channel increases thereby improving the subthreshold swing of the device.

4.5 Prospects and Challenges

The proposed doping scheme would bring changes in doping properties along the length (X direction) and depth (Y direction) of the device and keep the doping concentration along the width constant. The doping profile in X direction is kept somewhat constant in most of the previous designs and only the Y direction doping profiles have been varied. We propose a three-dimensional doping scheme, where doping profiles would be varied in both directions. We propose to adopt Gaussian distribution of doping density in the X direction and we are exploring four different doping profiles in the Y directions for subthreshold devices. Based on the proposal we would get four possible combinations of two-dimensional doping profiles illustrated in reference [20-22]. Superposition of two 2D doping profiles in X and Y directions would lead to a 3D doping profile for the devices under each combination. In this chapter we have focused on the second combination (Gaussian distribution in the X direction and exponentially decreasing in the Y direction) shown in figure 20. It is anticipated that each combination will have certain prospects and constrains for different applications of subthreshold circuits. Each of these four doping combinations opens the door for a new class of subthreshold devices optimized for specific set of ultra-low-power applications in memory, high frequency, analog, digital and mixed signal domains.

The proposed Y-directional exponential doping profile is characterized by the absence of halo and retrograde doping. This has the following positive implications: (a) this doping strategy will lead to a simplified process technology in terms of process steps and cost and (b) a significant reduction of the junction capacitances resulting in faster operation and lower power. The halo

regions near the source/substrate and drain/substrate junction regions of the conventional devices significantly increase the junction capacitances leading to increase of the switching power and the delay of the logic gates. The absence of the halo/retrograde doping will reduce this junction capacitance. However, the doping profile in these optimized devices should have exponentially decreasing profile towards the depth of the device, because it is necessary to have a low doping level in the bulk of the device to reduce the capacitance of the bottom junction and substrate noise effects and parasitic latch-up problems. Subthreshold devices operating at ultra-low-voltage levels would be very sensitive to these disturbances. From implementation point of view, the exponentially decreasing profile does not require any special sputtering or ion-implant step (as is required for halo/retrograde doping) and hence, significantly reduces the process complexity and cost.

Furthermore, device engineering in current nanometer scale process have matured so much that even at sub-20nm technology various doping schemes are being implemented successfully. Our proposed doping is actually much simpler than the existing halo and retrograde doping profiles adopted for the MOSFET devices. Our goal is to establish the fact that in the planar MOSFET device for subthreshold operation, we do not need the complex and expensive halo and retrograde doping. The proposed Gaussian doping profile along the channel length is nothing but the absence of halo doping both at the source and drain ends and higher doping in the middle of the channel area. It is simpler than the regular halo doping profile at the source and drain ends. The proposed exponentially decreasing (very high below the channel area and very low inside the substrate) doping profile towards the depth of the device will be somewhat opposite of the retrograde (lightly doped underneath the channel area and highly doped inside the substrate) doping profile. Since the halo and retrograde doping profile is already in practice in nanoscale low-power devices, we

anticipate no radical change in the process complexity for the proposed Gaussian and exponential profiles for the subthreshold device. In reference [6-8], various advancements in device doping are illustrated.

The main focus of this designr was to use existing planar device technology for subthreshold applications. Since, planar device technology still holds more than 90% of the market share, it would be beneficial if we can extend the life cycle of the planar in the ultra-low-power domain by introducing new doping schemes. The goal here is to establish the fact that in the planar device for subthreshold operation at lower V_{dd} we do not require conventional doping scheme, which involves complex halo and retrograde doping profiles. For planar device in subthreshold circuit we can adopt proposed simpler doping scheme. The proposed doping profiles will make the existing planar device technology faster for subthreshold applications compared to other planar subthreshold devices. For sub-nanometer device technologies like FinFET, nanowire-FET and TFET, the doping requirements could be completely different from the planar device.

Our future research will present detail analysis of the doping profiles with new results and analysis in more comprehensive form. In this project, we plan to show that lower power and higher performance can be achieved in the subthreshold circuits by redesigning the devices.

4.6 Conclusion and Future Work

In this chapter we have proposed a new doping scheme for subthreshold device. The proposed scheme is characterized by Gaussian doping profile along the length and exponentially decreasing doping profile across the depth of the device. Since the subthreshold devices operate at very low biasing voltage this leads to minimal impact on short channel effect. Our proposed Gaussian distribution along the channel length would lead to low doping at the drain and source

ends and it will lower the junction capacitance leading faster speed and lower power consumption. Similarly, exponentially decreasing doping density towards the bottom surface of the device will lead to lower body capacitance. It is observed that the ON current (I_{on}) of the subthreshold device with proposed doping profile is higher than in super-threshold device with identical doping profile for specific values of bias voltage and peak doping density.

This chapter presents a study of the doping profile optimization in the channel for subthreshold voltage operation. However, here we only show the variation of $I_{on,}$ I_{off} and V_t with V_{ds}, V_{gs} and peak doping density. In addition of these analysis we have modeled the threshold voltage and shown the threshold voltage variation with different device parameters. We have also analyzed the subthreshold swing characteristics of the proposed device design. In [6-8], we have described the concept of different doping scheme. In this chapter we have described the concept of Figure 20. Under our investigation there are two additional new doping schemes that are not analyzed here. Our future work will cover all possible options under our investigation and address all the factors listed here.

CHAPTER 5

COMPREHENSIVE IMPLANTATION PROFILE

Devices for subthreshold circuits do not require halo and retrograde doping like conventional super-threshold devices. This will reduce the number of steps in the fabrication process, parasitic capacitance and substrate noise dramatically in the subthreshold devices. This chapter introduces a new comprehensive doping scheme for the transistors in subthreshold circuits. The proposed doping scheme would bring doping changes in the source and drain areas along with the substrate and channel regions of the transistors. The proposed doping scheme is characterized by the absence of halos at the source and drain ends. We propose a Gaussian doping distribution inside the source and drain regions, and a low-high-low distribution across the depth of the transistor from the channel surface towards the body region. It also has a low-high-low doping distribution along the length of the transistor below the channel region. Results show that the optimized device with the proposed doping profiles would provide higher ON current (Ion) at smaller body bias condition. The analysis is performed by changing the doping profile, the body bias, and the gate-source voltage (V_{gs}) to observe the off-state current (I_{off}), threshold voltage variation, magnitude of I_{on}/I_{off} ratio, transconductance, and the output conductance with the proposed doping profiles.

5.1 Introduction

Ultra-low-power circuit design has become a very critical focus area due to the widespread use of battery powered and portable devices, sensors and biomedical applications. Operating devices in the subthreshold region is the most effective way to design ultra-low-power circuits. Subthreshold circuit's behavior is different from the super-threshold circuits. Therefore, device parameters like channel doping have to be optimized in different ways for subthreshold and super-threshold circuits. For super-threshold operation retrograde and halo doping profiles are normally used to minimize short channel effect, body punch through, drain induced barrier lowering (DIBL) and variation of the threshold voltage [19]. With retrograded channel profile (RCP) (known as low-high doping profile), the region close to transistor surface is lightly doped and the substrate is highly doped. If the transition from the lightly doped surface to the heavily doped substrate is sharp then it is referred to as the super-steep-retrograded (SSR) profile. The opposite of RCP is high-low doping profile that comes with higher doping at the surface and lower doping in the substrate. The alternative to low-high and high-low doping profiles is the uniformly doped (UD) profile. A comparison of SSR and UD channels is provided in [12]. For a given threshold voltage, a high-low profile gives a larger depletion width than a UD profile, while a low-high profile gives a smaller depletion width than a UD profile. Different channel engineering techniques like double-halo (DH) and single-halo (SH) or lateral asymmetric channel (LAC) devices were proposed to reduce short channel effects. Also scaled non-uniform doping profile is required for super-threshold circuit to provide better control of the electrical characteristics of the device.

Again, doping optimized for CMOS digital circuits may not be suitable for analog and mixed-signal circuits. In [1], the effects of scaling MOSFETs with LAC on analog and mixed-signal performances have been analyzed and compared with conventional MOSFETs. Significant

improvement in analog performance (device gain, transconductance to drive current ratio known as transconductance generation factor, output resistance, threshold voltage mismatch, and etc.) has been observed with LAC [6], [7]. Double pocket or super halo devices have very good digital performance (in terms of high I_{on}/I_{off} ratio and the control of leakage and short channel effects) but their analog performance is often inferior to that of SSR devices [1]. Analog circuits based on subthreshold device operation have the additional advantage of having significantly higher gain due to the exponential behavior of the drain-current in the subthreshold region. This exponential behavior ensures higher transconductance generation factor (g_m/I_d) [2]. It is shown that novel single pocket devices have better intrinsic analog performance compared to the conventional SSR devices. In conclusion there are many factors (gate capacitance, RF performance, carrier density, drifts velocity, DIBL and etc.) of analog, digital and mixed signal circuits that have conflicting dependences or requirements on doping profiles. Therefore, doping profile for subthreshold operation must be optimized for specific needs.

Subthreshold circuits operate at much lower voltage compared to super-threshold circuits. Many of the desired and undesired effects will be different in the subthreshold region. Researchers have concluded that halo doping is not required for subthreshold devices [3]. This will simplify the fabrication process and reduce many parasitic effects. This motivates us to find a suitable doping profile for the devices for subthreshold design. There has been a surge of interest recently to come up with various doping scheme for subthreshold circuits for ultra-low-power applications. We recently proposed a 3D doping scheme for the channel and the substrate regions of the transistors in subthreshold circuits [21-22]. Most of the existing works including our papers[21-22] focus on the optimization of doping profiles in the channel and body regions and assume uniform doping in the source and drain regions. In this chapter, we present a new comprehensive

doping scheme that will address the doping in the source and drain regions along with the channel and body regions.

5.2 Proposed Comprehensive Doping Scheme

Our proposed doping scheme for subthreshold circuits would bring changes both in the source and drain areas as well as the substrate and channel regions. The proposed comprehensive doping scheme is shown in Figure 30. The proposed doping scheme is characterized by the absence of halos at the source and drain ends. We propose a Gaussian doping distribution inside the source and drain regions, and a low-high-low distribution across the depth of the transistor from the channel surface towards the body region. It also has a low-high-low doping distribution along the length of the transistor below the channel region as shown in Figure 30.

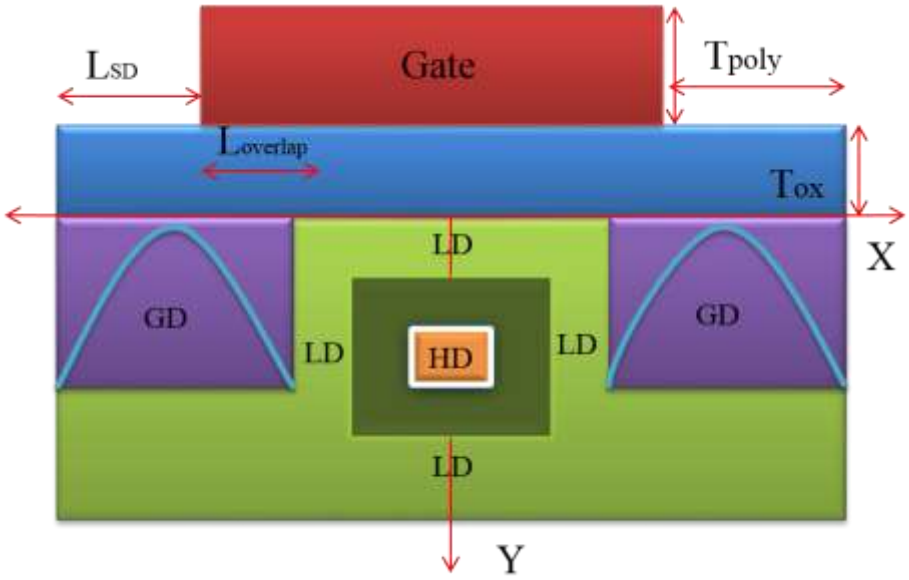


Figure 30: Proposed doping scheme: Gaussian distribution (GD) in the source/drain region, low-high-low doing along the depth of the device, and low-high-low doping along the length of the device under the channel region. Channel length of *15 nm*, channel width *1 μm* and oxide thickness is *1 nm*.

In the proposed scheme the overall doping process would consist of four steps. For an NMOS transistor, first a constant background acceptor dopant would be distributed in all areas. In the second step, the implanted doping of the source and drain regions would be performed. Here we propose to apply a Gaussian doping profile in the source and drain regions as shown in Figure 30. When defining a Gaussian doping distribution in the source/drain a rectangular region of constant high concentration donor doping is introduced. The Gaussian drop-off occurs away from the edge of this highly doped rectangular region. After that the length over which the Gaussian drop-off occurs has been specified. A constant background acceptor concentration doping level is distributed to complete the Gaussian drop-off.

A low-high-low doping profile is considered along the depth of the device underneath the gate towards the substrate. The uniform high doping area under the channel region does not extend from the source to drain. It rather covers the middle part leaving gaps (areas of low doping) at both ends as shown in Figure 30. Therefore, in the proposed scheme low-high-low doping profiles are considered both along the depth of the device and the length of the channel. First let us analyze low-high-low doping along the depth. The high doping at the center maintains the threshold voltage, while low doping near the gate surface reduce the tunneling effect and low doping near the substrate side ensures less body leakage. Low let us focus on the low-high-low distribution along the channel length from the edge of the source to the edge of drain. This low–high–low doping profile underneath the channel from source to drain reduces the gate misalignment effects on both the source and drain sides. Furthermore, low doping near the source and drain ends ensures high mobility, reduced peak electric field, and impact ionization.

In this chapter, we show that for a particular technology generation, lower power and higher performance can be achieved in the subthreshold region by redesigning the devices

specifically for subthreshold operation. In current design practice, standard transistors are operated in the subthreshold region to implement subthreshold logic [10]. However, to provide better control on the electrical characteristics of the device non-uniform doping profile is desired. Previously high-to-low doping profile has been proposed for subthreshold operation [10]. Subthreshold device with very low bias voltage experiences minimum short channel effect. This allows lowering the doping profile at the source and drain ends of the channel. Based on this observation we propose to have less amount of doping at the source and drain ends. The halo or LAC regions near the source/substrate and the drain/substrate regions in super threshold device significantly increase the junction capacitances thereby increasing the switching power and the delay of the logic gates. Our proposed low doping at both source and drain side will reduce the junction capacitance. The proposed low-high-low doping distribution in the Y-direction towards the bottom surface of the bulk will lead to reduced capacitance of the bottom junction and reduced substrate noise effects and parasitic latch-up problems. Strong doping between channel area and lower end of the bulk will help faster channel formation at low threshold voltage.

5.3 Results and Analysis

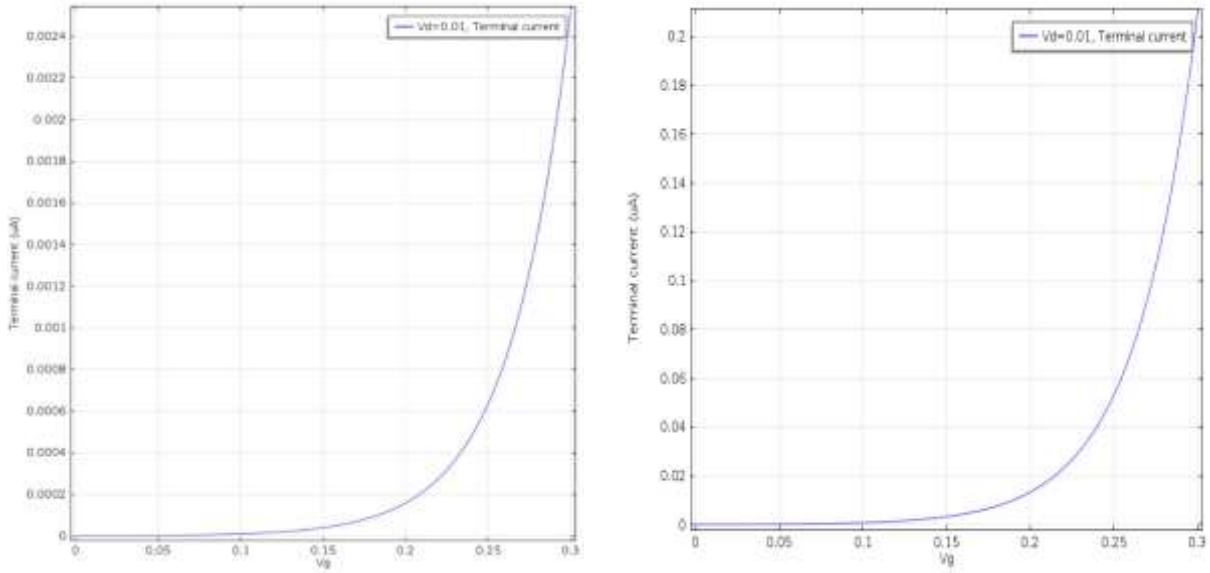
We have performed COMSOL Multiphysics analysis to investigate the impact of the proposed doping profiles on the device behavior. A metal contact is introduced to define metal-semiconductor interface for the source terminal. This terminal could be connected to zero or negative bias to regulate the threshold voltage. Similar type of metal-semiconductor interface is formed at the drain end and connected to *0V*. A third metal is connected to the bottom part of the substrate and connected to zero bias or any fixed bias as needed to control the threshold voltage. A thin insulator of *1nm* thickness and *4.5* oxide permittivity is used to form the gate. A technique based on the subthreshold current–voltage (I-V) characteristics to extract 2-D doping profiles is

proposed in [14]. We modeled MOSFET subthreshold current based on the proposed doping profile using the same approach as in [14]. The formulation of the model is shown for NMOS transistor and can be easily applied to PMOS transistor. In our analysis, the uniform dopant concentration in that rectangular region of the source and drain is considered to be $N_D = 1\times10^{20}$ cm^{-3}. There is no doping (except the background doping) till 1nm underneath the gate then a high uniform acceptor doping of $N_A = 1\times10^{19}$ cm^{-3} is distributed till *3.5nm* from the gate surface, and after that a low doping (background doping) is considered inside the substrate. Here we considered a channel length of *15nm*. The constant background acceptor dopant concentration is considered to be $N_0 = 1\times 10^{19}$ cm^{-3}.

In regular bulk transistor, short channel effect or pinch-off effects is a very familiar phenomena with the increase of drain voltage. In our simulation, electron concentration plot for the specific doping distribution shows very less short channel effect or pinch-off effect at the drain end. In case of very short channel device, short channel effect (SCE) will be crucial for device performance. Our analysis shows that no pinch-off occurs in our device simulation with the proposed doping. This makes it a perfect choice for the ultra-low-power circuit operation. Furthermore, before applying any bias voltage the electric field is uniform at the source and drain end. While biasing voltage is increased the inversion charge density at the drain decreases due to the lowering of the electron quasi-Fermi level that will lead to reduce the magnitude of the electric potential at the drain end. Also the electric potential in the y-direction changes more rapidly than the electric potential in the x-direction. At the same time magnitude of the electric potential is increased at the source end. Also the electric potential decreases with the increase of bias voltage.

Figure 31a shows the gate voltage versus drain current variation with zero body bias V_{bs} = *0 V* and Figure 31b with V_{bs} = *-0.1 V*. In both the cases, the biasing voltage was kept at V_d = *0.01*

V. From Figure 31a, we can see that the threshold voltage at zero body bias (bulk and source of the transistor are tied together) is around $V_{gs} = V_{th} = 0.17\ V$ and Figure 31b shows the threshold voltage of $V_{gs} = V_{th} = 0.2\ V$ while the body bias $V_{bs} = -0.1\ V$. In case of negative body bias, the source and body junction remains reverse biased. As V_{bs} become more negative more holes are attracted to the substrate connection, leaving a larger negative charge behind and the depletion region becomes wider.



(a) (b)

Figure 31: (a) Gate voltage vs drain current at $V_d = 0.01\ V$ and $V_{bs} = 0\ V$. The threshold voltage is approximately *0.17 V*. (b) Gate voltage vs drain current at $V_d = 0.01\ V$ and $V_{bs} = -0.1\ V$. The threshold voltage is approximately *0.20 V*.

From (5.1) it can be seen that the threshold voltage is a function of total charge in the depletion region because the gate charge must mirror the depletion charge before an inversion layer is formed. This is the reason behind the increase of the threshold voltage with the negative body bias. The transconductance is defined by $g_m = (dI_d/dV_{gs})$ is also affected by the body bias.

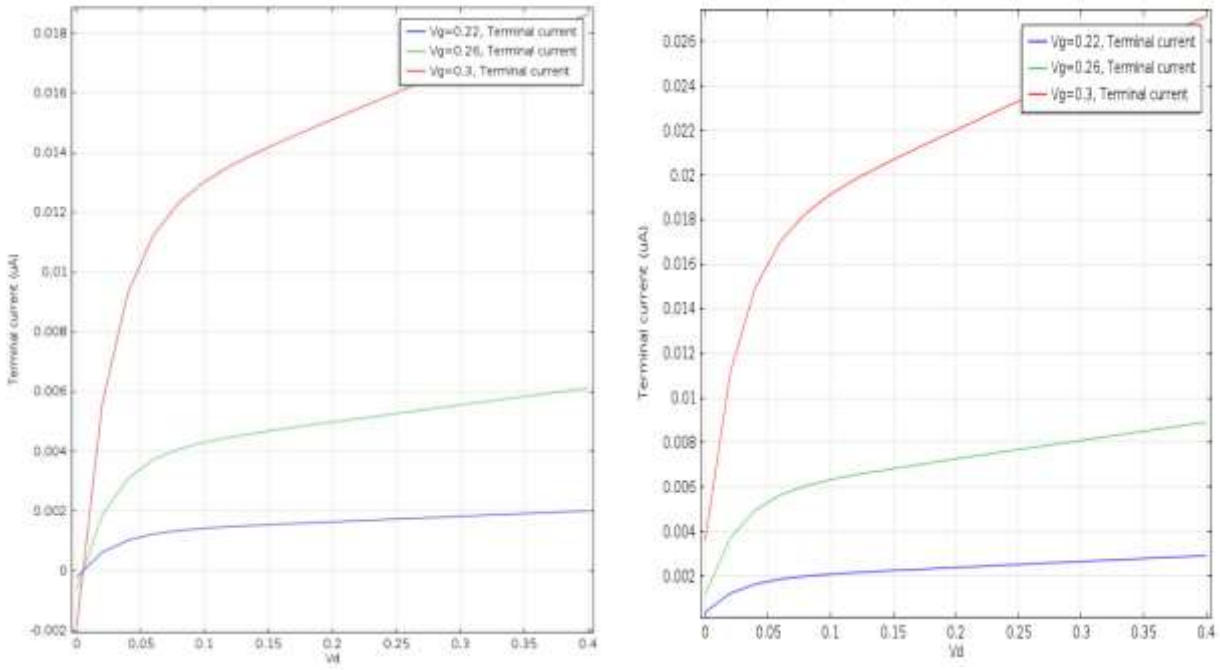
From Figure 31a and Figure 31b it is evident that zero body bias reduces the transconductance effect compared to V_{bs} = *-0.01 V* body bias.

$$V_{th} = V_{FB} + 2\psi_B + \frac{t_{ox}\sqrt{4\varepsilon_s\varepsilon_0 q N_{A\psi_B}}}{\varepsilon_{ox}\varepsilon_0} \tag{5.1}$$

$$V_{FB} = \varphi_m - \chi + \frac{k_B T}{q} ln \frac{n_{eq}}{N_c} \tag{5.2}$$

$$\psi_B = \frac{k_B T}{q} ln \frac{p_{eq}}{n_i} \tag{5.3}$$

Here t_{ox} is the thickness of the oxide, $\varepsilon_{ox}, \varepsilon_0$ and ε_s are the permittivity of the oxide, free space and the substrate respectively, q is the electron charge, N_A is the acceptor concentration into the channel, V_{FB} is the flat band potential and $\psi_B$is the potential difference between the intrinsic level and the Fermi-level. φ_m is the work function of the metal contact, χ is the electron affinity, N_c is the semiconductor density of states in the conduction band, n_i is the intrinsic carrier density, n_{eq} and p_{eq} are the equilibrium electron and hole density respectively.



(a) (b)

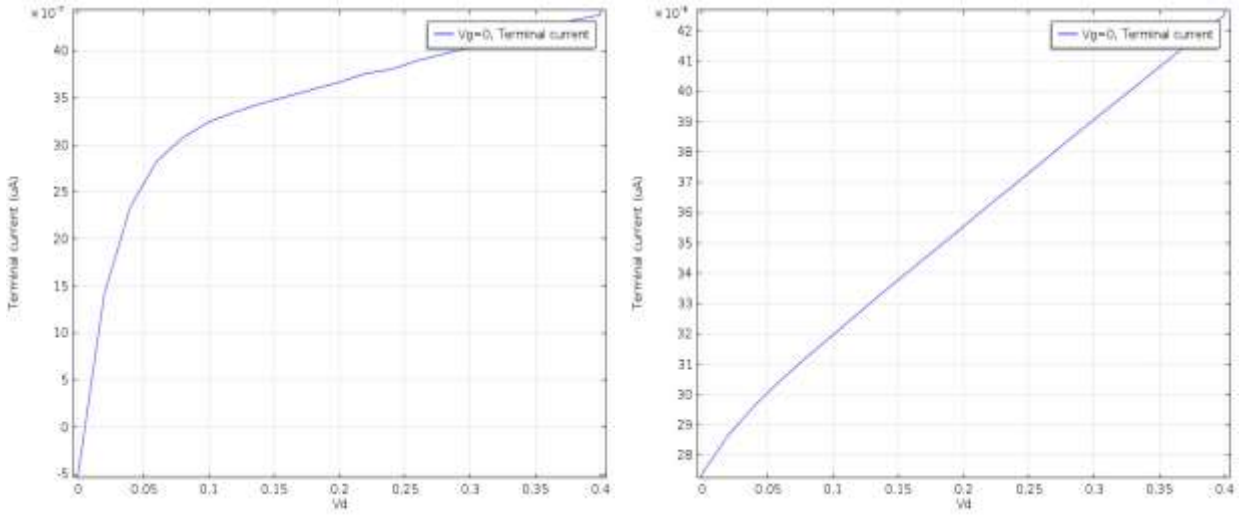
Figure 32: (a) Drain voltage versus drain current for different gate voltage and (a) $V_{bs} = 0\ V$, (b) $V_{bs} = -0.1\ V$.

Figure 32 shows the drain voltage versus drain current plots for different values of gate voltage. The curve shows three region of operation a) linear region at low voltage, b) nonlinear region at intermediate voltage and c) saturation region at higher voltage. The current saturation occurs due to phenomena known as pinch-off effects. As the drain current is increased more current flows along the channel and potential drop along its length increases. The voltage between the gate and the semiconductor therefore changes as a function of position along the channel. Figure 32a shows the variation of drain current with different gate voltage and zero body bias and Figure 32b shows the same current plot with body bias $V_{bs} = -0.1\ V$. This analysis shows the variation of the magnitude of the drain current for different body bias. In case of zero body bias the magnitude of drain current is lower than the current for body bias of $V_{bs} = -0.1\ V$. Negative body helps form the inversion layer faster and stronger that lead to higher Ion current at lower gate bias voltage. Off

current is the current from the source to drain at zero gate voltage. Figure 33 (a, b) shows the off current for $V_{bs} = 0$ and $V_{bs} = -0.1\ V$. Table 4 summaries the threshold voltage, ON current, OFF current and I_{on}/I_{off} ratio for two different body bias conditions (for $V_{bs} = 0$ and $V_{bs} = -0.1\ V$).

Table 4: Summaries of Transistor Behavior

Transistor Parameters	***V_{bs} = 0 V***	***V_{bs} = -0.1 V***
Threshold Voltage, V_{th}	*0.17V*	*0.2V*
On Current, I_{on}	*0.016µA*	*0.26µA*
Off Current, I_{off}	*4×10^{-6}µA*	*42×10^{-6}µA*
I_{on}/I_{off}	*4000*	*6190*



(a) (b)

Figure 33: Off current for body bias (a) $V_{bs} = 0\ V$, (b) $V_{bs} = -0.1\ V$.

To justify our proposed doping profile we have compared our results with most of the other published works on different MOS doping techniques in Table 5. Here, a brief overview of the other emerging and existing doping schemes that are used for the comparison is provided. In [25-

26], doping profile for an n-i-n TFET is presented, where deeply retrograde profile was used to obtain excellent ON-OFF characteristics and lower σ-V_{TH} compared to the conventional planar bulk MOSFET. A vertical Gaussian-like doping profile has been proposed in [27], where it is concluded that symmetric DG MOSFET would be more efficient compared to the asymmetric structure. In [29], it is shown that asymmetric drain doping profile improves the TFET performance in terms of subthreshold slope and suppression of ambipolar conduction, which makes a TFET suitable for the low-power circuit design. Graded channel dual material double gate (GCDMDG) [30] achieves higher drain current, peak transconductance, and higher values of cutoff frequency at lower drain currents. Less aggressive retrograde channel doping gradient in [31] indicate that the tri-gate MOSFET design is promising for continued bulk-Si CMOS transistor scaling and it can achieve similar ON-state current performance and intrinsic delay. In [32], Gaussian doping gradient of underlapped source/drain region has been studied and found that by increment of the underlapped source/drain length, the subthreshold swing, DIBL and gate work function are decreased and they are increased by increment of source/drain doping gradient. In [33], short-channel effects are effectively mitigated by employing an SSR channel doping profile and favorable subthreshold operation is achieved in [34] with asymmetric underlap DG MOSFETs. The proposed model in [35] captures the effect of lateral electric field spread via S/D dopant species, which lowers the threshold voltage and effective channel length of the device with the increase in lateral straggle of S/D profile. In this work proposed doping profile offers higher I_{on}/I_{off} ratio and moderate I_{on} current in the subthreshold device. We have analyzed the parameters I_{on}, I_{off} and V_{th} for subthreshold device applications by adopting the proposed comprehensive doping scheme for different body and gate bias conditions.

Table 5: Data table for the list of device (*** this work) with varying gate length (L_G), threshold voltage (V_{th}), I_{on}, I_{off}, I_{on}/I_{off}, MOSFET technology and doping profile.

L_G (nm)	V_{th} (V)	I_{on} (μA/μm)	I_{off} (μA/μm)	I_{on}/I_{off}	FET Technology	Doping Profile	Ref.
15	0.17	0.016 at (V_G=0.3V, V_D=0.4V)	4×10^{-6}	4×10^{3}	Bulk	Comprehensive	***
100	--	600 at (V_G=1V, V_D=0.5V)	0.3	2×10^{3}	Nanowire	n-i-n	[25]
250	0.5	70 at (V_G=1V, V_D=1V)	2×10^{-4}	3.5×10^{4}	Planar/Bulk	Deeply Retrograde	[26]
100	0.4	900 at (V_G=1V, V_D=1V)	--	--	Double Gate (DG)	Vertical Gaussian	[27]
15	0.3	400 at (V_G=0.5V, V_D=1V)	0.5	800	Double Gate (DG)	Graded Channel	[28]
45	0.7	0.12 at (V_G=0.5V, V_D=1V)	--	--	DG TFET	Uniform, Gaussian	[29]
15	0.4	300 at (V_G=0.5V, V_D=1V)	0.5	600	Double Gate (DG)	Low-High-Low (Abrupt)	[30]
18	0.2	45 at (V_G=0.3V, V_D=0.7V)	7×10^{-3}	6.4×10^{3}	FinFET, Trigate	Retrograde	[31]
9	--	-- at (V_G=--V, V_D=0.6V)	0.5	--	Nano DG	Gaussian	[32]
28	0.34, 0.32	476, 428 at (V_G=0.5V, V_D=0.38V)	1.08×10^{-3}	4.4×10^{5}, 3.9×10^{5}	Planar/Bulk	Uniform, Super Steep Retrograde	[33]
30	0.23	-- at (V_G=0.3V, V_D=0.3V)	--	--	Underlap DG	S/D Underlap	[34]
70	0.3	400 at (V_G=0.5V, V_D=1V)	--	--	Double Gate	S/D Lateral Gaussian	[35]

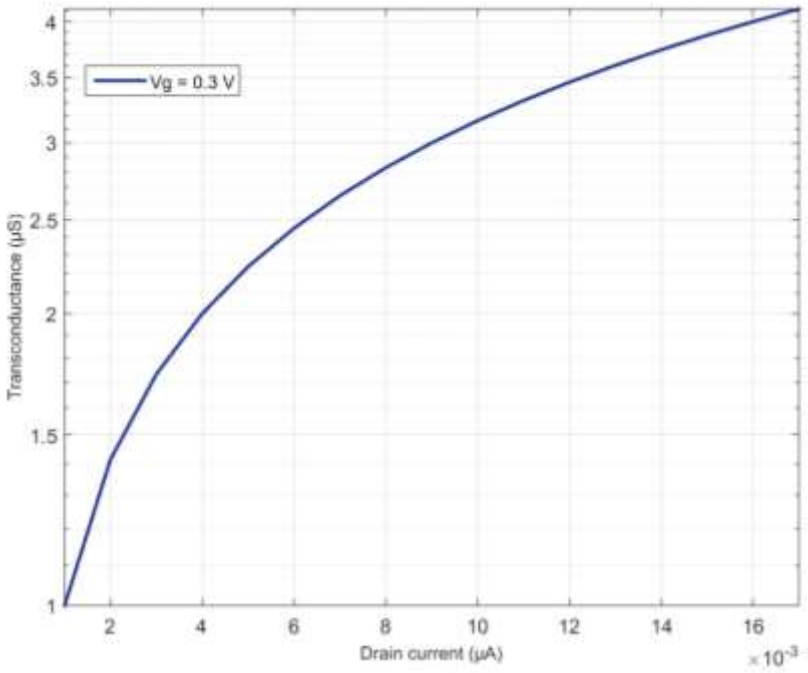


Figure 34: Transconductance as a function of the drain current under a gate voltage of *10 mV*.

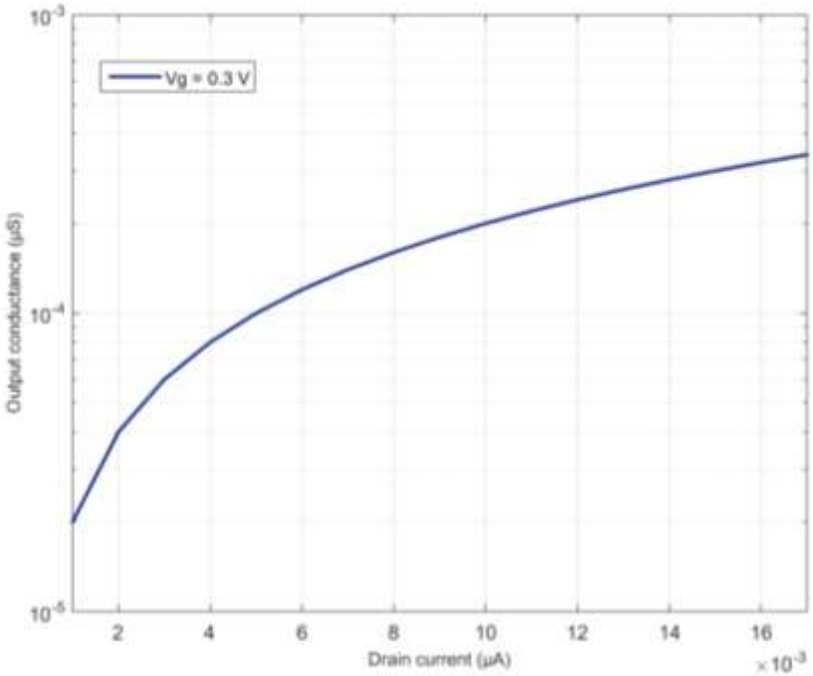


Figure 35: Output conductance as a function of the drain current under a gate voltage of *10 mV*.

For MOSFET, two small signal outputs are particularly interesting as they provide information on the device performance. These are the transconductance (g_m) and the output conductance (g_0). The transconductance is the ratio of the current change at the drain to the voltage change at the gate. Figure 34 shows the transconductance variation. Larger transconductance means greater amplification and MOSFET is capable of delivering more current for a given gate voltage. The transconductance increases rapidly with the drain current and reaches its maximum at *0.017 μA*. The output conductance is defined as the ratio of the current change at the drain port to the voltage change at the drain port (Output conductance: $g_0 = (\partial I_d)/(\partial V_D)$). Figure 35 shows the output conductance variation. Larger the output conductance larger the drain current for a given drain voltage. An AC signal is superimposed on the drain voltage using a frequency domain perturbation step. In this study the drain voltage is varied from 0 to 0.3V under a constant gate voltage of *0.3 V*. Using small signal analysis the output current expression can be given by (5.4), where, i_d is small signal current, g_m and g_0 are transconductance and output conductance respectively.

$$i_d = g_m v_{gs} + g_0 v_{ds} \tag{5.4}$$

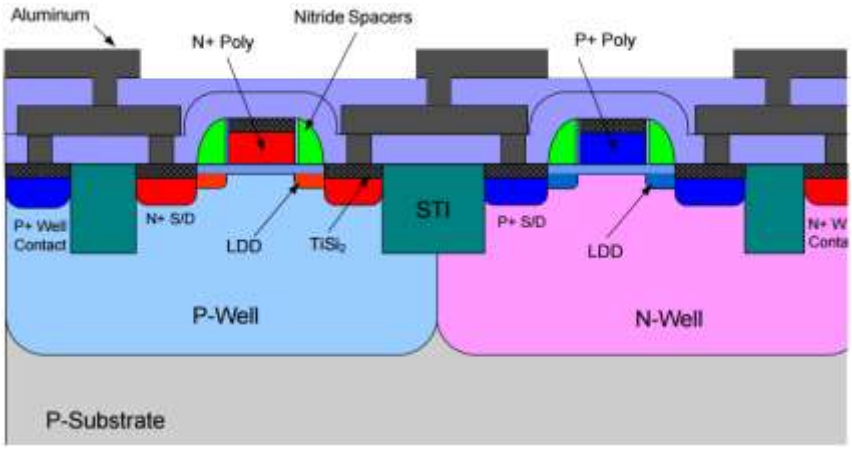


Figure 36: CMOS cross section showing NMOS (left) and PMOS (right) transistor [24].

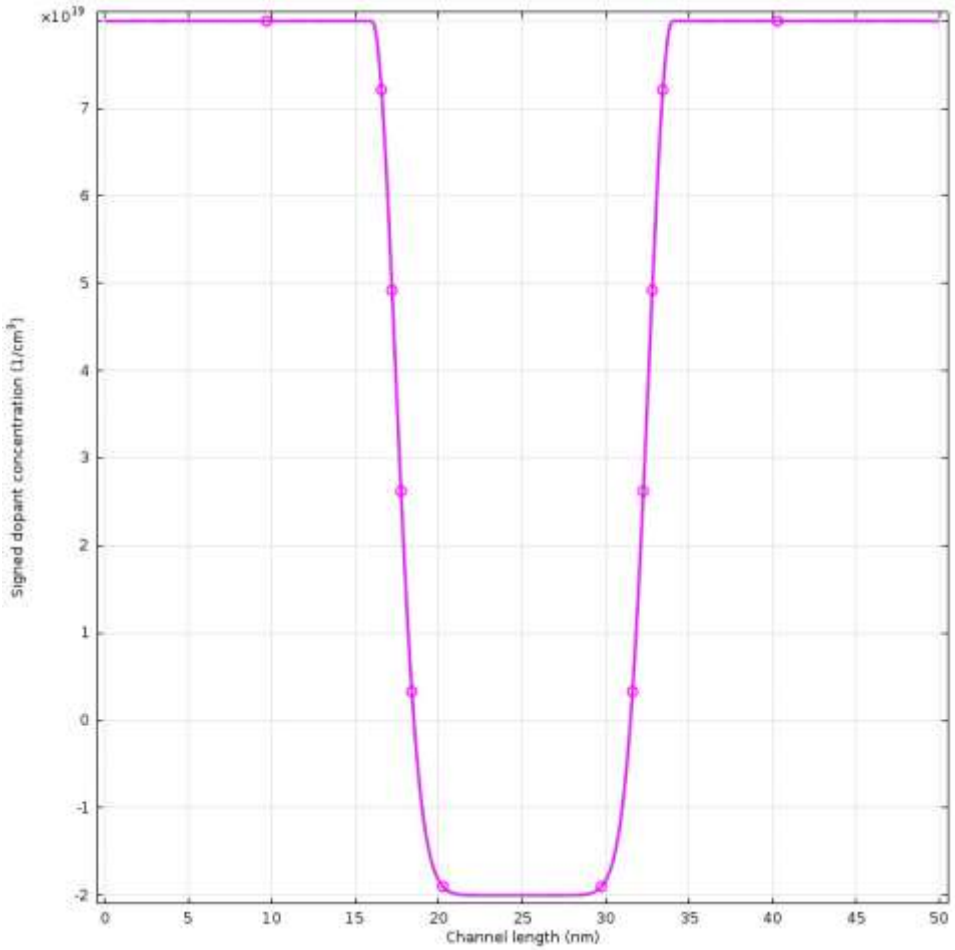


Figure 37: Dopant distribution along the channel length.

For device performance optimization perfect tuning of dopant distribution is a very crucial task. Figure 36 shows how NMOS is built inside P-well and PMOS is built inside N-well and both are placed on the same N-substrate. Also the lightly doped drain (LDD) and super steep retrograde well (SSRW) has been introduced inside the basic CMOS structure in Figure 36. How low-doped source and drain is introduced inside the device and metal contact is formed to build the desired logic circuit is also shown in Figure 36 for readers understanding.

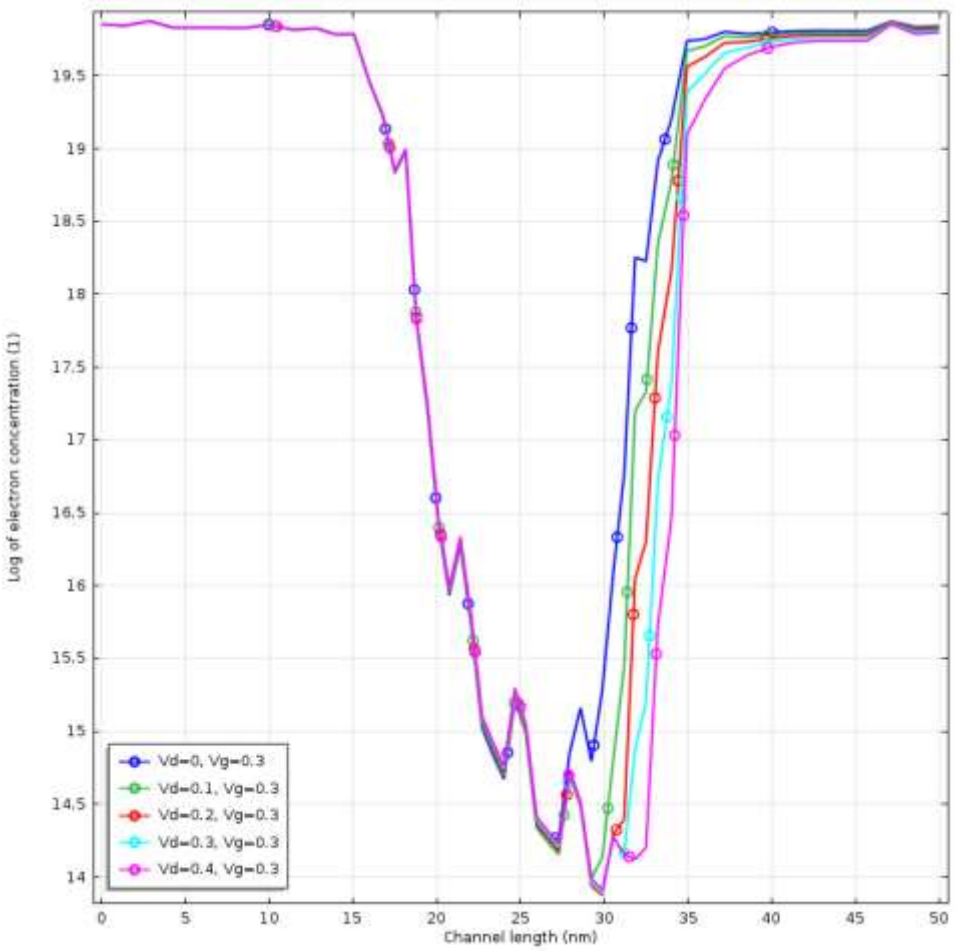


Figure 38: Electron concentration along the channel length.

Figure 37 shows the signed dopant concentration distribution across the channel length. Figure 38 shows the electron concentration distribution at constant gate voltage and varying drain voltage V_d. As drain voltage V_d increases the electron concentration inside channel area would decrease, which eventually leads to pinch-off condition. From Figure 38 it is observed that inside the channel the reduction of electron concentration is very low for different drain voltage. This phenomena also confirm that the device with our proposed doping would have significantly lower pinch-off effect in the saturation region. It also shows the perfect electron distribution plot at the source and drain end, which is supposed to be higher than the channel area. Figure 39 shows the

hole distribution plot in the device area. Hole distribution is supposed to be much smaller and inverse compared to the electron distribution inside the source/drain and channel area. Figure 39 confirms the desired shape of the hole distribution throughout the device. Electric potential is also another important factor for perfect device operation. Figure 40 shows the electric potential distribution at the drain end. As drain voltage goes up the electric potential at the drain end should go up. Figure 40 shows that at $V_d = 0.4\ V$ the electric potential at drain end is highest and at $V_d = 0\ V$ electric potential is the minimum.

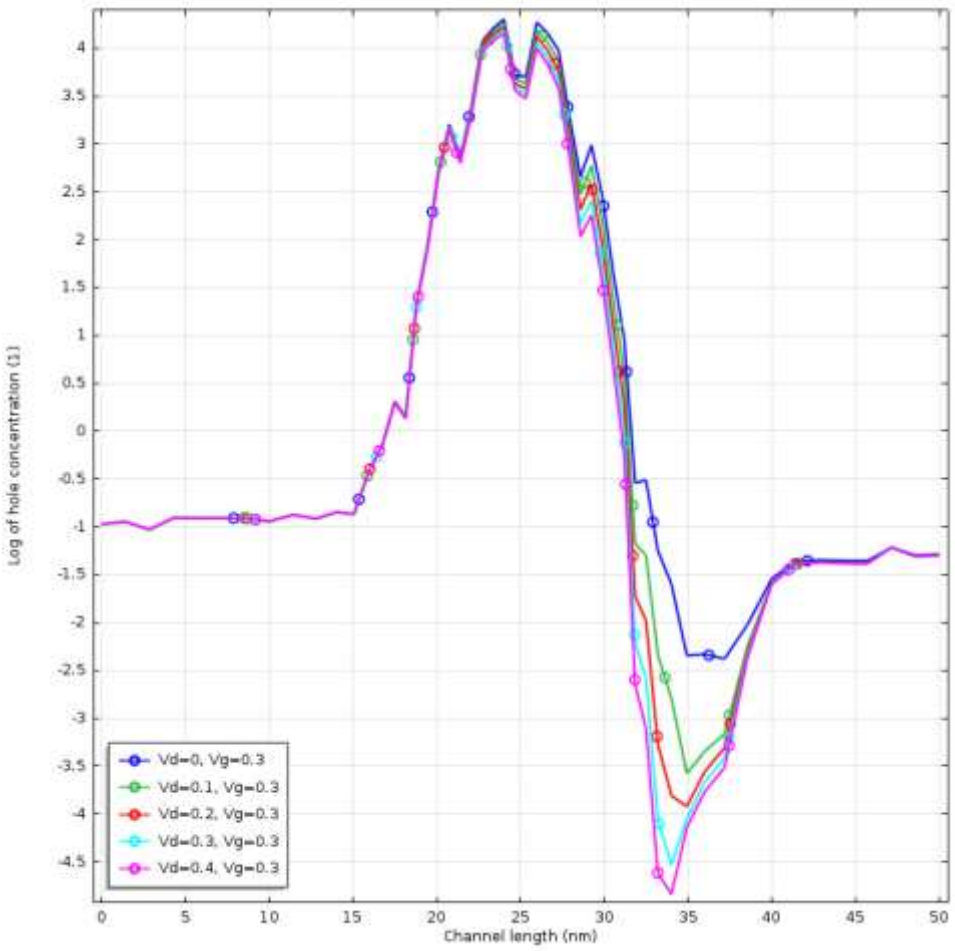


Figure 39: Hole concentration along the channel length.

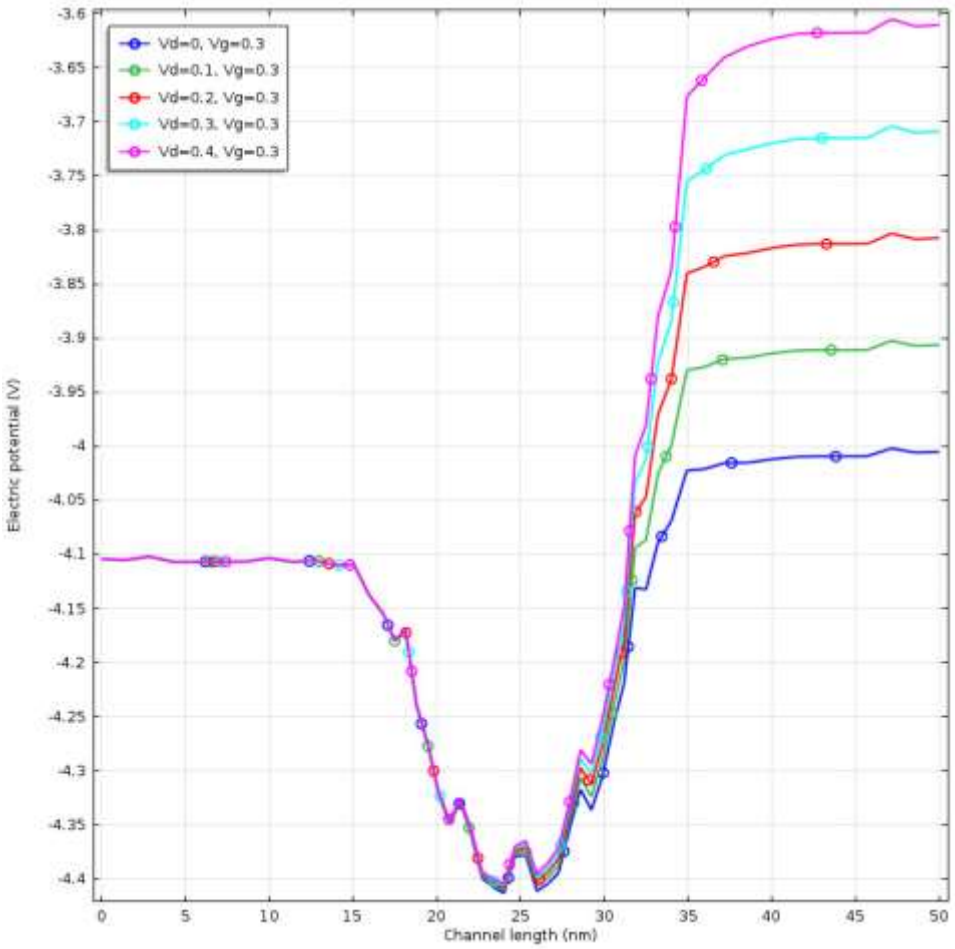


Figure 40: Variation of electric potential with channel length.

5.4 Conclusion

In this chapter, we proposed a comprehensive doping profile for subthreshold transistor. The proposed doping profile offers higher I_{on}/I_{off} ratio and moderate I_{on} current in the subthreshold device. We have analyzed the parameters I_{on}, I_{off} and V_{th} for subthreshold device applications by adopting the proposed comprehensive doping scheme for different body and gate bias conditions. We have also analyzed transconductance, output conductance, electron/hole distribution and electric potential for different biasing condition. Results show that the optimized device using the proposed comprehensive doping profile would provide better Ion current (at minimum V_D and V_G)

compared to the existing MOS technologies with different doping profiles that are listed in Table 5. Results also show that I_{on}/I_{off} ratio is higher while body bias is considered. It is important to know that most of the industry is still using optimized super-threshold designs and relying on device sizing for low-power operation. Halo implants in the super-threshold devices are introduced to provide a reverse short channel effect in the channel, which leads to devices being sized at lengths at node prior to the one actually being used (i. e $65nm\ node \geq 100nm$ channel length). Eradication of the halo implants in our proposed doping profile removes this influence leading to the optimal device sizing to revert to the node minimum. This results in a practical reduction in the silicon area. However, there are some difficulties and changeless that need to be addressed. Drain induced barrier lowering (DIBL) is one the issues. DIBL leads to punch-through at higher voltage, and it may lead to reduced control over device behavior. Our future work will present detail analysis of the other parameters like DIBL and subthreshold swing to perform a more comprehensive analysis of the proposed doping scheme compared to the existing doping techniques.

CHAPTER 6

CONCLUSION AND FUTURE WORK

In this dissertation four different subthreshold doping profile and one comprehensive doping profile has been proposed and mathematically solved for subthreshold application. The main four subthreshold doping profiles are composed of X dimension and Y dimension varying dopant distribution. This new doping scheme proposes to employ Gaussian distribution of doping concentration along the X dimension (length of the channel) with highest concentration at the middle of the channel. The doping concentration across the Y dimension (depth of the device) from the channel region towards the bulk of the device can follow one of the following four distributions: (a) exponentially decreasing, (b) Gaussian, (c) low to high, and (d) uniform doping. Results show that a device optimized with any of the four proposed doping profiles would offer higher ON current in the subthreshold region than a device with the conventional halo and retrograde doping profiles. Among the four 3D doping profiles for the subthreshold device some has better ON current than the others. Based on specific requirements one of these four doping profiles can be adopted for different ultra-low-power applications. Threshold voltage modelling has been performed and a comparative analysis is presented between super-threshold and sub-threshold devices threshold voltages. We have also analyzed the subthreshold swing characteristics

of the device with the proposed doping profiles. Our analysis shows that better subthreshold swing can be achieved using our new doping profile based subthreshold design.

In comprehensive doping scheme a Gaussian doping distribution inside the source and drain regions, and a low-high-low distribution across the depth of the transistor from the channel surface towards the body region. It also has a low-high-low doping distribution along the length of the transistor below the channel region. We simulated this comprehensive doping scheme using COMSOL Multiphysics simulation tools. Results show that the optimized device with the proposed doping profiles would provide higher ON current (I_{on}) at smaller body bias condition. The analysis is performed by changing the doping profile, the body bias, and the gate-source voltage (V_{gs}) to observe the off-state current (I_{off}), threshold voltage variation, magnitude of I_{on}/I_{off} ratio, transconductance, and the output conductance with the proposed doping profiles.

Based on specific application requirements in ultra-low-power regime we may need different I_{on} (higher or lower). The proposed doping scheme provides four different options for the subthreshold circuit. Any one of the options might be the perfect choice for a specific low power application. We anticipate that with the current progresses in the fabrication process it would be possible to incorporate the proposed doping profiles in the design of ultra-low-power circuits. This research presents a study of the doping profile optimization in the channel for subthreshold voltage operation. However, here we only show the variation of I_{on} with V_{gs}, V_{ds} and peak doping density. Also we have shown other factors like subthreshold swing, threshold voltage variation, intrinsic delay, R_{eff} and C_{eff} subcomponent of intrinsic delay and tabulated I_{on} value at constant I_{off} = $1nA/\mu m$. Here, we have explained the basic concept of the new doping scheme and analyzed the prospects of the new doping profiles for the subthreshold circuits. Our future work will cover all other factors and parameters that would impact the doping process and requirements in ultra-low-

power subthreshold circuits. However, there are some difficulties and changeless that need to be addressed. Drain induced barrier lowering (DIBL) is one the issues. DIBL leads to punch-through at higher voltage, and it may lead to reduced control over device behavior. Our future work will present detail analysis of the other parameters like DIBL and subthreshold swing to perform a more comprehensive analysis of the proposed doping scheme compared to the existing doping techniques.

REFERENCE LIST

[1] H. V. Deshpande, B. Cheng, J. C. S. Woo, "Channel engineering for analog device design in deep submicron CMOS technology for system on chip applications," *Electron Devices, IEEE Transactions on*, vol.49, no.9, pp.1558, 1565, Sep 2002.

[2] H. V. Deshpande, B. Cheng, J. C. S. Woo, "Analog device design for low power mixed mode applications in deep submicron CMOS technology," *Electron Device Letters, IEEE*, vol.22, no.12, pp.588, 590, Dec. 2001.

[3] S. Chakraborty, A. Mallik, C. K. Sarkar, "Subthreshold performance of pocket-implanted silicon-on-insulator CMOS devices and circuits for ultra-low-power analogue/mixed-signal applications, *"Circuits, Devices & Systems, IET*, vol.5, no.4, pp.343, 350, July 2011.

[4] E. Abou-Allam, T. Manku, M. Ting, M. S. Obrecht, "Impact of technology scaling on CMOS RF devices and circuits," *Custom Integrated Circuits Conference, 2000. CICC. Proceedings of the IEEE 2000*, vol., no., pp.361, 364, 200.

[5] M. Saito, M. Ono, R. Fujimoto, H. Tanimoto, N. Ito, T. Yoshitomi, T. Ohguro, H. S. Momose, H. Iwai, "0.15-μm RF CMOS technology compatible with logic CMOS for low-voltage operation," *Electron Devices, IEEE Transactions on* , vol.45, no.3, pp.737,742, Mar 1998.

[6] K. Narasimhulu, M. P. Desai, S. G. Narendra, V. R. Rao, "The effect of LAC doping on deep submicrometer transistor capacitances and its influence on device RF performance," *Electron Devices, IEEE Transactions on*, vol.51, no.9, pp.1416, 1423, Sept. 2004.

[7] H. Shin, L. Seungjun, "An 0.1-μm asymmetric halo by large-angle-tilt implant (AHLATI) MOSFET for high performance and reliability," *Electron Devices, IEEE Transactions on*, vol.46, no.4, pp.820, 822, Apr 1999.

[8] B. Cheng, V. R. Rao, J. C. S Woo, "Exploration of velocity overshoot in a high-performance deep sub-0.1-μm SOI MOSFET with asymmetric channel profile," *Electron Device Letters, IEEE*, vol.20, no.10, pp.538, 540, Oct. 1999.

[9] K. Narasimhulu, D. K. Sharma, V. Ramgopal Rao, "Impact of lateral asymmetric channel doping on deep submicrometer mixed-signal device and circuit performance," *Electron Devices, IEEE Transactions on*, vol.50, no.12, pp.2481, 2489, Dec. 2003.

[10] B. C. Paul, A. Raychowdhury, K. Roy, "Device optimization for digital subthreshold logic operation," *Electron Devices, IEEE Transactions on*, vol.52, no.2, pp.237, 247, Feb. 2005.

[11] A. Raychowdhury, B. C. Paul, S. Bhunia, K. Roy, "Computing with subthreshold leakage: device/circuit/architecture co-design for ultralow-power subthreshold operation," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, vol.13, no.11, pp.1213, 1224, Nov. 2005.

[12] I. De, C. M. Osburn, "Impact of super-steep-retrograde channel doping profiles on the performance of scaled devices," *Electron Devices, IEEE Transactions on*, vol.46, no.8, pp.1711, 1717, Aug 1999.

[13] S. Chakraborty, A. Mallik, C. K. Sarkar, V. R. Rao, "Impact of Halo Doping on the Subthreshold Performance of Deep-Submicrometer CMOS Devices and Circuits for Ultralow Power Analog/Mixed-Signal Applications," *Electron Devices, IEEE Transactions on*, vol.54, no.2, pp.241,248, Feb. 2007.

[14] Z. K. Lee, M. B. McIlrath, D. A. Antoniadis, "Two-dimensional doping profile characterization of MOSFETs by inverse modeling using I-V characteristics in the subthreshold region," *Electron Devices, IEEE Transactions on* , vol.46, no.8, pp.1640,1649, Aug 1999.

[15] Y. Taur and T. H. Ning, Fundamentals of Modern VLSI Devices, 1998. Cambridge Univ. Press.

[16] X. Zhou, K. Yong Lim, D. Lim, "A general approach to compact threshold voltage formulation based on 2D numerical simulation and experimental correlation for deep-submicron ULSI technology development [CMOS]," *Electron Devices, IEEE Transactions on* , vol.47, no.1, pp.214, 221, Jan 2000.

[17] A. Godoy, J. A. López-Villanueva, J.A. Jiménez-Tejada, A. Palma, F. Gámiz, A simple subthreshold swing model for short channel MOSFETs, *Solid-State Electronics*, Volume 45, Issue 3, March 2001, Pages 391-397.

[18] "Well-Tempered" Bulk-Si NMOSFET Device, www-mtl.mit.edu/researchgroups/Well/

[19] G. G. Shahidi, B. Davari, T. J. Bucelot, P. A. Ronsheim, P. J. Coane, S. Pollack, C. R. Blair, B. Clark, H. H. Hansen, "Indium channel implant for improved short-channel behavior of submicrometer NMOSFETs," *Electron Device Letters, IEEE* , vol.14, no.8, pp.409,411, Aug. 1993.

[20] M. Hossain and M. H. Chowdhury, 2014. “Transistor Doping Profile Optimization for Low Power Subthreshold Circuits”, *MWSCAS*, August 3-6, 2014, College Station, TX, USA.

[21] M. Hossain and M. H. Chowdhury, “New Three Dimensional Doping Profile for Devices in Subthreshold Circuit”, *MWSCAS*, August 1-5, 2015, Fort Collins, Colorado, USA.

[22] M. Hossain and M. H. Chowdhury, 2016. “Comprehensive Doping Scheme for MOSFETs in Ultra Low Power Subthreshold Circuits Design”, Microelectronics journal, Accepted.

[23] C. Hu, M. Jeng, et all, 1993. "Threshold voltage model for deep-submicrometer MOSFETs," *Electron Devices, IEEE Transactions on*, vol.40, no.1, pp.86, 95, Jan 1993.

[24] M. Aquilino, “Advance RIT to Submicron Technology. Design and Fabrication of 0.5 μm NMOS Transistor,” RIT Microelectronics Research Journal, 2004.

[25] A. W. Dey, C. Thelander, E. Lind, Kimberly A. Dick, B. M. Borg, M. Borgstrom, P. Nilsson, L. E. Wernersson, "High-Performance InAs Nanowire MOSFETs," IEEE Electron Device Letters, vol.33, no.6, pp.791,793, June 2012.

[26] J. Woo, P.Y. Chien, Frank Yang, S.C. Song, C. Chidambaram, J. Wang, G. Yeap, “Improved device variability in scaled MOSFETs with deeply retrograde channel profile,” Microelectronics Reliability, Volume 54, Issues 6–7, June–July 2014, Pages 1090-1095, ISSN 0026-2714.

[27] S. Dubey, P. Kumar Tiwari and S. Jit, “On-current modeling of short-channel double-gate (DG) MOSFETs with a vertical Gaussian-like doping profile,” Journal of Semiconductors, vol. 34, no. 5, November 2012.

[28] R. K. Sharma, M. Gupta, R. S. Gupta, "TCAD Assessment of Device Design Technologies for Enhanced Performance of Nanoscale DG MOSFET," IEEE Transaction on Electron Devices, vol.58, no.9, pp.2936, 2943, Sept. 2011.

[29] V. Vijayvargiya, S.K. Vishvakarma, "Effect of Drain Doping Profile on Double-Gate Tunnel Field-Effect Transistor and its Influence on Device RF Performance," IEEE Transactions on Nanotechnology, vol.13, no.5, pp.974,981, Sept. 2014.

[30] R. K. Sharma, M. Bucher, "Device Design Engineering for Optimum Analog/RF Performance of Nanoscale DG MOSFETs," IEEE Transactions on Nanotechnology, vol.11, no.5, pp.992, 998, Sept. 2012.

[31] B. Ho, Xin Sun, Changhwan Shin, Tsu-Jae King Liu, "Design Optimization of Multigate Bulk MOSFETs," IEEE Transactions on Electron Devices, vol.60, no.1, pp.28, 33, Jan. 2013.

[32] M. Charmi, Ali A. Orouji, Hamid R. Mashayekhi, “Design considerations of underlapped source/drain regions with the Gaussian doping profile in nano-double-gate MOSFETs: A quantum simulation,” Materials Science in Semiconductor Processing, Volume 16, Issue 2, April 2013, Pages 311-317.

[33] N. Damrongplasit, N. Xu, H. Takeuchi, R. J. Stephenson, N. W. Cody, A. Yiptong, X. Huang, M. Hytha, R. J. Mears, T. J. K Liu, "Comparative Study of Uniform Versus Supersteep Retrograde MOSFET Channel Doping and Implications for 6-T SRAM Yield," IEEE Transactions on Electron Devices, vol.60, no.5, pp.1790,1793, May 2013.

[34] R. Vaddi, R. P. Agarwal, S. Dasgupta, "Compact Modeling of a Generic Double-Gate MOSFET With Gate–S/D Underlap for Subthreshold Operation," IEEE Transactions on Electron Devices, vol.59, no.10, pp.2846,2849, Oct. 2012.

[35] A. Nandi, A. K. Saxena, S. Dasgupta, "Analytical Modeling of a Double Gate MOSFET Considering Source/Drain Lateral Gaussian Doping Profile," IEEE Transactions on Electron Devices, vol.60, no.11, pp.3705,3709, Nov. 2013.

[36] A. Wang, B. H. Calhoun, and A. P. Chandrakasan, *Sub-Threshold Design for Ultra Low-Power Systems*. Springer, 2006.

[37] R. Jaramillo Ramirez, Variability-Aware Design of Subthreshold Devices, Electrical and Computer Engineering Department, University of Waterloo, Canada.

[38] S. Hanson, Bo Zhai, Kerry Bernstein, David Blaauw, Andres Bryant, Leland Chang, Koushik K. Das, Wilfried Haensch, Edward J. Nowak, and Dennis Sylvester. Ultralow-voltage, minimum-energy CMOS. *IBM Journal of Research and Development*, 50(4-5):469–490, 2006.

[39] C. Hyung-II Kim, Hendrawan Soeleman, and Kaushik Roy. Ultra-low-power DLMS adaptive filter for hearing aid applications. *IEEE Transactions on Very Large Scale Integration Systems*, 11(6):1058–1067, December 2003.

[40] J.E. Franca and Y.P. Tsividis. *Design of Analog-Digital VLSI circuits for Telecommunication and Signal Processing*. Prentice-Hall, 1994.

[41] H. Soeleman and K. Roy. Ultra-low power digital subthreshold logic circuits. In International Symposium on Low Power Electronics and Design (ISLPED 99), pages 94–96, San Diego, California, USA, July 1999.

[42] E. Vittoz and J. Fellrath. CMOS analog integrated circuits based on weak inversion operation. *IEEE Journal of Solid-State Circuits*, 12:224–231, June 1977.

[43] H. Soeleman and K. Roy. Digital CMOS logic operation in the sub-threshold region. In Tenth Great Lakes Symposium on VLSI, pages 107–112, Chicago, Illinois, USA, March 2000.

[44] B. H. Calhoun, A. Wang, and A. P. Chandrakasan. Device sizing for minimum energy operation in subthreshold circuits. In IEEE Custom Integrated Circuits Conference, pages 95–98, October 2004.

[45] M. Jamal Deen, M. H. Kazemeini, and S. Naseh, "Ultra-Low Power VCOs – Performance Characteristics and Modeling (invited)," in *Proceedings of the Fourth IEEE International Caracas Conference on Devices, Circuits and Systems*, 2002, pp. C033–1–C033–8.

[46] S. Hanson, B. Zhai, M. Seok, B. Cline, K. Zhou, M. Singhal, M. Minuth, J. Olson, L. Nazhandali, T. Austin, D. Sylvester, and D. Blaauw, "Exploring Variability and Performance in a Sub-200-mV Processor," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 4, pp. 881–891, Apr. 2008.

[47] C. H. I. Kim, H. Soeleman, and K. Roy, "Ultra-Low-Power DLMS Adaptive Filter for Hearing Aid Applications," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 11, no. 6, pp. 1058–1067, 2003.

[48] M. Seok, S. Hanson, Y. S. Lin, Z. Foo, D. Kim, Y. Lee, N. Liu, D. Sylvester, and D. Blaauw, "The Phoenix Processor: a 30pW Platform for Sensor Applications," in *Proceedings of IEEE Symposium on VLSI Circuits*, 2008, pp. 188–189.

[49] A. Wang and A. Chandrakasan, "A 180mV FFT Processor Using Subthreshold Circuit Techniques," in *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, 2004, pp. 292–529.

[50] B. Zhai, S. Hanson, D. Blaauw, and D. Sylvester, "A Variation-Tolerant Sub-200 mV 6-T Subthreshold SRAM," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 10, pp. 2338–2348, Oct. 2008.

[51] J. Kwong, Y. K. Ramadass, N. Verma, and A. P. Chandrakasan, "A 65 nm Sub-Vt Microcontroller With Integrated SRAM and Switched Capacitor DC-DC Converter," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 1, pp. 115–126, Jan. 2009.

[52] A. Wang, A. P. Chandrakasan, and S. V. Kosonocky, "Optimal Supply and Threshold Scaling for Subthreshold CMOS Circuits," in *IEEE Computer Society Annual Symposium on VLSI*, 2002, pp. 5–9.

[53] B. H. Calhoun and A. Chandrakasan, "Characterizing and Modeling Minimum Energy Operation for Subthreshold Circuits," in *Proceedings of International Symposium on Low Power Electronics and Design*, 2004, pp. 90–95.

[54] www.synopsys.com, HSPICE User Guide: Simulation and Analysis.

[55] J. M. Soden, C.F. Hawkins, and A.C. Miller. Identifying defects in deep-submicron CMOS ICs. *IEEE Spectrum*, 33:66–71, September 1996.

[56] M. Anis and M. Elmasry. *Multi-Threshold CMOS Digital Circuits: Managing Leakage Power. Kluwer*, Norwell, MA, USA, 2003.

[57] A. Bryant, J. Brown, P. Cottrell, M. Ketchen, J. Ellis-Monaghan, and E. J. Nowak, "Low-Power CMOS at Vdd = 4kT/q," in *Proceedings of Device Research Conference*, 2001, pp. 22–23.

[58] K. Roy, S. Mukhopadhyay, and H. Mahmoodi-Meimand. Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits. *Proceedings of the IEEE*, 91:305–327, February 2003.

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