INVESTIGATION OF INTERCONNECT AND DEVICE DESIGNS FOR EMERGING POST-MOSFET AND BEYOND SILICON TECHNOLOGIES

A DISSERTATION IN
Electrical and Computer Engineering
and
Physics

Presented to the Faculty of the University
of Missouri-Kansas City in partial fulfillment of
the requirements for the degree

DOCTOR OF PHILOSOPHY

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2016

INVESTIGATION OF INTERCONNECT AND DEVICE DESIGNS FOR EMERGING POST-MOSFET AND BEYOND SILICON TECHNOLOGIES

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University of Missouri-Kansas City, 2016

ABSTRACT

The integrated circuit industry has been pursuing Moore's curve down to deep nanoscale dimensions that would lead to the anticipated delivery of 100 billion transistors on a 300 mm^2 die operating below 1V supply in the next 5-10 years. However, the grand challenge is to reliably and efficiently take the full advantage of the unprecedented computing power offered by the billions of nanoscale transistors on a single chip. To mitigate this challenge, the limitations of both the interconnecting wires and semiconductor devices in integrated circuits have to be addressed.

At the interconnect level, the major challenge in current high density integrated circuit is the electromagnetic and electrostatic impacts in the signal carrying lines. Addressing these problems require better analysis of interconnect resistance, inductance, and capacitance. Therefore, this dissertation has proposed a new delay model and analyzed the time-domain

output response of complex poles, real poles, and double poles for resistance-inductance-capacitance interconnect network based on a second order approximate transfer function. Both analytical models and simulation results show that the real poles model is much faster than the complex poles model, and achieves significantly higher accuracy in order to characterize the overshoot and undershoot of the output responses.

On the other hand, the semiconductor industry is anticipating that within a decade silicon devices will be unable to meet the demands at nanoscale due to dimension and material scaling. Recently, molybdenum disulfide (MoS_2) has emerged as a new super material to replace silicon in future semiconductor devices. Besides, conventional field effect transistor technology is also reaching its thermodynamic limit. Breaking this thermal and physical limit requires adoption of new devices based on tunneling mechanism. Keeping the above mentioned trends, this dissertation also proposed a multilayer MoS_2 channel-based tunneling transistor and identifies the fundamental parameters and design specifications that need to be optimized in order to achieve higher ON-currents. A simple analytical model of the proposed device is derived by solving the time-independent Schrodinger equation. It is analytically proven that the proposed device can offer an ON-current of 80 μA/μm, a subthreshold swing (S) of 9.12 mV/decade, and a I_{ON}/I_{OFF} ratio of 10^{12}.

APPROVAL PAGE

The faculty listed below, appointed by the Dean of the School of Graduate Studies, have examined a dissertation titled "Investigation of Interconnect and Device Designs for Emerging Post-MOSFET and Beyond Silicon Technologies," presented by Muhammad Sana Ullah, candidate for the Doctor of Philosophy degree, and certify that in their opinion it is worthy of acceptance.

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LIST OF ABBREVIATIONS

AWE	Asymptotic Waveform Evaluation
BTBT	Band To Band Tunneling
CAD	Computer Aided Design
CDMA	Code Division Multiple Access
CMOS	Complementary Metal Oxide Semiconductor
CNTTFET	Carbon Nanotube Tunnel Field Effect Transistor
DFT	Density Functional Theory
DOS	Density of States
FDMA	Frequency Division Multiple Access
GNR	Graphene Nanoribbon
h-BM	Hexagonal Boron Nitrite
IC	Integrated Circuit
LTI	Linear Time Invariant
MIMO	Multiple Input Multiple Output
MRA	Matrix Rational-function Approximations
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NC-FET	Negative Capacitance Field Effect Transistor
PRIMA	Passive Reduced-order Interconnect Macromodeling Algorithm
RLC	Resistance Inductance Capacitance

SCE	Short Channel Effect
SI	Signal Integrity
SPICE	Simulation Program with Integrated Circuit Emphasis
TDMA	Time Division Multiple Access
TFET	Tunneling Field Effect Transistor
TMD	Transition Metal Dichalcogenides
VLSI	Very Large Scale Integration
WKB	Wentzel Kramers Brillouin

LIST OF SYMBOLS

V_{DD}	Supply voltage
V_{th}	Threshold voltage
ε_0	Dielectric constant
ε_r	Relative permittivity
μ_0	Permeability in free space
C_l	Load capacitance
R_d	Driver resistance
T_D	Time constant
t_p	Propagation delay
ζ	Damping factor
ω_n	Natural frequency
$H(s)$	Transfer function
$g(s)$	Normalized transfer function
t_r	Rise time
F_f	Frequency-of-flight
T_{ED}	Elmore delay
τ_c	Propagation delay for complex pole
τ_r	Propagation delay for real pole

τ_d	Propagation delay for double pole
m^*	Effective mass
E_g	Energy Bandgap
k	Extinction coefficient
λ	Tunneling screening length
t_{ox}	Oxide thickness
S	Subthreshold swing
L	Channel length
ξ	Electric field

ACKNOWLEDGEMENTS

I would like to express my deepest sense of gratitude to my advisor, Dr. Masud Chowdhury, for giving me an opportunity to work in the exciting area of emerging device and interconnect issue in high density integrated circuits. I am very thankful to him for his time, patience and effort in mentoring me. I learned a great deal about research and the scientific method through my work with him. In addition, I have profited from his knowledge, wisdom, kindness, confidence and great humanity. His immense knowledge and technical expertise throughout the research made it possible to overcome all the hurdles towards the completion of the dissertation. His constant encouragement, motivation and guidance helped me from the beginning to the end of my dissertation work.

My dissertation committee, Dr. Ghulam Chaudhry, Dr. Deb Chatterjee, Dr. Corey Beard, and Dr. Paul Rulis have been helpful, serene and generous throughout this process and I feel honored that they have invested their valuable time and served on my dissertation committee. In addition, I am truly grateful to Professor Ghulam Chaudhry for his continuous help and support from the department during my doctoral study.

I would like to convey my special thanks and appreciation to the staff in the Department of Computer Science and Electrical Engineering at University of Missouri-Kansas City, especially our Research Associate Nan Lorenz for the correction of my technical papers. I would also like to sincerely thank my colleagues Azzedin Es-Sakhi, Emeshaw Ashenafi, Abdul

Hamid, Munem Hossain, Marouf Khan, Nahid Hossain, and Abdullah Alharbi for technical discussions.

I am profoundly grateful to my loving family, especially to my mother who has always provided moral support and noble advice. I could not begin to express in a few lines how grateful I am to my elder brothers and sisters for their love, moral and logistical support. It is a blessing for me to have such a wonderful family who has always been an inspiration to achieve the goal of my life.

Finally, I would like to thank the School of Graduate Studies and the Department of Computer Science and Electrical Engineering for awarding the research grant and travel grant for this research work which encouraged me to work harder and helped my research work gain recognition nationally as well as internationally.

CHAPTER 1

INTRODUCTION

Problem Identification and Significance

Due to rapidly shrinking feature size and exponentially growth of the complexity of conventional CMOS technology, the integrated circuit (IC) industry has been pursuing Moore's curve down to deep nanoscale dimensions. It is anticipated that it will deliver over a 100 billion of transistors on a 300 mm^2 die operating below 1V power supply at GHz range frequency in the next 5-10 years. However, the grand challenge is to reliably and efficiently take the full advantage of the unprecedented computing power offered by the billions of nanoscale transistors on a single chip. The speed of an electrical signal in an IC is governed by two components. The first component is the switching time of an individual transistor, known as transistor gate delay [5], and the second one is the signal propagation time between transistors, known as wire delay or interconnect delay [4]. Therefore, to mitigate this challenge, the limitations of both the interconnect wires and semiconductor devices in integrated circuits (ICs) have to be addressed.

At the interconnect level, the major challenge in current high density integrated circuit is the electromagnetic (due to inductance) and electrostatic (due to capacitance) impacts in the signal carrying lines [2]. Addressing these problems require better analysis of interconnect resistance (R), inductance (L), and capacitance (C). Inductance, which is more prominent in the wider top-layer interconnect lines used for clock and global signal

distribution, introduces various anomalies like oscillation, overshoot, ringing in signal waveform and electromagnetic interference in integrated circuits [1]. As a consequence, both signal delay and noise would increase with higher inductance [3]. Therefore, accurate and efficient modeling and estimation of RLC interconnect parameters is very critical for high performance integrated circuits. Modeling and analysis of interconnect parasitics are computationally very difficult due to the 3D effects inside complex ICs. Including inductance further complicates the analysis of integrated circuits. Therefore, both accuracy and efficiency are equally important in interconnect modeling and signal propagation characterization. Also, accuracy of the estimation of inductive effects is important for the precise quantification of its impact on performance and optimization.

At the semiconductor device level, although reducing the size of MOSFET has enabled extraordinary improvements in the switching speed, density, functionality and cost of integrated circuit, silicon devices are reaching the limits of dimension and material scaling. Semiconductor industry is anticipating that within a decade silicon devices will be unable to meet the demands at nanoscale. At present, advanced MOSFET technology now faces many challenges. Increasing power consumption of integrated circuits is one of the main hindrances to furthering progress of computation technologies today [5]. Scaling of the supply voltage (V_{DD}) is the most effective way to reduce the dynamic power [6]. However, the degradation of dynamic performance with decreasing V_{DD} is today particularly challenging. In addition, lower supply voltage dictates lowering the threshold voltage, which leads to exponential increase of subthreshold leakage and degraded the transistor performance (ON/OFF current ratio) [6]. A better tradeoff between dynamic performance and standby power can be achieved with

electronic switches capable of a subthreshold swing (S) smaller than 60mV/decade at room temperature, which is the fundamental or thermodynamic (kT/q) limit of conventional MOSFETs [7]-[8]. This fundamental limit is not scalable because this limit depends on the fundamental material and physical parameters of the MOSFET transistor. The subthreshold swing indicates the ability of a transistor to deliver current for a certain voltage. Lower value of S means lower voltage requirement to generate a certain amount of current. Transistors based on quantum tunneling have been singled out by the International Technology Roadmap for Semiconductor (ITRS) as the most promising small subthreshold swing devices. To overcome this fundamental material and technological barrier, the only path is to move the integrated circuit designs to post-MOSFET technology platform, where device gain would not depend on the above-mentioned thermodynamic limits.

Due to growing interest and exciting progress in this research area, this dissertation has introduced new steep devices, and replaced silicon by emerging two-dimensional (2D) nanomaterials that can push the scaling and performance limits beyond the capabilities of MOSFET and silicon technologies. Since any IC solution must also address interconnect level issues, this dissertation also investigates better modeling approach for RLC parasitics of interconnect lines.

Specific Goals and Objectives

In general, the goals of this dissertation are divided into two phases: Phase I and Phase II. Phase I is included the RLC interconnect delay model for distributed network which mainly focus on the following objectives:

i. To investigate the evolution of delay models with the scaling of technology. Our specific focus would be to investigate delay models used to analyze signal communication networks in very large scale integration (VLSI) circuits.

ii. To develop an analytical delay model for distributed RLC network using second order approximation for real and complex poles scenarios.

iii. To analyze the electromagnetic effects to validate the analytical models for distributed RLC interconnect network.

On the other hand, Phase II of this dissertation mainly focuses on investigating and resolving the key fundamental issues and finding an innovative design solution for next generation tunnel field effect transistor (TFET) based on emerging 2D molybdenum disulphide (MoS_2) for ultra-low-power applications. The specific technical objectives of Phase II are as follows:

i. To find the material, electrical and optical properties of MoS_2 and investigate the prospects of MoS_2 for tunneling device.

ii. To build an appropriate device structure of tunnel FET (TFET) based on emerging 2-D MoS_2.

iii. To develop the analytical model of tunneling current and subthreshold swing based on proposed device structure.

iv. To analyze and optimize the electrical behavior of proposed tunnel FET in terms of process and parametric variations.

The Interdisciplinary Nature of this Research

New applications of physics can push the boundary of what is possible in electrical engineering, particularly in the areas of materials and devices, both solid-state electronic and optical. Materials with electronic band gaps of up to ~3 eV, and resistivities in the range typically 10^{-3} to 10^{9} Ohm-cm, are known as semiconductors [9]-[10]. Their electronic properties are strongly dependent on temperature, and may be readily manipulated through the controlled addition of dopants. Through an understanding of the physics of semiconductors, it is possible to create designer electronic materials with a wide range of properties. Junctions between differently doped semiconductors can be readily fabricated, which form the basis of simple electronic components that underpin all modern solid-state electronics. Understanding the physics behind devices is vital for anyone who aspires to master their craft and fully understand the complex mechanisms that modern technology takes advantage of. In particular, without a basic understanding of quantum physics, it is impossible to understand how and why semiconductor electronic devices function that is proposed in this dissertation. Therefore, by thoroughly understanding the science such as mathematical physics, quantum mechanics, classical mechanics, physics of electronics, and many others, I provide myself a set of skills that allows me to comprehend the theory behind the applications studied in electrical engineering, which is related with my research. Not only this, but these classes bolster my mathematical abilities by teaching me a variety of techniques which is always advantageous for my research. Many times it turned out that I learned things in physics and was able to reuse it in my research and it ultimately saved my time and helped to finish my PhD in time.

Broader Impacts of this Research

This dissertation problem will directly affect the lives of many communities and the IC industry itself. The outcome of this research is expected to help the extended life cycle of conventional field effect transistor based technologies in the subthreshold domain. It will also generate knowledge towards successful deployment of a new technology in the consumer sector. Fast ultra-low-power subthreshold devices and circuits are expected to find a wide spectrum of application areas, ranging from homeland security, emergency and crisis management, disaster recovery, military battlefield coordination, biomedical devices, transportation, portable computing and communication devices, as well as complex social applications such as distributed gaming and the management of distributed learning services. Network-based micro-sensors will enable a variety of applications such as warehouse inventory tracking, location sensing, machine-mounted sensing, patient monitoring, and building climate control. Since many of these micro- and nano-devices would be operated on low energy scavenged from nature, the proposed research will also indirectly contribute towards the progression of another very important emerging field: energy scavenging for ambient electronics. In the context of current interests and progresses in introducing radical alternatives to conventional integrated circuit design, it can be inferred that the implementation challenge will be resolved in the near future. The outcome of this research is also expected to fuel the interest to bring technological and engineering breakthroughs for successful implementation and manufacturing of post-silicon systems.

Organization of this Dissertation

This dissertation is organized as follows. Chapter 2 presents a detail trend of high speed VLSI interconnects by describing previous analytical delay models. Chapter 3 describes the proposed RLC interconnect delay models for complex and real poles including the accuracy characterization using second order approximation transfer function. Investigation of tunneling for field effect transistor from silicon to 2-D graphene is and limitations of conventional MOSFET technology are described in Chapter 4. The electronics and optical properties of molybdenum disulfide (MoS_2) -a 2-D emerging material for transistors applications is explored in Chapter 5. Chapter 6 is described the device structure and operating principle of proposed MoS_2 based tunnel transistor. An analytical model and how to optimize of tunneling current and subthreshold swing in terms of process and parametric variations are also described in Chapter 6. Finally, Chapter 7 summarizes and concludes this dissertation with future research directions.

CHAPTER 2

PREVIOUS MODELS ON INTERCONNECT DESIGNS

Why VLSI Interconnect

The IC industry has been pursuing Moore's curve down to deep nanoscale dimensions that lead to the anticipated delivery of 100 billion transistors on a 300mm^2 die below a 1V supply at GHz range frequency [1]-[3], [11]. However, conventional two-dimensional (2D) integration of the enormous number of transistors on a single substrate would not provide the expected improvements in terms of functionality, reliability and performance. Three-dimensional (3D) integrated circuits have evolved as the most potential future direction to increase the integration capacity of CMOS devices and facilitate integration of heterogeneous materials, devices and technologies based on silicon, group III-V semiconductors, carbon nanotubes, graphene and other 2D nanomaterials. However, the grand challenge is to reliably and efficiently take the advantage of the unprecedented computing power offered by the billions of transistors on a single chip. Electrical interconnects, which will remain as the primary medium of signal communication in all existing and emerging IC technologies, are limited by interconnect parasitic effects. All the investigations and predictions indicate that the overall signal propagation delay will be governed by interconnect delay in the scaled integrated circuits, and interconnect centric limitations prevent us from taking full advantage of what nanoscale technology can offer. It is important to predict signal degradation like propagation

delay, crosstalk noise, signal overshoot, ringing and attenuation in the early design cycles [12]-[14] which can critically affect system response. By using the CAD tools for signal integrity, simulations have replaced the more time consuming and inefficient practice of circuit development and testing at every stage of the design cycle for modern IC circuitry. However interconnect simulations suffer from a myriad of issues which require sophisticated CAD tools for analysis.

In the early years of IC technology design, interconnects were modeled as lumped capacitance [2]. As the technology has advanced, the dimensions of devices and interconnects have shrunk. As a result, line resistance has also become significant and interconnect line has been modeled as a lumped RC circuit [4]. Later, in order to improve accuracy and capture high frequency effects, the interconnect wire is modeled as distributed RC sections [15]. Furthermore, in nanometer regimes, ICs are operated at very high frequencies and the lengths of global interconnect have increased manifolds. Therefore, interconnect parasitic inductances, which were ignored in earlier designs, cannot be disregarded due to the longer length of wire and the higher signal frequencies in extremely dense integrated circuits [1]-[2]. Inductance, which is more prominent in the wider top-layer interconnect lines used for clock and global signal distribution, introduces various anomalies like oscillation, overshoot and ringing in signal waveform and electromagnetic interference in the integrated circuits. As a consequence, both signal delay and noise would increase with higher inductance [3]. Therefore, accurate and efficient modeling and estimation of interconnect parameters are very critical for high performance integrated circuits. Modeling and analyzing interconnect parasitic elements are fundamentally difficult from a computational point of view due to the 3D effects inside

complex ICs. Including inductance makes it further complicated. Therefore, both accuracy and efficiency are equally important in interconnect modeling and signal propagation characterization. Also, accuracy of the estimation of inductive effects is essential for correct output realization, and the quantification of the impact of inductance on interconnect and circuit behavior at high frequency. Hence, at highly scaled technology nodes, the distributed RLC or transmission line model is used [1]-[2], [16]-[18].

Existing well-established RLC interconnect analysis techniques are based either on analytical or simulation methods. Simulation methods, such as full circuit SPICE/HSPICE simulation, give the most accurate understanding of the behavior of random interconnect configurations. However, computationally this method is very expensive and is not feasible at all stages of design hierarchy since this requires simulating circuit networks composed of millions of logic gates. Therefore, the analysis of transient simulation for lossy interconnect structures was used by the convolution technique and faster analytical methods established on moment computation are suggested in [19]-[24]. In addition, complex frequency hopping [25], asymptotic waveform evaluations [26], scattering parameter macro models [27], cascaded ABCD matrixes [28], effective lumped resistance and capacitive models [29], methods of characteristics [30], and rational approximation model (such as PRIMA [31], MRA [32]-[33], compact differences [34]) are broadly used to investigate and model the propagation delay of interconnect transmission lines. Since these techniques are computationally too expensive to be used throughout the repeating layout and/or circuit minimization, the Elmore propagation delay model is most widely used for delay analysis. The Elmore delay model gives the RC delay of the interconnect line that signifies the first pole of the transfer function in the Laplace

domain. However, the Elmore delay cannot estimate the propagation delay for the RLC interconnect lines for which inductive impedance effects cannot be ignored [35].

In order to avoid the computational complexity of SPICE simulations, closed-form analytic models have been developed and derived for on-chip interconnects. In this closed form analytical model, far end transistor is modeled as parasitic capacitor and near end transistor is modeled as resistor serially connected to a voltage source. These models are usually effective for obtaining the far end solutions. To obtain more accurate models, Fourier analysis [1], multi-pole transfer functions [36]-[40], traveling-waveform technique [41]-[42], and modified Bessel function [43]-[46] were introduced later on. However, extending these techniques to efficiently analyze RLC tree structures is still a challenging task.

For analysis, including inductance, an approach based on moment matching is better [11]. For faster analysis, including a lower number of moments is necessary. However, a lower number of moments leads to higher errors in the estimation. During the initial design steps, it is often necessary to quickly estimate and monitor the anticipated performance. In those cases, a faster approach with a minimum number of moments will be very valuable. Therefore, this dissertation introduces a novel mathematical approach to model delays in distributed RLC interconnect networks under a constant V_{dd} supply to include the effects of inductance in the propagation delay estimation. This novel mathematical delay model is based on the quadratic equation that represents the first and second poles of the transfer function in the Laplace domain, where a pole can be either real or complex at specific interconnect structures.

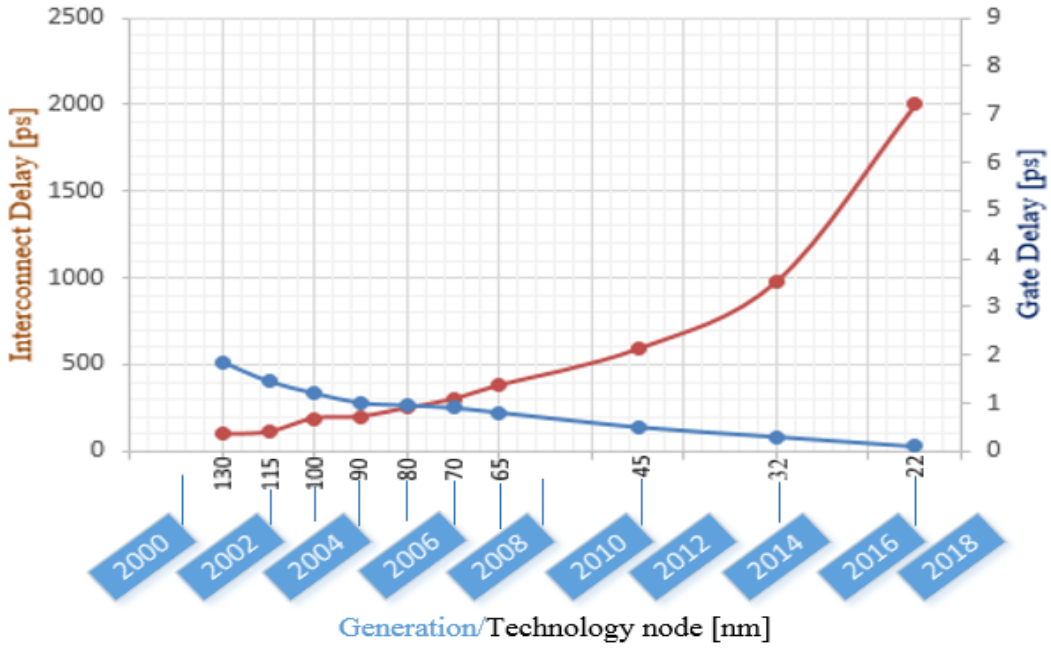


Figure 1 Interconnect and gate delay with IC technology evolution [47]

Physical and Electrical Parameters of Interconnect

As technology is scaled, interconnect delay starts to dominate the gate delay which is shown in Figure 1. Since inductance effect can no longer be ignored due to high operating frequencies and technology shrink, inductive coupling can be considered over a long distance. In fact, inductance is a physical property of a closed current loop. Besides, capacitive coupling is limited to adjacent interconnects. As a result, it is not straightforward to extend the existing parasitic extraction approach to perform inductance extraction in on-chip interconnects.

Interconnect in VLSI and Integrated circuits can be considered as strip lines or microstrip transmission lines. For microstrip lines, it consists of a conductive strip of controlled width on a low-loss dielectric material mounted on a conducting ground plane. Microstrip is the most popular structure, especially for VLSI and other integrated circuits. The major advantage of microstrip is that all active components can be mounted on the top of the board.

The physical structure of such interconnect is shown in Figure 2, where w, t, h are the interconnect width, height (or thickness), inter-layer dielectric thickness respectively. Interconnect width, height and length can be controlled by the circuit designer. Transmission lines are best described by Telegraphers equation where per unit length resistance (R), inductance (L) and capacitance (C) are needed. From the physical design of interconnect structures, it is important to extract the electrical parameters of the interconnect in terms of per unit length of R, L, and C before performing the timing analysis in the design flow. In standard cell design, quick interconnect parasitic extraction and delay estimation are done at the place and route stage for optimum placement. This extraction becomes important since the interconnect design affects every stage of the design flow.

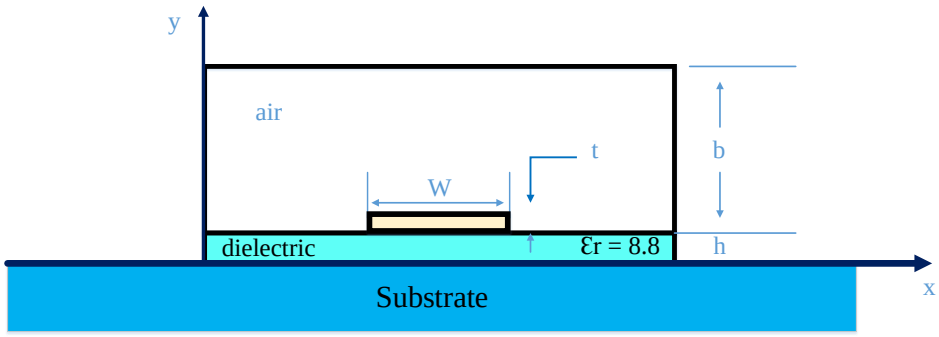


Figure 2 Cross-section of a single-strip shielded transmission line.

$$R = \rho \frac{l}{wt} \tag{2.1}$$

$$C = l\left[\frac{2\pi\varepsilon_0\varepsilon_r}{\ln(h/t)} + \frac{(\omega - 0.5t)\varepsilon_0\varepsilon_r}{h}\right] \tag{2.2}$$

$$L = \frac{\mu_0 l}{2\pi}\left[\ln\left(\frac{2l}{w+t}\right) + 0.5 + \frac{0.22(w+t)}{l}\right] \tag{2.3}$$

There are usually two ways to extract electrical parameters of interconnect from their physical parameters. One way is to use analytical expressions, which are fast to calculate. Another way is to use field solver [48]-[49]. Analytical expressions [50] of interconnect per unit length resistance and capacitance are given by equation of (2.1) and (2.2) for the structure that is shown in Figure 2, where ε_0 and ε_r are dielectric constant, and relative permittivity, respectively. From the predictive technology model [51], the interconnect inductance equation is given in equation (2.3) where μ_0 is the permeability in free space. Another approach for determining the per unit length parameters is to use 2D and 3D electro-magnetic field-solvers [49], [52]. In HSPICE, the physical parameters of interconnect based on latest technology can be given to extract the electrical R, L, and C parameters. Field solver provides better accuracy when compared to analytical formulas at the expense of computational complexity. Once the electrical parameters are identified, it is necessary to develop a model to estimate the delay. There are several closed form interconnect models which have been developed over the years. Next section will discuss some of those closed form models.

Review of Closed form RLC Interconnect Models

Analysis of on-chip interconnects are based on either simulation techniques or closed-form analytic formulas. When it comes to modeling of on-chip interconnects for signal integrity verification, the most important difficulty is the numerical integration problem. This is because the distributed interconnects are best described by Telegrapher's partial differential equations which can provide an exact transfer function for the far end response in the frequency domain only. However it does not have an exact time domain representation. To provide an accurate time domain representation, numerical integration techniques [53] are required at

every time step. Simulation tools such as SPICE use numerical integration or convolution techniques at every time step to provide accurate results. However, these techniques are computationally expensive to be used in layout optimization [41].

For an iterative layout design of densely populated integrated circuits composed of hundred millions of gates, accurate analytic models are needed to efficiently predict the delay and rise times of interconnects. One of the traditional methods was to express the frequency domain transfer function of interconnects as a simple rational function which could then be converted to poles and residues form [36]-[40], [54]. As poles and residues have a direct representation in the time domain, the interconnect response can now be evaluated without numerical integration at every time step. Using this idea, on-chip interconnects were analyzed as single-pole Elmore-based RC models [4], [36]-[38] to estimate signal delay at early stages. In current integrated circuit designs, wire inductance can no longer be ignored due to higher operating speeds and longer electrical line lengths. Thus, analytic RLC interconnect models are required to efficiently characterize the signal responses of today's high-performance integrated circuits. All of the above factors contribute to make on-chip interconnect modeling highly challenging. Closed form models are important because of their simplicity while maintaining reasonable accuracy as compared to SPICE. The next sub sections deal with various closed form models proposed in the literature.

Elmore Delay Based Models (Single Pole Model)

One of the earliest and popular models for SI verification in interconnects was the Elmore delay based models as proposed in [36]. For ease of presentation without loss of generality, each interconnect is explained as simple lumped RC circuits as shown in Figure 3.

This model is commonly used in VLSI design theory [12]-[13], [30], [32]-[33], [39]-[40], [56]-[59]. Transfer function of such RC circuit is given in equation (2.4) where $R_T = R_s + R$ and $C_T = C + C_l$ are the total interconnect resistances and capacitances respectively which includes sources resistance and load capacitance. Now if the input is a unit step function, then the time domain solution is given by equation (2.5) where T_D represents the time constant which is $R_T C_T$.

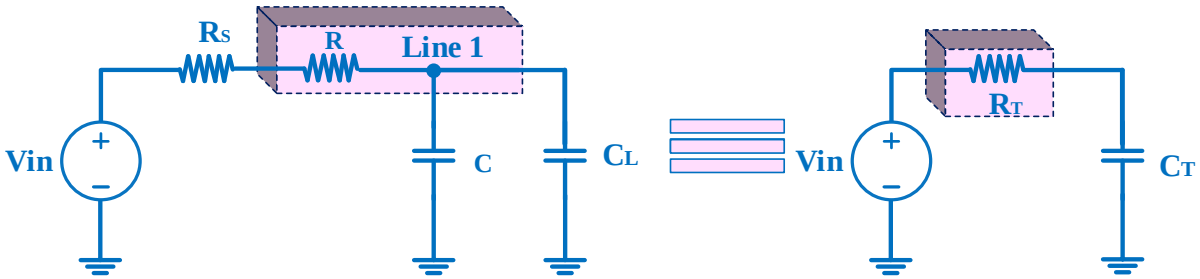


Figure 3. Circuit model of Elmore RC interconnect.

$$H(s) = \frac{1}{1 + sR_T C_T} \tag{2.4}$$

$$V_{out}(t) = 1 - e^{-\frac{t}{T_D}} \tag{2.5}$$

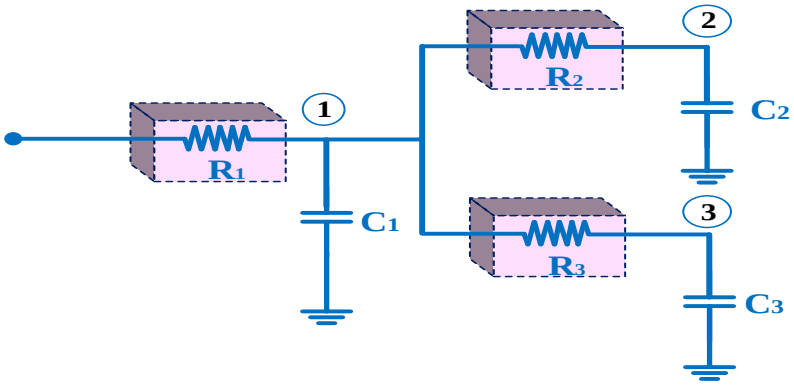


Figure 4 Circuit Model Elmore RC Tree Structure Interconnects

$$H(s) = \frac{1}{1 + \sum_k C_k R_{ik}} \tag{2.6}$$

$$H(s) = 1 + m_1 s + m_2 s^2 + \cdots \ldots \ldots \tag{2.7}$$

$$= 1 - s\left(-\sum_k C_k R_k\right) + s^2\left(-\sum_k C_k R_{2k}\right)^2 + \cdots \ldots \ldots \ldots$$

The Elmore model is particularly appealing for tree structure interconnects where each interconnect in tree structure is considered as lumped RC circuits which is shown in Figure 4. From the input to the node i and index k, the transfer function of such tree structure at node i is given by equation (2.6) where k is the index that covers every capacitor in the circuit; and R_{ik} is the common resistance [2], [36]. This first-order approximation matches the first moment of the transfer function at node *i* but approximates the higher-order moments by $m_i = (-\sum_k C_k R_{ik})^i$as seen by the expansion of equation (2.7).

$$T_{Di} = \sum_k C_k R_{ik} \tag{2.8}$$

$$t_{p(50\%)} = 0.693 T_D \tag{2.9}$$

The Elmore model is basically single pole model (first order approximation).There is a simple closed-form solution for the time constant T_{Di} for the tree structure that is shown in Figure 4. As a result, the time constant at node i and 50% propagation delay for unit step input are given by equation (2.8) and equation (2.9) respectively. Since the delay of an exponential function of (2.5) is well defined and easy to analyze, this model was very popular among circuit designers. However, this model does not consider inductance effect, which is very obvious when modern switching speeds touch the GHz range. As a result transient response of

interconnects may become non monotonic due to the large line inductances. For such cases, instead of RC model, RLC models (two pole) or even multi-pole models are required.

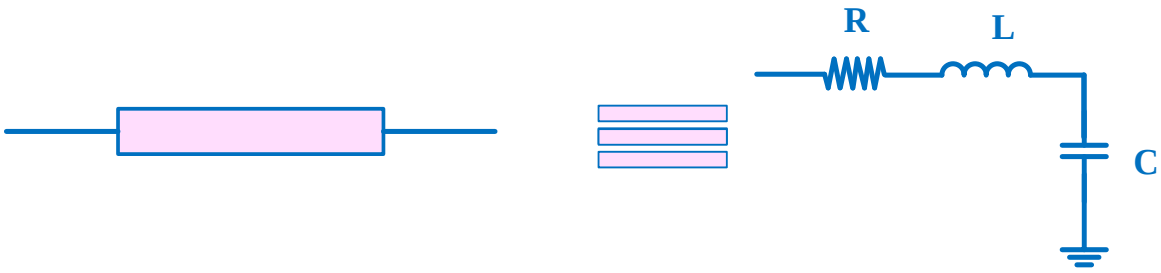


Figure 5 Lumped RLC Section for Equivalent Elmore Delay

Elmore Delay Based Two Pole Lumped Models

The transfer functions of single line interconnect or tree structure interconnect include hyperbolic functions of the complex frequency variable s and do not have a direct representation in the time domain. This makes it difficult to analytically predict the signal delay of interconnect networks. As a result, the extension of equivalent two-pole Elmore delay models for RLC tree networks is developed in [2], [60]-[61]. For the case of the two pole lumped model [56], single line interconnect is represented as lumped RLC elements as shown in Figure 5. As a result, the circuit of Figure 5 has second order transfer function which is given by (2.10). This transfer function is expressed in terms of its damping factor ζ and natural frequency ω_n as shown in (2.11) where $\zeta = \frac{RC}{2\sqrt{LC}}$ and $\omega_n = \frac{1}{\sqrt{LC}}$. After solving, the poles of the transfer function of (2.11) are given as $P_{1,2} = \omega_n\left(-\zeta \pm \sqrt{\zeta^2 - 1}\right)$.

$$H(s) = \frac{1}{LCs^2 + RCs + 1} \tag{2.10}$$

$$H(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{2.11}$$

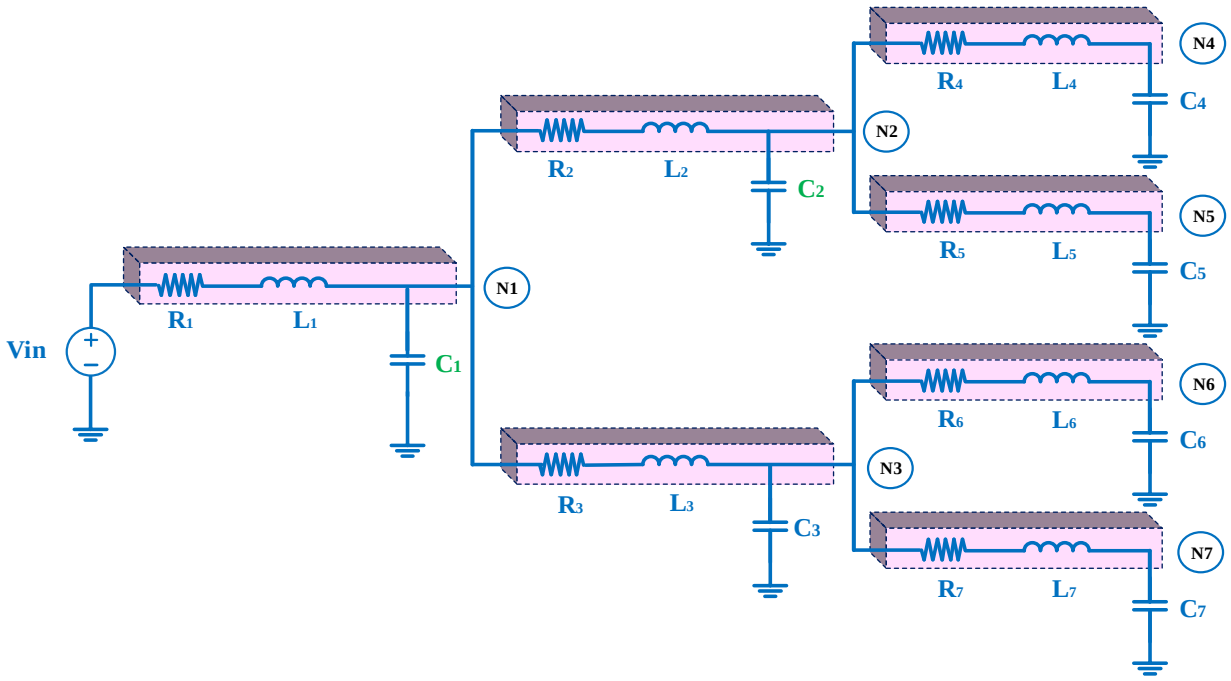


Figure 6 Circuit model for lumped *RLC* trees

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} \approx 1 + m_1 s + m_2 s^2 \approx \frac{1}{1 + b_1 s + b_2 s^2} \tag{2.12}$$

$$m_j = \frac{1}{j!}\frac{d^j H(s)}{ds^j}, \qquad j = 1,2 \ldots\ldots \tag{2.13}$$

$$b_1 = -m_1 \qquad b_2 = m_1^2 - m_2 \tag{2.14}$$

$$m_1^i = \sum_k C_k R_{ik} \tag{2.15}$$

$$m_2^i = \left(\sum_k C_k R_{ik}\right)^2 - \sum_k C_k L_{ik} \tag{2.16}$$

For the case of the tree structure network, each interconnect in the tree is modeled as lumped resistive-inductive-capacitive (RLC) elements, as shown in Figure 6. Typically, moment matching techniques are used to express the transfer functions of this tree structure interconnect as a power series [61] of (2.12) where the moment m_j is defined as (2.13). The

first two moment of (2.13) (alternative representation of (2.15) and (2.16)) of this tree network at node N_j can be calculated using the following simple closed-form expressions [2] where first moment is similar to $m_i = (-\sum_k C_k R_{ik})^i$ of RC circuit of Figure 4. Here k is the index that covers every capacitor in the circuit; R_{ik} and L_{ik} are the common resistance and inductance, respectively, from the input voltage node to node N_i and N_k [2]. For the general RLC tree that shown in Figure 6, the voltage drop at any node as N_i compared to the input voltage is expressed as (2.17). If the input is a unit impulse, $V_{in}(s)$ is equal to 1.0 and the voltages at the nodes of the tree are the unit impulse responses of these nodes. Thus, the normalized transfer function $g_i(s)$ at node N_i of tree structure is written as (2.18). Using the moment matching techniques, the natural frequency(ω_{n_i}) and damping factor (ζ_i) at this transfer function of node N_i of general tree structure is given by equation (2.19). The time constants RC and $\sqrt{LC}$ in single line structure are replaced by the summations of the equivalent time constants in the tree structure.

$$V_{in}(s) - V_i(s) = \sum_k C_k V_k(s) s(R_{ik} + L_{ik} s) \tag{2.17}$$

$$g_i(s) = 1 - \sum_k C_k V_k(s) s(R_{ik} + L_{ik} s) \tag{2.18}$$

$$\omega_{n_i} = \frac{1}{\sqrt{\sum_k C_k L_{ik}}} \qquad \& \qquad \zeta_i = \frac{\sum_k C_k R_{ik}}{2\sqrt{\sum_k C_k L_{ik}}} \tag{2.19}$$

$$V_{out}(t) = V_{DD} + \frac{V_{DD}}{2\sqrt{\zeta^2 - 1}} \left(\frac{e^{t\left(-\zeta + \sqrt{\zeta^2 - 1}\right)}}{-\zeta + \sqrt{\zeta^2 - 1}} - \frac{e^{t\left(-\zeta - \sqrt{\zeta^2 - 1}\right)}}{-\zeta - \sqrt{\zeta^2 - 1}} \right) \tag{2.20}$$

$$t_{d(50\%)} = \frac{1.047 e^{-\zeta/0.85} + 1.39\zeta}{\omega_n} \tag{2.21}$$

Once the transfer function of single line or tree structure interconnect is obtained in the form of damping factor and natural frequency, the time domain response of (2.11) for a step input with supply voltage of V_{DD} is given by (2.20). The output voltage of (2.20) is a nonlinear function with respect to the variable ζ. As a result, an analytic formula is not directly available for the 50% delay since the solution of (2.20) is obtained iteratively using methods so called Newton-Rhapson's method. For this reason, equation (2.20) is solved for various values of ζ by setting V_{out} to $0.5V_{DD}$ and solving for time (t). The results of this analysis are stored and fitted to the following functions [2] where $t_{d(50\%)}$ corresponds to 50% delay with respect to time *t*. This equation is like the extension of 50% delay of Elmore model of (2.9) considering the inductance effect of interconnect. Equation (2.21) can also be used to calculate the rise time by setting V_{out} to $0.1V_{DD}$ and $0.9V_{DD}$ and solving t for different values of ζ. So the expression of rise time [2] is shown in (2.22). Elmore based models such as the fitted expression of (2.21) and (2.22) are widely used in VLSI circuit design for fast delay estimation due to its computational efficiency.

$$t_r = \frac{6.017e^{-\zeta^{1.35}/0.4} - 5e^{\frac{-\zeta^{1.25}}{0.64}} + 4.39\zeta}{\omega_n} \tag{2.22}$$

$$\frac{\partial}{\partial x}V(x,s) = -(R + sL)I(x,s) \tag{2.23}$$

$$\frac{\partial}{\partial x}I(x,s) = -sCV(x,s)$$

$$\begin{bmatrix} V(l,s) \\ -I(l,s) \end{bmatrix} = e^{\phi l}\begin{bmatrix} V(0,s) \\ I(0,s) \end{bmatrix} \tag{2.24}$$

Frequency Domain Representation of Transfer Function

The analysis of on-chip RLC interconnects starts with Telegrapher's equation in frequency domain. All closed form RLC models assume a quasi-TEM mode of signal propagation. This means that the effect of imperfect line conductors and inhomogeneous surrounding medium resulting in a component of the mutually transverse electric and magnetic fields along the line axis is considered negligible [55]. The Telegrapher's equations are a pair of linear differential equations which describe the voltage and current on a transmission line with distance and time. The equations come from Oliver Heaviside who in the 1880s developed the transmission line model. These equations are [55] are shown in (2.23), where s is Laplace transform variable, x is the position variable; $V(x,s)$ and $I(x,s)$ represent the voltage and current of the transmission line, respectively in the frequency domain; R, L and C are the per-unit-length resistance, inductance and capacitance, respectively. The per unit length conductance G is assumed to be negligible for on-chip interconnects. The solution of (2.23) can be expressed using the exponential matrix as (2.24) where $\phi = \begin{bmatrix} 0 & -Z \\ -Y & 0 \end{bmatrix}$, and $Z = R + sL$, $Y = sC$ and l is the length of the transmission line. The exponential matrix of (2.24) can be expressed using the $cosh$ and $sinh$ functions [55] as shown below in (2.25) where $Y_0 = Y\left(\sqrt{YZ}\right)^{-1}$.

$$\begin{bmatrix} V(l,s) \\ -I(l,s) \end{bmatrix} = \begin{bmatrix} \cosh\left(l\sqrt{ZY}\right) & -Y_0^{-1}\sinh\left(l\sqrt{YZ}\right) \\ -Y_0\sinh\left(l\sqrt{YZ}\right) & \cosh\left(l\sqrt{ZY}\right) \end{bmatrix} \begin{bmatrix} V(0,s) \\ I(0,s) \end{bmatrix} \tag{2.25}$$

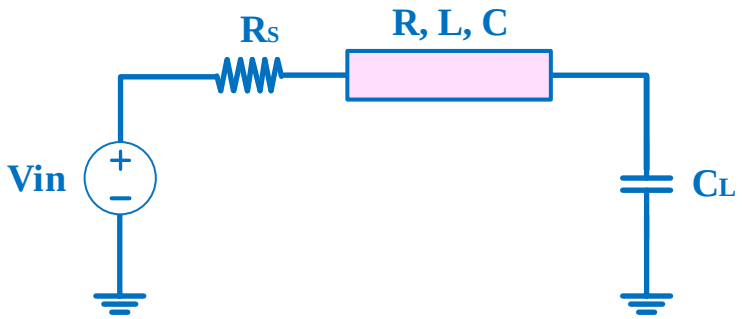


Figure 7 Circuit Model for Single Line Interconnect

Now we look at the circuit structure for a RLC interconnect line, which is shown in Figure 7. This represents a point-to-point interconnection driven by a transistor (modeled as voltage source V_{in} serially connected to a driver resistance R_d) and connected to the next gate (modeled as a capacitance C_l) and is commonly used in VLSI design theory [12]-[14], [30]-[33], [39]-[40], [56]-[59]. Considering this interconnect circuit as shown in Figure 7, the boundary conditions are represented as the following equations of (2.26) and (2.27), respectively.

$$V_{in} = V(0,s) + R_s I(0,s) \tag{2.26}$$

$$V(l,s) = -sC_l I(l,s) \tag{2.27}$$

Using (2.25)-(2.27), the far end transient response of single line interconnect can be described as (2.28) where $\Gamma = l\sqrt{YZ}$. This transfer function of single line and tree structure interconnect of (2.28) has no direct representation in the time domain and thus real-time prediction of delay of RLC interconnects. Various closed form models [12]-[14], [31]-[41] were developed to provide efficient representation of (2.9) in time domain and will now be discussed.

$$V_f = \frac{V_{in}}{(1 + sR_sC_l)\cosh(\Gamma) + (R_sY_0 + sC_lY_0^{-1})\sinh(\Gamma)} \tag{2.28}$$

However, the accuracy of Elmore models is limited since two poles may not be accurate enough to capture the high frequency effects and signal delays of RLC lines. The next chapter provides a methodology to improve Elmore based two pole model of RLC interconnects by extracting the delay from the transfer function.

CHAPTER 3

PROPOSED DELAY MODEL FOR INTERCONNECT DESIGN

Transfer Function of M-distributed RLC Interconnect

Figure 8 shows a schematic view of M-distributed parallel RLC interconnect model of a transmission line. This transmission line interconnect model is symbolized by a distributed RLC segment. Each segment has an interconnect resistance (R), inductance (L), and capacitance (C) per unit length, respectively. A total of 2000 micrometer lengths is considered to analyze this model and the interconnect length is denoted by l. The source or driver resistance is connected in series with each RLC segment. A linearized voltage source V_{in} is connected with each interconnect device (inverter for example). The output voltage of the inverter is directly applied to each interconnect transmission line. A load capacitance (C_l) is serially connected with each of the RLC segments in order to complete the electrical circuit. For simplification of calculation, all load capacitances assumed same values.

The electrical circuit of Figure 8 is an LTI system [62]-[64], whose response in time-domain can be estimated from the inverse Laplace transform of a LTI system. Equation (3.1) represents the exact transfer function [65] of each RLC segment from the input to the far end, where $\theta = l\sqrt{(R+sl)sC}$ in s domain, and R, L, C, R_d and C_l are the line resistance, line inductance, line capacitance, source or driver resistance and load capacitance per unit length of interconnect of length l respectively. Since each transmission line has one transfer function and each transfer function is connected in parallel in the schematic of the LTI system model,

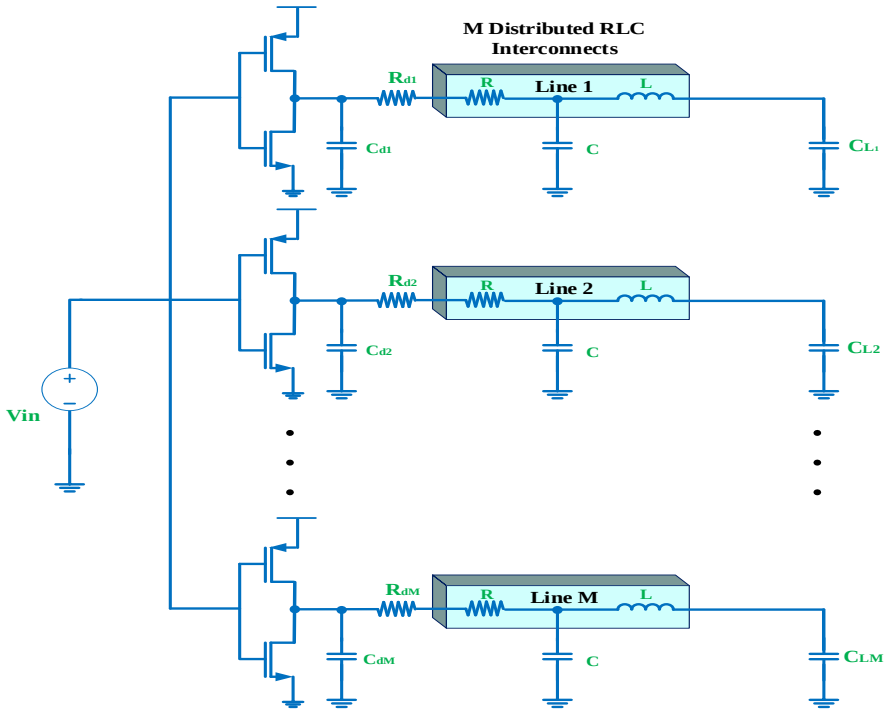


Figure 8 Schematic view of a distributed RLC interconnect network.

$$H_{exact}(s) = \frac{1}{(1 + R_d C_l s)cosh\theta + \left(\frac{R_d}{\sqrt{\frac{R + sL}{sC}}} + \sqrt{\frac{R + sL}{sC}} C_l\right) sinh\theta} \tag{3.1}$$

$$H_{Texact}(s) = \frac{M}{(1 + R_d C_l s)cosh\theta + \left(\frac{R_d}{\sqrt{\frac{R + sL}{sC}}} + \sqrt{\frac{R + sL}{sC}} C_l\right) sinh\theta} \tag{3.2}$$

the overall exact transfer function can be written as in (3.2). As the denominator of (3.2) consists of sine hyperbolic and cosine hyperbolic functions, converting the inverse Laplace transform would be very challenging due to the imaginary term in frequency, $s(jw)$. Therefore, the denominator of the exact transfer function is stretched into an infinite power series shown in (3.4) to simplify the task. Due to simplify the exact transfer function, it is collecting the

coefficient factors of the second order polynomials in the denominator and the exact transfer function can be approximated by two dominant poles as in (3.4), where the coefficients are $C_1 = R_d C_l + \frac{l^2}{2} RC + lR_d C + lRC_l$ and $C_2 = \frac{l^2}{2}(R_d C_l RC + LC) + lLC_l$, respectively.

$$H_{Texact}(s) \tag{3.3}$$

$$= \frac{M}{(1 + R_d C_l s)\left\{1 + \frac{1}{2!}\left(\left(l\sqrt{(R + sl)sC}\right)^2 + \cdots\right)\right\}} + \left(\frac{R_d}{\sqrt{\frac{R + sL}{sC}}} + \sqrt{\frac{R + sL}{sC}}\, C_l\right)\left\{\left(l\sqrt{(R + sl)sC}\right) + \frac{1}{3!}\left(\left(l\sqrt{(R + sl)sC}\right)^3\right) + \cdots\right\}$$

$$H_{Tapproximate}(s) \approx \frac{M}{1 + C_1 s + C_2 s^2} \tag{3.4}$$

In Figure 9, the approximate transfer function of (3.4) is compared to the exact transfer function of (3.2). For our investigation, we have considered 180 nm CMOS technology and the following interconnect parameters are considered: $l = 2000\ \mu m$, $R = 8.829\ m\Omega$, $L = 1.538\ pH$, and $C = 0.18\ fF$, which show the complex pole nature [11]. The total driver/source resistance and total load capacitance are $30\ \Omega$ and $50\ fF$ respectively. All interconnect resistance, inductance, and capacitance values are in per micrometer lengths. In addition, for analyzing the real pole nature, the following interconnect parameters are used: $l = 2000\mu m$, $R = 1.5 m\Omega$, $L = 0.246\ pH$, and $C = 0.176\ fF$. Also, the total driver/source resistance and total load capacitance are used $25\ \Omega$ and $0.176\ fF$, respectively [66]. As demonstrated in Figure 9, for this example, a normal two-pole model would be accurate up to 5.42 GHz and 14.62 GHz for complex pole and real pole models, respectively. For the LTI system, the poles of the transfer functions are directly related to the resonance frequency in the s-domain.

Resonance frequency is the frequency where the peaks occur in the frequency domain function. So we see from Figure 9 that the approximate second order transfer function can pick the first harmonic frequency (first resonance frequency) of the exact transfer function. Therefore, we can say that this model can almost accurately define two poles of the system. The magnitude of the transfer function carries the same information in both negative- and positive-frequency domains. Therefore, the other pole with the same magnitude is located in the negative-frequency domain and the high peaks (see Figure 9) occur in both transfer functions due to high inductance values.

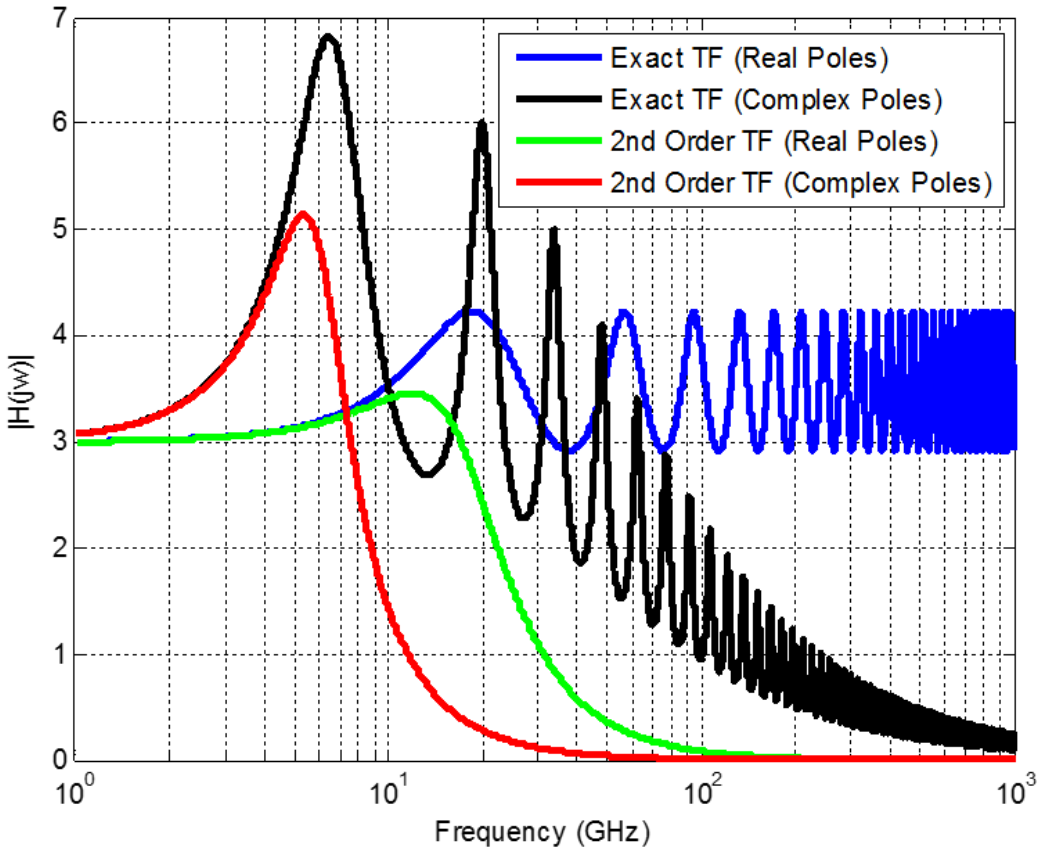


Figure 9 Exact and approximate transfer function models of an RLC interconnect for complex and real poles.

Effect of Inductance on Transfer Function

If the interconnect lines are modeled as a RC network, the magnitude of the transfer function would have no overshoots and decrease gradually with the increase of the frequency, which means no resonance frequency effect will occur. Figure 10 shows the effect of different inductance values using the exact transfer function model of the RLC interconnect. Figure 10 shows that when $L = 0.162\,pH$ and $R_d = \sqrt{L/C}$ (the characteristics impedance at high frequencies) there is no resonance effect. When R_d is larger than $\sqrt{L/C}$ (for $L = 1.538\,pH$), the basic resonance frequency is about $F_f/5$, where $F_f = \frac{1}{l}\sqrt{\frac{C}{L}}$ is the frequency-of-flight. Alternatively, when R_d is less than $\sqrt{L/C}$ (for $L = 0.072\,pH$ or $0.028\,pH$), the basic resonance frequency is about $2nF_f$, where $n = 1, 2$.

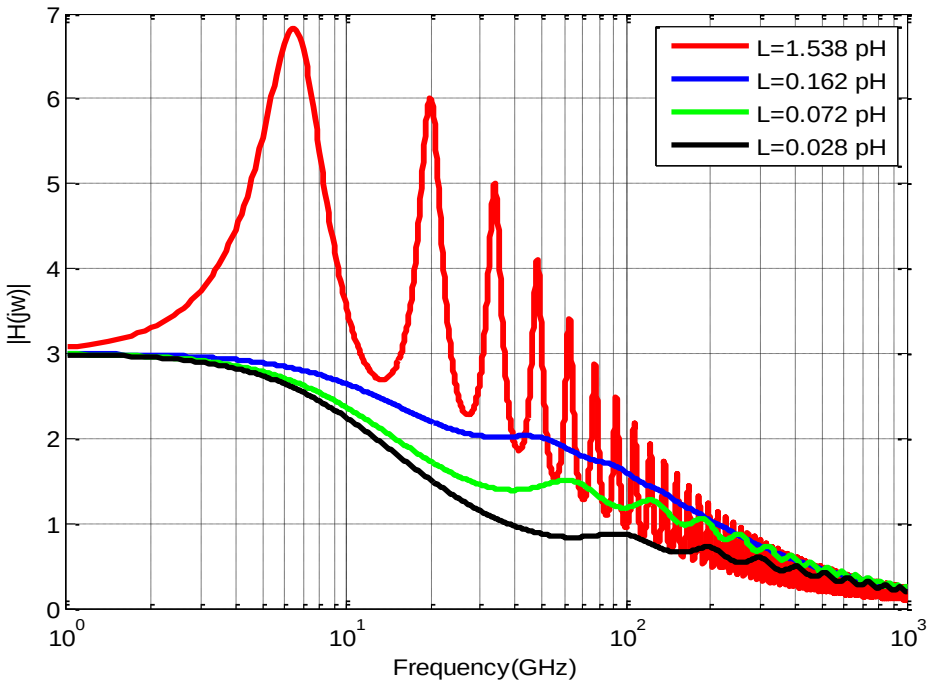


Figure 10 Inductive effects on amplitude transfer function of RLC interconnect for different inductance values.

Proposed Analytical Delay Models

We have developed the delay model for the RLC interconnect lines from (3.4) based on the first and second moments to consider the effects of inductance. Depending on the sign of $C_1^2 - 4C_2$, the roots of the denominator of the approximate transfer function can be real or complex. The real roots will have two different scenarios - two different real roots and two identical roots. Here, we present models for complex, real and double pole cases.

Complex Pole Model

When $C_1^2 - 4C_2 < 0$ in the solution of the quadratic equation of the denominator in (3.4), the poles will be complex. The output response for complex poles in the Laplace domain is given in (3.5) and we need to solve (3.5) in time domain by taking the inverse Laplace transform [62]-[64] that is shown in (3.6), where $p_1 = \alpha + j\beta, p_2 = \alpha - j\beta$, $\alpha = -\frac{C_1}{2C_2}$, and

$$V_{out}(s) = V_{in}(s)H_{Tapproximate}(s) = \frac{V_{dd}}{s}\left(\frac{M}{(s-p_1)(s-p_2)}\right) \tag{3.5}$$

$$V_{out}(t) = \frac{MV_{dd}}{p_1 p_2}\left(1 - \frac{p_2}{p_2 - p_1}e^{p_1 t} + \frac{p_1}{p_2 - p_1}e^{p_2 t}\right) \tag{3.6}$$

$\beta = \frac{\sqrt{C_1^2 - 4C_2}}{2C_2}$. Using (3.6) and the output-to-input voltage ratio (V_r), we obtain (3.7) for optimized delay, where $\theta = tan^{-1}\left(\frac{\beta}{\alpha}\right)$. The propagation delay at a given output-to-input voltage ratio can be calculated by solving (3.7) recursively in time. One approach for solving (3.7) recursively is to estimate the time adjustable in an exponential stretch by the Elmore delay (T_{ED}) and the time of sine function. This time of sine function is replaced by time delay for complex poles (τ_c) and $\theta = tan^{-1}\left(\frac{\beta}{\alpha}\right)$, which are substituted in (3.7) and yields (3.8). Note

that the Elmore delay for this interconnect model is $T_{ED} = R_d(C + C_l) + R\left(\frac{C}{2} + C_l\right)$. The details of the derivation of (3.8) is provided in the Appendix A.

$$e^{\alpha t} sin(\beta t + \theta) = \beta\left(1 - \frac{\alpha^2 + \beta^2}{M} V_r\right) \tag{3.7}$$

$$\tau_c = \frac{1}{\beta}\left[sin^{-1}\left(\beta e^{-\alpha T_{ED}}\left(1 - \frac{\alpha^2 + \beta^2}{M} V_r\right)\right) - tan^{-1}\left(\frac{\beta}{\alpha}\right)\right] \tag{3.8}$$

Real Pole Model

When $C_1^2 - 4C_2 > 0$ in the solution of the quadratic equation of the denominator in (3.4), the poles are real. The output response for the case of two different real poles in time domain is given by (3.9), where $p_1 = \frac{-C_1 + \sqrt{C_1^2 - 4C_2}}{2C_2}$ and $p_2 = \frac{-C_1 - \sqrt{C_1^2 - 4C_2}}{2C_2}$.

$$V_{out}(t) = \frac{MV_{dd}}{p_1 p_2}\left(1 - \frac{p_2}{p_2 - p_1} e^{p_1 t} + \frac{p_1}{p_2 - p_1} e^{p_2 t}\right) \tag{3.9}$$

$$V_{out}(t) \approx \frac{MV_{dd}}{p_1 p_2}\left(1 - \frac{p_2}{p_2 - p_1} e^{p_1 t}\right) \tag{3.10}$$

Since $p_2 - p_1 = -\frac{\sqrt{C_1^2 - 4C_2}}{C_2}$ is negative, the coefficients $\frac{p_2}{p_2 - p_1}$ and $\frac{p_1}{p_2 - p_1}$ are positive. Also, since the amplitude of $|p_2|$ is much larger than the amplitude of $|p_1|$, the second term $(\frac{p_1}{p_2 - p_1})$ is significantly less (almost negligible) compared to the first term $(\frac{p_2}{p_2 - p_1})$ in time domain output voltage responses. Therefore, the two-pole output voltage response of the inferior constrained voltage can be approximated by (3.10). Since the voltage is inferior constrained, the delay acquired is higher bound on the actual delay. Therefore, for real poles, the delay (τ_r) at the output-to-input voltage ratio (V_r) can be given by (3.11).

$$\tau_r = \frac{1}{p_1} ln\left[\left(\frac{p_2 - p_1}{p_2}\right)\left(1 - \frac{p_1 p_2}{M} V_r\right)\right] \tag{3.11}$$

Double Pole Model

When $C_1^2 - 4C_2 = 0$ the poles are real and equal (double poles). The corresponding s-domain output response is shown in (3.12), where $p_1 = -\frac{C_1}{2C_2}$. By finding the inverse Laplace transform, the output voltage response in time domain for this case can be given by (3.13). Using the recursive method, the delay (τ_d) for the case of double poles can be calculated by solving (3.13) and the delay (τ_d) can be achieved by (3.14). In a practical scenario, a double-pole phenomena may be applied when the magnitude of $C_1^2 - 4C_2$ is within the range of output-to-input voltage ratio. We have experimentally investigated a variety of interconnect network structures with various combinations of drivers and load impedances. We noticed that the value of $C_1^2 - 4C_2$ should be of the same order as the value of C_1 for both the real and complex pole cases. However, the value of $C_1^2 - 4C_2$ never goes to zero because the $C_1^2 - 4C_2$ term evidently shows either greater than or less than zero. Therefore, the result of (3.14) is not shown in simulation results. The behavior of the proposed time delay model (for complex and real poles)

$$V_{out}(s) = \frac{MV_{dd}}{p_1^2}\left(\frac{1}{s} - \frac{1}{s - p_1} + \frac{p_1}{(s - p_1)^2}\right) \tag{3.12}$$

$$V_{out}(t) = \frac{MV_{dd}}{p_1^2}(1 - e^{p_1 t} + p_1 t e^{p_1 t}) \tag{3.13}$$

$$\tau_d = \frac{1}{p_1}\left[1 - e^{-p_1 T_{ED}}\left(1 - \frac{p_1^2}{M} V_{th}\right)\right] \tag{3.14}$$

is shown in Figure 11. All drivers and load parameters values are considered per micrometer length. From Figure 11, we observed that the real pole propagation delay model is much faster than the complex pole propagation delay model. Another finding from this research is that the

driver resistance has significant impact to switch from real to complex and vice-versa. We also see that our delay model is almost constant for different interconnect parameters (for example $R_d = 100$ and $C_l = 0.1$), even if we changed the ratio of output-to-input voltage from 0.5 V to 0.9 V. Only the driver resistance has a significant contribution to increase the time delay.

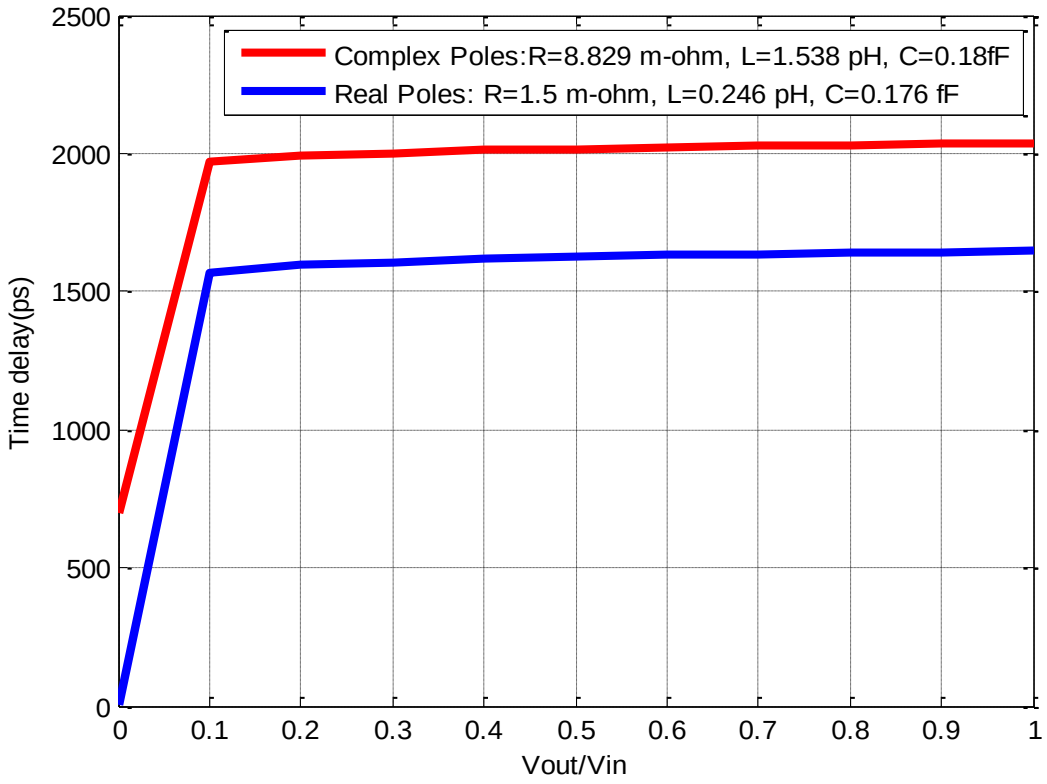


Figure 11 Characteristics of proposed complex and real poles based delay model.

Simulation Results of Proposed Analytical Delay Models

Table 1 is configured for complex poles by considering the ratio of V_{out}/V_{in} is 0.5 V. It is noticed that the proposed propagation delay model provides a good estimate as expected from Figure 11. It is noticed that the proposed propagation delay model provides a good estimate as expected from Figure 11.

Table 1. Simulation results for a line of length 2000 μm with complex poles at vout=0.5vdd. Here we consider a step input and 1V supply

Interconnect Parameters R, L, C (per μm)	Driver Resistance, $R_d(\Omega)$	Load Capacitance, C_l(fF)	SPICE Delay (ps)	Proposed Delay (ps)
0.008829 Ω 1.538 pH 0.18 fF	25	0.01	1549.6	1762.3
	50	0.01	1789.8	1903.9
	100	0.01	2564.6	3047.9
	25	0.1	1645.5	1762.8
	50	0.1	1605.6	1904.4
	100	0.1	2483.9	3048.7
0.0015 Ω 0.246 pH 0.176 fF	25	0.176	775.8	807.0
	50	0.176	2456.8	3028.4
	100	0.176	662.6	716.7
	25	1.76	653.9	719.8
	50	1.76	720.5	810.5
	100	1.76	2538.7	3036.4

Table 2. Simulation results for a line of length 2000 µm with real poles at vout=0.5vdd. Here we consider a step input and 1V supply

Interconnect Parameters R, L, C (per µm)	Driver Resistance, $R_d(\Omega)$	Load Capacitance, C_l(fF)	SPICE Delay (ps)	Proposed Delay (ps)
0.0015 Ω 0.246 pH 0.176 fF	100	0.01	1520.9	1623.8
	500	0.01	7570.7	8646.4
	1000	0.01	14720.8	17304.8
	100	0.1	1420.4	1624.2
	500	0.1	7776.9	8648.4
	1000	0.1	14320.9	17308.6
0.015 Ω 0.246 pH 0.176 fF	100	0.176	1468.4	1875.6
	500	0.176	7679.8	8883.5
	1000	0.176	15939.6	17542.0
	100	1.76	1548.7	1883.4
	500	1.76	7480.6	8913.4
	1000	1.76	15530.7	17585.7

Application and Accuracy of the Delay Models

In nanometer regimes, accurate characterizations of output responses for RLC interconnect networks have serious implications as they affect the signal integrity and other aspects of the system. Therefore, an accurate analysis of the output response is a very critical issue. Here in this section, we demonstrate how the proposed propagation delay model can be used in interconnect analysis. More specifically, we explain how to select the values of α and β in order to achieve higher accuracy of the proposed real and complex poles delay models. This is done by considering a driver resistance (R_d) and a load capacitance (C_l) with a simple RLC interconnect line model that is considered in Figure 8. The characteristic impedance (R_0) of the parallel interconnect line can be given by (3.15). Preferably, the value of driver resistance

and RLC parameters are needed to be matched so that R_d adjusts with R_0. However, if the driver resistance (R_d) is less than the characteristics resistance (R_0) of the interconnect line, the output voltage response will show ringing phenomenon that can decrease the delay [67]. The ringing leads to overshoots and undershoots that may lead to switching mismatch (erroneous switching).

$$R_o = \frac{1}{M}\sqrt{\frac{R + sL}{sC}} \tag{3.15}$$

$$V_{out}(t) = \frac{MV_{dd}}{\alpha^2 + \beta^2}\left(-\frac{e^{\alpha t} sin(\beta t + \theta)}{\beta}\right) \tag{3.16}$$

$$\delta V = -\frac{MV_{dd}}{\alpha^2 + \beta^2} e^{\alpha T_1} \sin(\beta T_1 + \theta) \tag{3.17}$$

$$\frac{\alpha}{\beta} \cong \frac{1}{2\pi} ln \left|\frac{1}{M}\frac{V_{dd}}{\delta V}\right| \tag{3.18}$$

$$C_1^2 = 4\left|\frac{(\alpha/\beta)^2}{(\alpha/\beta)^2 - 1}\right| C_2 \tag{3.19}$$

The voltage response with ringing behavior can be given by (3.16), where $\theta = arctan\left(\frac{\beta}{\alpha}\right)$ [67]. To obtain the output response in time domain, we look at the highest points of the oscillation in the transfer function and equate the output response derivative ($V'_{out}(t)$) to zero, compliant $\beta t = n\pi$, when n is the odd integer for overshoots and n is the even integer for undershoots. At $T_1 = 2\pi/\beta$, the first undershoot is occurred, which may be estimated by (3.17). After simplifying (3.17), the limit for a specified proportion of undershoot ($V_{dd}/\delta V$) can be derived from equation (3.18). For instance, we have $\delta V = 0.05V_{dd}$ and $\alpha/\beta = 0.30$ in

order to attain a 5% undershoot. We can find the ratio of $\frac{\alpha}{\beta}$ in terms of the coefficients of the quadratic equation of (3.4), i. e. $\frac{\alpha}{\beta} = \frac{C_1}{\sqrt{C_1^2 - 4C_2}}$. Therefore, we can get the relation between the coefficient of C_1 and C_2 from (3.19). Equation (3.19) condenses to $C_1^2 = 0.40C_2$ for approximately at 5% undershoot. Correspondingly, for 5% overshoot, the relation between C_1 and C_2 will be $C_1^2 = 9.8C_2$. In general, the value of α and β are summarized the undershoot and overshoot responses that might be useful to the proposed propagation model. This model is shown in (3.8) and (3.11), respectively to analyze the synthesis of integrated circuits.

The second order approximation and simplified transfer function, which is shown in (3.4), and introduced in this chapter can be applied to any arbitrary input signals. However, here we have analyzed the preciseness of the proposed model for exponential and periodic ramp input signals to validate the proposed analytical delay model for RLC interconnect line.

Effect of the Exponential Input Signal

To illustrate the behavior of the LTI system of Figure 8 for an exponential input with a second-order approximation the following input signal of (3.20) is considered.

$$V_{in(exp)}(t) = V_{dd}\left[1 - exp\left(-\frac{t}{\tau}\right)\right]u(t) \tag{3.20}$$

Here $u(t)$ is the unit step function, V_{dd} is the supply voltage, and τ is the time constant. The output response of a RLC line with this exponential input can be given by $V_{out}(t) = V_{in(exp)}(t) * h(t)$, where $h(t)$ is the inverse Laplace transform of the approximate transfer function of (3.4).

Effect of Periodic Ramp Input Signal

To illustrate the output behavior for a periodic ramp input [68] the following input signal in (3.21) is considered. Here T is represented as the time cycle of $V_{in}(t)$, n is an integer and τ_t is the switching time. The output response in time domain can be obtained by the convolution sum of the approximate transfer function and periodic ramp signal of (3.21).

$$V_{in(ramp)}(t) = \begin{cases} \frac{t}{\tau_t} V_{dd} & nT \le t \le nT + \tau_t \\ V_{dd} & nT + \tau_t \le t \le \left(n + \frac{1}{2}\right) T \\ \left(1 - \frac{t}{\tau_t} + \frac{T}{2\tau_t}\right) V_{dd} & \left(n + \frac{1}{2}\right) T \le t \le \left(n + \frac{1}{2}\right) T + \tau_t \\ 0 & \left(n + \frac{1}{2}\right) T + \tau_t \le t \le (n+1)T \end{cases} \quad (3.21)$$

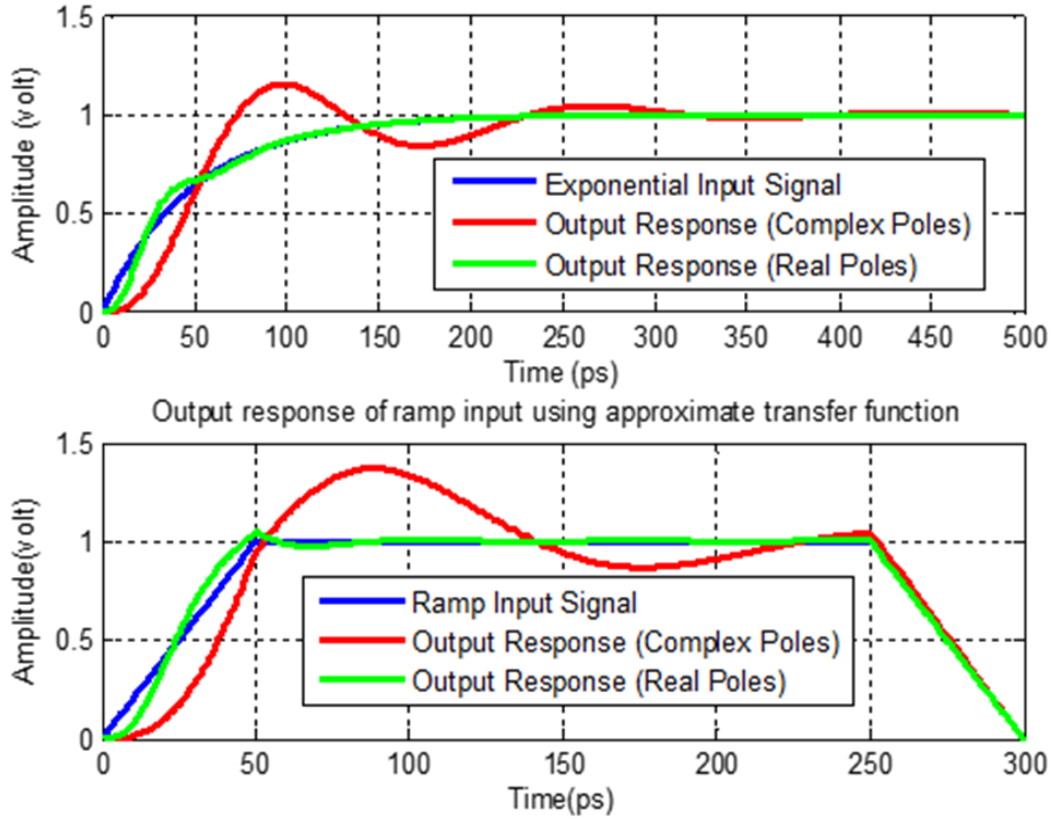


Figure 12 Output characteristics of exponential input signal using proposed complex and real pole transfer function model.

The output characteristics of the circuit model of Figure 8 for exponential and ramp input signals using the proposed real and complex pole based second order approximate transfer function of (3.4) are illustrated in Figure 12. The overshoots and undershoots in the output responses can be observed due to the capacitive and inductive natures of the circuit model. The second order approximation gives a higher performance in the estimation of the output behavior in the case of real poles compared to the output behavior in the case of complex poles.

CHAPTER 4

INVESTIGATION OF TUNNELING FOR FIELD EFFECT TRANSISTOR

Limitations of Conventional CMOS Technology

Continuous reduction of geometric dimensions of the field effect transistors (FETs) in the complementary metal-oxide-semiconductor (CMOS) circuits has enabled extraordinary improvements in the switching speed, density, functionality, and cost of micro- and nano-electronic applications [5]. But due to the physical limitations of silicon, advanced CMOS technology now faces some severe problems like excessive short channel effects (SCEs), high power consumption, and thermal stress beyond the limits of the materials used in integrated circuits at nanoscale domain. Increasing demand for faster operation dictates higher supply voltage (V_{DD}), which is actually being reduced to meet the power budget. Subthreshold leakage, which is the primary source of standby power, is going up due to lower threshold voltage (V_{th}) leading to degraded switching ratio of 'ON' and 'OFF' currents $\left({I_{ON}}/{I_{OFF}}\right)$[6]. With supply voltage (V_{DD}) reduction, the threshold voltage (V_{th}) needs to go down to ensure higher gate drive. However, reduction of V_{th} leads to exponential increase of the subthreshold leakage, making it the dominant component of power consumption. Conventional hardware-software coordination techniques would provide dynamic or switching power reduction [5], but the static power due to subthreshold leakage cannot be minimized if we continue using the

conventional MOSFET technology. This is because the subthreshold swing (S) of the conventional MOSFET and all the emerging transistors based on FET principle is not scalable below 60mV/decade at room temperature [7]-[8]. S = 60mV/decade is the theoretical minimum for any FET device, where the switching process involves the thermionic (temperature-dependent) injection of electrons over an energy barrier in order to flow current [70]. This theoretical minimum is only achievable under ideal condition that cannot be satisfied. This sets a fundamental limit to the steepness of the transition slope from the 'OFF' to the 'ON' state. The inverse of the slope of the I-V curve in the subthreshold region is defined as S, which can be given by (4.1), where V_G is the gate voltage, I_D is the drain current, kT/q is the thermal voltage, and C_d and C_{ox} are the depletion and oxide capacitances, respectively. The term m is the transistor body factor and n is a factor that characterizes the change of the drain current with the surface potential, and Ψ_s reflects the conduction mechanism in the channel.

$$S = \frac{dV_G}{\underbrace{d\Psi_s}_{m}} \frac{d\Psi_s}{\underbrace{d(\log_{10} I_D)}_{n}} \cong \left(1 + \frac{C_d}{C_{ox}}\right)\frac{kT}{q}\ln 10 \rightarrow \frac{kT}{q}\ln 10 \cong 60\frac{mV}{decade}|T = 300k \quad (4.1)$$

Faster operation of transistor requires steeper subthreshold slope (lower value of S). Only way to accomplish this is to find a radical solution beyond the conventional and emerging FET devices. Many innovative designs of transistor and circuits are under exploration to lower the value of S below the thermionic limit of MOSFET by decreasing the factor m and/or n in (4.1). One approach is to change the underlying physics of the way MOSFET transistor works by modifying the carrier-injection mechanism. For this, impact ionization [71] and quantum-mechanical band- to-band tunneling (BTBT) [72] have been proposed. The resulting transistor technology is known as the tunnel field effect transistor (TFET). Another approach is to lower

the subthreshold swing by developing an effective negative capacitance based field effect transistor (NC-FET) [73]-[75] or micro-/nano-electromechanical (M/NEM) movable electrodes in M/NEM-FET [76]-[77]. Achieving the NC effect required for these new type of transistors is still an elusive target, because the fundamental scientific principles that guide this NC effect is not yet fully understood. Therefore, the first approach, Tunnel FET seems to be a more feasible solution. Tunnel FETs (TFETs) avoid the thermionic limit by using quantum-mechanical band-to-band tunneling, rather than thermal injection, to inject charge carriers into the device channel.

Background Study of Tunneling Field Effect Transistor

TFETs represent the most promising candidate to implement very steep-slope switching device (transistor), having the potential to use a supply voltage significantly below 0.5V. Because of their low off currents, they are ideally suited for low-power and low-standby-power logic applications operating at moderate frequencies. Other promising applications of TFETs include ultralow-power specialized analog integrated circuits with improved temperature stability and low-power SRAM. Before introducing our proposed TFET, it would be helpful to explore the fundamental concept of tunneling device. Therefore, in this section, the basic principles of TFET is presented and discussed some real challenges.

The Concept of Tunneling

Electron has an ability to penetrate barriers - a phenomenon known as the quantum tunneling that represents a particle tunneling through an energy barrier similar to evanescent wave coupling of electromagnetic waves. One interpretation of this duality involves the Heisenberg uncertainty principle, which defines a limit on how precisely the position and the

momentum of a particle can be known at the same time. This implies that there are no solutions with a probability of electron charge distribution of exactly zero (or one). Therefore, the probability of a given particle's existence on the opposite side of an intervening barrier is non-zero. But with the scaling of technology, chipmakers are able to put increasingly more transistors inside a chip as transistors have become smaller and the distances between different regions of the transistor have decreased. As a consequence, electronic barriers that were once thick enough to block the tunneling current are now so thin that electrons can barrel right through them. For thick barrier, both Newtonian and Quantum mechanics ensure that the electrons cannot cross the barrier. It can only pass the barrier if it has more energy than the barrier height (see Figure 13(a)). But for thin barrier, Newtonian mechanics still dictates that the electrons cannot cross the barrier. However, Quantum mechanics dictates that the electrons' wave nature will allow it to tunnel through the barrier as shown in Figure 13(b).

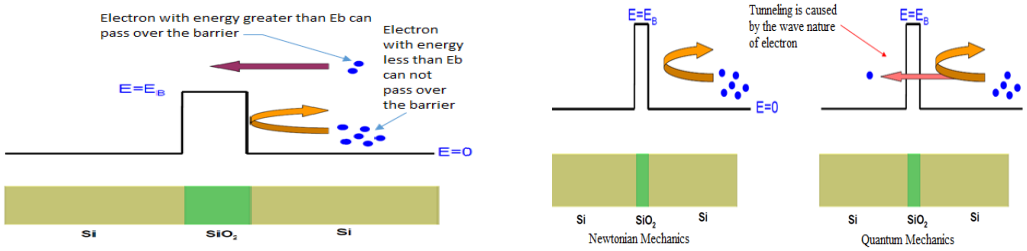


Figure 13 Concept of Newtonian and Quantum mechanics for (a) a thick barrier; and (b) a thin barrier

The Working Principle of Tunnel Transistor

The p-i-n diode structure of a TFET (see Figure 14), which is always reverse biased to get the ultralow leakage current. For NTFET the substrate is lightly n or p doped. The increase of gate voltage results in an accumulated or inverted n-channel. The surface tunnel junction is at the cross-point of gate oxide/channel/p++ doped region (Figure 14c). Electrons are tunneling

from the valence band (p++ doped region) to the conduction band (channel region) and flow to the n+ doped region. TFET's working principle is based on the gate controlled band-to-band tunneling. For NTFET, the p++ doped region is considered as the source (source of electrons) and the n+ doped region is considered as the drain (drain of electrons). The nTFET is switched on when the gate voltage is greater than the threshold voltage ($V_{gs} > V_{th}$).

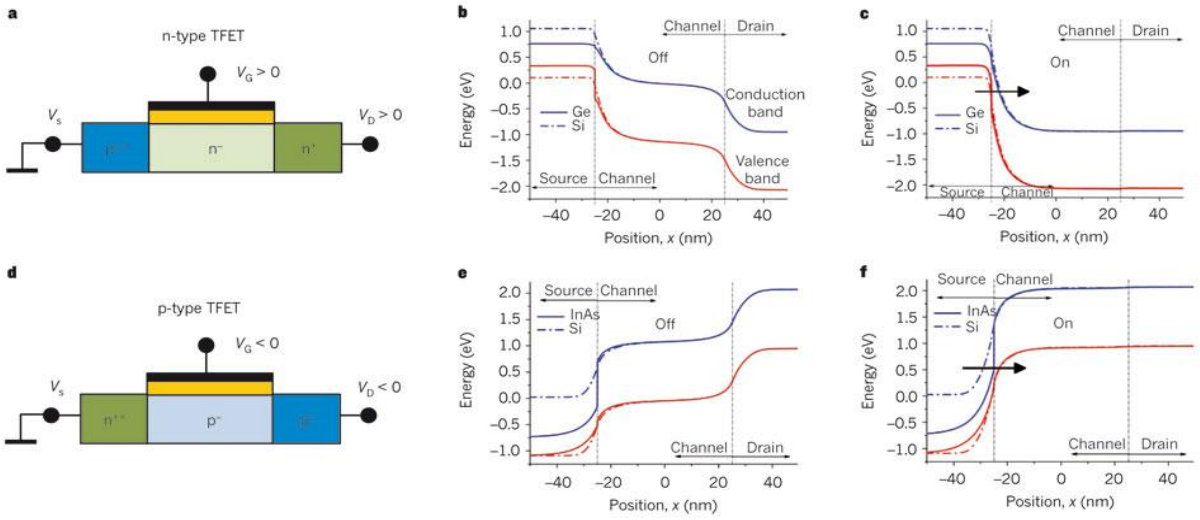


Figure 14. Basic Structure of TFET. (a) NTFET Structure, (b-c) related band diagram of NTFET in 'OFF' and 'ON' state. (d) PTFET structure, (e-f) related band diagram of PTFET in 'OFF' and 'ON' state [4].

Design of the First Tunnel Transistor

The first band-to-band tunneling based three terminal device was introduced as Trench Transistor Cell in [79]. Another three-terminal tunnel device using this effect was proposed in 1987 [80]. This device required gate overlap of the source. The device structure and phenomena can be used in a planar MOS structure, such as the one shown in Figure 15, which acts as a three-terminal tunnel device. A MOS capacitor is fabricated with a localized p^+ region separated from an n^+ contact by a p^- spacer region, which prevents breakdown of the p^+-n^+

junction. If the gate bias is increased, the p^+ substrate region depletes but cannot go into inversion if the n^+ drain is held positive with respect to the substrate. If the p^- doping is very high, the depletion region is narrow enough to allow band-to band tunneling. The generated electrons are collected by the n^+ drain.

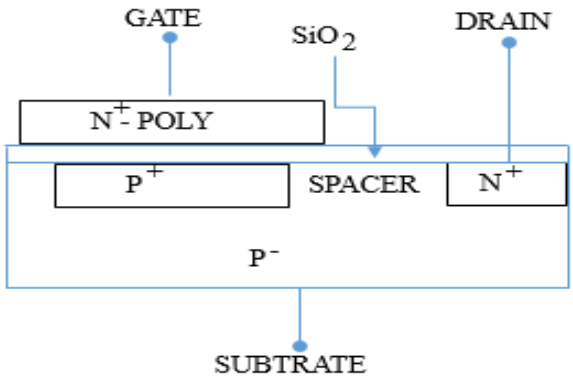


Figure 15. A three-terminal MOS tunneling device

Performance of TFET Technology: From Silicon to Graphene Technology

To analyze the performance of current TFET in terms of ON-current, OFF-current, and subthreshold swing [81]-[82], two comparison figures (Figure 16 and Figure 17) have been shown. The most frequently used method, as illustrated by the reports summarized in Figure 16, is to give the tangential inverse slope of the $I_D - V_{GS}$ curve at the steepest part of the characteristic. In this comparative study, only the TFETs that exhibit subthreshold swing below 60mV/decade are included in [8], [83]-[88].While the TFET ON-current is not dependent on the gate length, the gate length is indicated in the figure as is the gate oxide thickness to provide a scale for the experimental report. The subthreshold swings demonstrated thus far are not now in a current range of interest for logic applications as the low swing typically occurs at less than$1\text{nA}/\mu\text{m}$. Figure 17 provides the same plot of I_D/w versus V_{GS} for the theoretical TFET reports across material systems versus 3-nm CMOS technology [89]-[98]. The simulations

range over a wide space, but are consistent overall.

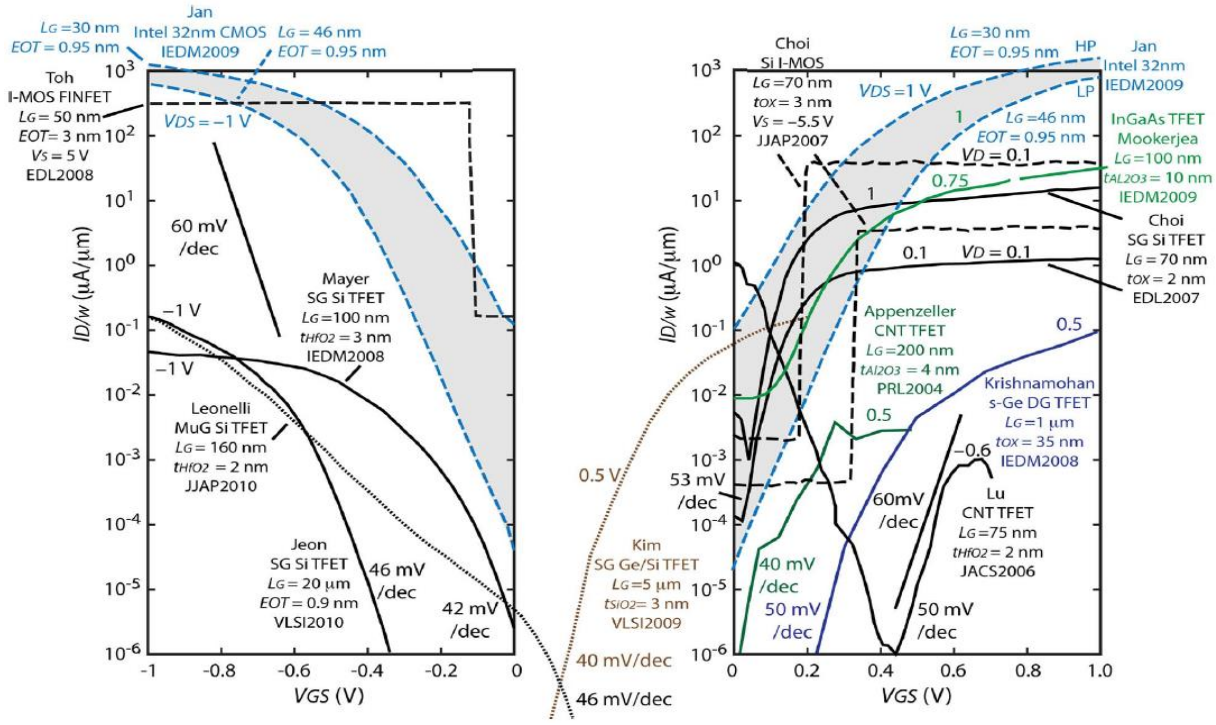


Figure 16. Comparison of published TFET channel current per unit width versus gate-to-source voltage for p-channel (left) and n-channel (right) transistors [81]-[89]. Included are devices that show a subthreshold swing less than 60 mV/decade in the forward characteristics of the tunnel junction. Dashed lines bordering the shaded area indicate measured high-performance (HP) and low-power (LP) 32-nm node MOSFET technology. The black dashed lines are measured characteristics for I-MOS transistors. The acronyms SG, DG, and MuG mean single, double, and multigate, respectively. All measurements were reported at room temperature. The CNTTFET drain current per unit width was computed by dividing the measured current by 10 nm as a representative effective tube pitch.

Higher ON-currents at lower voltages are obtained in the lower band gap material like Ge [99], InAs [96] and GNRs [91], [95]. Heterojunction systems like AlGaSb/InAs [92], [93], and

AlGaAsSb/InGaAs [100] boost the ON-currents. The wide range of TFET characteristics are clearly apparent from this analysis. These variations are generally consistent with a wide design space that includes many transistor geometries (gate-all-around, double gate, or single gate), in-line or perpendicular gate orientation with respect to the tunnel junction, tunnel junction doping level and profile, and dimensionality of the transport.

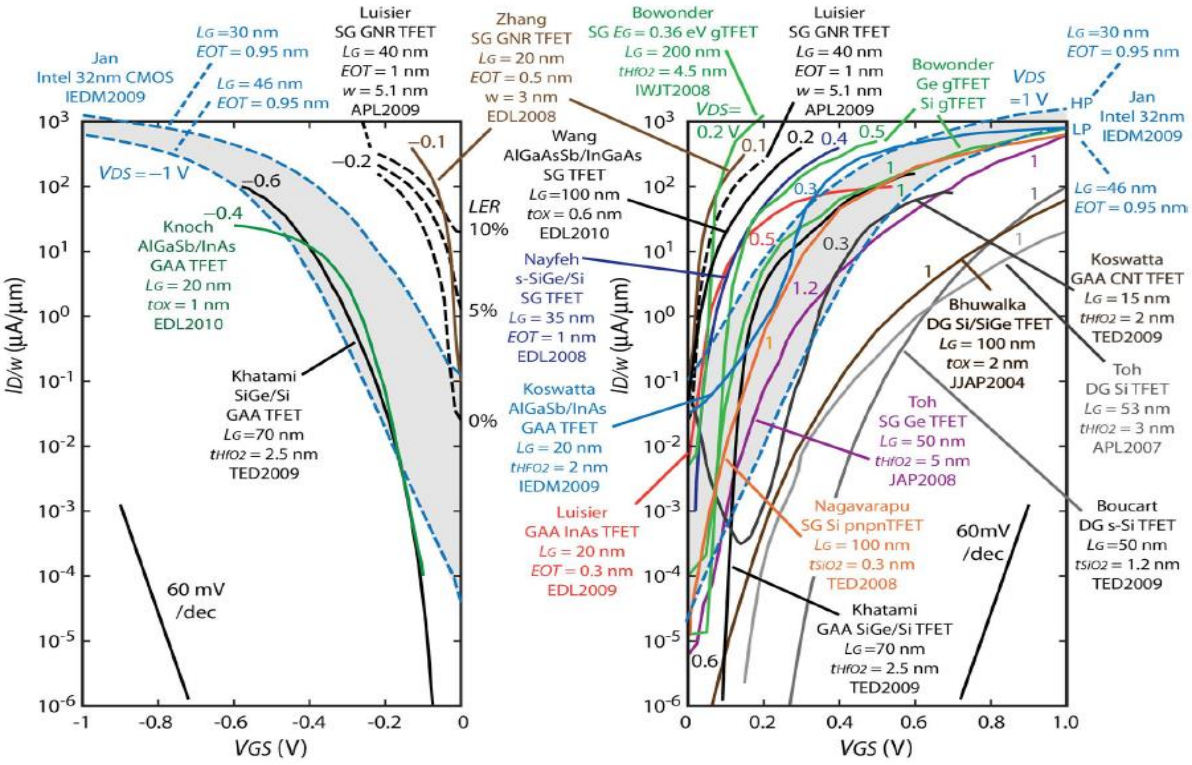


Figure 17. Comparison of simulated TFET channel current per unit width versus gate-to-source voltage for p-channel (left) and n-channel (right) transistors [91]-[100]. Light dashed lines bordering the shaded region indicate experimental high-performance (HP) and low-power (LP) 32-nm node MOSFET technology. Other notation in the figure includes SG for single gate, DG for double gate, GAA for gate-all-around, LER for line-edge roughness, and the numbers are for the drain-to-source voltages VDS. The GNR currents are given per unit ribbon width.

Limitations of TFET Technology from Material Perspectives

Although it has been shown that TFETs can be scaled down to 20 nm or below in channel length without much degradation of the subthreshold slope, I_{ON} and I_{OFF} [101]-[103], however current TFET designs suffer from a low ON-current with a higher threshold voltage mainly because of the large BTBT barrier, especially for large band gap semiconductors including silicon, the material of choice for mainstream semiconductor technology. To overcome this shortcoming and further improve the subthreshold characteristics and the ON-current, many efforts [7], [8], [104] have been focused on proposing new structure/materials for TFETs, among which several [105]-[106] exhibit near perfect switching characteristics, i.e. an ultra-small subthreshold swing. In addition, a vertical n-type TFET has been proposed in [89] to improve I_{ON} and S, and an n-type double-gate TFET using high-*k* material is proposed in [81] to improve performance. However, the ON-currents reported in these works are well below that of CMOS, or they exhibit threshold voltages higher than 0.4 V. However, the underlying physics and the design rules leading to such ideal subthreshold characteristics are still not apparent. As a result, a certain degree of ambiguity prevails over the choice of structures and materials for achieving a small subthreshold swing in these TFETs.

For the last two decades researchers have been exploring graphene based nanotechnology to replace silicon technology for innovative designs and new technologies at the architecture, circuit and device levels. However, there have been several roadblocks in materializing graphene nanotechnology on an IC platform. Recently, researchers started thinking about other 2D material like molybdenum disulfide (MoS_2) for beyond-graphene technology that can push the scaling and performance limits beyond the capabilities of

MOSFET and silicon technologies. Therefore, at the device level, we need to look the 2D emerging material like molybdenum disulfide (MoS_2) to replace silicon even graphene technologies.

CHAPTER 5

STUDY OF MOLYBDENUM DISULFIDE FOR FET APPLICATIONS

Why 2-D Material MoS_2

Molybdenum disulfide (MoS_2) is one of the transition-metal dichalcogenides (TMDs) material in which d-electrons interactions can give rise to new physical phenomena. It shows very promising properties for not only future nanoscale device applications, but numerous photonic applications such as light emitters [107], photodetectors [108]-[109], and solar cells [110]. It is also considered the new super material that replaces conventional silicon, semiconductor III-V material and even graphene in the next generation nanoelectronic devices due to its unique set of material, electrical and optical properties [111]. Excellent mechanical flexibility of MoS_2 also makes a new open door for flexible electronics in front of MoS_2 research community [112]-[113]. The two dimensional crystal of TMD i.e. MoS_2 is an inorganic analogue of graphene and represent the fundamental building blocks for other low-dimensional nanostructure such as inorganic nanotubes and fullerene [114]. In addition, MoS_2 is a solid state lubricant and catalyst for hydrodesulfurization and hydrogen evolution. Remarkable electrical properties of *mono*-layer and *multi*-layer MoS_2 is increasingly revealed in its field effect transistor characteristics such as large ON/OFF ratio ranging from 10^8 [115] to 10^{12} [116]-[117], steep subthreshold swing ranging from 9 mV/dec [118] to 70 mV/dec [119], large current carrying capacity ranging from 120 µA/µm [116]-[117] to 150µA/µm [120] with reported electron mobility ranging from $1cm^2V^{-1}s^{-1}$ (in air/MoS_2/SiO_2 structure)

to 480$cm^2V^{-1}s^{-1}$ (in $HfO_2/MoS_2/SiO_2$) [121]-[125] depending on the device structures, dielectric environment and processing [126]-[128]. Some of the distinct characteristics of MoS_2 2D crystal highlights high electronic quality of the material coupled with thickness dependent optical properties, mechanical flexibility and access valley degree of freedom.

As a result, there has been an extensive investigation on the 2D materials for TFET applications due to the tight gate control over the channel that results in high electric fields at the tunnel junction. Since the BTBT transmission probability depends on the bandgap and electric field exponentially, high ON-currents are expected in 2D nanomaterial based Tunnel FETs. Since tight gate control is not the only one parameter in determining the high ON-currents, other critical factors (such as effective mass (m^*) and doping concentration etc.) are also significantly contributed on tunneling current. Therefore, there has been a surge of interest to introduce and replace silicon by molybdenum disulfide (MoS_2) that shows promising properties for future nanoscale FETs due its non-zero tunable band gap (1.12 eV~1.8 eV), atomic scale thickness, pristine interfaces, excellent electrostatic integrity and mechanical flexibility [129]-[132]. The atomically-thin single or multilayer MoS_2 allows excellent gate electrostatics to suppress short channel effects (SCE), which is one of the major issues in scaled MOSFETs [129], [133]. The bulk MoS_2 crystal, which is composed of stacked layers have indirect bandgap (~1.12eV) and single layer MoS_2 crystal form direct band gap (~1.8 eV) at the first Brillouin zone [131]-[139]. Indirect bandgap of multilayer MoS_2 implies that phonons need to be involved in the BTBT process. However, degenerately doped source and drain region, which is basically shifts the Fermi level down below what was originally the top of the valence band, and indirect thin bandgap allow tunneling from valence band to the conduction

band at the source and channel junction due to the wave nature of electrons. Also due to higher effective mass, the density of states (i. e. no. of states per unit volume and per unit energy) of multilayer MoS_2 is three times that of a single layer MoS_2. This will leads to considerable high drive currents in the ballistic limits [140]. As a result, it is preferable to use the multilayer MoS_2 and explore other factors, such as, effective mass (m^*) and doping profile simultaneously in order to improve the tunneling current.

Atomic Structure of MoS_2

The atomic structure of 2D molybdenum disulfide is shown in Figure 18(a), where three layers are shown. In each layer the atoms of molybdenum and sulfur are attached to each other through strong covalent bond that gives it very high tensile strength (30 times more than steel of identical structure), thermal stability up to 1090 °C in inert environment [141], and a surface free of dangling bonds. The thickness of each layer is about 0.65nm. The 2D and flat nature of MoS_2 layer leads to intrinsically low surface scattering and dimension scaling possibilities in term of electronic devices. The force between adjacent layers is a very weak van der Waal force. Therefore, this weak inter-layer van der Waal's force allows *mono*- or few layers MoS_2 thin films to be created through micro-mechanical cleavage technique [142] and through anisotropic 2D growth by chemical vapor deposition [143]-[144]. The thickness dependent tunable bandgap (0.9 eV ~1.8 eV) that is shown in Figure 18(b) from bulk MoS_2 to *mono*-layer MoS_2 overcome the limitation of zero bandgap Graphene and insulating hexagonal boron nitride (h-BN) [145]. Bulk MoS_2 is an indirect gap semiconductor with the bandgap in the near-infrared frequency range [146] and *mono*-layer MoS_2 is a direct gap semiconductor with bandgap in the visible frequency range[147]-[148]. In general, this unique property of

MoS_2, and 2D materials enables the creation of atomically smooth material sheets and the precise control on its number of molecular layers. The indirect to direct crossover occurs at the *mono*-layer limit, resulting in strong contrast in photoluminescence efficiency between *mono*- and *multi*-layer sheets [147]-[148].

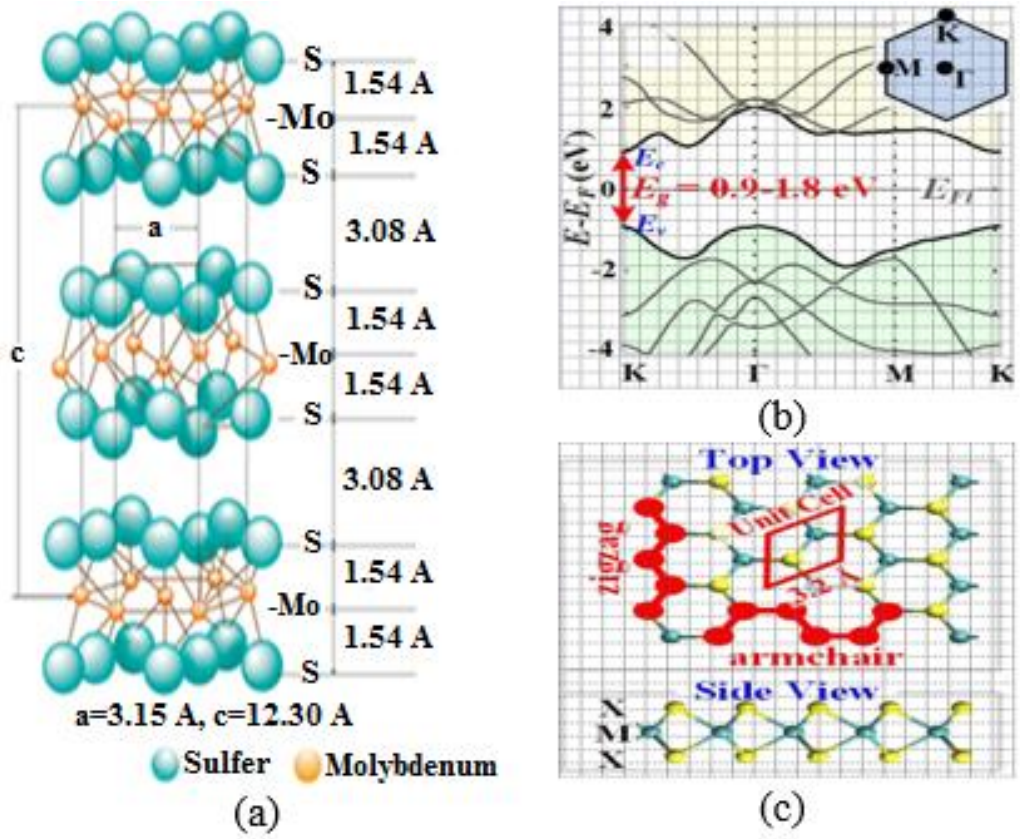


Figure 18 (a) Atomic view of the layer structure of 2D-hexagonal MoS_2 crystals. *Mono*-layer consists of a sandwich of three hexagonally packed atomic layers, S-Mo-S, where within two S layers, the Mo atoms in the intermediate layer are bonded with the S atoms through ionic-covalent interactions in a trigonal prismatic arrangement [157], (b) band diagram of multilayer MoS_2 crystal, and (c) top and side view of MoS_2 crystal at zigzag pattern

Analysis of Optical and Electronic Properties of MoS_2

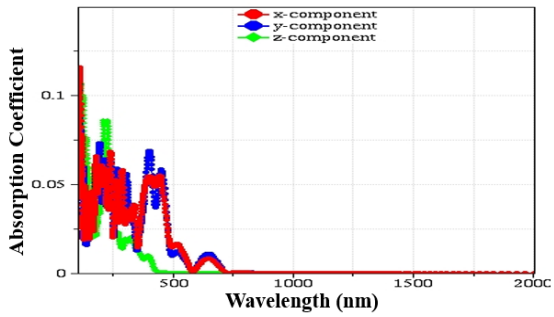
The electrical, material and optical properties of geometrically optimized MoS_2 have been evaluated by using the density function theory (DFT)-based material properties simulator from nanoHUB of Purdue University [149]. Computation the properties of MoS_2 are based on the self-consistent density functional theory. Material modeling provides a cost and time efficient method for studying their properties, especially in nanotechnology where length and times scales are not accessible experimentally. Therefore, to investigate the optical and electronics properties of semiconducting *mono*- and *multi*- layers MoS_2 was considered theoretically using DFT method dependent on the amount and distribution of atoms of dopant. Since we are particularly interested in MoS_2 –based LASER and FET applications, this section discusses optical properties in terms of absorption coefficient, extinction coefficient and reflective index, and electronic properties in terms of DOS profile and bandgap properties.

Optical Properties of MoS_2

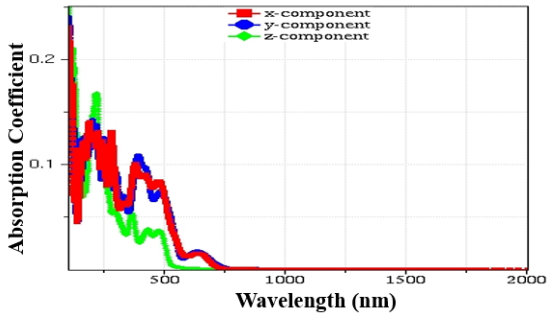
The absorption coefficient of *mono*- and *multi*-layer MoS_2 is shown in Figure 19(a) and Figure 19(d), respectively. As the wavelength is inversely proportional to bandgap energy, photons with smaller energy or longer wavelength compared to bandgap energy is not absorbed. When photon energy of an incident light is smaller than the bandgap energy of a material, the material appears to be transparent for that light. The absorption coefficient defines the penetration depth of light of a certain wavelength into a material before the light is absorbed by the material completely. Because of the phenomena called fundamental absorption, the absorption coefficient increases rapidly for light with wavelength shorter than the bandgap [150]. From Figure 19 (a) and Figure 19 (d), it is observed that the absorption coefficient of

both *mono* and *multi*-layer MoS_2 is relatively high near the visible spectrum (400-500nm) but they doesn't cover the whole visible spectrum (~400-700nm). These Figures show a sharp decay of absorption coefficient after 500nm, which indicates a photodetector made of MoS_2 is only useful in detecting light below 500nm. The fluctuation in the curve is because of the absorption coefficient is measured in scale of nm^{-1}. The extinction coefficient determines how easily light of a particular wavelength can penetrate a material. The extinction coefficient (k) is related to absorption coefficient (α) by $k = \frac{\alpha\lambda}{4\pi}$, where λ is the wavelength. Figure 19 (b) and Figure 19 (e) show the extinction coefficient of *mono*- and *multi*-layer MoS_2. For *mono*-layer MoS_2 it is observed that the extinction coefficient reaches its peak at ~450nm. That indicates that at this particular wavelength the light absorbed most by *mono*-layer MoS_2. After 500nm the extinction coefficient is very low which means that *mono*-layer MoS_2 is transparent for the wavelength above 500nm. The same conclusion we can draw from the absorption coefficient curve as well. For *multi*-layer MoS_2 the peak also occurs at nearly ~400nm. But the magnitude of the peak is higher than *mono*-layer MoS_2, which means *multi*-layer MoS_2 absorb light better than *mono*-layer MoS_2 at that wavelength.

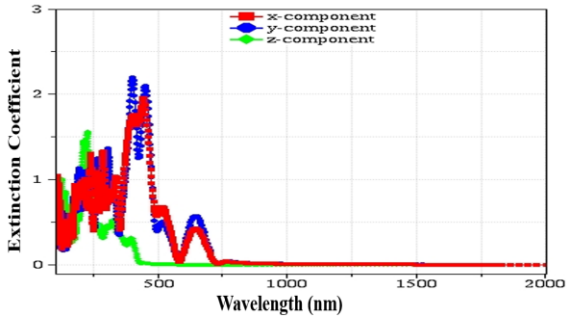
The refractive index of a material is the ratio between the speed of light in free space and speed of light in that material. Figure 19 (c) and Figure 19 (f) show the refractive index variation of *mono*-layer and *multi*-layer MoS_2 with respect to wavelength. For *mono*-layer MoS_2 it is observed that below 250nm the refractive index lies between 1 and 2, indicates it is transparent to visible light. On the other hand for *multi*-layer MoS_2 the refractive index is always above 2 (with some exception at around 100nm). The maximum refractive index is found at around 500nm for both *mono*- and *multi*-layer MoS_2.



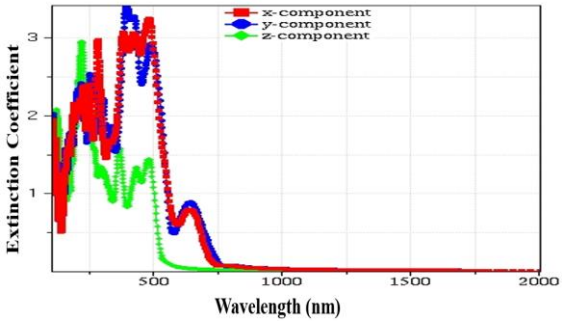
(a) Absorption coefficient of *mono*-MoS_2



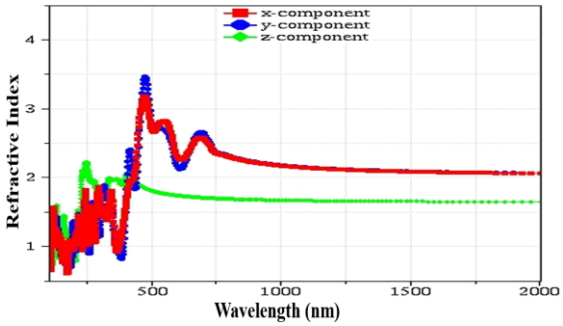
(d) Absorption coefficient of bulk-MoS_2



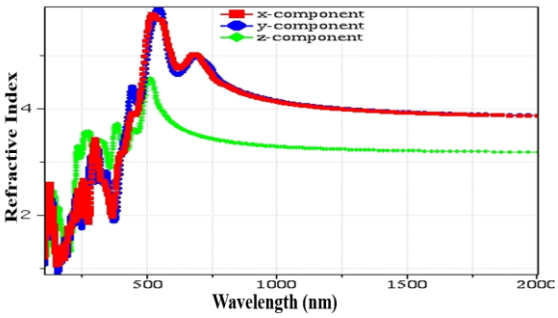
(b) Extinction coefficient of *mono* -MoS_2



(e) Extinction coefficient of bulk-MoS_2



(c) Refractive index of *mono*-layer MoS_2

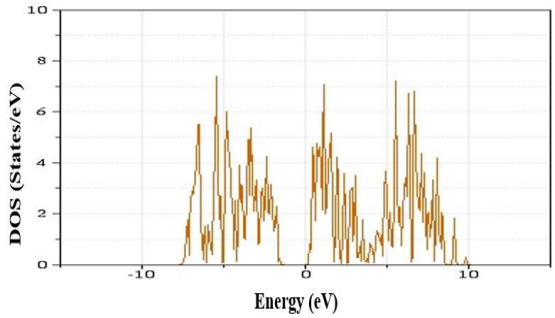


(f) Refractive index of bulk-MoS_2

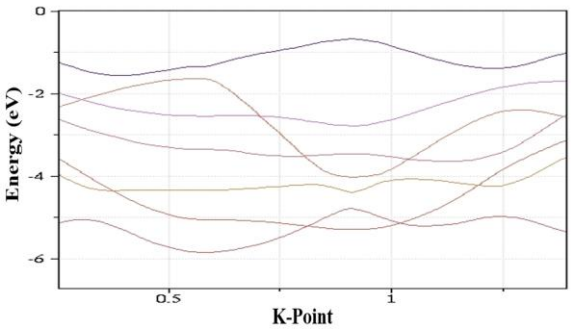
Figure 19 Optoelectronics properties of SL-MoS_2 and bulk-MoS_2: simulation consider GGA as exchange and correlation function, wave function kinetic energy cutoff (Ry): 40, charge density kinetic energy cutoff (Ry): 160, SCF convergence criterion (Ry): 1E-6, Occupation: smearing, Smearing: Gaussian, Gaussian spreading : 0.0038, Density of states: Minimum energy: -10, Maximum energy: 20, Dielectric option: Smearing: 0.1, Min E: 0.62, Max E=12.

Electronics Properties of MoS_2

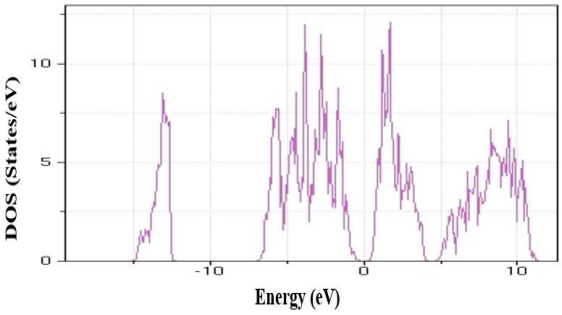
The DOS profile and bandgap for *mono*-layer and *multi*-layers MoS_2 are shown in Figure 20 (a) and Figure 20 (b), respectively. Figure 20 (a) and Figure 20 (b) shows the clear distinction of DOS profile between *n-type mono*-layer and *multi*-layers MoS_2 with energy. The single rhenium (Re) atoms in low absorption at molybdenum (Mo) sites only marginally altered the DOS profile. This alteration demonstrated itself through the existence of an impurity level at ~0.25 eV underneath the conduction band of MoS_2. A doping of *mono*-layer MoS_2 does not change cardinally the DOS profile roughly up to 1.6% Re with random distribution where DOS profile significantly change for the case of *multi*-layer MoS_2. It also leads to the increased intensity and the position of the band of the donor level compare to *multi*-layer MoS_2. However, the average number of states per eV is almost double in *multi*-layer MoS_2 compare to *mono*-layer MoS_2. Figure 20 (c) and Figure 20 (d) demonstrates the bandgap simulation for *mono*- and *multi*-layer MoS_2. It is observed that MoS_2 has a very unique property which is called 'tunable bandgap'. This tunable bandgap is varied with the number of layers. When the number of layers has changed from *mono*-layer to *multi*-layer, the bandgap is also changed from direct (~1.8 eV) from indirect (~0.9 eV). This direct bandgap semiconductor (*mono*-layer MoS_2) is suitable for field effect transistor (FET) applications as phonon does not need to be involved at carrier charge mechanism. On the other hand *multi*-layer MoS_2 indirect tunable low bandgap characteristics that makes attractive for band-to-band-tunneling (BTBT) devices. Together with effective mass, this tunable low bandgap semiconductor (*multi*-layer MoS_2) has significant impact on tunneling probability that directly increase the tunneling current.



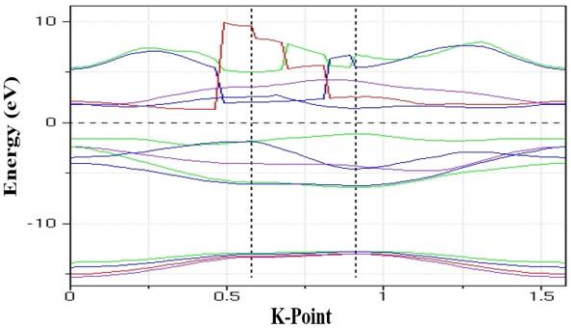
(a) DOS profile of *mono*-layer MoS_2



(c) E-K diagram of *mono*-layer MoS_2



(b) DOS profile of bulk-MoS_2



(d) E-K diagram of bulk-MoS_2

Figure 20 Electronics properties of *mono*-layer and multi-layer MoS_2. (a and b)represent the DOS profile as function of states/eV based on plan waves and *ab* initio code, (c and d) represent the band structures in the first region of Brillouin Zone. Simulation consider GGA as exchange and correlation function, wave function kinetic energy cutoff (Ry): 40, charge density kinetic energy cutoff (Ry): 160, SCF convergence criterion (Ry): 1E-6, Occupation: smearing, Smearing: Gaussian, Gaussian spreading: 0.0038, Density of states: Minimum energy: -10, Maximum energy: 20, Dielectric option: Smearing: 0.1, Min E: 0.62, Max E=12.

CHAPTER 6

PROPOSED MOLYBDENUM DISULFIDE BASED TUNNEL TRANSISTOR

Proposed TFET Device Structure and Its Operating Principle

The structure of the proposed multilayer MoS_2 TFET is shown in Figure 21. In the design, we propose to use silicon dioxide (SiO_2) and Hafnium oxide (HfO_2) as the insulators. HfO_2 has been widely investigated as gate insulator in recent time in various device designs as it is the most stable compounds of hafnium. HfO_2 has a high dielectric constant of ~25, bandgap of 5.7 eV [81], [115]. These advantages allow a lower leakage (gate tunneling) and better gate control at lower thickness of HfO_2 as well as mobility enhancement in the channel. Besides, the growth of SiO_2 is much easier on silicon substrate, which prevents leakage. That is why we used SiO_2 to separate the active area of the transistor and the silicon substrate.

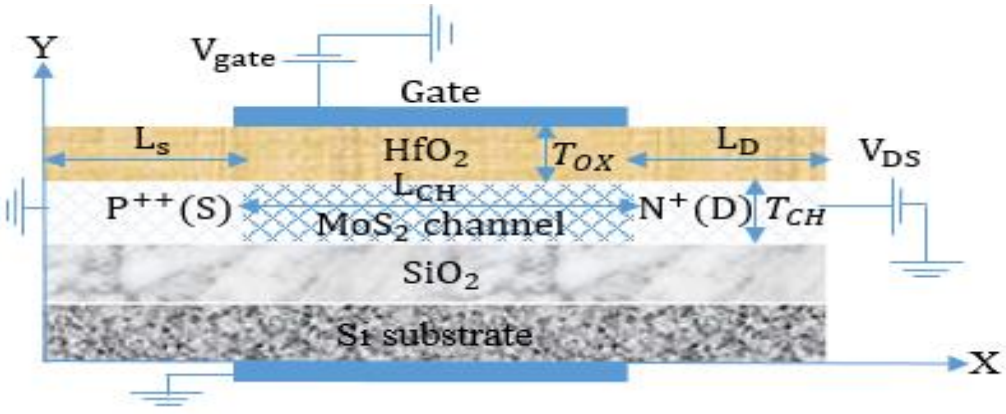


Figure 21 Device architecture of multilayer MoS2 based TFET with channel (n-) and source (p++)/drain (n+) lengths of 50 and 10 nm, respectively. Source and drain regions have a doping level of 1e19 cm-3 and oxide thickness is 2 nm.

As shown in Figure 22, the p-i-n diode structure of N-type TFET is always reverse biased to ensure ultra-low leakage current. For NTFET, the substrate is lightly n or p doped. In the OFF-state ($V_{gs} = 0V, V_{ds} = 1V$), the transmission probability is low due to the wider barrier (low electric field) at the source-to-channel tunnel junction resulting in very low OFF-currents. In the ON-state ($V_{gs} = 1V, V_{ds} = 1V$), the increasing gate voltage results in an accumulated or inverted n-channel. The surface tunnel junction is at the cross-point of gate oxide/channel/p++ doped region, where the tunnel barrier shrinks. As a result, electrons tunnel from the valence band (p++ doped region) to the conduction band (channel region) and flow to the n+ doped region. The operation of TFET is based on this gate controlled band-to-band-tunneling. The NTFET is switched ON when $V_{gs} > V_{th}$.

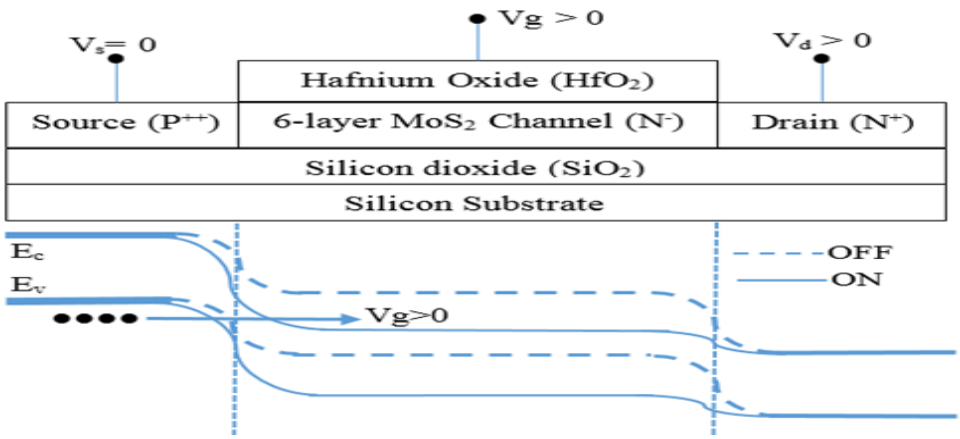


Figure 22 Schematic and energy band diagram p^{++}-n^{-}-n^{+} TFET having a multilayer MoS_2 as channel material in OFF-state and ON-state respectively.

Analytical Model of Tunneling Current

In this section, the performance of NTFET with multilayer MoS_2 channel is investigated as a function of the thickness of the channel (t_{MoS_2}) and the thickness of the gate oxide (t_{HfO2}). In

order to reveal the wave nature of electron for this proposed device, we solved the time independent modified Schrodinger's equation as in (6.1),

$$\frac{d^2\Psi}{dx^2} = \frac{2m^*(V(x)-E)}{\hbar^2}\Psi \tag{6.1}$$

where x is the direction along the channel, E is built-in potential energy respectively, $\hbar$ is the reduced Planck's constant, m^* is the effective mass, and Ψ is the wave function. The applied voltage (V) is a function of the position (x) and can be given by $V(x) = V_g\left(1-\frac{x}{L}\right)$ in terms of gate potential $\left(V_g\right)$, and channel length (L) along the x-direction (see Appendix B). Assuming that $qV(x) - E$ is independent of position (x) in a section between x and $x + dx$. Applying the following boundary conditions: (i) zero electric field at $x = \pm\infty$, (ii) continuous electric field and potential at the source-channel and drain-channel junction, and (iii) channel length $(L) \gg$ tunneling screening length (λ). Equation (6.1) can be solved analytically, leading to a solution in the form of $\Psi(x + dx) = \Psi(x)exp(-kdx)$ with $k = \frac{\sqrt{2m^*(V(x)-E)}}{\hbar}$. The minus sign is chosen because we assume that the particle moves from source to drain. For a slowly varying potential, the amplitude of wave function at $x = X_0$ can be related to the wave function at $x = 0$. Therefore, we can represent the wave nature of electron within the tunneling screening length in MoS_2 channel area in terms of (6.2).

$$\Psi(x) = \Psi(0)exp\left(-\int_0^{X_0}\frac{\sqrt{2m^*(V(x)-E)}}{\hbar}dx\right) \tag{6.2}$$

According to Max Born's postulate [10], the probability density of complex wave function can be written as $|\Psi(x)|^2 = \Psi(x)\Psi^*(x)$, where $\Psi^*(x)$ is the complex conjugate

wave function. Using the modification of Wentzel-Kramers-Brillouin (WKB) approximation [151]-[153] for tunneling screening length, the tunneling probability for the BTBT process can

$$T_{BTBT} = \frac{\Psi(x)}{\Psi(0)} \times \frac{\Psi^*(x)}{\Psi^*(0)} = exp\left(-2 \int_0^{x_0} \frac{\sqrt{2m^*(V(x)-E)}}{\hbar} dx \right) \tag{6.3}$$

$$= exp\left(-\frac{4L\sqrt{2m^*}}{3\hbar q V_g} E_g^{3/2} \right) = exp\left(-\frac{4\sqrt{2m^*}}{3\hbar q \xi} E_g^{3/2} \right)$$

be approximated as(6.3), where m^* is the effective mass $\left(\frac{1}{m^*} = \frac{1}{m_e^*} + \frac{1}{m_h^*}\right)$, q is the electronic charge, ξ is the resultant electric field $\left(\xi = \sqrt{\xi_x^2 + \xi_y^2}\right)$ due to the effect of channel length and MoS_2 body thickness along the directions of $x-$ and $y-$ axis respectively.

In [129], it is shown that the absence of short channel effect for 50 nm channel length and the characteristic tunneling screening length (λ) can be assumed to be one third of the channel length. In literature, the tunneling screening length can be defined as (6.4), where

$$\lambda = \sqrt{\frac{\varepsilon_{MoS_2}}{\varepsilon_{ox}} t_{ox} t_{MoS_2}} \tag{6.4}$$

ε_{MoS_2} is the in-plane dielectric constant of MoS_2 and t_{MoS_2} is MoS_2 channel thickness. The experimental result [129] as well as theoretical results [131] reveal that 6-layer MoS_2 flakes have in-plane dielectric constant of 6.4~6.5, which is a critical parameter in determining the scalability of any channel material. If we compute the λ for few layers of MoS_2 (~ 4nm thick) by considering 2 nm thick HfO_2 (ε_{ox}~$25\varepsilon_0$) as a gate dielectric, it gives only 1.41nm whereas 5nm thick ultrathin-body Si or InAs provides a λ of 2.35 or 2.48nm. Thus, multilayer MoS_2 provides two times smaller value of λ than the conventional ultrathin materials. From (6.3), it

is also noticed that tunneling probability depends exponentially on the barrier height to the power of $^{3}/_{2}$. In case of tunable bandgap material (e.g. multilayer MoS_2), the bandgap is significantly low. Therefore, the product of $\lambda \times E_g^{3/2}$is significantly improved the tunneling probability. In this way, the use of high-k oxide and few-layers MoS_2 channel material is helped to improve the device performance significantly.

Now, applying the electric field that controlled by a third terminal (gate) in TFET, T_{BTBT} can be calculated instantly when other parameters of the material are enumerated. To understand the origin of ON-current of this proposed device, one needs to consider the following factors: i) tunneling screening length; ii) electron and hole effective masses; iii) bandgap; iv) MoS_2 body thickness; v) oxide thickness; vi) source-to-channel potential difference; and vii) source and drain doping level. This factors are needed to consider in the analytic equation in order to improve the high ON-current of a TFET [154]. Therefore, under these circumstances, the BTBT tunneling current [155] can be written in the form of (6.5),

$$I_{Tunneling} = A_{area} q V_R N_c T_{BTBT} = A_{area} q V_R N_c exp\left(-\frac{4\sqrt{2m^*}}{3\hbar q\sqrt{\xi_x^2+\xi_y^2}} E_g^{3/2}\right) \quad (6.5)$$

where A_{area} is the area of p^{++}-i^{-}-n^{+} TFET region, V_R is the Richardson's velocity $\left(\sqrt{\frac{kT}{2\pi m^*}}\right)$, N_c is the source-drain doping concentration, ξ_x and ξ_y are the electric field along the x- and y-direction which can be defined as V_g/L and V_g/t_{MoS_2}, respectively.

Analytical Model of Subthreshold Swing

According to the definition, subthreshold swing equals the gate voltage swing needed to change the drain current by one decade [104]. For the MoS2 Tunnel FET, the tunneling current that is calculated from (6.5) can be represented as the simplified form of (6.6). Here, the coefficients of A and B are determined by the materials properties of the junction and the cross-sectional area of the device. More specifically, the coefficients of A and B are equal to $A_{area}qV_RN_c$ and $\frac{4\sqrt{2m^*}}{3\hbar q}E_g^{3/2}$, respectively. The derivative of the logarithmic tunneling

$$I_{Tunneling} = Aexp\left(-\frac{B}{\xi}\right) \tag{6.6}$$

current of (6.6) with respect to the gate-to-source voltage can be used to determine the subthreshold swing of tunnel FET. The definition of subthreshold swing is modified from (6.7) a logarithmic scale to a natural log scale by the factor of *ln* 10. After solving (6.7), the model of subthreshold swing can be achieved as (6.8). The details of subthreshold swing model is given in Appendix C.

$$S = \left[\frac{dlog_{10}I_{Tunneling}}{dV_{GS}}\right]^{-1} = ln10\left[\frac{d\left(lnI_{Tunneling}\right)}{dV_{GS}}\right]^{-1} \tag{6.7}$$

$$S = \begin{cases} ln10\left[\frac{B}{\xi^2}\frac{d\xi}{dV_{GS}}\right]^{-1} \\ ln10\left[\frac{BL}{V_{GS}^2}\right]^{-1} \\ ln10\left[\frac{3B}{V_{GS}^2}\sqrt{\frac{\varepsilon_{MoS_2}}{\varepsilon_{ox}}t_{ox}t_{MoS_2}}\right]^{-1} \end{cases} \tag{6.8}$$

Characteristics of Proposed Tunnel Transistor

All the results that shown in this section is based on the analytical model of tunneling current and subthreshold swing of the proposed device that is shown in Figure *21*. The channel length is considered 50 nm. A doping level of 1e19 cm^{-3} is assumed in the source and drain region, which seems feasible by molecular doping of the source and drain contact regions [156].

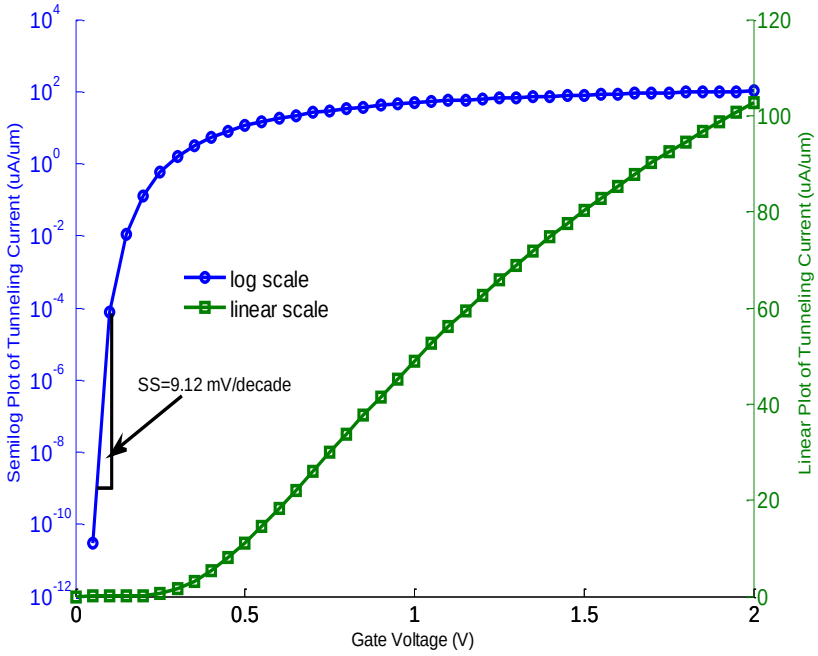


Figure 23 Transfer characteristics (logarithmic scale at the left, linear scale at the right) of proposed multilayer MoS_2 Tunnel FET

I-V Characteristics of Proposed TFET Device

By using the equation (6.5), and taking the resultant electric field (ξ), the tunneling current ($I_{Tunneling}$) at room temperature can be calculated as a function of gate voltage (V_g). Figure 23 shows the transfer characteristics of multilayer MoS_2 channel based n-type tunnel

FET. It is meaningful to notice that a lower OFF-current is achieved without losing too much ON-current in multilayer MoS_2 TFET. This is because the slope of the I_d vs V_g curve is very steep below the subthreshold region. As a result, a much lower OFF-current can be obtained with a very small reduction of gate voltage (V_g). In particular, an OFF-current of $0.5 \times 10^{-11}\ \mu A/\mu m$ can be obtained with OFF-current of $80\ \mu A/\mu m$ at gate voltage of 1.5V. Since multilayer MoS_2 (6 layers) has smaller band gap and high effective mass compare to silicon or semiconductor III-IV materials, its ON-current is significantly higher. An average subthreshold swing is less than 10 mV/dec (extracted from transfer characteristics curve in Figure 23 using the same method as in [104]), OFF-current is very low in the order of $0.5 \times 10^{-11}\ \mu A/\mu m$, and ON-current is very high that shows the enormous potential of multilayer MoS_2 channel based TFET. Therefore, it can be said that multilayer MoS_2 based TFET is suitable candidate for high performance and ultra-low-power logic devices applications.

Process and Parameter Variation on Proposed TFET Device

Process and parameter variation significantly impacts on performance in nanoscale integrated circuit. Since process induced variations in device dimension, oxide thickness, doping profiles, and threshold voltages lead to variations in leakage levels, it will be very hard to control process and parametric variations, which are present within die as well as die-to-die at nanoscale range. Variable device parameters – mainly the drive current and subthreshold leakage currents – are the major outcomes of random and systemic process variations. Therefore, in this subsection, we will discuss the variations of oxide thickness, gate voltage, doping profile to meet the transistor performance goal.

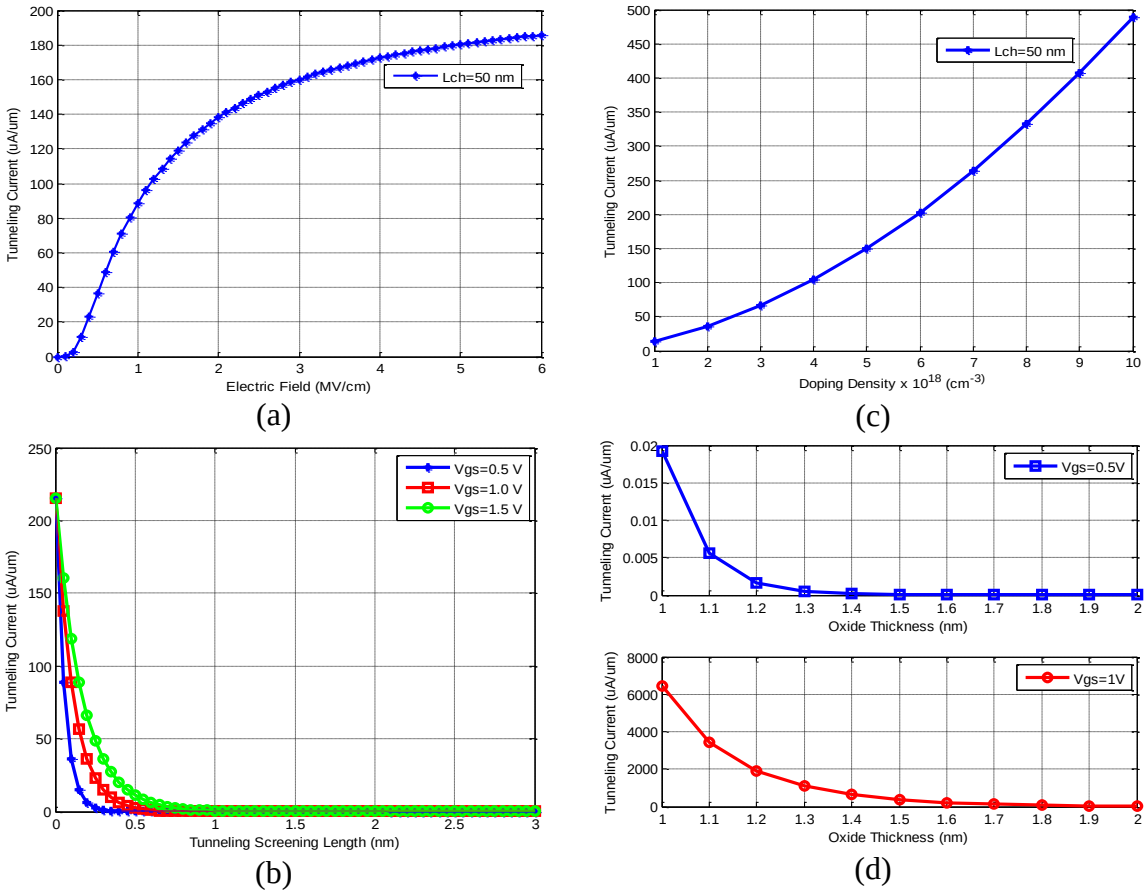


Figure 24. Characteristics of tunneling ON-current in terms of (a) resultant electric field; (b) tunneling screening length; (c) doping density and (d) high-k oxide thickness

Effect on tunneling ON-current. The characteristic of direct BTBT current per micron width as a function of $\sqrt{\xi_x^2 + \xi_y^2}$ for 6-layer MoS_2 sheet is shown in Figure 24 (a). From Figure 24 (a), it is seen that the output characteristics of this tunnel FET is very similar to the output characteristics of the MOSFET and the linear and saturation regions are evident. At relatively higher electric field, a comparatively lower ε_{MoS_2} and t_{MoS_2} provides much lower tunneling screening length and consequently it delivers a better ON-current. The tunneling current characteristics in terms of tunneling screening length for different gate voltage is shown

in Figure 24 (b). It is seen that tunneling ON-current is significantly improve at lower screening length, which is consistent with the result of [157]. Similarly, it is also seen from Figure 24 (c) that the tunneling ON-current significantly increases with increasing the doping density for specific gate voltage. On the other hand, the variation of tunneling current in terms of oxide thickness is shown in Figure 24 (d) for gate voltage of 0.5 V (top) and 1.0 V (bottom). It is noticed that tunneling current is inversely related with oxide thickness. Reducing the oxide thickness leads to increase the tunneling ON-current. Notice that despite the fact that a much tunneling ON-current is achieved when applying the higher gate voltage with same oxide thickness, which is also consistent with the result of [104] and [157].

Effect on subthreshold swing. Figure 25 shows the subthreshold swing characteristics in terms of different parameter variations. From Figure 25 (a), it is seen that the subthreshold swing is very close to 5.2 mV/decade at gate voltage of 0.5V when the channel length is 25 nm. Figure 25 (b) shows how the tunneling screening length significantly impacts the subthreshold swing. It is depicted that the value of the subthreshold swing can be achieved approximately 4.9 mV/decade at gate voltage of 0.5V for 2 nm screening length. The characteristics of the subthreshold swing are also observed in terms of oxide thickness and MoS_2 body thickness from Figure 25 (c) and Figure 25 (d) respectively. By applying gate voltage of 0.5V, we attain the value of a subthreshold swing of 5.1mV/decade for 2nm oxide thickness and 8nm MoS_2 body thickness.

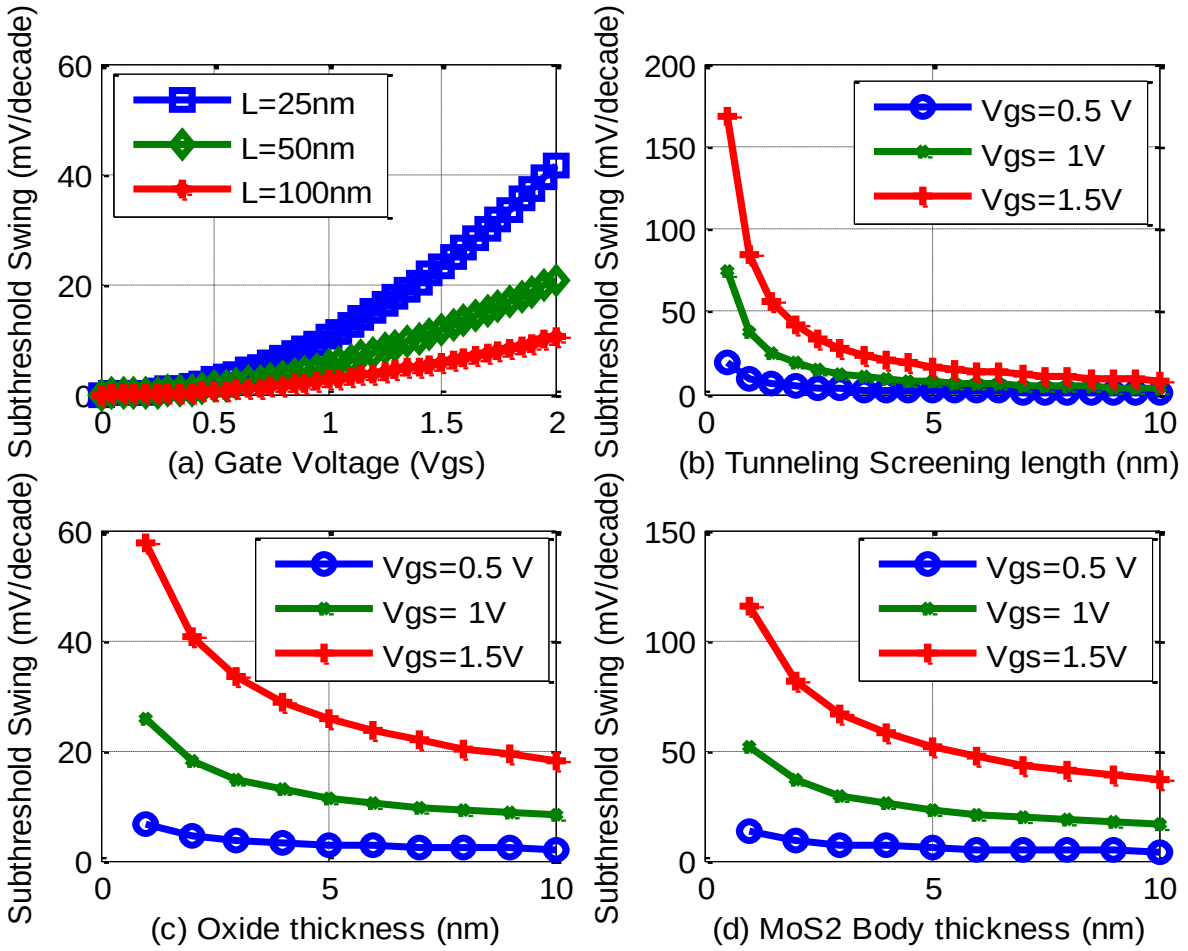


Figure 25. Impact of process and parametric variations on subthreshold swing of multilayer MoS_2 tunnel transistor. Characteristics of subthreshold swing in terms of (a) gate voltage for various channel length (V), (b) tunneling screening length (nm), (c) Oxide thickness (nm), and (d) MoS_2 body thickness (nm) for different gate voltage (V) scaling

Optimization of Proposed TFET Device

In this particular subsection, we have analyzed the impact of the doping density, gate voltage, oxide thickness, dielectric constant, and the length of the channel material to optimize the tunneling current in the ON state.

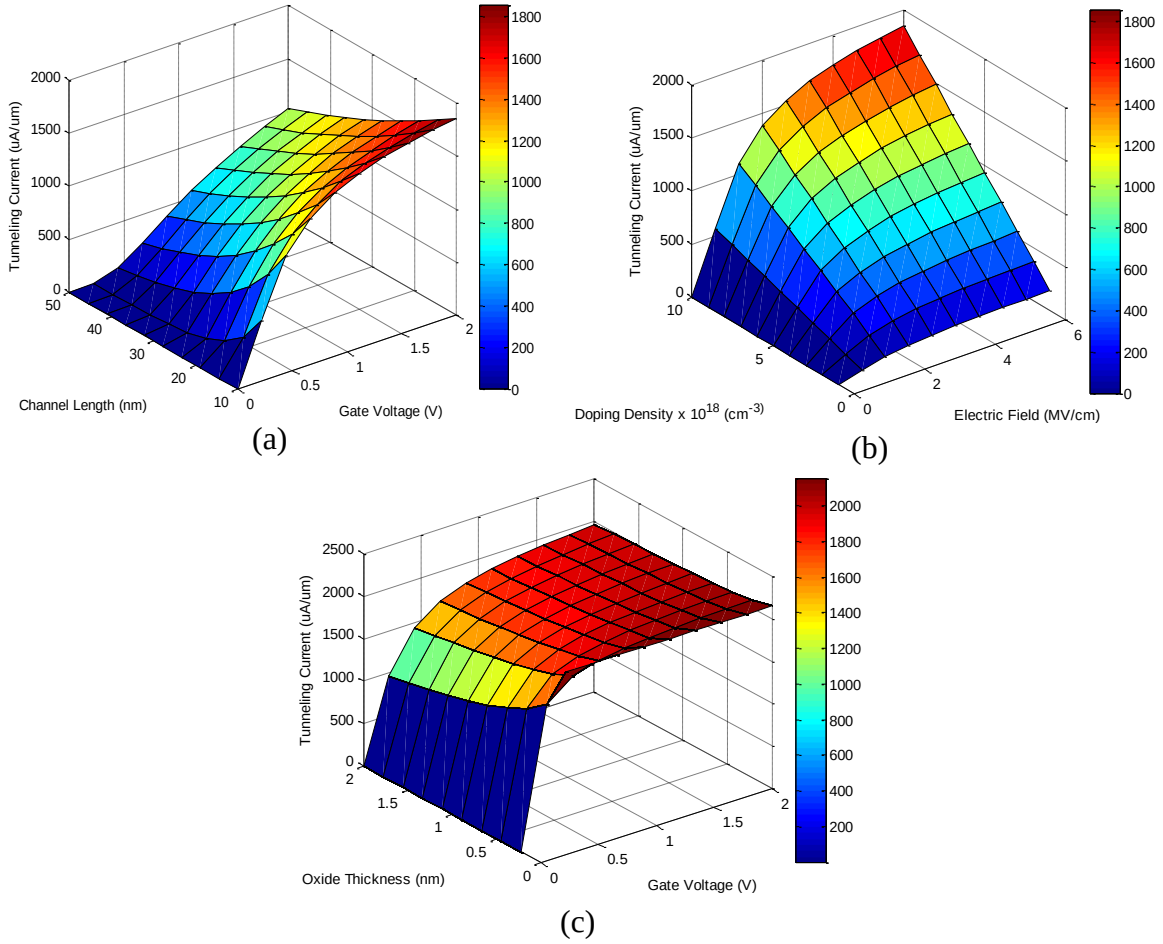


Figure 26. Optimize the tunneling ON-current in terms of (a) gate voltage and channel length, (b) doping density and resultant electric field, and (c) high-*k* oxide thickness and gate voltage.

Tunneling ON-current maximization. The tunneling current density as a function of channel length and gate voltage is revealed by Figure 26 (a). Analytical result shows that 50 nm channel length with a gate voltage of 2V gives the maximum tunneling ON-current very close to 1100 μA/μm. Figure 26 (b) depicts the tunneling ON-current as a function of doping density and resultant electric field. It is seen that higher doping leads to improve the ON-

current. As higher doping is required in source and drain region for tunneling, we have to keep the doping density as high as possible to spinning the Fermi level. Therefore, we can achieve the maximum ON-current of 1750 μA/μm with increasing resultant electric field of 6 MV/cm. In addition, we have shown the ON-current performance in Figure 26 (c) by considering the high-*k* oxide thickness and gate voltage. It appears that ON-current increases maximum up to 2000 μA/μm for 2nm of high-*k* oxide and 2V gate voltage.

While in comparison to the conventional Si TFET which shows only 0.4 μA/μm [8] and 0.15 μA/μm [158], multilayer MoS_2 sheets provide much higher ON-currents. In case of Graphene nanoribbon (GNR), as investigated earlier by Q. Zhang et al. [91], it can be seen that the ON-current is 800 μA/μm for 5nm wide monolayer GNR $(E_g \sim 0.25eV)$. However, owing to much higher band gap $(E_g \sim 1.12eV)$ for 6-layers, MoS2-TFET offers negligible OFF-current in comparison to Graphene.

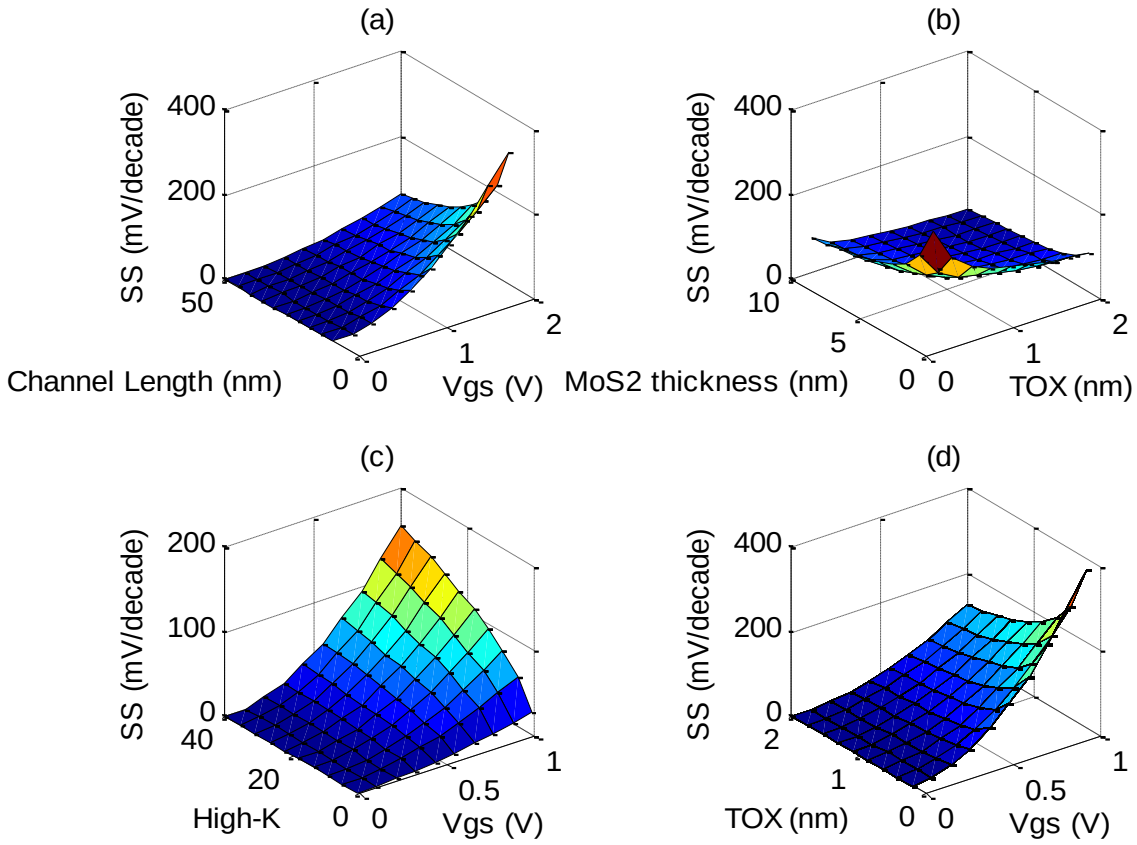


Figure 27 Optimization of subthreshold swing in terms of (a) gate voltage and channel length (b) MoS2 body thickness and oxide thickness, (c) high-k dielectric and gate voltage, and (d) Oxide thickness and gate voltage.

Subthreshold swing minimization. Figure 27 shows the way to minimize the subthreshold swing by tuning the proposed device parameters dimensions with the effect of the applied gate voltage. Figure 27 (a) shows the result of *S* in terms of gate voltage and channel length. It is observed that the subthreshold swing can be achieved 8.126 mV/decade at a gate voltage of 0.5V with 20 nm of channel length. Figure 27 (b) depicts how the MoS_2 body and

Table 3. Theoretical Demonstration of Tunnel FET based on Si, semiconductor III-V, Graphene and MoS_2 with subthreshold swing less than 60 mV/decade

Ref.	**Analytical Model**	**ON-Current ($\mu A/\mu m$)**	**OFF-Current ($\mu A/\mu m$)**	**Gain $\left(\frac{I_{ON}}{I_{OFF}}\right)$**	**S (mV/dec)**
[159]	$I \approx WLTe^{Bq\sqrt{\frac{2E_g\epsilon_s}{qN_a}}\frac{1}{\gamma}\sqrt{V_{GS}-V_{onset}}}\sqrt{V_{GS}-V_{onset}}$ $T = q\frac{A}{Bq^{3/2}}\cdot\frac{qN_a}{2\epsilon_s}\sqrt{\frac{1}{E_g\gamma}}e^{-BqE_g\sqrt{2\epsilon_s}/q^2N_a}$	10^{-1}	10^{-6}	10^{5}	~
[160]	$I_{ds} = 2BE_g^{3/2}T_{max}W_g t_{ch} f_{fermi}$ $T_{max} = AE_g^{3/2}\frac{1}{W_{min}^2}exp\left[-\frac{qW_{min}}{BE_g^{1/2}}\right]$	80	0.1	800	~
[120]	$I_{BTBT} = \frac{g_s g_v q}{h}\int_0^{\Delta\phi} T_{BTBT}\{f_i(E) - f_f(E)\}dE$ $T_{BTBT} = exp\left\{-\frac{2}{q\xi}\int_0^{E_g} k(E)dE\right\}$	150	0.5	300	4
[104]	$I_{ds} = \frac{2q}{h}T(\Delta E)kTln\left(\frac{1+exp[(E_{fs}-E_{vs}+\Delta E)/kT]}{1+exp[(E_{fs}-E_{vs})/kT]}\right)$ $T(\Delta E) \approx exp\left(-\frac{\pi\sqrt{2m_T}E_g^{3/2}}{4q\hbar\xi}\right)$ $S = \frac{2\sqrt{2}\ln(10)\hbar}{-q\pi\sqrt{m_T E_g}\frac{dW_T}{d\Delta E}}$	1000	10^{-8}	10^{11}	50
This work	$I_{Tunneling} = A_{area}q\sqrt{\frac{kT}{2\pi m^*}}N_c T_{WKB}$ $T_{WKB} = exp\left(-\frac{4\sqrt{2m^*}}{3\hbar q\sqrt{\xi_x^2+\xi_y^2}}E_g^{3/2}\right)$ $S = \begin{cases} ln10\left[\frac{B}{\xi^2}\frac{d\xi}{dV_{GS}}\right]^{-1} \\ ln10\left[\frac{BL}{V_{GS}^2}\right]^{-1} \\ ln10\left[\frac{3B}{V_{GS}^2}\sqrt{\frac{\varepsilon_{MoS_2}}{\varepsilon_{ox}}t_{ox}t_{MoS_2}}\right]^{-1} \end{cases}$	80	10^{-11}	8×10^{12}	10

oxide thickness effect the subthreshold swing. We can achieve a minimum 33.17 mV/decade for 8 nm MoS_2 body thickness and 2 nm hafnium oxide (HfO_2) thickness respectively at gate voltage of 0.5V. In addition, Figure 27 (c) shows how high-*k* material reduce the subthreshold

swing. The dielectric constant of hafnium oxide approximately 25, shows significant improvement of a subthreshold swing (23.53mV/decade) at a gate voltage of 0.5V. Similar results can also be achieved from Figure 27 (d).

Table 3 gives a few materials (Si, InAs, monolayer MoS_2, GNR) options for the tunnel FET that have exhibited reasonable ON-current, OFF-current and sub-60mV/decade with high-*k* gate stack technology and compare with our proposed work. It is seen that our model significantly improves the subthreshold swing, reasonable ON-current, extremely low OFF-current, very high transistor gain compared to previous research work.

CHAPTER 7

CONCLUSION

Summary

In this research at the interconnect level, we developed an analytical delay model for complex and real poles based on a second order approximation that considers the effect of inductance. The impact of mutual driver/source resistance and output load capacitance has been taken into account. The proposed delay model for the RLC distributed interconnect analyzed up to three-line, for example, interconnects. For a wide range of driver, load, and interconnect line constraints, we calculated the delay of the circuit model of Figure 8 and compared it with a SPICE simulation. It is seen that the error rate is within a 10%-15% range of our developed model (both real and complex pole models) with SPICE simulation. The simulation result shows that SPICE delay increases significantly with an increase in the effect of inductance. Our developed model also shows that the propagation delay increases due to an increase in the effect of inductance. In our research, we have found that the real pole based delay model is much faster in comparison to the complex pole based delay model. The driver resistance has a significant contribution in making a transition from the real pole model to the complex pole model and vice versa. It is also found that the output response of the real pole model based transfer function shows better accuracy than the complex pole model based transfer function. Although, this model is considered only two poles, it is believed that the

resulting delay is a good estimation for an early stage in modern iterative IC layout synthesis methodologies.

In the second part of this research at device level, the essential physics of a tunneling current and subthreshold swing of a multilayer MoS_2 based tunnel transistor is studied from the perspectives of device operations and tunneling probability variations. We have developed a closed form analytical model of the tunneling current and subthreshold swing of the proposed Tunnel FET. The novelty of this work can be attributed to greatly improved insights gained from the tunneling current and subthreshold swing characteristics of multilayer MoS_2 TFET. The analysis of the tunneling current and subthreshold swing of the proposed TFET reveals that by optimizing the device process and parameters (the doping level, gate voltage, oxide thickness, MoS_2 body thickness, and tunneling screening length), it is possible to obtain reasonable high ON-current and a very steep and low value of a subthreshold swing. Overall multilayer MoS_2 based TFET shows a strong potential to significantly lower the subthreshold swing leading to an ultra-low-power operation and better performance. The key technical challenges would be to develop advanced processes for nanoscale transistors using group III-V materials. Gate alignment, low-interface-trap-density gate stacks, accurate and abrupt tunnel junctions, and low resistance contacts are some critical needs for this device to become useful. Considering the intense interest in two dimensional (2D) planner materials like MoS_2 based devices for the next generation nanoelectronics, we anticipate that many of these challenges and issues of processing and fabrication will be resolved soon.

Future Research Directions

This doctoral research (Part I) is showing that real pole based delay model much faster than the complex pole model. By controlling the driver resistance and parasitics values of interconnect, we can achieve the real pole scenarios in the IC. Interconnect limits potentially threaten to decelerate or halt the historical progression of the semiconductor industry because the miniaturization of interconnects. Scaling interconnects into the nanometer regime is plagued with many challenges, such as resistivity degradation, material integration issues, high-aspect ratio via and wire coverage, planarity control, and reliability problems due to electrical, thermal, and mechanical stresses in a multilevel wire stack [69], and once these challenges are overcome, minimum interconnect scaling will still degrade interconnect delay. Radio frequency or wireless interconnect technologies have been considered as viable candidates for either on-chip or, more likely, for off-chip interconnects replacing metal/dielectric global wires. This new approach has become possible because of the confluence of wireless technologies for communications applications with high-frequency silicon technologies. RF interconnect was proposed as a high aggregate bandwidth, low latency alternative to a traditional interconnect. Its concept and benefits of enhancing it with FDMA and CDMA were also demonstrated, mainly for off-chip on-board applications. However, a wireless multiple input-multiple output (MIMO) system significantly enhances system performance compared to conventional systems like TDMA, FDMA or CDMA. Broadly speaking, all these MIMO techniques are based on proper handling of signals transmitted and received by an *array* of antennas. There is a need for thorough literature review and original

innovations in this area, which could be an exciting research topic for future RF interconnect in the VLSI field.

Besides, the second part (at device level) of this doctoral research has shown that MoS_2 based Tunnel FET could be one of the potential candidate for ultra-low-power and logic applications. However, one of the key bottlenecks is the realization of Ohmic contacts to improve FET device's on-state performance. A very good Ohmic contact with low contact resistance is essential for better device performance. However, it is difficult to find metals with desired work function for good Ohmic contact. Tunneling contacts using Schottky junctions, which is a more practical way to realize Ohmic contacts, may suffer from Fermi-level pinning due to defects and interface states, resulting in a significant tunneling barrier, hence an increased contact resistance [155]. Therefore, to achieve higher performance from MoS_2 based transistor several other issues need to be investigated: (i) the resistivity of the metal-semiconductor junction; (ii) interference between MoS_2 and the insulating materials; (iii) material doping to improve certain parameters; (iv) power management and performance at radio frequency range; (v) how to deposit a high quality dielectric on 2D crystal.

APPENDIX A

DERIVATION OF TIME DELAY MODEL

The denominator of an approximate transfer function for the two poles model that is shown in equation (3.4) can be rearranged in the form of a quadratic equation and can be shown as (A.1).

(1) *Complex Poles' Model:* The denominator of (A.1) is a quadratic part. Therefore, we get the complex roots by solving the quadratic equation from (A.2). Thus, we can write the output response in the Laplace domain as (A.3).

$$H_{Tapproximate}(s) = \frac{M}{C_2 s^2 + C_1 s + 1} \tag{A.1}$$

$$C_2 s^2 + C_1 s + 1 = 0 \tag{A.2}$$

$$or,\ s_1, s_2 = \frac{-C_1 \pm \sqrt{C_1^2 - 4C_2}}{2C_2} = -\frac{C_1}{2C_2} \pm \frac{\sqrt{C_1^2 - 4C_2}}{2C_2} = \alpha \pm j\beta$$

$$= \alpha + j\beta, \alpha - j\beta = p_1, p_2$$

$$V_{out}(s) = V_{in}(s) H_{Tapproximate}(s) = MV_{dd}\left(\frac{1}{s(s-p_1)(s-p_2)}\right) \tag{A.3}$$

$$= MV_{dd}\left(\frac{A}{s} + \frac{B}{s-p_1} + \frac{C}{s-p_2}\right)$$

Now, we solve (A.3) using the partial fraction method and equating the coefficient of s, s^2 and the constant coefficient from (A.4) and yields (A.5), (A.6) and (A.7).

$$\frac{1}{s(s-p_1)(s-p_2)} = \frac{A}{s} + \frac{B}{s-p_1} + \frac{C}{s-p_2} \tag{A.4}$$

$$or, 1 = A(s^2 - p_2 s - p_1 s + p_1 p_2) + B(s^2 - p_2 s) + C(s^2 - p_1 s)$$

$$or, 1 = (A + B + C)s^2 - (Bp_2 + Ap_2 + Ap_1 + Cp_1)s + Ap_1 p_2$$

$$Ap_1 p_2 = 1 \tag{A.5}$$

$$Bp_2 + Ap_2 + Ap_1 + Cp_1 = 0 \tag{A.6}$$

$$A + B + C = 0 \tag{A.7}$$

From (A.5), we get $A = 1/p_1p_2$ and put $A = 1/p_1p_2$ in (A.6) and (A.7), which gives (A.8) and (A.9). Firstly, multiply (A.8) by $-p_2$ and add with (A.9) to get the constant coefficient value of C. Secondly, multiply (A.8) by $-p_1$ and add with (A.9) to get the another constant coefficient value of B.

$$B + C = -\frac{1}{p_1p_2} \tag{A.8}$$

$$Bp_2 + Cp_1 = -\frac{1}{p_1} - \frac{1}{p_2} \tag{A.9}$$

After solving (A.8) and (A.9), we get the value of $B = \frac{1}{p_1(p_1-p_2)}$ and $C = \frac{1}{p_2(p_2-p_1)}$, respectively. Therefore, the output voltage response in the Laplace domain can be written from (A.3) and by taking the inverse Laplace transform from (A.10) or (A.11), which gives (A.12).

$$V_{out}(s) = MV_{dd}\left(\frac{\frac{1}{p_1p_2}}{s} - \frac{\frac{1}{p_1(p_2-p_1)}}{s-p_1} + \frac{\frac{1}{p_2(p_2-p_1)}}{s-p_2}\right) \tag{A.10}$$

$$= \frac{MV_{dd}}{p_1p_2}\left(\frac{1}{s} - \frac{p_2}{p_2-p_1}\frac{1}{s-p_1} + \frac{p_1}{p_2-p_1}\frac{1}{s-p_2}\right)$$

$$V_{out}(s) = MV_{dd}\left(\frac{\frac{1}{p_1p_2}}{s} - \frac{\frac{1}{p_1(p_2-p_1)}}{s-p_1} + \frac{\frac{1}{p_2(p_2-p_1)}}{s-p_2}\right) \tag{A.11}$$

$$= \frac{MV_{dd}}{p_1p_2}\left(\frac{1}{s} - \frac{p_2}{p_2-p_1}\frac{1}{s-p_1} + \frac{p_1}{p_2-p_1}\frac{1}{s-p_2}\right)$$

$$V_{out}(t) = \frac{MV_{dd}}{p_1p_2}\left(1 - \frac{p_2}{p_2-p_1}e^{p_1t} + \frac{p_1}{p_2-p_1}e^{p_2t}\right) \tag{A.12}$$

Since $p_1 p_2 = \alpha^2 + \beta^2$, $\frac{p_2}{p_2 - p_1} = \frac{\alpha - j\beta}{-2j\beta}$, $\frac{p_1}{p_2 - p_1} = \frac{\alpha + j\beta}{-2j\beta}$, and $V_{ratio} = \frac{V_{out}}{V_{dd}}$ therefore, we modify (A.12) and end up with (A.13).

$$\frac{\alpha^2 + \beta^2}{M} V_{ratio} = 1 + \frac{\alpha - j\beta}{2j\beta} e^{(\alpha + j\beta)t} - \frac{\alpha + j\beta}{2j\beta} e^{(\alpha - j\beta)t} \tag{A.13}$$

$$or, \frac{\alpha + j\beta}{2j\beta} e^{(\alpha - j\beta)t} - \frac{\alpha - j\beta}{2j\beta} e^{(\alpha + j\beta)t} = 1 - \frac{\alpha^2 + \beta^2}{M} V_{ratio}$$

$$or, \frac{e^{\alpha t}}{2j\beta} \left[\alpha \left(e^{-j\beta t} - e^{j\beta t} \right) + j\beta \left(e^{-j\beta t} + e^{j\beta t} \right) \right] = 1 - \frac{\alpha^2 + \beta^2}{M} V_{ratio}$$

$$or, \frac{e^{\alpha t}}{\beta} (\beta \, cos\beta t - \alpha \, sin\beta t) = 1 - \frac{\alpha^2 + \beta^2}{M} V_{ratio}$$

$$or, \frac{e^{\alpha t}}{\beta} sin(\beta t + \theta) = 1 - \frac{\alpha^2 + \beta^2}{M} V_{ratio}$$

From (A.13), we can derive the time delay model for complex poles in the distributed RLC interconnect structure that was given in section of Complex Pole Model.

(2) *Real Poles' Model*: The derivation method of the real pole model is almost the same as the complex pole model. For the case of real pole, $\mathrm{p}_1, \mathrm{p}_2 = -\frac{\mathrm{C}_1}{2\mathrm{C}_2} \pm \frac{\sqrt{\mathrm{C}_1^2 - 4\mathrm{C}_2}}{2\mathrm{C}_2}$ are real values and time domain response of output voltage is written as (A.14).

$$V_{out}(t) = \frac{M V_{dd}}{p_1 p_2} \left(1 - \frac{p_2}{p_2 - p_1} e^{p_1 t} + \frac{p_1}{p_2 - p_1} e^{p_2 t} \right) \tag{A.14}$$

Since $p_2 - p_1 = -\frac{\sqrt{C_1^2 - 4C_2}}{C_2}$ is negative for the real poles' cases, the value of $\frac{p_2}{p_2 - p_1}$ and $\frac{p_1}{p_2 - p_1}$ are positive. Subsequently, the magnitude $|p_2|$ is higher compared to $|p_1|$, the term of $\frac{p_1}{p_2 - p_1}$

reduces more quickly than the term of $\frac{p_2}{p_2-p_1}$. Therefore, the output voltage response for inferior constrained in the time domain can be approximated by (A.15).

$$V_{out}(t) \approx \frac{MV_{dd}}{p_1 p_2}\left(1 - \frac{p_2}{p_2 - p_1} e^{p_1 t}\right) \tag{A.15}$$

Now, once we rearrange (A.15), we will end up with a time delay model for the real pole that is shown in section of Real Pole Model.

(3) **Double Poles' Model***:* If we solve (A.1) for the case of double pole, we will get two roots exactly the same like as (A.16).

$$C_2 s^2 + C_1 s + 1 = 0 \tag{A.16}$$

$$or,\ s_1, s_2 = \frac{-C_1 \pm \sqrt{C_1^2 - 4C_2}}{2C_2} = -\frac{C_1}{2C_2}, -\frac{C_1}{2C_2} = p_1, p_2$$

Therefore, we can write the output response for the real poles model in the Laplace domain as (A.17)

$$\begin{aligned} V_{out}(s) = V_{in}(s) H_{Tapproximate}(s) &= MV_{dd}\left(\frac{1}{s(s-p_1)^2}\right) \\ &= MV_{dd}\left(\frac{D}{s} + \frac{E}{s-p_1} + \frac{F}{(s-p_1)^2}\right) \end{aligned} \tag{A.17}$$

Again, solving (A.17) using the partial fraction method and equating the coefficient of $s, s^2$and the constant coefficient from (A.18) yields (A.19), (A.20) and (A.21).

$$\frac{1}{s(s-p_1)^2} = \frac{D}{s} + \frac{E}{s-p_1} + \frac{F}{(s-p_1)^2} \tag{A.18}$$

$$or, 1 = D(s-p_1)^2 + Es(s-p_1) + Fs$$

$$or, 1 = D(s^2 - 2p_1 s + p_1^2) + E(s^2 - p_1 s) + Fs$$

$$or, 1 = (D+E)s^2 - (2Dp_1 + Ep_1 - F)s + Dp_1^2$$

$$Dp_1^2 = 1 \tag{A.19}$$

$$2Dp_1 + Ep_1 - F = 0 \tag{A.20}$$

$$D + E = 0 \tag{A.21}$$

From (A.19), the constant coefficient value of D is $\frac{1}{p_1^2}$ and by substituting the value of D in (A.21), we get the coefficient value of E, which is $-\frac{1}{p_1^2}$. Now, by putting the value of D and E in (A.20), it yields (A.22 to get the coefficient value of F.

$$F = 2Dp_1 + Ep_1 = 2 \times \frac{1}{p_1^2} \times p_1 - \frac{1}{p_1^2} \times p_1 = \frac{1}{p_1} \tag{A.22}$$

Therefore, the output voltage response in the Laplace domain can be written from (A.17) which gives us (A.23).

$$\begin{aligned} V_{out}(s) &= MV_{dd}\left[\frac{1}{p_1^2 s} - \frac{1}{p_1^2(s-p_1)} + \frac{1}{p_1(s-p_1)^2}\right] \\ &= \frac{MV_{dd}}{p_1^2}\left(\frac{1}{s} - \frac{1}{s-p_1} + \frac{p_1}{(s-p_1)^2}\right) \end{aligned} \tag{A.23}$$

To get the time domain response, we need to take the inverse Laplace transform again of equation (A.23) and modify (A.24) to get the desired time delay model for the double pole that is shown in section of Double Pole Model.

$$V_{out}(t) = \frac{MV_{dd}}{p_1^2}(1 - e^{p_1 t} + p_1 t e^{p_1 t}) \tag{A.24}$$

$$or, \frac{p_1^2}{M} V_{ratio} = 1 - e^{p_1 t} + p_1 t e^{p_1 t}$$

$$or, e^{p_1 t} - p_1 t e^{p_1 t} = 1 - \frac{p_1^2}{M} V_{ratio}$$

APPENDIX B

DERIVATION OF TUNNELING CURRENT MODEL

To derive the tunnel current, we start from the time independent Schrodinger equation which is shown in (B.1), where the reduced Plank's constant $\hbar = \frac{h}{2\pi}$, $\Psi(x)$ is a wave function, $V(x)$ is the potential energy and E is the energy for majority carrier. The Schrodinger equation in (B.1) can be rewritten as (B.2).

$$-\frac{\hbar^2}{2m^*}\frac{d^2\Psi(x)}{dx^2} + V(x)\Psi(x) = E\Psi(x) \tag{B.1}$$

$$\frac{d^2\Psi(x)}{dx^2} = \frac{2m^*(V(x)-E)}{\hbar^2}\ \Psi(x) \tag{B.2}$$

Assuming that $V(x) - E$ is independent of position in a section between x and $x + dx$. Therefore, the solution of (B.2) can be as $\Psi(x + dx) = \Psi(x)\exp(-kdx)$ with $k = \frac{\sqrt{2m^*[V(x)-E]}}{\hbar}$.The minus sign is chosen since we assume that the particle moves from left to right. For a slowly varying potential the amplitude of the wave function at $x = X_0$ can be related to the wave function at $x = 0$ by (B.3). Equation (B.3) is referred to as the WKB approximation. The value of X_0 and the potential $V(X_0)$ can be obtained from the well-known triangular tunnel barrier diagram of Figure 28. From the geometric information of the triangular barrier in Figure 28, we can get (B.4). By simplifying (B.4) we obtain two different equations. One is the variable length, $X_0 = L\left(1 - \frac{E}{qV_0}\right)$ and the other is the potential as a function of x_0, $V(X_0) = qV_0\left(1 - \frac{X_0}{L}\right)$, where V_0 is considered as a gate voltage (V_G).

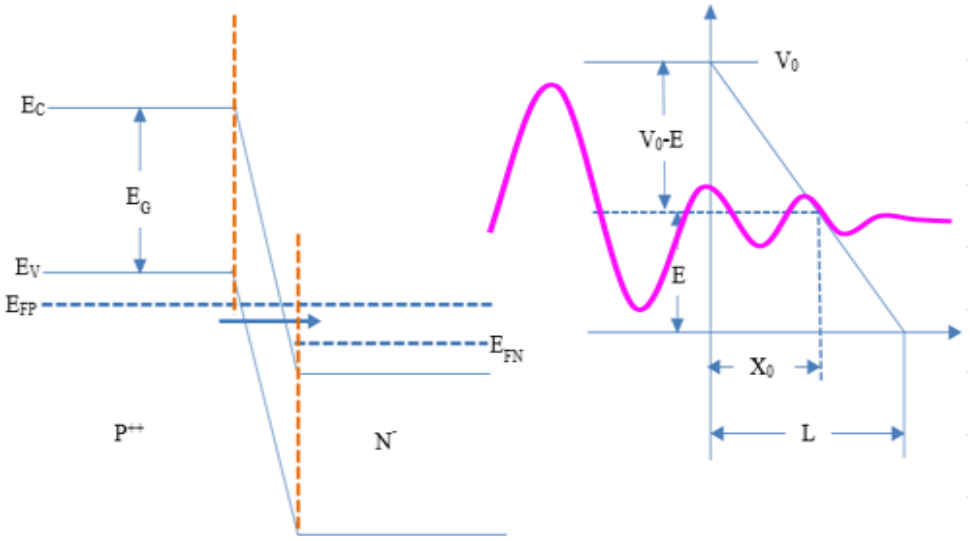


Figure 28. Energy band diagram and triangular barrier of proposed NTFET

$$\Psi(X_0) = \Psi(0) exp\left(-\int_{x=0}^{x=X_0} \frac{\sqrt{2m^*[V(x)-E]}}{\hbar} dx\right) \tag{B.3}$$

$$\frac{X_0}{qV_0 - E} = \frac{L}{qV_0} \tag{B.4}$$

Now, the wave function $|\Psi(x)|^2 dx$ is the probability of finding the particle between x and $x + dx$ or that $|\Psi(x)|^2$ is probability density function, which can be written as $|\Psi(x)|^2 = \Psi(x)\Psi^*(x)$ where $\Psi^*(x)$ is a complex conjugate function. Therefore, the tunneling probability can be expressed as (B.5). Substitute $V(x) = qV_G\left(1 - \frac{x}{L}\right)$ in (B.5) and end up with (B.6).

$$T = \frac{\Psi(X_0)\Psi^*(X_0)}{\Psi(0)\Psi^*(0)} = exp\left(-2\int_{x=0}^{x=X_0} \frac{\sqrt{2m^*[V(x)-E]}}{\hbar} dx\right) \tag{B.5}$$

$$T = exp\left(-2 \int_{x=0}^{x=X_0} \frac{\sqrt{2m^* \left[\left\{ qV_G \left(1 - \frac{x}{L}\right)\right\} - E \right]}}{\hbar} dx \right) \tag{B.6}$$

$$= exp\left(-2 \int_{x=0}^{x=X_0} \frac{\sqrt{2m^* \left[qV_G - \frac{qV_G x}{L} - E \right]}}{\hbar} dx \right)$$

The calculation of integration part in (B.6) is shown below:

Let consider $qV_G - \frac{qV_G x}{L} - E = z$, Therefore, $-\frac{qV_G}{L} dx = dz$.

When $x = 0$, then $z = qV_G - E$.

When $x = X_0$, then $z = qV_G - \frac{qV_G X_0}{L} - E = qV_G - \frac{qV_G}{L} \times L\left(1 - \frac{E}{qV_G}\right) - E = 0$

Therefore

$$\int_{x=0}^{x=X_0} \frac{\sqrt{2m^* \left[qV_G - \frac{qV_G x}{L} - E \right]}}{\hbar} dx = -\frac{L\sqrt{2m^*}}{q\hbar V_G} \int_{z=qV_G-E}^{0} \sqrt{z}\, dz = \frac{2L\sqrt{2m^*}}{3q\hbar V_G} \left(z^{3/2}\right)\Big|_{z=0}^{qV_G-E}$$

$$= \frac{2L\sqrt{2m^*}}{3q\hbar V_G} (qV_G - E)^{3/2}$$

From the energy band diagram in Figure 28, it can be noticed that the maximum tunneling probability occurs at $qV_G - E = E_G$. After solving this above integration, the tunneling probability can be expressed as (B.7).

$$T = exp\left(-\frac{4L\sqrt{2m^*}}{3q\hbar V_G} {E_G}^{3/2} \right) \tag{B.7}$$

Therefore, the tunneling current can be obtained from the product of the carrier charge, velocity and density of electron. The velocity is equal to the Richardson velocity, the velocity with which on average the carrier approaches the barrier while the carrier density is equal to the density of available electrons multiplied with the tunneling probability. From this

information, we can write the tunneling current as in (B.8) where the Richardson velocity, $V_R = \sqrt{\frac{kT}{2\pi m}}$.

$$I_{Tunneling} = A_{area} q V_R N_c exp\left(-\frac{4L\sqrt{2m^*}}{3q\hbar V_G} {E_G}^{3/2}\right) \tag{B.8}$$

APPENDIX C

DERIVATION OF SUBTHRESHOLD SWING MODEL

From Appendix B, the drain to source through the channel tunneling current can be obtained as (C.1). According to the definition, subthreshold swing equals the gate voltage swing needed to change the drain current by one decade. Mathematically, subthreshold swing can be defined as $S = \left[\frac{dlog_{10}(I_{Tunneling})}{dV_{GS}}\right]^{-1}$. For the proposed tunnel FET, the tunneling current that is modeled in (C.1) can be represented as the simplified form of (C.2) where the coefficients of A and B are $A_{area}qN_cV_R$ and $\frac{4\sqrt{2m^*}}{3\hbar q}E_G^{3/2}$, respectively which are determined by the materials properties of the junction and the cross-sectional area of the device.

$$I_{Tunneling} = A_{area}qN_cV_R exp\left(-\frac{4\sqrt{2m^*}}{3\hbar q\xi}E_G^{3/2}\right) \tag{C.1}$$

$$I_{Tunneling} = Aexp\left(-\frac{B}{\xi}\right) \tag{C.2}$$

The derivative of the logarithmic tunneling current of (C.2) with respect to the gate-to-source voltage can be used to determine an expression of subthreshold swing of tunnel FET. Some steps are shown below:

$$S = \left[\frac{dlog_{10}(I_{Tunneling})}{dV_{GS}}\right]^{-1} = \ln(10)\left[\frac{d(lnI_{Tunneling})}{dV_{GS}}\right]^{-1} \tag{C.3}$$

Now, if we take the natural log on both sides of (C.2) and differentiate with respect to V_{GS}, we get (C.4) and (C.5), respectively.

$$ln(I_{Tunneling}) = lnA - \frac{B}{\xi} \tag{C.4}$$

$$\frac{dln(I_{Tunneling})}{dV_{GS}} = \frac{B\frac{d\xi}{dV_{GS}}}{\xi^2} \tag{C.5}$$

$$S = \ln(10)\left[\frac{d\left(lnI_{Tunneling}\right)}{dV_{GS}}\right]^{-1} = ln(10)\left[\frac{B}{\xi^2}\frac{d\xi}{dV_{GS}}\right]^{-1} \quad \text{(C.6)}$$

$$S = \begin{cases} ln(10)\left[\frac{B}{\xi^2}\frac{d\xi}{dV_{GS}}\right]^{-1} \\ ln(10)\left[\frac{BL}{{V_{GS}}^2}\right]^{-1} \\ ln(10)\left[\frac{3B}{{V_{GS}}^2}\sqrt{\frac{\varepsilon_{MoS_2}}{\varepsilon_{HfO_2}}t_{HfO_2}t_{MoS_2}}\right]^{-1} \end{cases} \quad \text{(C.7)}$$

It is seen from (C.6) that the subthreshold swing will decrease if the term $\frac{d\xi}{dV_{GS}}$ is increased. This occurs when the gate is placed parallel to the channel length with the internal field of the tunnel junction. In this way, the gate field adds to the internal field to increase the tunneling probability, which leads to a higher tunneling current and a reduced subthreshold swing.

In [129], it is shown that the absence of a short channel effect for 50 nm channel length, and the characteristics screening length can be assumed to be one third of the channel length for a 6-layer MoS_2, Mathematically, it can be expressed as $\lambda = \sqrt{\frac{\varepsilon_{MoS_2}}{\varepsilon_{HfO_2}}t_{HfO_2}t_{MoS_2}}$. From [129], we can also estimate an upper limit of the in-plane dielectric constant that is a critical parameter in determining the scalability of any channel material. Experimental result reveals that the dielectric constant is 6.5 for 8nm MoS_2 flakes and it is possible to get a significant amount of current by appropriate doping. In [131], theoretically it is shown that 6-layer MoS_2 flake has a dielectric constant of 6.4. For bulk MoS_2, the in-plane dielectric constant is 8.9, which cannot provide a current. This significant information (both theoretical work [131] and experimental work [129]) helps us model the subthreshold swing in terms of other critical parameters

(electric field, gate voltage, channel length, tunneling screening length, and oxide thickness), which is shown in (C.7).

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