NANOSTRUCTURED POROUS MATERIALS FOR MICRO- AND NANO-ELECTRONICS APPLICATIONS

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Porous silicon is a new morphology of the chemical element Silicon.

ABSTRACT

This thesis work presents new research on porous silicon technologies for the heterogeneous integration on silicon platforms, as a key enabling technology for future 3D integrated systems. Porous silicon can be obtained with CMOS compatible processes on localized area on silicon wafer and, due to its tunable electrical, mechanical and thermal characteristics is an effective buffer material. Moreover, macroporous morphologies of porous silicon can can be exploited for the realization of "bed-of-nails" type through wafer interconnects, paving the way to high density, low-cost, through silicon vias.

This work is divided in three parts: the first part introduces porous silicon, summarizes the available literature and presents process characterization for the porous layers obtained in this work and their properties; the second part describes the layer transfer technology and the buried cavities technologies developed in this work using the porous layers presented in the previous part; the last part introduces two applications of the layer transfer technology: compliant contacts and integrated physically small antennas.

PUBLICATIONS

Some ideas and figures have appeared previously in the following publications:

4 COPPER DEPOSITION INTO POROUS SILICON LAYERS

- [1] Bandarenka, H.; Redko, S.; Nenzi, P. & Balucani, M., "Copper displacement deposition on nanostructured porous silicon", *Technical Proceedings of the 2011 NSTI Nanotechnology Conference and Expo, NSTI-Nanotech 2011*, 2011, 2, 269-272.
- [2] Bandarenka, H.; Petrovich, V.; Komar, O.; Nenzi, P.; Balucani, M. & Bondarenko, V., "Characterization of Copper Nanostructures Grown on Porous Silicon by Displacement Deposition", *ECS Transactions*, 2012, 41, 13-22.
- [3] Bandarenka, H.; Redko, S.; Nenzi, P.; Balucani, M. & Bondarenko, V., "Optimization of Chemical Displacement Deposition of Copper on Porous Silicon", *Journal of Nanoscience and Nanotechnology*, 2012, 12, 8725-8731.
- [4] Bandarenka, H.; Redko, S.; Smirnov, A.; Panarin, A.; Terekhov, S.; Nenzi, P.; Balucani, M. & Bondarenko, V., "Nanostructures formed by displacement of porous silicon with copper: From nanoparticles to porous membranes", *Nanoscale Research Letters*, 2012, 7, 1-10.

5 POROUS SILICON SUPERHYROPHOBIC SURFACES

- [5] Balucani, M.; Bolognesi, G.; Casciola, C. M.; Chinappi, M.; Giacomello, A. & Nenzi, P., "Superhydrophobic porous silicon surfaces", *Technical Proceedings of the 2011 NSTI Nanotechnology Conference and Expo, NSTI-Nanotech 2011*, 2011, 2, 493-496.
- [6] Nenzi, P.; Giacomello, A.; Bolognesi, G.; Chinappi, M.; Balucani, M. & Casciola, C. M., "Superhydrophobic porous silicon surfaces", *Sensors and Transducers*, 2011, 13, 62-72.

6 THE CONTROLLED RELEASE METAL LAYER TECHNOLOGY

- [7] Balucani, M.; Nenzi, P.; Crescenzi, R.; Dolgyi, L.; Klyshko, A. & Bondarenko, V., "Transfer layer technology for the packaging of high power modules", *Electronic System-Integration Technology Conference (ESTC), 2010 3rd*, 2010, 1-6.

- [8] Nenzi, P.; Crescenzi, R.; Dolgyi, A.; Klyshko, A.; Bondarenko, V.; Belfiore, N. & Balucani, M., "High density compliant contacting technology for integrated high power modules in automotive applications", *Electronic Components and Technology Conference (ECTC), 2012 IEEE 62nd*, 2012, 1976 -1983.

- [9] Balucani, M.; Nenzi, P.; Palma, F.; Bandarenka, H.; Dolgyi, L. & Shapel, A., "Gold in flux-less bonding: Noble or not noble", *Materials Research Society Symposium Proceedings, 2011*, 1299, 15-20.

8 compliant contacts using crml technology

- [10] Nenzi, P.; Crescenzi, R.; Klyshko, A.; Bondarenko, V. & Balucani, M., "Compliant interconnect technology for power modules in automotive applications", *Technical Proceedings of the 2011 NSTI Nanotechnology Conference and Expo, NSTI-Nanotech 2011*, 2011, 2, 430-433.

9 u-helix antennas

- [11] Nenzi, P.; Tripaldi, F.; Balucani, M. & Marzano, F., "Three-dimensional micro-antenna array for millimetre and sub-millimetre-wave remote imaging", *Antennas and Propagation (EUCAP), Proceedings of the 5th European Conference on*, 2011, 2596 -2600

- [12] Nenzi, P.; Tripaldi, F.; Marzano, F. S.; Palma, F. & Balucani, M., "U-Helix 3D-antenna technology", *Technical Proceedings of the 2011 NSTI Nanotechnology Conference and Expo, NSTI-Nanotech 2011*, 2011, 2, 434-437

- [13] Nenzi, P.; Tripaldi, F.; Marzano, F.; Palma, F. & Balucani, M., "60 GHz tapered-helix antenna for WPAN applications", *Electronic Components and Technology Conference (ECTC), 2012 IEEE 62nd*, 2012, 2042 -2047

- [14] Nenzi, P.; Tripaldi, F.; Varlamava, V.; Palma, F. & Balucani, M., "On-chip THz 3D antennas", *Electronic Components and Technology Conference (ECTC), 2012 IEEE 62nd*, 2012, 102 -108

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LISTINGS

ACRONYMS

AUT Antenna Under Test

BER Bit Error Rate

BOE Buffered Oxide Etch

BSG BoroSilicate Glass

C4 Controlled Collapse Chip Connection

CA Contact Angle

CB Current Burst

CBM Current Burst Model

CRML Controlled Release Metal Layer

CNT Carbon Nanotubes

CTE Coeffiecient of Thermal Expansion

CVD Chemical Vapour Deposition

DI Deionized Water

DBC Direct Bond Copper

DRIE Deep Reactive Ion Etching

DMF Dimethylformamide

DMSO Dimethyl Sulfoxide

EDX Energy-dispersive X-ray spectroscopy

ELYMAT Electrolytical Metal Tracer

EMA Effective Medium Approximation

ENIG Electroless-Nickel, Immersion Gold

EtOH Ethanol

FA Formamide

FCC Federal Communication Commission

FEM Finite Element Method

FTIR Fourier Transform Infrared Spectroscopy

HF Hydrofluoric Acid

HPBW Half Power Beam Width

HREM High Resolution TEM

HW Handle Wafer

IMC InterMetallic Compounds

IPA Isopropyl alchool

IHPM Integrated High Power Module

IR Infrared

ITRS International Technology Roadmap for Semiconductors

ITS Intelligent Transportation Systems

ITU International Telecommunication Union

IUPAC International Union of Pure and Applied Chemistry

KOH potassium hydroxide

LP-PVD Low Pressure Physical Vapor Deposition

LUT Look-Up Table

MeCN Acetonitrile

MeOH Methanol

MoM Method of Moments

MEMS Micro Electro Mechanical Systems

MPT Mimistry of Post & Telecommunications

NPs nanoparticles

OTS Octadecyltrichlorosilane

PAN Personal Area Network

PS Porous Silicon

PCBs Printed Circuit Boards

PDMS Polydimethylsiloxane

QC Quantum Confinement

QW Quantum Wire

QWs Quantum Wires

RAA Radially Averaged Autocorrelation

RDF Radial Distribution Function

RDL ReDistribution Layer

RIE Reactive Ion Etching

RT Room Temperature

RTV Room Temperature Vulcanizing

SEM Scanning Electron Microscope

SERS Surface Enhanced Raman Scattering

SCR Space Charge Region

SHE Standard Hydrogen Electrode

SHS Superhydrophobic Surface

SHSs Superhydrophobic Surfaces

SiP System in Package

SL Sacrificial Layer

SoC System on Chip

SW Support Wafer

TAB Tape Automated Bonding

TEM Transmission Electron Microscopy

TL Transferred Layer

TPS Terahertz Pulsed Spectroscopy

TSV Trough Silicon Via

TMAH Tetramethylammonium Hydroxide

UV Ultraviolet

VSWR Voltage Standing Wave Ratio

WPAN Wireless Personal Area Network

XPS X-ray photoelectron spectroscopy

XRD X-Ray Diffraction

1 INTRODUCTION

The integration of heterogeneous components onto System on Chip (SoC) or System in Package (SiP) is one of the line of research of today's electronics industry. This line is conventionally called "More than Moore" and aims to include new functions on existing electronics systems by diversification and not by scaling. Wireless communications, optical communications, Micro Electro Mechanical Systems (MEMS), energy storage and harvesting devices are only but a few of the functions that will be (or are already) integrated in conventional integrated circuits. The implementation of the vision of cyber-physical systems, depends on the availability of a set of technologies that will make this integration possible and economically viable.

This thesis work addressed the problem of heterogeneous integration of different functions on silicon integrated circuit exploiting porous silicon layers. This morphological form of silicon has been already studied in the past for its photoluminescence properties and, almost immediately, abandoned due to the aging problems caused by its reactive surface. Today porous silicon is used mainly as a functional material for the realization of biosensors or as a sacrificial material in microfabrication technologies.

The research carried on in this work targets the identification of porous-silicon based technologies for the realization of:

- cost effective vertical contacting structures through silicon wafers. This technology would be a key to replace the more expensive Deep Reactive Ion Etching (DRIE) or LASER based technologies for the realization of cheaper silicon interposers,
- superhydrophobic layers and channels for the integration of microfluidics paths on silicon chips. This technology would be a key to simplify the 3D integration of lab-on-chips on silicon ICs,
- cost effective realization of arbitrarily shaped, three dimensional structures on top of silicon wafers.

The first target is addresses the problem of integration of different dies over an interposer and devices to implement the concept of a System-on-Package, an extension of the SiP concept, in which the substrate that hosts the different dies does not limits its function to provide mechanical stability and electrical connectivity but can provide energy storage through integrated batteries, embedded passives, optical connections, antennas and microfluidic paths.

The second target aims to integrate microfluidic functions on dies (or interposers) characterized by low friction and self cleaning properties.

The third target aims to integrate vertical metal structures on silicon wafer, like compliant contacts for off-chip interconnections and non-planar antennas.

This thesis is divided in three parts:

- The first part is about porous silicon and porous silicon technology: it recalls the fundamental concepts and reports the research on this material and the electrochemical processes for the realization of porous layers necessary to reach the above mentioned targets. The first chapter in this part is a review of actual knowledge on porous silicon and the others describe the research done in this work to optimize the characteristics of the porous layers an of the metal (copper) deposition onto that layers.

- The second part describes two technologies developed in this work: the CRML technology and the buried cavities technology. The sequence of process steps, and characterization data are presented for each process involved.

- The third part presents two application that has been realized to demonstrate the CRML technology: a probe card contactor and an on-chip integrable antenna. These are, among the tested application that reached the industrialization level (probe card) and prototype-level (antennas).

Part I

POROUS SILICON

This part deals with porous silicon. The first chapter introduces porous silicon (micro- meso- and macro-porous morphologies), its characteristics, the involved chemistry, and its formation models. In the second chapter the characterization of the porous silicon layers used in the rest of thesis is presented, with a focus on macroporous silicon on low doped p-type silicon wafer. The third chapter deals with copper deposition onto and into porous silicon layers to form nano-particles and uniform thin and thick layers. In the fourth chapter the hydrophobicity study of macroporous surfaces is presented.

2

POROUS SILICON

2.1 INTRODUCTION TO POROUS SILICON

Porous silicon was discovered by accident in 1956 by Arthur Uhlir Jr. and Ingeborg Uhlir [36, 37] during experimental studies on electropolishing. They discovered that electropolishing of silicon happened at a certain current density threshold, below which, a brownish residue remained on the surface, that was porous silicon (Porous Silicon (PS)).

The interest of the scientific community in porous silicon was not very high until the '90s of the past century when Leigh Canham published his studies on the photoluminescence of porous silicon. He observed that small silicon crystallites (with dimensions less than the dimensions of the free exciton of bulk silicon ($\sim$ 50 Å), show a significantly more intense photoluminescence than bulk silicon. This is to impute to the Quantum Confinement (QC) effects on band structure of small structures of silicon [38]. This discovery triggered the interest on porous silicon as light emitter [39, 40, 41] as the curve in figure 1 clearly shows. The difficulties in stabilizing the photoluminescence of porous silicon, due to the oxidation of its highly chemically reactive surface, diminished the interest on photonic applications of porous silicon. This happened only a few years after the discovery of photoluminescence, around 1993, and it is evident in the curve in figure 1 as the trend in published papers becomes linear. Today porous silicon it is studied as a sacrificial material in MEMS, as functional material (a material that can be functionalized) in biochemistry applications, or as template for structuring of other materials. PS has some interesting properties that can be exploited in micro- and nano-electronics applications:

- Its thermal conductivity is comparable to that of silicon dioxide (SiO_2) [42],
- its electrical properties (permittivity and electrical conductivity) can be controlled over wide ranges by altering porosity and pore morphology [43, 44],
- its mechanical properties, that are influenced by porosity and pore morphology [20],
- its explosive properties , that can be exploited in tamper-proofing electronic systems [45, 46].

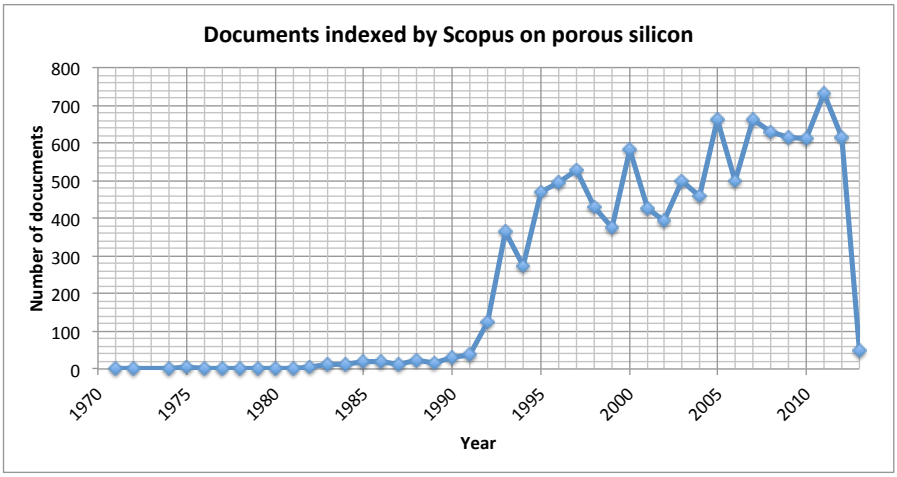


Figure 1: Number of documents (including papers and patents) that have the keyword "porous silicon" in title, abstract or keywords since 1970 as reported by Scopus. The sharp rise in 1991 is due to the discovery of photoluminescence of porous silicon by Leigh Canham that triggered the interest of the scientific community. In 2013, almost 50 papers have been indexed in January only.

The above mentioned properties of porous silicon pertain mostly to micro- and meso-porous morphologies and constitute the main reason for the research interest in this material. The strong dependence of those properties on porous structure morphology allows microsystems designers to locally (on-die) tailor substrate characteristics to their needs. This would be fundamental for the heterogeneous integration of different functions in a SiP or SoC, a largely unexplored field. Today porous silicon is mainly used in the following applications:

- Sensors [47, 48, 49]: porous silicon allows to develop low cost chemical and biosensors due to the ease manufacturing processes, its optico-physico properties and the versatile surface chemistry.

- Active biomaterial [50, 51]: PS has been demonstrated to be biocompatible, bioactive and biodegradable. *In-vitro* and *in-vivo* tests demonstrated that it can be used as a coating for implanted micro-electrodes to increase their bio-compatibility.

- Antireflection coating in solar cells [52]: The refractive index of meso-PS (pores with characteristic size greater than 2 nm) depends on porosity and can be modulated varying the process current density. This characteristic has been exploited for the formation of an anti-reflection coating on the surface of silicon solar cells (crystalline, poly/multi-crystalline).

- Bragg reflectors and interferential filters [53, 54]: PS multilayers have been demonstrated for the realization of integrated distributed Bragg reflectors and Fabry-Pérot interference filters.

- Growth substrate for nanotubes [55]: forests of vertically aligned Carbon Nanotubes (CNT) have been grown from PS layers by Chemical Vapour Deposition (CVD).

- Electrode material in supercapacitors devices[56, 57]: the high surface to volume ratio of micro- and meso-PS allows to fabricate high specific-capacitance (greater than $5\,^{mF}/_{g}$) supercapacitors devices.

- Template for metal and polymer electro-deposition[58, 33]: ordered and random templates of PS have been used for the electrodeposition of metals and polymers (using the electropolymerization technique). Depending on the final application the silicon template can be removed to release the metallic or polymeric structures or it can be kept.

- Buffer layer [59]: meso-PS has been use to grow ZnO (Zinc Oxide) onto silicon for optoelectronics component integration.

The previous list covers only but a few of the applications of this versatile material. Most of them exploit the large surface to volume ratio of meso- and micro-porous morphologies (greater than $500^{m^2}/_{cm^3}$) or QC effects in micro-PS. The third and most elusive morphology, macro-PS, has been discovered later than the others and, has been mostly used as a template. The most important discoveries of research in PS have been summarized in figure 2 (re-organizing the same data present in [15]), and presented in chronological order. It is not the aim of this work to provide a thorough analysis of all the literature on PS and there is no need as, a few outstanding resources are available. The interested reader is invited to refer to them, in particular to the Canham's book "*Properties of Porous Silicon*" [60], the seminal work in this field; or to the Lehmann's book "*The electrochemistry of silicon: instrumentation, science materials and applications*" [17], the ideal companion reference for experimenting with PS. A third reference book is Zhang's "*Electrochemistry of Silicon and its Oxide*" [15], that introduces PS in the more general context of silicon electrochemistry and gives to the reader a comprehensive view of the subject.

Last, but not least, two review papers must be cited: "*Silicon Porosification: State of the Art*" [61] written by Korotcenkov and Cho, published in 2010 that updates the state of the art and "*Porous Silicon: Theoretical Studies*" [62] written by John and Singh, that reviews the study on photo and electroluminescence of PS.

The rest of this chapter introduces some fundamental concepts of porous silicon and definitions that will be used in the rest of this work.

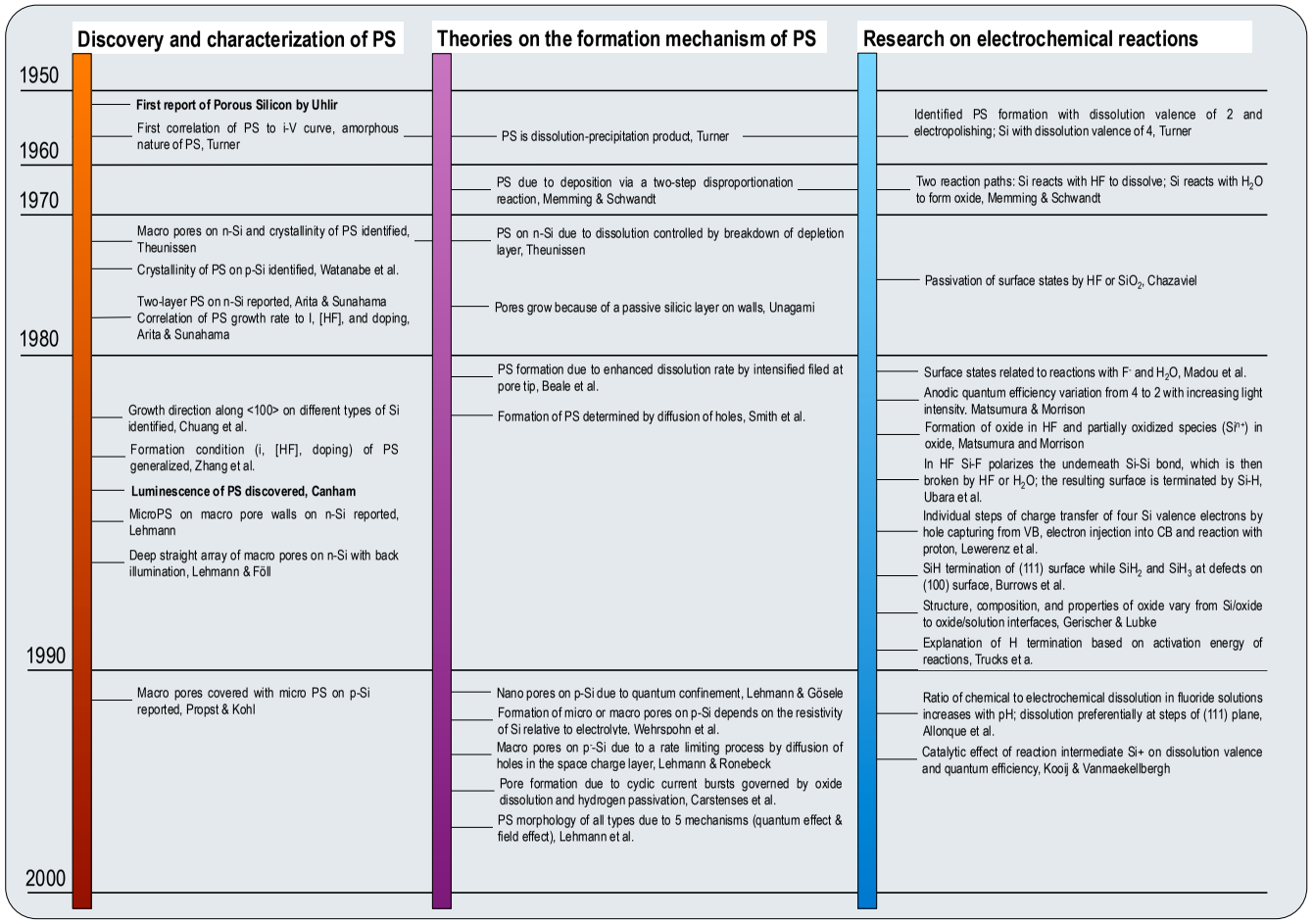


Figure 2: Porous silicon discoveries timeline. This picture is a reorganization of the timelines reported in [15], in figure 8.58, 8.59 and 8.60. It shows the progress of research on PS up to year 2000 in three different fields: discoveries in PS features and characterization (left), theories on formation mechanisms (center), and theories on fundamental electrochemical reactions (right).

IUPAC **Nomenclature for porous materials**	
Category	Pore width
micropore / microporous	$w < 2\,\text{nm}$
mesopore/mesoporous	$2\,\text{nm} < w < 50\,\text{nm}$
macropore/macroporous	$w < 50\,\text{nm}$

Table 1: IUPAC classification of porous materials.

2.2 USEFUL DEFINITIONS

The essential concept that must be introduced when working with porous materials is the concept of "pore". In this context, the definition given by Canham in [60]: *"Pore is an etch pit whose depth, d, exceeds its width, w"* is the most fitting and allows to discriminate between porous and rough surfaces. Both kind of surfaces can be obtained by electrochemical processes on silicon and thus is necessary to provide a criterion to distinguish them. International Union of Pure and Applied Chemistry (IUPAC) has classified porous materials in three classes, according to the median width of the pores. The classes and the dimensional characteristics are reported in table 1.

Most authors, in available literature, indicate the pore width as pore "diameter" because the most common encountered morphology is cylindrical or quasi-cylindrical. In this work the words "width" and "diameter" are both used and letter w is adopted for both. The value of w is computed according to the Feret's diameter definition (or maximum caliper diameter): *the longest distance between any two points along the selection boundary*, i.e. the maximum distance between parallel lines tangent to the boundary of the feature (the pore in this case). This is the definition commonly employed in microscopy to measure the dimension of a feature with irregular border, and it is used by the software tool used in this work to characterize PS: ImageJ [63, 64, 65].

Figure 3 shows an example image analysis of a sample of macro-PS that has the sole purpose of clarify the definition of Feret's diameter. The Scanning Electron Microscope (SEM) image (figure 3.(a)) is initially thresholded and binarized (figure 3.(b)) to extract the contours of the pores (they appear as black areas in the image). The binarized image is processed with ImageJ particles analysis tools to extract dimensional information (diameter, area, circularity, etc.). The Feret's diameter of a single pore, with its numerical value, is highlighted in figure 3.(c). The two insets show the Feret's diameter and area distribution of the sample. This technique is employed, in this work, on images with higher number of pores, to compute statistical parameters of realized macro-PS samples (porosity, pore diameter, etc.).

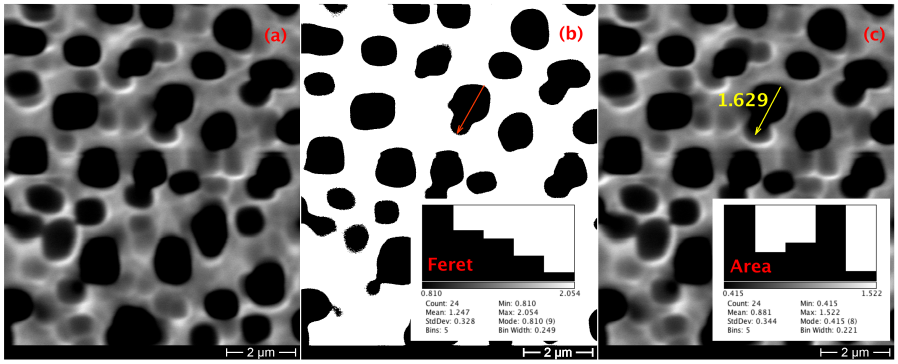


Figure 3: Example of image analysis of macroporous silicon done with ImageJ. The original SEM image on the left (a) is thresholded and analyzed with ImageJ *particles analysis tool* (b), and the distribution of dimensional parameters of the pores are extracted (c and insets).

2.2.1 *Porosity*

Porosity is one of the principal parameters (the other is morphology) of PS. It is defined as: *the ratio of volume of the void (all the pores)* V_{pores} *to the volume of the whole* V_{ps},

$$p = V_{pores}/V_{PS} \tag{1}$$

and it is usually expressed as a fraction over the total volume (i.e. 0.0 - 1.0) or, as percentage 0 - 100%. The *gravimetric method* is usually employed to evaluate the porosity of a PS sample. The density of the porous layer ρ_{PS} is defined as the ratio m_{PS}/V_{PS}, i.e. the ratio of PS mass and PS volume. The porosity is defined as:

$$p = 1 - \rho_{PS}/\rho_{Si} \tag{2}$$

(with $\rho_{Si} = 2330\, kg \cdot m^{-3}$ the density of silicon). The gravimetric method is based on, at least, two out of three weight measurements on a precision balance: m_1, m_2, and m_3. The first measurement (m_1) is done on the silicon sample before the porosification process, the second measurement (m_2) is done on the sample after the porosification process, and the last one (m_3), after the dissolution of the porous layer. It is possible to compute porosity from the determination of the dissolved mass [17], i.e. the mass lost in the anodization process, $\Delta m_D = m_1 - m_2$:

$$p = \frac{\Delta m_D}{(\pi r)^2 t \rho_{Si}} \tag{3}$$

with reference to the geometry in figure 4. This measure is not destructive but the volume of the porous layer must be known. A second procedure [17] to compute porosity is by selective etching of the porous silicon layer (e.g. by potassium hydroxide (KOH) etching). The

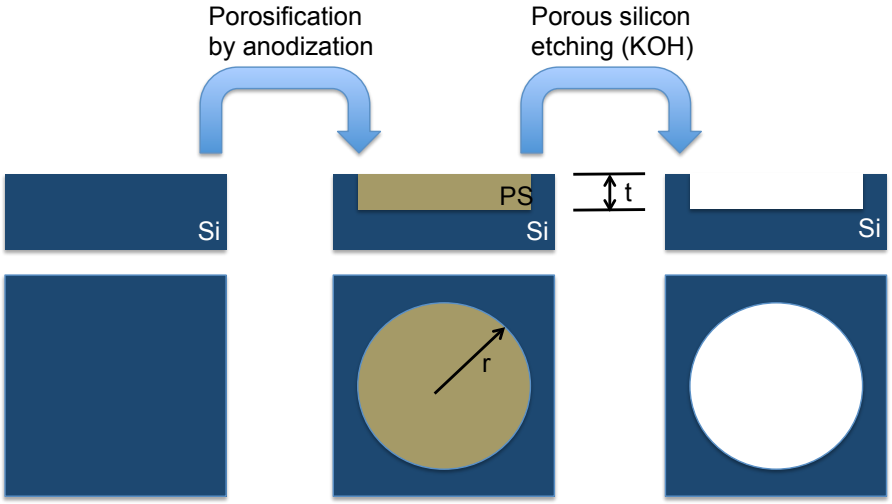


Figure 4: Gravimetric method for evaluation PS porosity. The weight of a silicon sample (cross-section and top-view) is measured before and after anodization (the porosification process) and a third time after the removal of the porous layer, e.g. by immersion in a KOH solution.

mass of porous silicon $m_{PS} = m_2 - m_3$ is determined and the porosity is computed with:

$$p = 1 - \left[\frac{m_{PS}}{(\pi r)^2 \, t \rho_{Si}} \right] \tag{4}$$

This measure is destructive and requires a highly-selective (to silicon) etching process (usually a solutions 2wt.% to 10 wt.% o KOH in Deionized Water (DI) are employed). Both the procedure require the knowledge of the porous volume that, in some cases, can be irregular and of difficult determination. A third procedure that is independent from volume considerations, involves all three measurements:

$$p = \frac{m_1 - m_2}{m_1 - m_3} \tag{5}$$

In this work, a second measure of porosity has been introduced to better characterize the surface effects of macro-PS layers: the *superficial porosity* "p_s". The superficial porosity is computed from grayscale SEM images of porous surfaces (top-view), ratioing the area of pixels whose intensity is below a set threshold (A_{pores}) to the total image area (A_{total}):

$$p_S = \frac{A_{pores}}{A_{total}} \tag{6}$$

The superficial porosity is computed with the same tool used for computing pore morphology (shown in figure 3). The area occupied by pixels belonging to pores (the ones below the intensity threshold) is the area of the void fraction (pores). The obtained value of porosity with this measurement coincides with the gravimetric, for uniform

cross-section pores of equal depth. This coincidence is rarely found in practice because of the presence of "*shallow pores*" in random macroporous layers. The superficial porosity is, in general, higher than the gravimetric porosity because of "shallow pores", i.e. pores that do not fully develop and do not contribute significatively to the loss of weight but, contribute to the surface properties. In figure 3 shallows pores are clearly visible between black areas (fully developed pores); they appear as dark grey depressions.

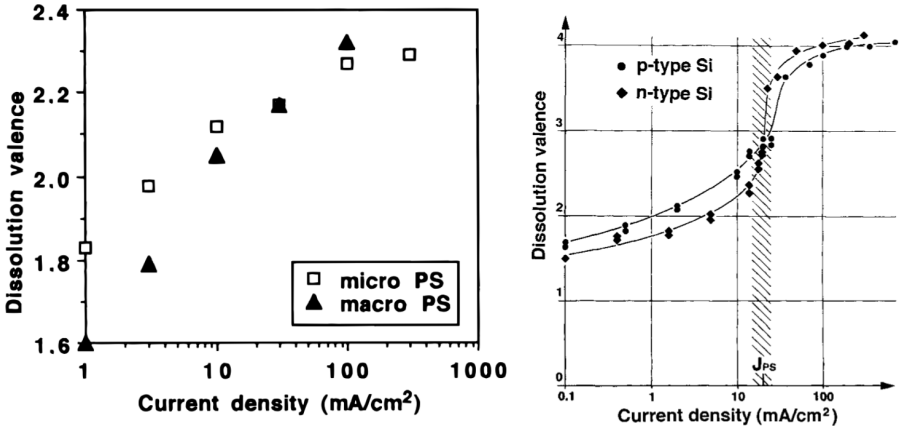


Figure 5: (Left) Effective dissolution valence for p-type silicon electrode in *ethanoic HF* (1:1, EtOH : HF 50 wt.%) [16] for two different resistivities: (▲) macropores on 50 Ωcm, (□) micropores on 1 Ωcm. (Right) Effective dissolution valence of n- and p-type silicon electrodes in 2.5% HF [17].

2.2.2 *Effective dissolution valence*

The *effective dissolution valence* n_v is defined as the exchanged charge carriers n_{he} per dissolved silicon atom. It reflects the nature of the reactions involved in silicon dissolution processes in fluoride-containing solutions. The number of exchanged charge during the dissolution process is given by the current-time product It, divided by the elementary charge e ($1,60210 \times 10^{-19}$C). The number of dissolved silicon atoms is computed from sample weight loss (Δm_D measured gravimetrically) divided by the atomic mass of silicon m_{Si} ($4,6638 \times 10^{-23} g$). The dissolution valence n_v can be calculated as the ratio of the two [17]:

$$n_v = (It/e)/(\Delta m_D/m_{Si}) \tag{7}$$

The dissolution valence n_v of silicon electrodes in fluoride-containing solutions assumes values between 2 and 4. Values of n_v below 4 indicates that the dissolution process is governed by both chemical and electrochemical components, whereas a value of 4 indicates that the process is totally electrochemical. The effective dissolution valence of

silicon has been found to vary with silicon material, solution composition, anodic polarization, and illumination conditions. In fluoride-containing solutions the dissolution valence varies from 2 in the exponential region to near 4 in the electropolishing region as shown in figure 5.

The two panels (left and right) reports the effective dissolution valence for the formation of macro-pores in low-doped (dopant concentration $< 10^{17} {}^{atoms}/_{cm^3}$) n- and p-type silicon electrodes in the same current density range at different HF concentrations. The dissolution valence increases with current for all types of materials as shown in figure 5. There is a sharp increase in n_v corresponding to the "peak current", (J_{PS}), i.e. the current at which electropolishing starts. This sharp increase is not visible in the left panel of figure 5 because its value shifts to higher values with increasing HF concentration. The dissolution valence at low current densities, for each solution, assumes values around 2 because of the chemical dissolution of porous silicon surface. The value of dissolution valence in the electropolishing region is somewhat lower than 4 as shown in figure 5 in the right panel. This indicates that hydrogen reaction, which is a chemical reaction, still occurs at high anodic potentials, where the reactions are characterized by the formation and dissolution of an anodic oxide film.

2.3 MICRO- AND MESO-POROUS SILICON

Micro- and meso-porous silicon morphologies have been the most studied due to their porosity-dependent thermal and electronics properties. In this work they have been used as sacrificial material or adhesion layer, respectively and, only a small introduction to them is given, with pointers to relevant literature. Macroporous silicon and its formation mechanism are described in detail as the formation of macropores on low-doped p-type silicon wafer has been integral part of this work.

2.3.1 *Microporous silicon*

Microporous silicon is characterized by pores with dimensions of a few nanometers. Micro-PS can be obtained either with n-type [66] or with p-type silicon [67, 68]. This particular morphology has been used, in this work, only as sacrificial layer in the suspended macroporous membranes described in chapter 7. The QC effects become important at this scale and produce an increase of silicon's bandgap and alter its electronic properties [17, 69, 70]. The widening of the bandgap, i.e. an increase of the bandgap energy $\triangle E_G$, in the wall region of the pores, produces an energy barrier for *holes* ($\triangle E_V$) that regulates PS formation. While there is no universally accepted model

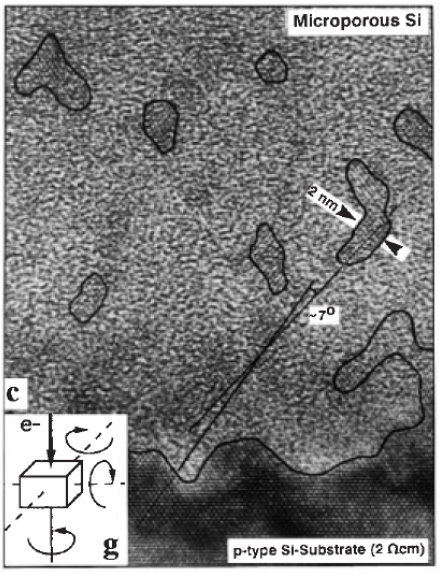


Figure 6: Interface between micro-PS and (100) substrate [17].

for the formation of PS, all authors (and all experiments) attribute to *holes* at the silicon/electrolyte interface the cause of silicon dissolution. If the increase in bandgap energy produces a barrier $\triangle Ev$ at pore walls that is larger than the energy of *holes*, the pore walls will become depleted (of *holes*) and therefore passivated against further dissolution. This QC effect explain the formation of the nanopores: *holes* will enter the electrolyte only at the pore tip (the barrier is thinner and tunneling happens), and rarely via the wall area of the pore, and being *holes* necessary for the reaction of dissolution of silicon, it will occur only at the tip [30].

The morphology of micro-PS is not simple to investigate with optical or electronic microscopy because of the small dimensions of the crystallites. However it has been studied with superposition of results of different technique such as Transmission Electron Microscopy (TEM), Raman spectroscopy, X-Ray Diffraction (XRD), etc. Figure 6 shows a High Resolution TEM (HREM) micrograph of the interface between micro-PS and a (100) substrate. The lattice fringes of micro-PS crystallites (about 2-4 nm in diameter) rotated around an axis parallel to electron beam are evident. Crystallites rotated around the other two axes are imaged like amorphous silicon. A high density of silicon microcrystallites is present in micro-PS. TEM and HREM observations indicate that microporous silicon is a sponge-like silicon structure with crystallites dimension in the order of few nanometers. Other techniques used to investigate confirm these considerations [17, 31].

Micro-porous silicon, studied for its photoluminescence properties, is used in this work as sacrificial layer. In microstructuring and integrated sensor fabrication there is often the necessity of cavities, bridges, or multilayer structures. In conventional silicon technology

these are realized employing double-side lithography and back-side silicon etching, together with conventional front-side processes. In porous silicon technology, micro-PS layers can be grown on lithographically defined areas with controlled porosity and depth. This layer can be dissolved selectively to bulk silicon, using wet chemical or electrochemical processes, leading to the formation of cavities with controllable dimensions. The chemistry of the etching process can be based on KOH [71], HF [72] or Tetramethylammonium Hydroxide (TMAH), the last two more interesting for their CMOS compatibility.

2.3.2 *Mesoporous Silicon*

Mesoporous silicon layers can be obtained with a porosity in the range of 30-80%. Mesoporous silicon morphology can be seen in figure 7.

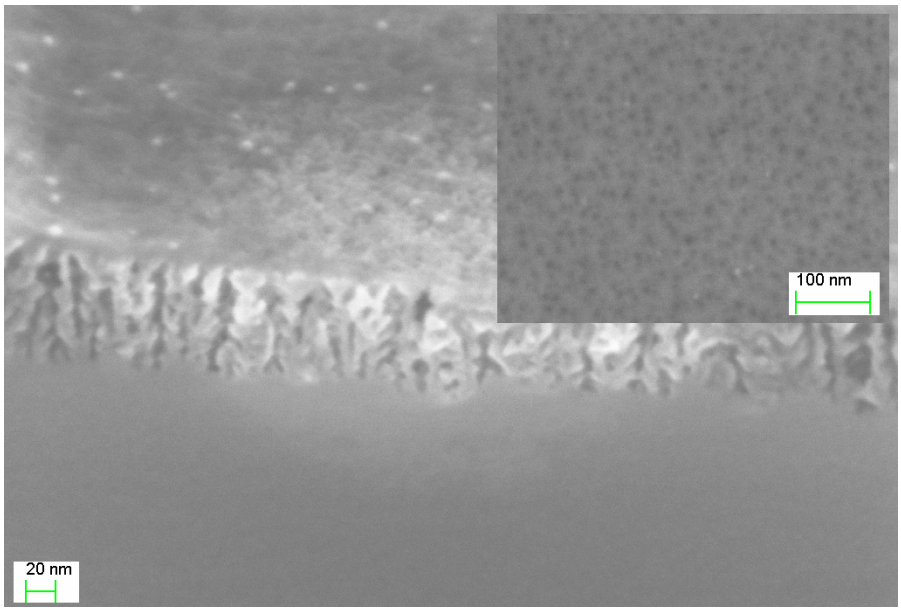


Figure 7: SEM image of the cross-section and the top-view (inset) of a meso-PS sample (from a p+ wafer) with a porosity of about 50%.

This morphology has been extensively studied for its properties that depend on porosity. Some authors report the meso-PS structure having a *coral shape* composed by interconnected Quantum Wires (QWs). The walls of each Quantum Wire (QW) is covered by a thin oxide layer. The usual model for meso-PS consists of three phases: vacuum, silicon crystallites and oxide. Figure 8 reports the most important for the applications: the bandgap increases with porosity 8.(a) and this, in turns, cause the increase of the light absorption coefficient 8.(b): the "a" curve is for a porosity of 32%, and "b" curve for a porosity of 80%.

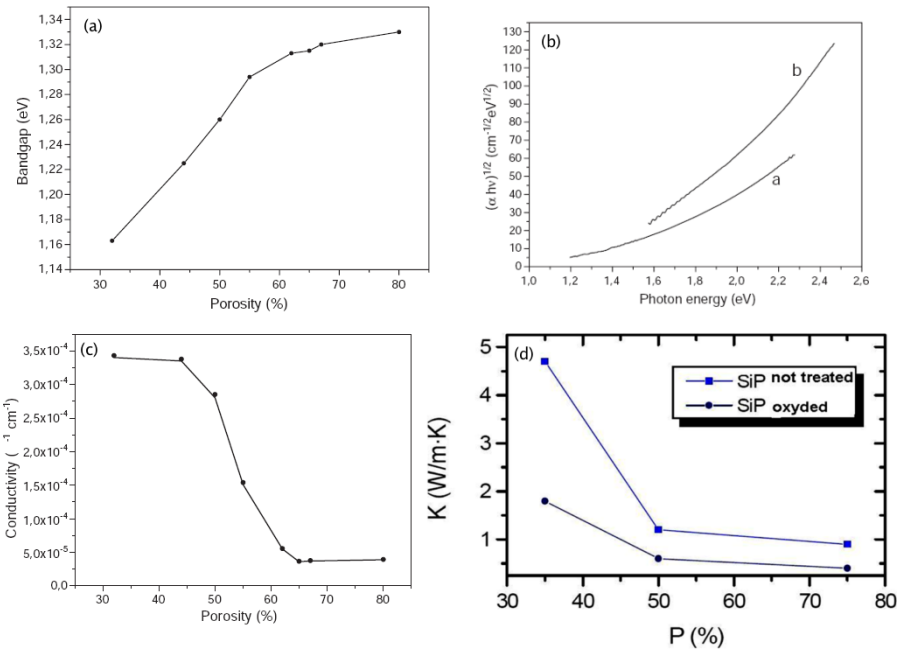


Figure 8: Summary of the properties of meso-PS at different porosities: (a) bandgap [18], (b) absorption [18], (c) electrical conductivity [18], and (d) thermal conductivity for fresh and oxidized (1h in dry O_2) samples [19].

The electrical conductivity of mesoporous silicon has been computed using the Bruggeman Effective Medium Approximation (EMA) model and QC considering the three phases model introduced above [18]. 8.(c) shows the comparison of the theoretical model (the continuous line) with experimental data (•). The thermal conductivity of meso-PS is reported in 8.(d), where it is shown to decrease with porosity as should be expected and has a maximum value of 5 $^{W}/_{mK}$ (bulk silicon has a thermal conductivity of 149 $^{W}/_{mK}$) that is close to the one of silicon dioxide (1.4 $^{W}/_{mK}$).

Mesoporous silicon is an unstable material, its properties suffer of aging phenomena even at Room Temperature (RT) [73] and, in the past, many surface stabilizing treatments have been developed. Mesoporous silicon finds applications in the biomedical field as a template for sustained/controlled drug delivery applications where it is used as hydrophobic or hydrophilic (by properly treating the surface) carrier. The possibility of controlling pore size modifying the experimental parameters (substrate, electrolyte and current density) is of particular interest in drug delivery as, pore diameters of the order of the drug molecule size prevent its crystallization (the drug remains in amorphous form) avoiding lowering of solubility [74, 75].

Mesoporous silicon finds application in layer transfer technologies due to its porosity dependent mechanical characteristics [20]. The ultimate strength of porous layers with different porosities have been measured for both <100> and <111> orientation. Figure 9 shows the

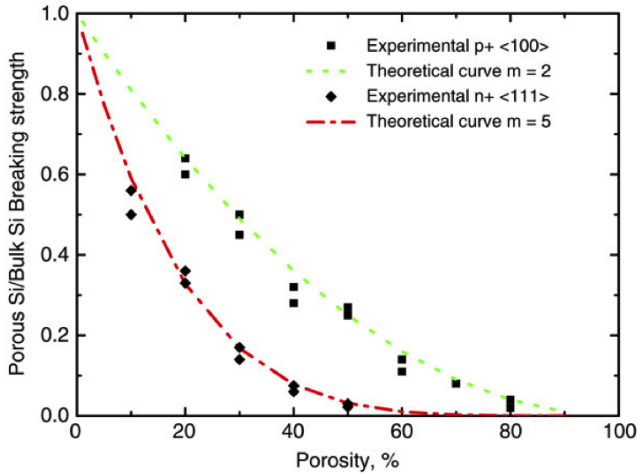


Figure 9: Relative (to bulk silicon) breaking strength of meso-PS layers (10 μm thick) with porosities between 10% and 80% [20].

results. The nonlinear characteristic is usually attributed to the non-uniform stress distribution along the pores. The measurements have been fit with a generally accepted empirical model [20]:

$$\sigma = \sigma_0 (1 - p)^m \tag{8}$$

where σ is the breaking strength of porous silicon sample of porosity p, σ_0 is the ultimate tensile strength of bulk silicon (7000 MPa) and m is a fitting coefficient. It has been found that at low porosities the dependence is almost exponential:

$$\sigma = \sigma_0 \cdot exp(-B_k p) \tag{9}$$

where B_k is a fitting parameter in the range 4 to 7. The data in figure 9 have been fitted with 8 (dashed lines). The porous layer on n+ has a fitting exponent of $m = 5$ (the relationship is closet to the exponential), whereas the one on p+ has a fitting exponent of $m = 2$ (close to a linear relationship). This difference has been attributed to different pore morphologies: vertical pores on the p+ <100> substrate and branched on the n+ <111>.

2.4 MACROPOROUS SILICON

Macroporous silicon is the morphology of PS used in this work for producing thick membranes. Macropore formation on p-type silicon has been obtained in the following types of electrolytes:

- water free mixtures of anhydrous HF with an organic solvent [76],
- organic HF electrolytes with a certain fraction of water [77],
- aqueous HF electrolytes [16].

The formation of macropores is not really well understood and most authors seems to agree that only HF is necessary for macropores development (as for other pore types). However there are other factors that influences pore morphology such as the electrolyte concentration, the use of additives, etc. The morphology of macroporous layers on p-type silicon is a consequence of the depletion of pore walls as described in Lehmann's Space Charge Region (SCR) model. In such model, the width of pore walls equals twice the space charge layer of the silicon-electrolyte junction (see section 2.6). This value depends on applied bias and doping density, in particular, there is a linear dependence with the latter. The values of pore density (not a synonym of porosity) observed on non-structured p-type substrates is about one order of magnitude larger than that of n-type electrodes.

The interest in macroporous silicon is in the possibility to define regular or random patterns of macropores with diameters in the micron range that extends, potentially, through the entire silicon wafer. Such structures find applications in optoelectronics, microfluidics and micromachining. The random arrangement of macropores differs in porosity and pore diameters depending on the substrate type; macropore in p-type wafers tends to reach porosities around 50% (gravimetric) and, when the doping density becomes higher than $10^{16}\,cm^{-3}$ (corresponding to wafer with resistivities of 1-2 Ωcm), the porous structure becomes fragile. Pore diameter is controllable on n-type by varying process parameters (like illumination intensity and current density) and almost independent from process parameters in p-type wafers, where pore diameters depends strongly on wafer resistivity (see figure 10) . The main reason for this lack of control on p-type silicon resides in the polarization of the silicon-electrolyte junction, that is reverse in n-type silicon and forward in p-type and, in the latter case the width of SCR is less controllable. The influence of current density on macropore growth in low-doped p-type silicon (wafer resistivities above 10 Ωcm) is limited to the growth rate only, and does not influence significatively the pore diameter, at least below the electropolishing threshold.

The dependence of pore morphology on crystal orientation has been found to be weak in aqueous HF. On (110) and (111) substrates pores tend to branch more compared to (100), where pore walls tend to be smooth. At high HF concentrations or in mixtures with organic solvents, most of the pore volume is found to be filled with micro-PS (see figure 11) while the presence of water or other oxidizing species, reduces this amount of pore filling.

It is common to introduce artificial etch pits on the surface of p-type samples to initiate pore growth at well defined position as arrays of predefined pores has been observed to be more stable than the one formed by random pores [78].

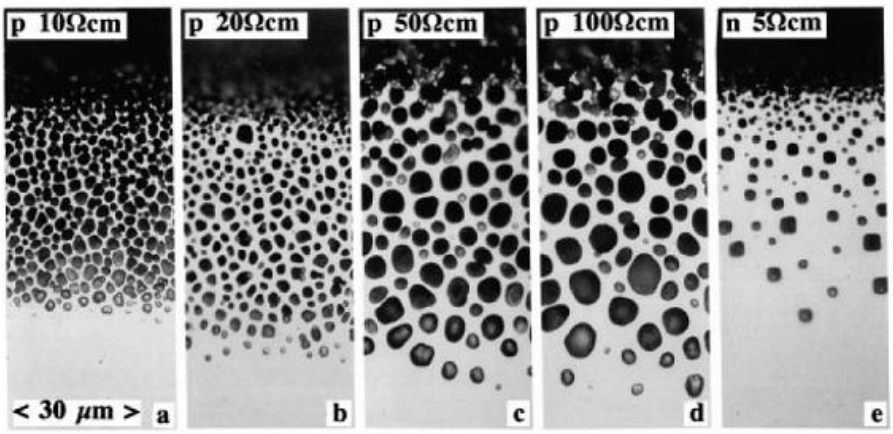


Figure 10: (a-d) Optical micrographs of p-type substrates of different doping densities polished under a small angle to the electrode surface, after anodization under identical conditions in the dark (10% aqueous HF, 3 mA cm^{-2}, 90 min). (e) An n-type substrate anodized under similar conditions is shown for comparison (10% HF, 3 mA cm^{-2}, 30 min) [17].

The formation of macropores in non degenerate n-type silicon (see figure 12) requires sample illumination to photo-generate the *holes* (that are the minority carrier in n-type silicon) to obtain the electrochemical dissolution. Illumination affects the pore tip current during macropore formation. Low doped n-type wafers do not anodize in dark due to the lack of *hole* injection to the surface. It is interesting to report that hole injection into n-type material can be obtained by a p-type doped region and not only with illumination. In most of the experimental setups, the backside of the wafer is illuminated as, under frontside illumination (the side exposed to the electrolyte), a full passivation of the pore walls cannot be not obtained and, for short wavelengths (< 700 nm), macropore growth even becomes suppressed. Under illumination with long wavelength light (700-1100 nm) the resulting pores are conically shaped. An electrode surface covered with such tapered pores appears pitch black to the eye. This is due to light trapping in the porous layer, which reduces the reflectivity to values below 1% in the visible region of the spectrum.

No further discussions will be carried on macropores on n-type silicon, because it's not of interest in this work and there is an extensive literature on this subject, as n-type has been the most used material for macroporous structuring due to the controllability of the involved processes.

In conclusion, as Lehmann stated: it's important to note that the flexibility of pore array design on low doped p-type silicon is less respect to the macropore formation on n-type substrate, because of the limitations in array porosity and substrate doping range [17].

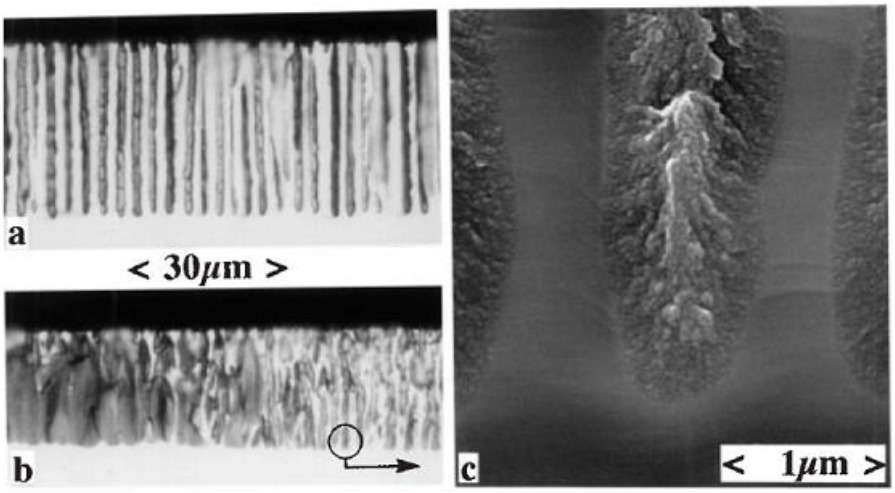


Figure 11: (a,b) Cross-sectional optical micrographs of macroporous silicon formed by anodization of (100) p-type 20 Ωcm silicon electrodes in (a) 2 M HF in MeCN (3 $mA\,cm^{-2}$, 90 min, RT) and in (b) 30% aqueous HF (40 $mA\,cm^{-2}$, 7.5 min, RT). (c) A SEM micrograph of the macropores in (b) reveals that most of the pore volume is filled with microporous silicon [17].

Doping type	**Doping level p-type** [cm^{-1}]	**Resistivity p-type** [Ωcm]
Lowly doped p-type	$<10^{15}$	$> 13,5$
Moderately doped p-type	$10^{15} \div 10^{18}$	$13,5 \div 0,04$
Highly doped n- | p-type	$> 10^{19}$	$< 0,005$ | < 0.009
n-type	$<10^{18}$	$> 0,02$

Table 2: Doping concentration of silicon wafers.

2.4.1 *Morphology*

It's difficult to characterize morphology of PS. There are many different aspects to inspect like size, shape, orientation and distribution, and many are the factors that influences it, like doping concentration, current density, HF concentration, etc. Zhang [15] groups the concentration of doping in four categories a shown in table 2, where corresponding wafer resistivities are tabulated.

The PS formed on moderately doped p-type silicon has extremely small pores ranging typically from 1 to 10 nm. The pores are highly interconnected as illustrated in figure 13. For heavily doped p- and n-type, the pores have diameters typically ranging from 10 to 100 nm. The pores show clear orientation and are less interconnected. For n-type silicon, the pores, with a wide range of diameters from 10 nm to 10 μm are generally straight and clearly separated. For lowly doped p-type silicon, the PS can have two distinctive and continuous pore diameter distributions: large pores on the order of micrometers and small pores on the order of nanometers. The large pores can be

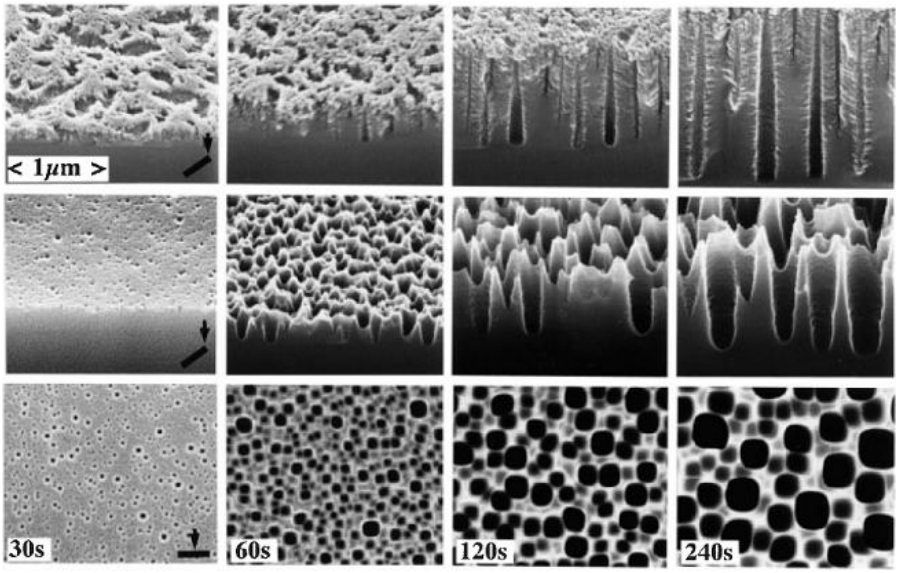


Figure 12: SEM micrographs of surface and cross section of an 0.4 Ωcm n-type (100) silicon electrode anodized for the indicated times under white light illumination of the front side (2.5% HF, 10 mA cm^{-2}, 14 V). Microporous silicon covering the macropores, as shown in the top row, has been removed by alkaline etching for better visibility of the macropore initiation process in the center and bottom rows [21].

fully or partially filled by the small pores. In figure 13 a schematic representation on the various cases presented.

2.4.2 *Pore Density*

The density of the pores, defined as the number of pores per surface unit (usually cm^{-2} or μm^{-2}), increases with doping concentration and decreases with pore size. Micro-PS constitutes an exception to this rule. In macroporous silicon there are two different pore densities that can be measured: superficial density and bulk density; generally the former is higher than the latter, due to the presence of shallow (not fully developed) pores.

The density of pores is determined by the diameter and pore spacing, and depends on any factors that have an effect on the diameter and spacing. Except for micro-PS (less than 2nm in size) the density of pores increases with doping concentration. Generally, the density of pores increases with decreasing pore size. According to data reported in figure 14.(a), pore density decreases with the increasing potential for low-doped substrates and has exactly the opposite behavior on high-doped substrate. In the latter PS was obtained near the electropolishing peak (this concept will be introduced in section 2.5, in the next pages) where the wall thickness decreases with increasing potential. Such a dependence of pore density on doping has

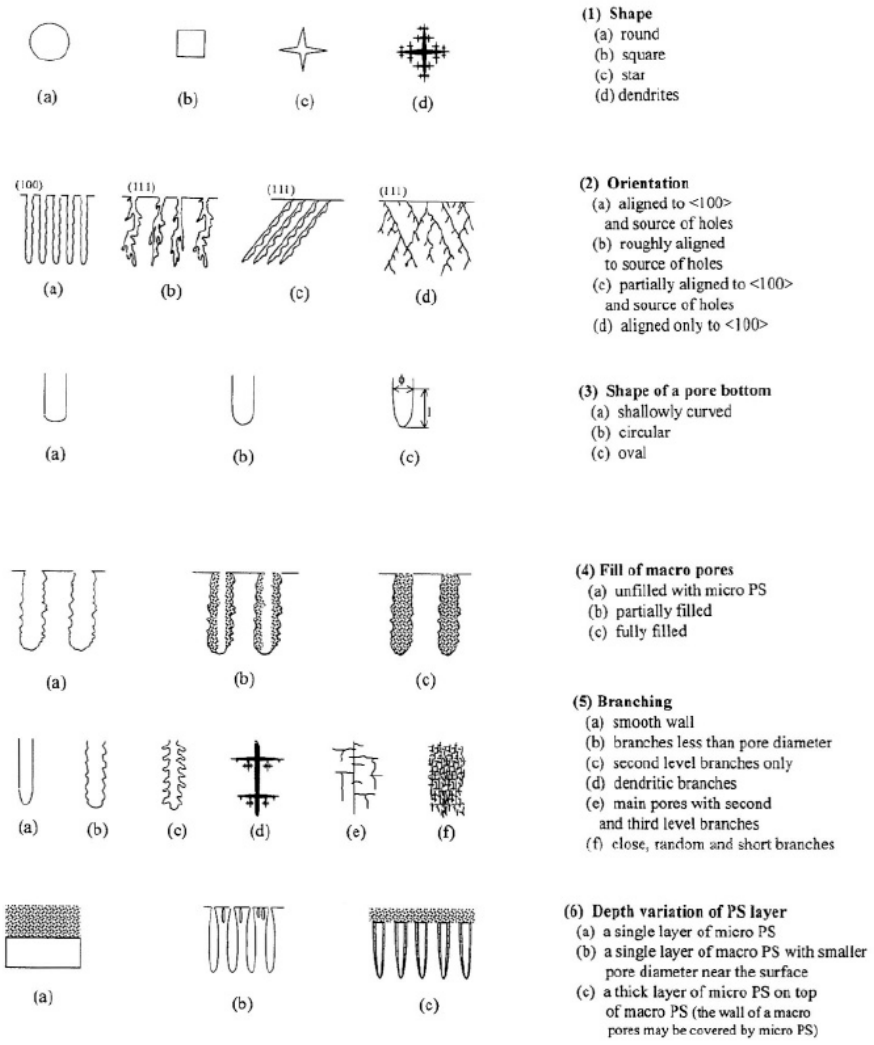


Figure 13: Schematic illustration of the morphological features of PS [15].

been modeled by Zhang: *the pore density decreases with increasing potential at low potentials due to increase of the space charge layer thickness and decrease with potential at high potentials due to the reduced wall thickness* [15]. In figure 14.(b) a summary by Lehmann [22] of pore density as a function of doping concentration is presented as reference.

2.4.3 *Pore orientation and shape*

Macropores can be classified into two categories: crystal-defined pores (crysto-pores) and current-defined pores (curro-pores). Crystal-defined pores grows along one particular crystallographic direction, while current-defined pores, grows along current lines. The orientation of primary pores (the pores initiated at the silicon surface) is, in general, in the <100> direction for all of the PS formed on (100) substrate. The

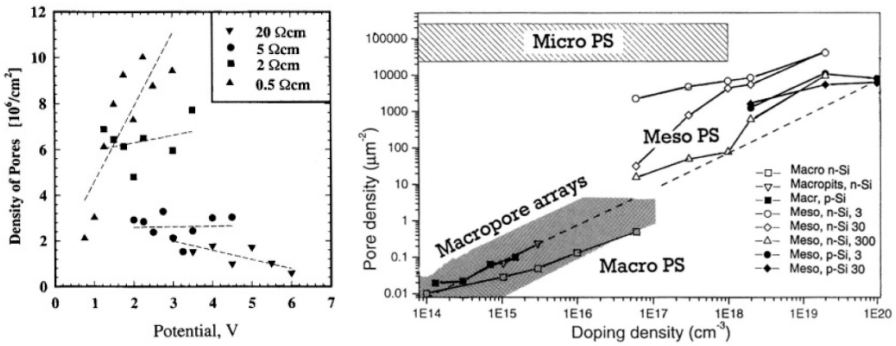


Figure 14: (a) Pore density in the stable growth phase as a function of etching potential and doping. The density of pores decreases with potential for low-doped material but increases for high-doped material [15]; (b) pore density versus silicon electrode doping density for PS layers of different size regimes [22].

dendridic pores, like the ones shown in figure 15.(a), propagate along the <100> direction even on (110) and (111) substrates [21].

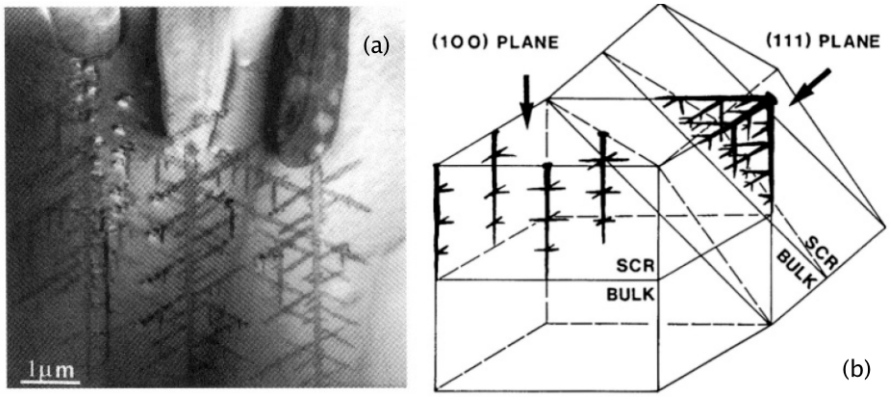


Figure 15: (a) Dendritic PS morphology formed on n-type (100) [23]; (b) Schematic illustration of the growth direction of dendritic PS in relation to the crystal orientation of the silicon sample [21].

Taking in account p-type silicon only, the macropores formed in anhydrous HF organic solutions are straight and well oriented along the <100> or <133> directions on substrates of different orientations, while those formed in solutions containing water, tend to be perpendicular to the surface (less anisotropic effect) and are poorly aligned. According to Christophersen [79], the supply of oxygen and hydrogen in the solution are important to the anisotropic growth of pores based on their current burst theory (described in the "chemistry and models" section 2.6.14); oxygen is necessary for smoothing pore tips, whereas hydrogen is the decisive factor for the anisotropic growth and passivation of macropore side walls. Large pores tend to have

less anisotropic effect and grow more dominantly in the direction of current lines, namely, perpendicular to the surface. On the other hand, for pores with extremely small diameters, on the order of few nanometers, the direction of individual pores is not well defined. The macropores formed on p-type silicon, generally, have smooth walls and an orientation toward the source of *holes*, that is (usually) perpendicular to the surface, even on (110) and (111) samples [16, 77].

The shape of the pores formed on (100) substrate is a square bounded by (011) planes with corners pointing to the <100> directions [80, 81]. The shape of individual pores formed on n-type silicon tends to change from circular to square to star-like and to dendrite-like with increasing potential [21]. Low voltages in the anodization process tends to favor circular shape and high voltage, starlike shape. Near-perfect square shape of pores can be obtained for the PS formed on n-type silicon at a certain current density, HF concentration, anodic bias, and illumination intensity. For macropores formed on lowly doped p-type silicon the shape of pores tends to be round at low current densities but tends to be square at high current densities on a (100) substrate and triangular on a (111) substrate [77]. The bottom of pores is always curved, varying from a shallowly curved semicircle to an elongated cone depending on the formation conditions; the shape of pore bottoms, in terms of the ratio of the length to the diameter, can vary from as small as 0.3 for very shallow bottoms to as large as 5 for highly elongated bottoms [15].

2.5 CHEMISTRY AND MODELS

In this section an introduction on chemistry of silicon and PS formation models is presented. When references are not explicitly stated, data are taken from Zhang's book [15], that summarizes most of the known aspects and data on PS reported in the past.

PS can be formed by anodization in solution containing HF with an anodic bias applied, or by electroless processes like stain etching or plasma discharge. In figure 16 the typical J-V curves for silicon electrodes in HF solutions are reported.

At small anodic overpotentials the current density increases exponentially with the electrode potential. As the potential is increased, current density exhibits a peak and then remains at a relatively constant value. PS grows in the exponential region up to the current peak, J_1, where electrochemical polishing occurs. The PS obtained in the non exponential region that precedes the electropolishing peak (see figure 16.(a)) does not completely cover the sample surface, and the surface coverage of PS decreases as the potential approaches the peak value. Figure 17 shows that J-V curves greatly vary with solution composition, particularly the fluorine concentration and pH value.

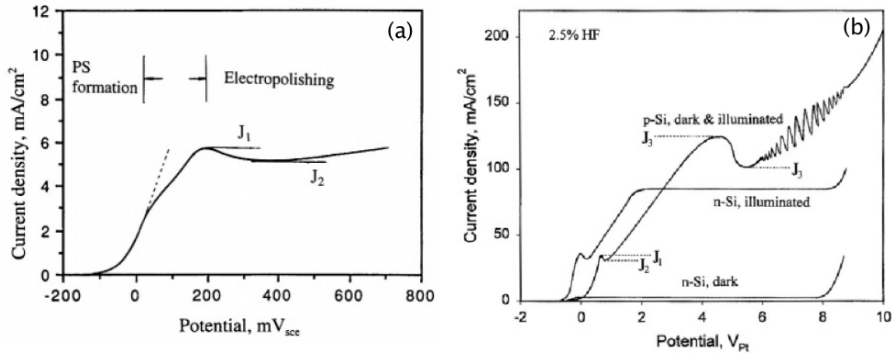


Figure 16: (a) Current-potential curves for dark and illuminated p- and n-silicon electrodes in a 2,5 wt.% HF electrolyte; (b) detailed current-potential curve for p+ silicon sample in 1% HF solution with potential sweep rate of 2 mV/s [15].

The characteristic current density values, J_1 to J_4 (in figures 16 and 17) as a function of pH and fluoride concentration are shown in figure 18.

The current increases at increasing fluoride concentrations for all pH levels and all exhibit a maximum. The plateau currents densities, i.e. J_2 and J_4, which are determined by the chemical dissolution rate of the oxide film, have been empirically fitted to pH and fluoride concentration:

$$J_2 \backsim \left\{ \left(0.1 \left[HF_2^-\right] + 0.01 \left[HF\right]\right)^{-1} + \left(10 \left[HF_2^-\right]\right)^{-1} \right\}^{-1} \tag{10}$$

$$J_4 \backsim 10 \left[HF_2^-\right] \left[H^+\right]^{0.5} \tag{11}$$

2.5.1 *Photoeffect*

This effects is important only in the formation of PS from n-type silicon and thus, is not covered in detail. Illumination with a wavelength larger than the band gap of silicon generates a photocurrent under an anodic potential on an n-type silicon electrode but has essentially no effect on p-type silicon, as would be expected from the basic theories of semiconductor electrochemistry [66]. Even if the formation of an oxide film on the surface of the sample passivates the silicon surface, so photocurrent may not be sustained, the presence of fluoride species in solutions, that continuously dissolves this film, permits that sustained photocurrent. The photocurrent value increases with increasing light intensity until it reaches a value which is twice the value in the absence of fluoride in the solution. At higher light intensities, depending on fluoride concentration, photocurrent will again decay because the rate of formation of oxide film becomes faster than the rate of its dissolution.

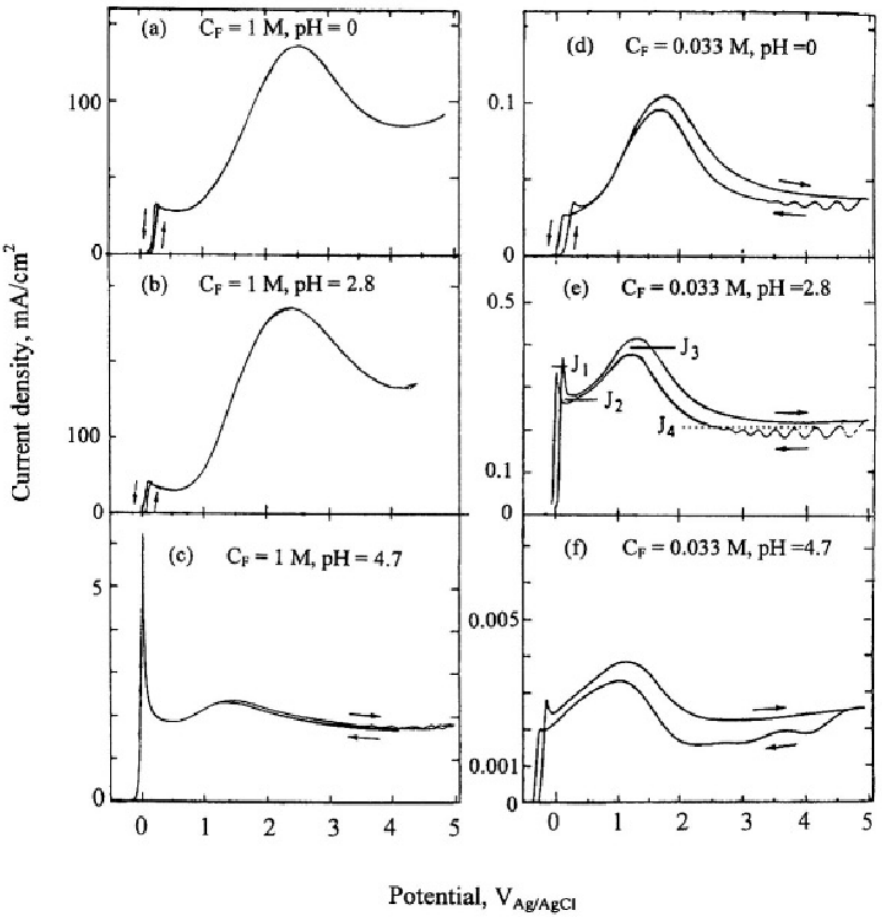


Figure 17: Voltammograms obtained for a (100)-oriented p-type silicon electrode in various electrolytes. Rotation rate 3000 rpm. Fluorine concentration of electrolyte is reported in each panel, with the pH value of the solutions. Sweep rates 100 mV/s (a,b), 10 mV/s (c), 1 mV/s (c), 1 mV/s (d), 5 mV/s (e), and 0.05mV/s (f) [15].

2.5.2 *Hydrogen evolution*

Hydrogen evolution occurs in HF solutions at anodic potentials in the exponential region. As the potential approaches the current peak, the rate of hydrogen evolution decreases, and ceases above it. Since this evolution is a reduction reaction and consumes *electrons*, it is responsible for an apparent dissolution valence smaller than 4 below the current peak. Thus, the effective dissolution valence can be used as a measure for the hydrogen efficiency. A silicon dissolution valence of 2 means 100% efficiency for hydrogen evolution, i.e., for every dissolved silicon atom one hydrogen molecule is generated. Results from rotating a ring-disk electrode indicate that the efficiency of hydrogen evolution is near 100% in the exponential region, but drops to about 50% at the first peak potential as shown in figure 19. In addition, a considerable number of hydrogen molecules, corresponding to 10% to 13% efficiency, are generated throughout the electropolish-

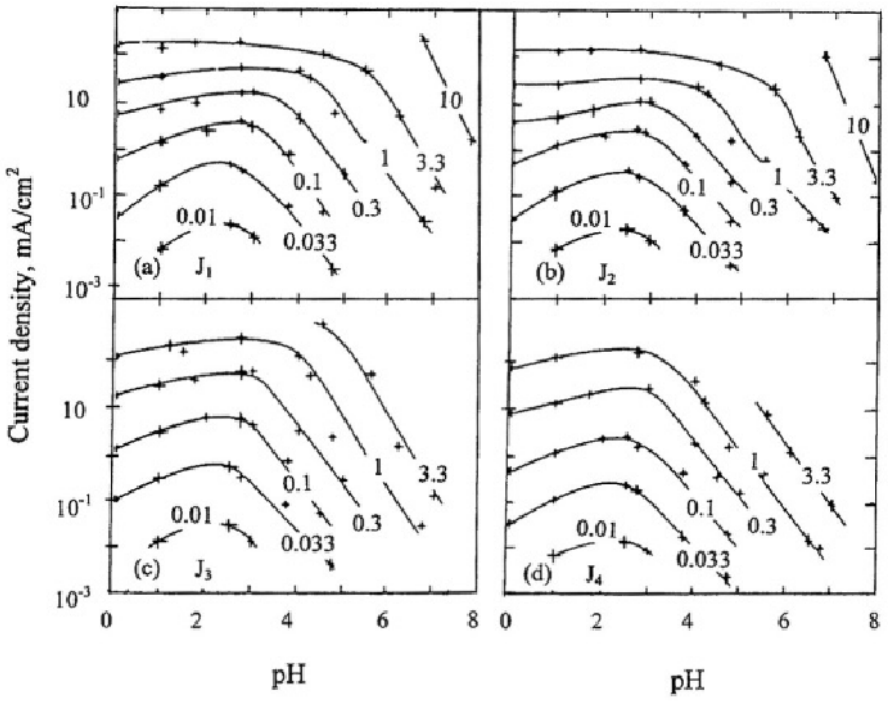


Figure 18: Plots of the characteristic current densities J_1 (a), J_2 (b), J_3 (c), and J_4 (d) as a function of pH, for different values of fluorine concentration (labeled on the curves in units of mol/liter).

ing region. An equivalent of about 10% of the silicon atoms dissolve into the solution effectively divalent at potentials up to 10 V. In the electropolishing region, silicon dissolution proceeds with oxide formation and dissolution of the oxide. An apparent dissolution valence less than 4 means that some silicon atoms are only partially oxidized in the oxide forming stage but the oxidation is completed during the dissolution stage.

Hydrogen evolution simultaneously occurs in the exponential region and its rate decreases with potential and almost ceases above the peak value. The existence of these different regions are similar for other fluoride-containing solutions of various compositions and pH values.

2.5.3 *Electropolishing*

As said, for low current densities and high electrolyte concentrations pores are formed. Increasing the current density over a threshold value, which decreases with the increasing of HF concentration in the electrolyte , results in electropolishing. This means the silicon surface is etched layer by layer and remains essentially flat. No hydrogen evolution has been observed during electropolishing. The overall reaction is:

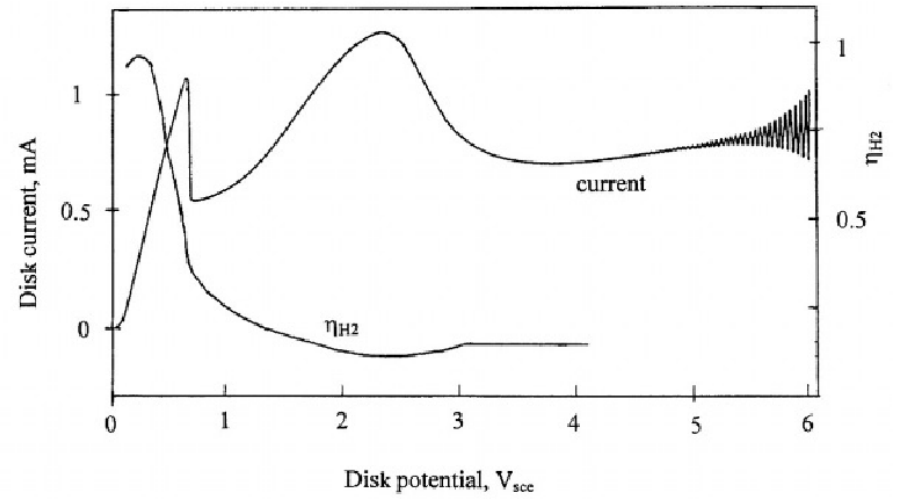


Figure 19: The I-V curve and efficiency for hydrogen evolution η_{H2} during positive sweep of a p-type silicon (100) disk in 0.3 mol dm^{-3} NH_4F at pH 3.5 [24].

$$Si + 6HF + 4h^+ \rightleftharpoons SiF_6^{2-} + 6H^+ \tag{12}$$

Being consumed 4 *holes* the valence in the dissolution of silicon is 4. All charges needed to oxidize the silicon atom are delivered by the electrical current and there is no hydrogen formation [82]. This process can be used to etch silicon layers of several microns maintaining the surface of silicon flat.

2.5.4 *Growth rate*

The growth rate of PS depends on the concentration of HF in the electrolyte, the current density, and silicon doping. The growth rate of pores, increases linearly with HF concentration in p-type silicon and non-linearly in n-type as shown in figure 20 (the n-type plot has log-log scale). Linear growth with current density is verified for p-type electrodes, whereas a saturation appears for n-type (figure 21.(a)).

Growth rate dependence on doping of silicon wafer is shown in figure 21.(b). A linear dependence with the logarithmic dopant concentration is found for p-type. The dependence for n-type electrode is more complicated. In general, it is verified that, under identical conditions, PS formed on n-type silicon has a higher growth rate than that on p-type silicon. The temperature of HF solutions is found to have little influence on the growth rate of PS [37].

2.5.5 *Electrolytes*

The composition of the electrolyte is one of the key factors for PS growth. Porous silicon on p-type silicon can be formed either in or-

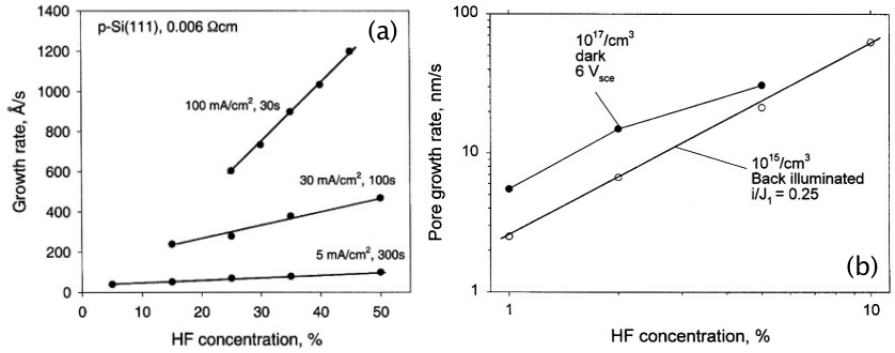


Figure 20: Growth rate of pores as a function of HF concentration: (a) p-type silicon [25], (b) n-type silicon [26].

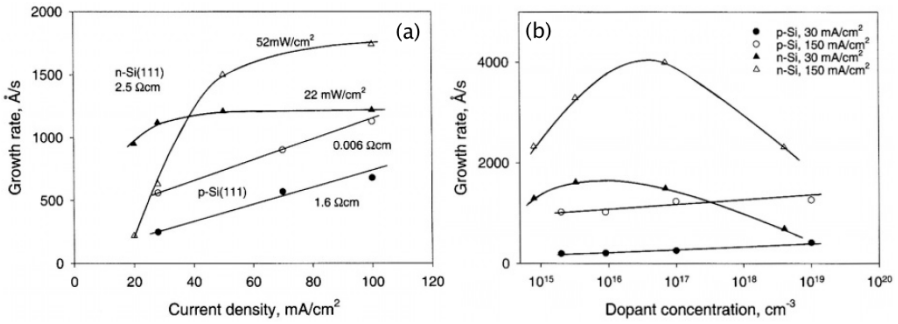


Figure 21: Growth rate of pores as: (a) function of the anodization current density, (b) doping concentration of silicon electrode. [25].

ganic or aqueous electrolytes. Aqueous electrolytes derives from the $HF - H_2O$ system, and includes mixtures of HF with water, as well fluorine bearing salts (e.g. NH_4F) dissolved in H_2O. It is common to add ethanol (C_2H_4OH) and/or acetic acid (C_2HOH) to the solution to reduce the surface tension, adjust the pH value or the viscosity. The nominal concentration of fluorine atoms may range from 0.001 to 49%. The aforementioned electrolytes have in common a "PSL-peak" (a peak in j_{PSL}, see figure 22) in the J-V characteristics and that they are rather strongly oxidizing, i.e. tend to form SiO_2.

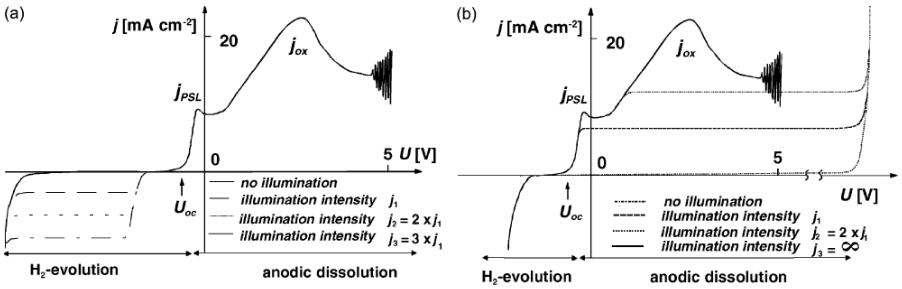


Figure 22: Representative J-V characteristics for aqueous electrolytes: (a) p-type silicon, (b) n-type silicon [27].

The organic electrolytes are solutions of HF (always including some water from stock solution) and an organic solvent as Acetonitrile (MeCN), Dimethylformamide (DMF), and Dimethyl Sulfoxide (DMSO). The "organic" name can create confusion as they would include HF/Ethanol (EtOH) electrolytes, because ethanol is an organic compound, but such electrolytes are considered aqueous. The correct way to classify an electrolyte "organic" (or not) is to analyze their J-V characteristics for the presence of a PSL-peak: organic electrolytes have in common that their J-V characteristics do not show a PSL-peak. The absence of this peak signals that formation models tied to the current density j_{PSL} (or j_1 as it has been referred on some texts) found limited application.

The "aqueous" and "organic" electrolytes constitutes the two major systems for PS growth but they are not the only available, there are other two kind of electrolytes with rather limited applicability: oxidizing and mixed.

Oxidizing electrolytes are solutions that contains strong oxidizing agents without F^- ions. They oxide the silicon and, since there is no oxide etch compound, the resistivity of the surface raises. Pure oxidizing electrolytes have only limited applications, mainly in anodic oxidation of porous silicon (a subject that will not be discussed here).

The other system, "mixed electrolytes", is a potentially large group of electrolytes that contains everything not contained in the sets defined above, but so far not much practical significance has emerged. Examples that can be found in the literature include H_3PO_4 (by itself an "oxidizing" electrolyte) with a dash of HF, absolutely water free organic electrolytes, or diluted HF with some CrO_4 [27].

2.5.5.1 *Organic Electrolytes*

In figure 23 are listed the major organic compounds used so far with some of their properties. The numbers in the entry "oxidizing power", are expressed in arbitrary units (a.u.) and are related to the slope of the voltage curves obtained during anodic oxide formation (with a constant current density and for a 4 wt.% addition).

It is important to make clear that HF based solutions always contain some water coming from the stock HF solution that is 48-50 wt.% (in water). The following considerations, from Föll et al.[27], applies:

- The doping of the silicon is rather important. Increasing the doping level acts to some extent like increasing the applied potential. In general, higher doping levels reduce the ability to form macropores. Viewed relative to aqueous electrolytes, the switch-over to mesopores occurs already at lower doping levels.

- The macropores on p-type silicon produced with organic solutions tend to become more "perfect" if the oxidizing power

Organic electrolytes used in Si electrochemistry and some of their major properties

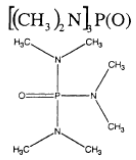
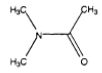
Symbol	Formula name	Polarity (DK)	Oxidizing power
MeCN	 Acetonitrile	6.2	Very weak; slope of anodic oxide, 0 a.u.
DMF	 Dimethylformamide	6.4	Slightly oxidizing, 0.5 a.u.
FA	 Formamide	7.3	Strong, 3.5 a.u.
DMSO	 Dimethylsulfoxide	6.5	Mild oxidizing, 2.5 a.u.
HMPA	 Hexamethylphosphoric triamide	6.6	Oxidizing, 6.5 a.u.
DMA	 Dimethylacetamide	6.3	Mild oxidizing, 2.1 a.u.

Figure 23: Table of principal organic electrolytes used for growing porous silicon[27].

of the electrolyte is not too small. Electrolytes with little oxidizing power as, e.g. MeCN, will hardly produce macropores at all, whereas electrolytes with strong oxidizing power (e.g. Formamide (FA), comparable to H_2O or stronger) produce micropores instead of macropores.

- Stable growth to considerable depth also requires the availability of hydrogen or, more precisely, it is related to the "passivation power" of the electrolyte in the context of the Current Burst Model (CBM) (see section 2.6.14). "Passivation power", like oxidizing power, is not a property of standard chemistry but has nonetheless a well defined meaning: it denotes the degree to which a given electrolyte can remove interface states in the band-gap of silicon by covering a freshly etched surface with hydrogen. This is a measurable quantity in principle but, while preliminary measurements based on the Electrolytical Metal Tracer (ELYMAT) technique have been made, no reliable data exist at present. The following remarks are either based on circumstantial evidence or may be taken as predictions. It is therefore of importance whether the electrolyte is protic or aprotic (i.e. donates or accepts hydrogen) and, of course, the pH value may be involved, but might not always be of prime importance. In the CBM, hydrogen passivation is the major process responsible for pore formation and it has been shown that additions of protic

substances to an organic electrolyte change the pore growth in the expected way.

- The dielectric constant of the electrolyte must be considered. Essentially, the dielectric constant determines to which degree HF will be fully dissociated and thus "active". Electrolytes with a low dielectric constant tend to have a reduced HF "activity" which slows down both direct dissolution and oxide dissolution.

- The conductivity of the electrolyte is of course of considerable importance, too. It would be too naive to assume that the resistance of the electrolyte can be easily compensated for by increasing the voltage, because diffusion of species in the electrolyte can lead to phenomena similar to the diffusion of *holes* in the semiconductor and therefore introduce instabilities that cause, modify or interfere with pore formation.

- Temperature, circulation of the electrolyte, small additions of surfaces reactant, or bubbling with N_2 to remove oxygen dissolved from the air, may also be of importance.

- The nucleation of macropores on p-type silicon produced with organic solutions can be achieved by supplying pre-structured nuclei as in the case of macropores on n-type silicon produced with back side illuminated solutions, but not many investigations have used this technique. Homogeneous random nucleation, on the other hand, can be rather difficult and may only occur after a certain period of larger voltages intentionally supplied for the nucleation phase or automatically employed by the potentiostat if galvanic conditions are used.

- The orientation dependence of macropores on p-type silicon produced with organic solutions is similar to that of macropores on n-type silicon produced with aqueous solutions, but often not quite as pronounced because the pores are often not well defined.

While the limitations with respect to pore geometries and morphologies are not known at present, recent experiments following the guide lines from above, and some rules derived from the CBM, demonstrate that $(0.2\ \mu m \times 0.4\ \mu m)/0.2\ \mu m$ pitches are possible, but never achieved with macropores on n-type silicon produced with back side illuminated solutions. The pores have rough walls, demonstrating the need of fine tuning any process that is to deliver "perfect" pores.
The series of considerations written above above has been deduced from the measurements shown in figure 24 and figure 25.
It's important to remove all traces of O_2 by bubbling the electrolyte with N_2 before use. Föll et al. had estimated DMSO and **DMA!** (DMA!)

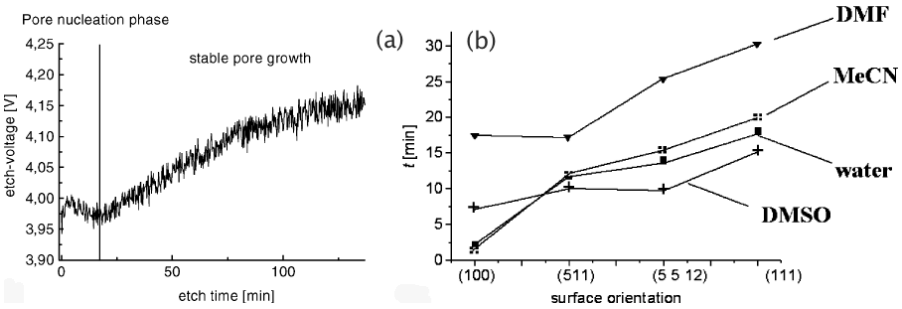


Figure 24: Nucleation time of macropores: (a) Development of the voltage over time for constant current and a DMF electrolyte. A nucleation phase and a stable growth phase can always be identified. (b) Nucleation time for various electrolytes and surface orientations [27].

produce the most perfect p-type silicon produced with organic solutions [27]. Figure 26 shows the morphology that can be obtained with optimized electrolyte and etching conditions.

2.5.5.2 *Aqueous electrolytes*

With electrolytes containing a large concentration of HF (often 49 wt.% HF mixed with an equal volume of ethanol), and at current densities close to the j_{PSL} value of the system, micro-PS is usually produced; macropores on p-type silicon produced with aqueous solutions are formed at current densities much lower than j_{PSL} and for medium to low HF concentrations. Figure 27 shows some representative morphologies. The macropores on p-type silicon produced with aqueous solutions occupy a defined region in the parameter space defined by the HF concentration (indicated with [HF]) and the current density. While there is a general agreement in the literature that [HF] determines j_{PSL} (although, no doubt, the nature of the additives will play a minor role, too), there are few and seemingly contradictive quantitative data. Lehmann [26] reported an exponential relationship of j_{PSL} on [HF], while van den Meerakker et al. [28] found a linear dependence. The actual data, however, if plotted in the same diagram, are reconcilable with the one shown in figure 28.

A concise summary of the general properties of macropores on p-type silicon grown with aqueous solutions, according to Föll [27] is:

- Macropores on p-type silicon produced with aqueous solutions are rather easily obtained for [HF] < 15 wt.% and $j < 0.05\, j_{PSL}$ if nucleation is provided for, e.g. by KOH etch pits.
- Without pre-defined nucleation (etch pits), an extensive nucleation period may be necessary.

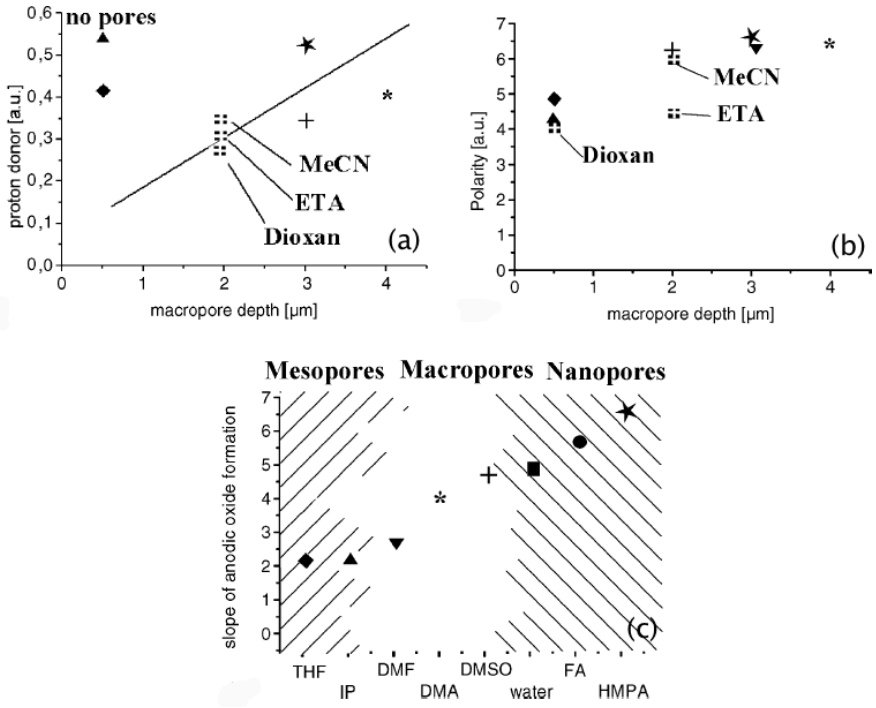


Figure 25: Various correlations between macropores (on p substrate, organic electrolyte) properties and electrolyte properties: (a) Dependence of macropores (on p substrate, organic electrolyte) depth on the ability to donate protons of the electrolytes [22]. (b) Polarity of organic electrolytes (scales with the value of the dielectric constant or index of refraction). (c) Correlation of the oxidizing power and pore formation for various organic electrolytes (and H_2O for comparison) [27].

- The walls between macropores on p-type silicon produced with aqueous solutions are always rather thin (corresponding to twice the SCR width).
- Lehmann's formula (Lehmann proposed a formula that related the cross-sectional area of the pore $A_{PO} \approx d^2$, with w diameter of the pore, to the area $A_{cell} = a^2$, with a lattice constant, of a unit cell of the pore lattice and to the current density j via: $\frac{A_{cell}}{A_{PO}} = \left(\frac{w}{a}\right)^2 = \frac{j}{j_{PSL}}$ [27]) does not apply: there is no defined relation between variables; pores with predefined nucleation always grow in diameter until they almost touch each other.
- Pores with large diameters obtained in this way, tend to have "cloudy" tip shapes figure 27.(b).
- Randomly nucleated macropores on p-type silicon produced with aqueous solutions, while still keeping pore wall dimensions small, have well defined average diameters with smooth tips and walls figure 27.(a).

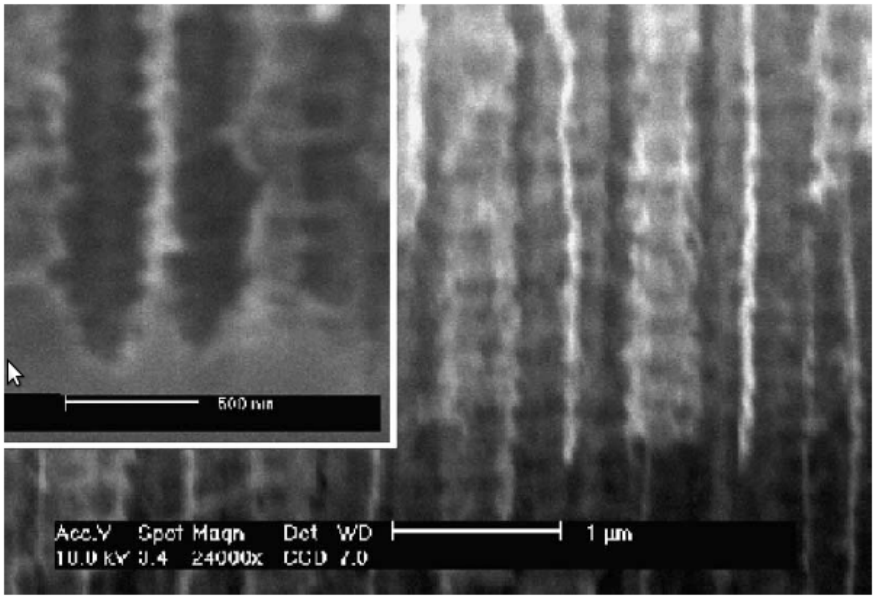


Figure 26: First 200 *nm* macropores obtained by optimized organic electrolytes and etching conditions (the smallest pitch is perpendicular to the cleavage plane) [27].

- Not much is known about the orientation dependence of macro-PS produced with aqueous solutions; but it appears to be similar to that of p-type silicon produced with organic solutions obtained from electrolytes with small oxidizing power. In particular, macropores produced with aqueous solutions from (111) p-type silicon, are practically indistinguishable from the one produced with organic solutions with MeCN as electrolyte.

2.5.6 *Pore size regime and Pore Growth Rates*

The growth rate r_P of a pore has been defined [17] as the increase in length dl divided by the required etch time dt. For a constant pore etching current and negligible diffusion gradients, the pore the growth rate becomes constant and can be calculated using the total pore length l and total etching time t.

$$r_P = l/t \tag{13}$$

Straight pores growing orthogonal to the electrode surface and forming a flat interface to the bulk are only a special case. For these pores l becomes equivalent to the layer thickness D. The growth rate of the whole porous layer, r_{PS}, depends of several parameters such as substrate doping density, crystal orientation, HF concentration, current density and temperature. The evidence of the dependence on crystal orientation is in figure 29.

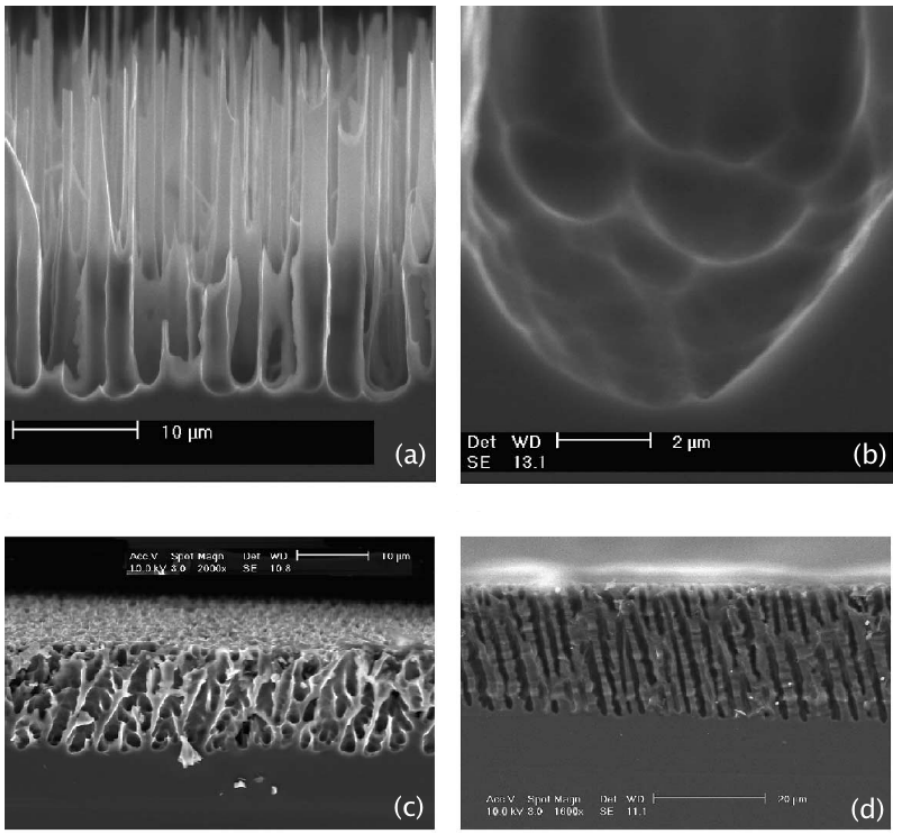


Figure 27: Some samples of macro-PS produced with aqueous solutions: (a) 10 Ωcm; 7% HF, j = 20 mA/cm^2, j_{PSL} = 90 mA/cm^2, random nucleation; (b) as (a), but induced nucleation (hexagonal lattice, a = 3 mm); (c) 10 Ωcm; 10% HF, j = 2 mA/cm^2, j_{PSL} = 150 mA/cm^2, random nucleation on (5, 5, 12) sample; (d) p-type silicon produced with organic solutions with MeCN (4 wt.% HF) on (111) for comparison with (c)[27].

The cleaved edge of a highly doped n-type silicon sample shows that the meso-PS growth rate is increased on (100) surfaces by a factor of about 1.5 compared to (110) surfaces. This orientation effect is not observed for micro-PS grown on a moderately doped p-type substrate. In this case, however, current density variations caused by the edge geometry produce inhomogeneities in PS layer thickness.

The pore growth rate is found to show an absolute maximum along the <100> direction. For the case of macropores a second relative maximum along the <311> direction has been observed [83]. For other substrate orientations the pores do not grow orthogonal to the electrode surface. In this case the growth rate of an individual pore r_P equals $r_{PS}/cos\alpha$, with α being the angle between pore direction and the vector normal to the surface plane. The dependence of r_{PS} on substrate orientation is shown in 30.(a).

Another interesting study Lehmann made, is the growth rate as a function of anodization current density for different PS structures

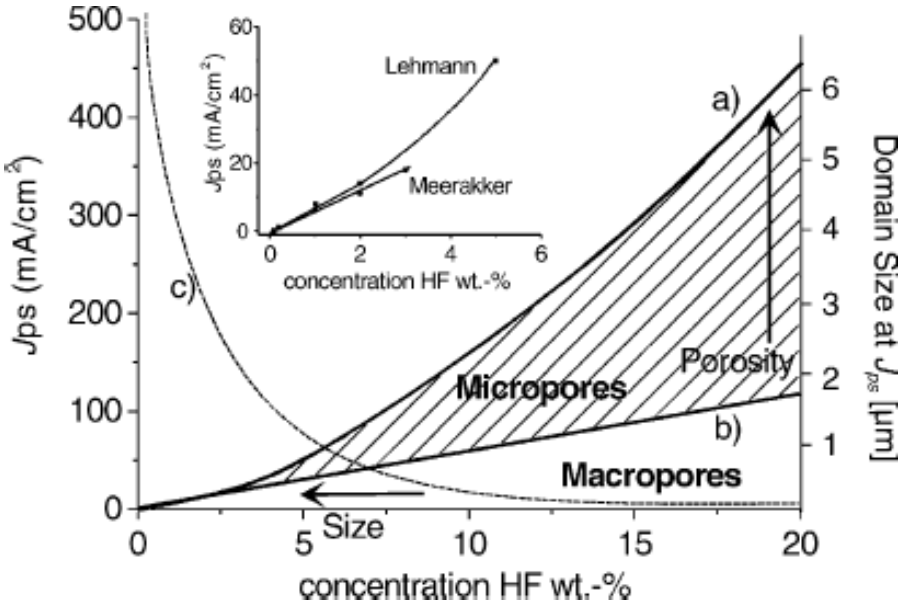


Figure 28: Parameter space for micro- and macro-PS produced with aqueous solutions. Curve (a) shows j_{PSL} as described by the Lehmann [26] model and curve (b) as described by van den Meerakker [28]. Curve (c) describes the size of a CB domain. The regions for macropore and micropore-growth are a result of a semi quantitative consideration of the CBM and may be considered as a prediction. The inset shows measured data taken from [28, 26] for low HF concentrations [27].

prepared in the same electrolyte, as shown in figure 30.(b). For p-type substrates r_{PS} shows a maximum for doping densities between 10^{18} and $10^{19} cm^{-3}$.

The PS layer thickness may show fluctuations over the electrode area on different length scales. The thickness variations may originate from a waviness of the bulk-PS interface, or the electrolyte-PS interface (usually due to a dissolution of PS during anodization or a collapse of the PS microstructure due to capillary forces during drying). A roughness on the millimeter scale is observed for micro, meso- and macro-PS if the HF concentration or temperature varies over the interface. HF concentration variations may be caused by inhomogeneous electrolyte convection at the electrolyte-electrode interface; another common cause are bubbles that stick to the electrode surface. A lateral variation of the anodization current will produce different growth rates and consequently an interface roughness for porous layers (except for macro-PS on n-type silicon). An inhomogeneous current distribution at the O-ring seal of an anodization cell or at masked substrates produces PS layer thickness variations figure 31; these inhomogeneities become more pronounced for low doped substrates.

A PS-bulk-interface roughness on the micro scale is found to develop for meso- and micro-PS layers with increasing PS thickness. This roughness especially impairs reflectivity measurements and the man-

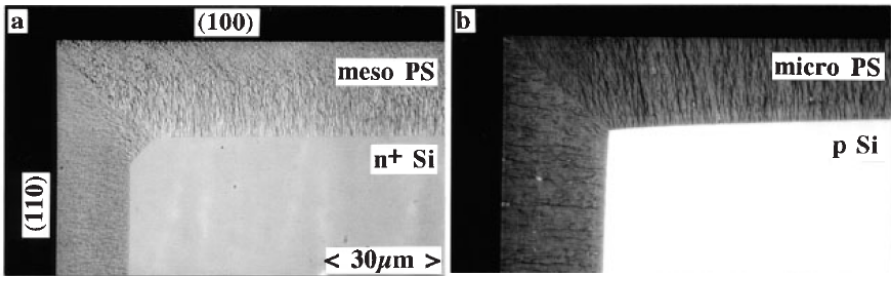


Figure 29: Optical micrographs of edges of cleaved silicon wafers showing different crystal planes anodized at 100 mA/cm^2 in ethanoic HF (1:1). (a) The growth rate of meso-PS formed on a highly doped n-type silicon substrate ($2 \times 10^{18} cm^{-3}$, 2 min) shows a clear dependence on crystal orientation. (b) An orientation dependence is not observed for micro-PS formed on moderately doped p-type samples ($1.5 \times 10^{16} cm^{-3}$, 4 min) but the PS thickness becomes inhomogeneous because of local variations in the current density caused by the edge geometry [17].

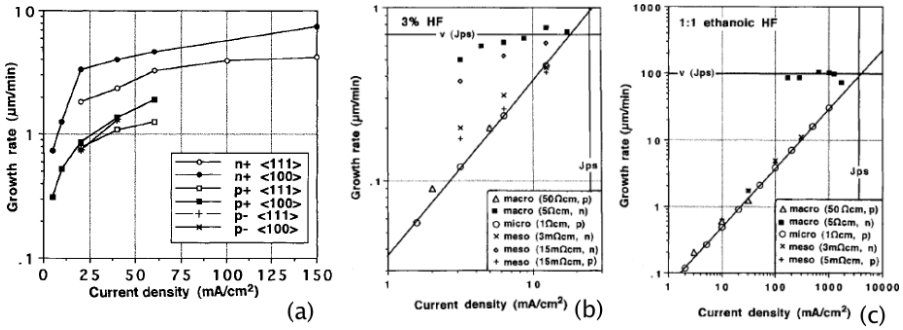


Figure 30: (a) Dependence of pore growth rates on crystal orientations of the substrate for different substrate doping densities and applied current densities (in HF : H_2O : EtOH, 2:5:1), b) Pore growth rates in (a) 3% aqueous HF and (b) ethanoic HF for different types of substrate doping and doping densities, as indicated. Note that high growth rates are observed for low and moderately doped n-type substrates [17].

ufacture of optical superstructures. The roughness frequency shows no strong dependence on doping density, while the amplitude increases from a few nm for degenerately doped material to several tens of nanometers for low doped substrates [17].

2.5.7 *Investigation on chemical composition*

Infrared (IR) spectroscopy has been used for investigate the chemical composition of PS. It's a useful tool because it can be used *in situ*, avoiding oxidation, absorption of hydrocarbons, etc. The analysis of bulk silicon surfaces in dilute HF solutions has revealed that the silicon surface is terminated with hydrogen. Hydrogen-associated silicon fluorides, such as SiH_2 (SiF), $SiHF_3$ and SiH_2F_2, expected from

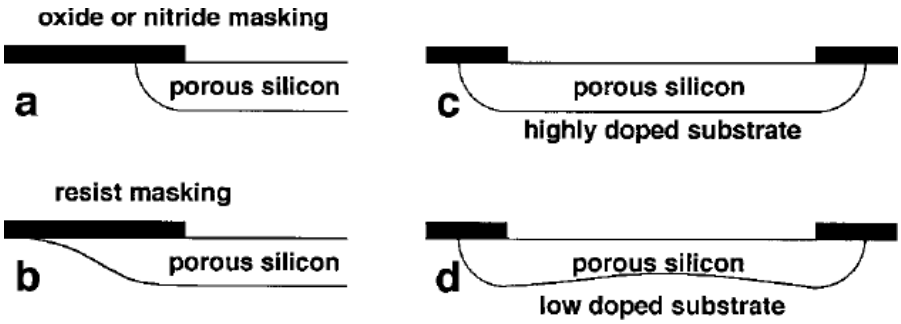


Figure 31: PS layer thickness inhomogeneities as a result of different kinds of masking layers and doping densities. (a) While under-etching is minimal for a silicon nitride mask, (b) a resist mask shows severe under-etching. (c) On substrates of low resistivity the etch profile is isotropic, (d) while the PS thickness increases towards the edges of the pattern for high substrate resistivities [17].

the dissolution reaction as shown in figure 32, have not been detected by spectroscopy. If they exist, their lifetime should be shorter than 0.3 ms. The total fluorine concentration in PS has been found to be usually below 1% and below the detection limit after a short DI water rinse. In the latter case only the $Si-H$, the $Si-H_2$ and the $Si-H_3$ vibrational modes have been observed and no $Si-O$ surface species is detectable. The same is basically true for PS if it is formed in aqueous HF: no oxygen is detectable in electrochemically formed PS during, or right after, the preparation. Only in very dilute solutions ([HF] < 0.1 M) are submonolayer oxide films found to be present at the porous-bulk interface during formation at current densities well below J_{PS}. The PS stoichiometry is reported to be between SiH and SiH_2. These results for electrochemically formed PS are in contrast to PS formed chemically in an $HF-HNO_3$ solution. In this case the composition is reported to be between H_2SiO and $HSiO_{1.5}$. Significant oxygen incorporation is also observed for PS formed by anodization in HF under Ultraviolet (UV) illumination, while addition of H_2O_2 to the HF electrolyte showed no increase in the oxygen content of PS.

On storage in ambient air or immersion in H_2O_2 the $Si-O-Si$ vibrational mode becomes detectable for electrochemically formed PS, without a significant change in the number of $Si-H_x$ bonds, as shown in figure 33. This supports the assumption that oxygen penetrates the silicon lattice and breaks the backbonds of the $Si-H$ surface groups, as observed for native oxidation of bulk silicon surfaces. The oxidation at ambient conditions is accompanied by a desorption of traces of SiH_4 from the surface. An investigation of the reaction of atomic hydrogen with hydrogenated PS revealed that trihydride is the surface precursor of SiH_4. As far as the etch rate in atomic hydrogen is concerned (30 nm/min, 10 *mTorr*, RT), the inner PS surface still behaves like the single crystal silicon surface.

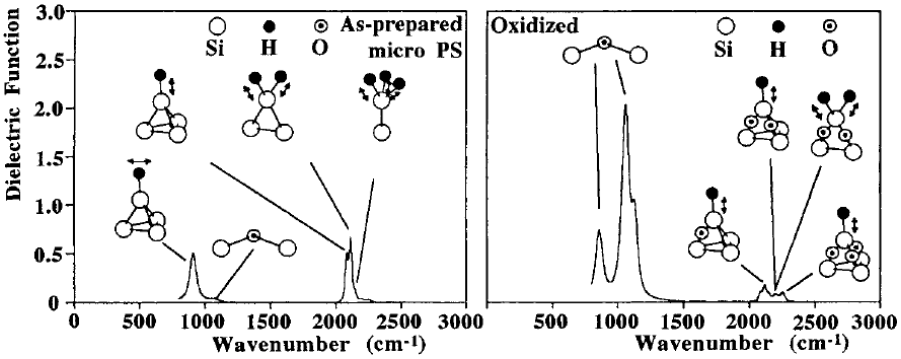


Figure 32: Characteristic dielectric functions (imaginary part), as observed by IR spectroscopy for the solid component of as-prepared PS (left) and an oxidized sample (right), with the most important vibrational modes assigned as indicated [17].

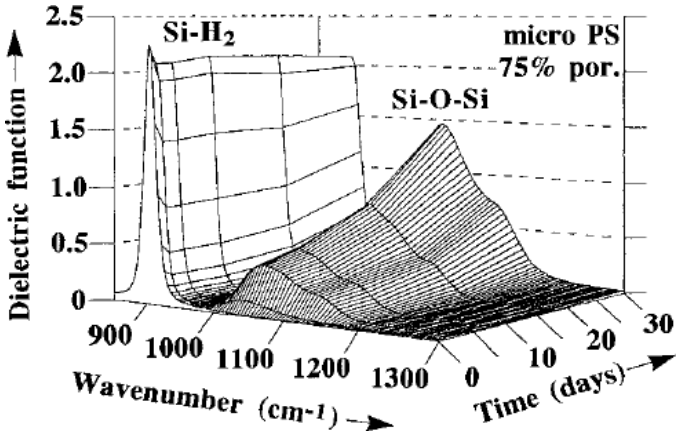


Figure 33: The increase in the $Si-O-Si$ vibrational modes (980-1200 cm^{-1}) upon storage of a high porosity (75%) micro-PS layer formed on a p-type substrate (0.2 cm) in ambient air. The $Si-H_2$ scissors mode (905 cm^{-1}) shows little time dependence [29].

PS attracts organic matter from the ambient atmosphere. The hydrocarbon coverage may be in the order of a monolayer, which leads to C/Si atom ratios as high as 1. Upon longer storage in ambient air at RT the hydrogen-passivated surface of PS gradually converts to a heavily hydrocarbon-contaminated native oxide (this process is often called aging) [17].

2.6 FORMATION MODELS

This section introduces some models of pore formation presented in literature. Its purpose is to provide an instrument to predict how PS formation and morphology can be controlled with process parameters.

2.6.1 *Discovery of PS and first model proposed*

Uhlir and Turner reported in the late 1950s a solid surface formed during dissolution of p-type silicon in aqueous HF solution below a critical current (J_1). The film created was amorphous and contained fluoride, so Turner suggested that the film could be a subfluoride $(SiF_2)_x$ grown on the surface during the anodic dissolution of silicon. In the mid-1960s, this film was found to consist mainly of polymerized silicon hydrides [36, 84, 37].

Based on these data, Memming and Schwandt [85] proposed that the solid film that formed on the silicon surface during anodic dissolution was a dissolution/precipitation product resulting from a two-step disproportionation reaction:

$$Si + 2HF + 2h \longrightarrow SiF_2 + 2H^+ + (2 - \lambda)e \tag{14}$$

$$2SiF_2 \longrightarrow Si^0_{amorphous} + SiF_4 \tag{15}$$

2.6.2 *Barrier Breakdown Model*

Meek [86, 87], based on I-V curve and capacitance measurements, proposed that the large current observed on n-type silicon, at an anodic potential, in the dark is due to barrier breakdown. The breakdown is not due to a bulk mechanism but rather to interface tunneling from the states at the surface into the conduction band. Also, the breakdown is not uniform but localized, causing the formation of the etch pits and tunnels.

Theunissen [88] found the possibility to etch deep tunnels in the dark on n-type silicon, and discovered that the resulting layer was a single crystal; thus he concluded that the solid layer formed during anodization is the remaining substrate silicon left after anodic dissolution. Channels have a rich texture that depends on formation conditions. The formation of channels is not related to crystal defects and the direction of the channels depends on the orientation of the substrate. The local breakdown of the depletion layer inside the silicon was postulated to be responsible for the formation of channels. The breakdown of the barrier layer occurs when the maximum field at the silicon/electrolyte interface is larger than the critical breakdown field.

2.6.3 *Depletion Layer*

The first model realized by analyzing the anodic I-V relations and correlating them with the current conduction mechanisms associated with silicon substrates, was proposed by Beale [89]. PS has a very high

resistivity and the spacing between pores is less than the width of the depletion layer; Beale proposed that silicon in PS is depleted of carriers and that depletion layer is the cause of the current localization at pore tips, where the field is intensified. This intensification of field is attributed to the small radius of curvature at the pore tips. For lowly doped p-type silicon the charge transfer is by thermionic emission and the small radius of curvature reduces the height of the Schottky barrier and thus increases the current density at the pore tips. Instead for heavily doped silicon the current flow is due to a tunneling effect depending of the width of the depletion layer. In this case the small radius of curvature results in a decrease of the width of the depletion layer and increases the current density at pore tips. The initiation was considered to be associated with the surface inhomogeneities, which provide the initial localized high current density at small surface depressions.

Concepts of this model would be adopted and developed in many of the later models, such as those by Föll, Zhang and Lehmann. The model considered only physical aspects and none of the chemical reactions, providing little insight morphological features related to current and HF concentration. Also, Beale's model assumed that the Fermi level of the semiconductor is pinned on the surface on the midgap which does not agree with the later experimental data.

2.6.4 *Independence of the electronic properties*

Zhang [90] in the late 1980s concluded, after studies on I-V curves for different silicon types and doping concentrations, current densities, and other parameters, that the condition for PS formation or electropolishing to occur, is largely independent of the electronic properties of silicon, such as doping type and concentration. It's the nature of chemical reactions that is responsible for the occurrence of the different regions. *The transition from PS formation to electropolishing was postulated to result from the two competing reactions: direct dissolution of silicon through reaction with fluoride species, and indirect dissolution through oxide formation and dissolution.* This hypothesis has been adopted in many of the later models on the formation mechanisms of PS [17].

2.6.5 *Carrier diffusion model*

Near the end of the 1980s Smith [91, 81, 92] proposed a model to describe the morphology of PS based on the hypothesis that the rate of pore growth is limited by diffusion of *holes* from the bulk of the silicon to the growing pore tip. In that model the pore structure is determined by the intrinsic nature of the random walk and the magnitude of the diffusion length. A *hole* randomly walking toward the growing

pore tips is more likely to contact those pores that are nearest to it. In this model the outer tips of pores have the highest probability of *hole* capture and growth. According to this model, the features of PS morphology are essentially determined by the hole diffusion length, which is a function of potential and dopant concentration. The interpore spacing is then on the order of two diffusion lengths. The PS density decreases with decreasing diffusion length along with an increasingly interconnected porous structure. To account for the variation in pore diameter and the transition from PS formation to electropolishing a sticking factor was introduced. A *hole* needs to hit and stick to the surface to promote a reaction at the active site. The pore tip was considered to be oxidized to a varying degree depending on the anodization conditions. The sticking factor is different along the surface of a pore tip which is partially covered with an oxide. When conditions are such that the sticking probability is much higher at the edge of the tip than in the middle, the dissolution process tends to result in electropolishing rather than PS formation.

Zhang moves some critiques to this model: it simulated some of the morphological features of PS, but it was too general to account for the different current conduction mechanisms for different types of silicon substrates. For example, for n-type silicon in the dark, the current is by electron injection into the conduction band from the surface, which cannot be explained by the carrier diffusion model. Also, there is no physical foundation for the sticking factor of carrier to the surface. Furthermore, the model did not consider the nature of the electrochemical reactions at the interface, which must be an important part of the formation mechanism [15].

2.6.6 *Quantum confinement model*

In 1990 Lehmann and Gösele [30] postulated that formation of PS on non degenerated p-type silicon is a self-adjusting process due to a geometrical quantum well or wire effect associated with the thin silicon walls remaining between the pores.

The model starts from the dissolution chemistry of silicon at anodic bias in HF. Silicon surface is virtually inert against attack of HF at low pH values. Under anodic bias, PS is formed as long as the reaction is limited by the charge supply of the electrode and not by ionic diffusion in the electrolyte. This condition is fulfilled for current densities below a critical current density j_{PSL} (dependent from the HF concentration) , as described before. The inner surface of PS become passivated with hydrogen. From this facts, and from charge transfer ratios at silicon electrodes in HF, the model in figure 34 was derived.

It is essential, in this model, that hydrogen-passivated silicon surface is virtually inert against further attack of fluorine ions as long as no electronic *holes* are available at the silicon electrode because the

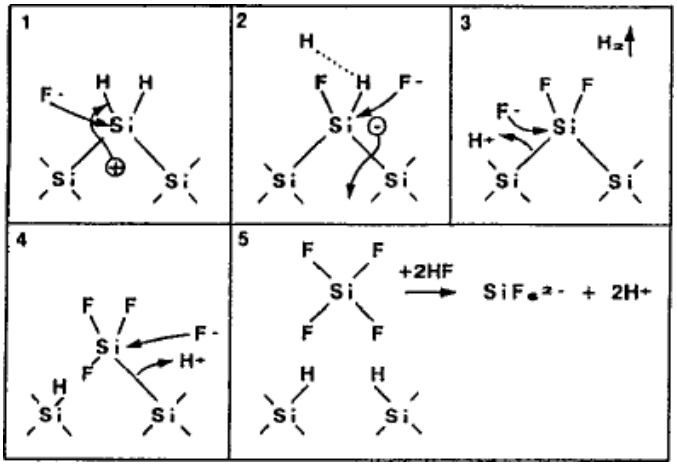


Figure 34: Proposed dissolution mechanism of silicon electrodes in HF associated with porous silicon formation. (l)-(5) indicate the sequence of reaction steps involving F, H, Si, *holes*, and *electrons* [30].

electronegativity of H is about that of Si and the induced polarization is low. The model is based on a five steps mechanism (with reference to figure 34):

1. Step 1: a *hole* reaches the surface, nucleophilic attack on Si-H bonds by fluoride ions can occur and, a Si-F bond is established.

2. Step 2: due to the polarizing influence of the bonded F, a second F^- ion bonds to the same site, injecting an *electron* in the electrode.

3. Step 3: hydrogen evolution occurs at the electrode an H_2, a third fluorine ion reaches the site and bonds.

4. Step 4, 5: due to the polarization induced by the Si-F groups, the electron density of the Si-Si backbonds is lowered and these weakened bonds will now be attacked by HF (or H_2O) leaving the silicon surface atoms passivated by hydrogen.

If a silicon atom is removed from an atomically flat surface by this reaction, an atomic size dip remains. This change in surface geometry will change the electric field distribution in such a way that hole transfer occurs at this location preferentially. Therefore, surface inhomogeneities are amplified. If the walls between the pores are depleted of *holes* they will be protected against dissolution. The condition of total depletion of the walls between the channels is that the thickest parts are smaller than two times the space-charge width W. If minority carriers are available in the electrode (generated by illumination or breakdown) dissolution will occur. For highly doped n- or p-type substrates the space-charge region width will be small enough that the charge transfer occurs via tunneling of *electrons* or *holes*, and no illumination or breakdown would be necessary to dissolute.

In p-type silicon electrodes under anodic bias, there is no space-charge region that could produce a depletion of the walls between the pores, and therefore stop the dissolution reaction. Lehmann and Gösele postulate that the depletion of the walls is caused by a quantum confinement effect on charge carriers caused by the small dimensions of the pore walls. This effect would increase the effective band-gap energy, and so an energy barrier $\triangle E_v$ for *holes* and $\triangle E_c$ for *electrons* must be overcome to enter the silicon region between the etched pores or channels. They considered these region as quantum wires (see figure 35). Assuming:

$$\triangle E_{(v,c)} = h^2/(4m^*q^2) \tag{16}$$

where h is Planck's constant and m^* the effective mass of *hole* or *electron* (depending if considering $\triangle E_v$ or $\triangle E_c$). The barrier energies, computed with this method are in the $0.1 \div 3$ eV range.

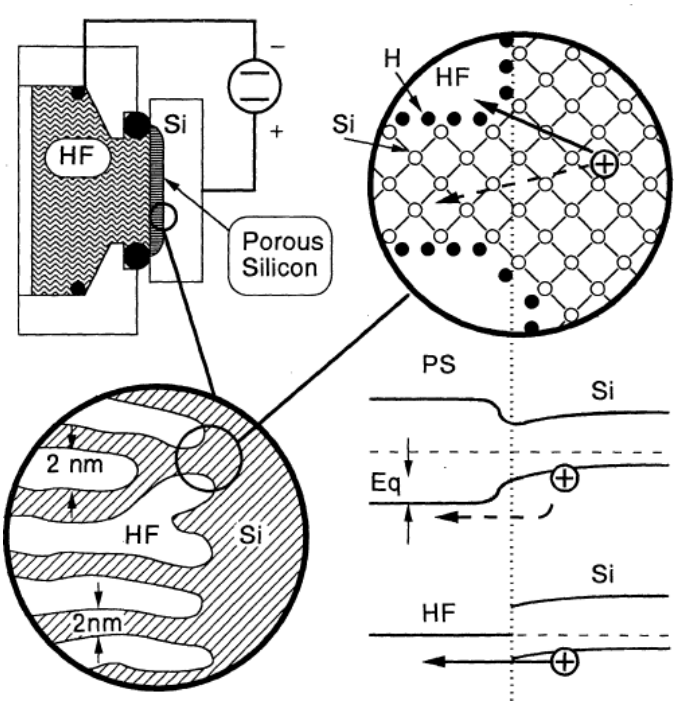


Figure 35: Left side shows a sketch of the setup used for porous silicon formation and an enlarged cross section of the PS-silicon interface. The upper right side shows the remaining wall between two pore tips and the two possible ways (broken and solid arrow) for a *hole* (h^+) to cross the interface. The lower right shows the corresponding band diagram of the interface above and the two different energy barriers for the hole penetrating into the wall (broken arrow) or a pore tip (solid arrow) [31].

This model has been extended by Frohnhoff [93] to account for the wide distribution of pore diameters of the PS formed on p-type silicon. It was proposed that the tunneling of *holes* through silicon crystallites was a process involved in the formation of microporous

silicon. The tunneling current oscillates with the crystallite size which was considered to be responsible for the uneven pore size distribution and for the stability of very small crystallites in the PS.

Quantum confinement model fits well with data about formation of crystallites with size in the nanometre scale, but it's not related to doping type and concentration, and does not explain what determines pore diameter.

2.6.7 *Surface curvature model*

This model was postulated by Zhang [15] in the early 1990s for PS on n-type silicon. On this model, the surface curvature on the order of the width of the space charge layer or smaller reduces the effective width of the space charge layer and so increase the interface tunneling current. Because of that the rate of reaction can be increase on the curved surface of the bottom of pores. Zhang studied the variation of radius of curvature from the tip to the wall and pointed out its importance in determining the distributions of reactions (silicon dissolution and oxide formation) and current density on the pore bottom. These parameters determines dimension and thickness of pores.

Although it was developed for n-type silicon, this model was considered to be applicable even for PS formed on the other type of silicon substrates. Zhang stated that it is the sensitivity of the semiconductor interface reactions to the curvature of the interface the enhances the preferential dissolution and leads to the formation of pores. The radius of curvature must affect more n-type silicon than p-type silicon and heavily doped n-type silicon which have much thinner space charge layers. In fact much smaller pores are formed.

2.6.8 *Formation of uniformly spaced pore array*

Lehmann and Föll [21] in 1990 reported the formation of straight, smooth, and well-spaced macropore arrays on n-type silicon using back-side illumination and surface patterning. In back-side illumination condition, the current is conducted through hole diffusion from the back, whereas it is by electron tunneling (or breakdown) from the front surface in the dark. It was postulated that all pore tips are limited by mass transfer in the electrolyte defined by j_1 (figure 16) in the steady state condition. Besides it was proposed that the relative rates of carrier transport in the silicon semiconductor and mass transport in the electrolyte determine the PS morphology of n-type silicon. At low current densities the reaction rate is limited by the transport of carrier to the pore tips and there is no accumulation of *holes* so that dissolution occurs only at pore tips while the pore walls do not dissolve because of the depletion of *holes*. At high current densities the reaction at pore tips is mass transport limited and *holes* accumulate

at the pore tips and some of them move to the walls resulting in the dissolution of walls and larger pore diameters. When the concentration of *holes* in the walls is close to that at the pore tips, the condition for the preferential dissolution at pore tips disappears and PS ceases to form.

The growth rate of macropores observed on n-type silicon is independent of current density when the current density at the tip equals j_1. The pore diameter w was related by Lehmann [26] to the ratio of actual current density to peak current density:

$$w = p(i/j_1)^{1/2} \tag{17}$$

where p is the spacing between two pores. Assuming an orthogonal pattern the wall thickness wt is then given as:

$$wt = p\left[1 - (i/j_1)^{1/2}\right] \tag{18}$$

These equations are in good agreement with experimental data. However they are only phenomenological correlations of pore diameter and interpore spacing with current density, HF concentration (embedded in j_1), and doping concentration (embedded in p.) under the specific condition. Besides they are applicable with good results only for a limited range in the continuum of these parameters. Also, according to Lehmann's data the concentration reduction at the pore tip due to the diffusion effect is only about 20% at a PS thickness of 150 μm which indicates that diffusion has only a minor role in the rate-determining process. Processes other than diffusion must play a major role particularly for relatively shallow pores.

2.6.9 *Formation of Two-Layer PS on Illuminated n-type silicon.*

In the 1990s two different formation models were proposed from the results on two layer PS on n-type silicon (with illumination). The two layer structure is composed by a micro PS layer on top of a macro PS and on the walls of the individual macropores. The first the formation of micro PS is believed to be mainly due to the effect of the photogenerated carriers. According to Arita [94], the anodic current under front illumination consists of three parts:

$$i = i_{drift} + i_{diff} + i_{tunnel} \tag{19}$$

where i_{drift}, i_{diff} and i_{tunnel} are the drift current due to carriers generated in the depletion layer, the diffusion current due to minority carriers outside of the depletion layer, and the electron tunneling current through the barrier into the conduction band.

In the second model, Clement *et al.*[95] proposed that the micro-PS found under illumination could result from shattering of the macro PS into fine filaments due to residual stress.

2.6.10 *Theories on the Macro PS formed on low doped p-type silicon*

The first model that tried to describe the formation of macro-PS on p-type silicon was proposed by Propst and Kohl in 1994 [76]. They related the formation of macropore to the differences in electrochemical reactions between organic and aqueous solutions (as hydrogen evolution for example) during PS formation.

A second model, by Wehrspohn *et al*. [96], was based on the resistance of electrolyte, interface, and substrate, and of the stability of current against perturbation. The model suggests that, in low-resistivity p-type silicon, the resistivity of the substrate must be higher than that of the electrolyte in order to obtain macro-PS. This model was proven to be invalid when macro-PS was obtained with electrolytes having much higher resistance than the silicon substrate.

2.6.11 *Lehmann and Ronnebeck model for macro-PS on low doped p-type silicon*

Lehmann and Ronnebeck in 1999 proposed another model for macro-PS on low doped p-type silicon [16]. Macropore morphologies on such substrate are depicted in figures 36.

They modeled the silicon electrode during the process as a Schottky diode like interface. They modeled first the electrostatics of the porous electrode (as sketched in figure 37): geometry is a key factor, because the width of the space-charge region W is directly related to shape and dimension of surface, and is minimal at the pore tip, while the barrier height is independent of geometry (being related to the materials electrical properties).

Subsequently they modeled charge-transfer (see figure 38). In a Schottky diode the forward current is either dominated by diffusion, thermionic emission, or tunneling of carriers (*holes*, in this case). The I_{diff}, compensated by field current at zero bias, is maximum at the pore tip (as well as I_{field}) and will increase (contrarily of I_{field}) if a forward field is applied. So a depression in the electrode surface grows faster than on a planar area. The thermionic emission is studied with Bethe theory, it is due to *holes* that have sufficient energy to overcome the potential barrier and are traversing it, and is related to the main free path of such *holes*. The result is that for substrates with doping densities above $10^{17} cm^{-3}$ this effect is assumed to dominate the charge transfer.

This emission is sensitive to the barrier height but not to the barrier width W, if the latter is smaller than the mean free path, so depressions show no higher current density than planar section: no pores forms. The last phenomenon is tunneling current: this charge transfer mechanism is not relevant to macropore formation and becomes the dominant transfer process at doping densities of $10^{18} cm^{-3}$ at RT.

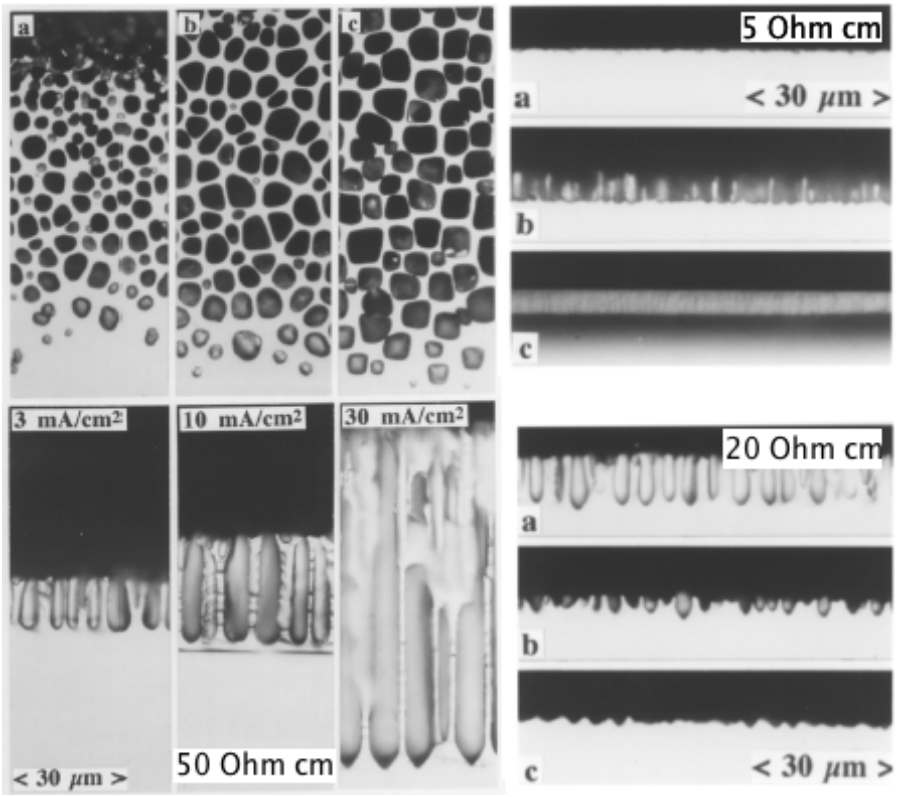


Figure 36: Macropore formation on p-type (100)-oriented silicon as a function of applied current density for three different substrate resistivities. 50 Ωcm: electrolyte 10% HF, 90 min, (a) 3, (b) 10, and (c) 30 mA/cm^2. 20 Ωcm: electrolyte 3% HF, 16.2 As/cm^2 (constant charge process), (a) 2, (b) 3, and (c) 4.5 mA/cm^2; this sample shows that for low concentration of HF pore growth is suppressed for current density above a threshold. 5 Ωcm: 3 mA/cm^2, 90 min (constant charge process), (a) 3% HF, (b) 10% HF, and (c) 30% HF; pore morphology changes with HF concentration, only an increase of roughness is present in (a), macropores with thin walls in (b) and a microporous layer in (c) [16]. All processes were carried at RT.

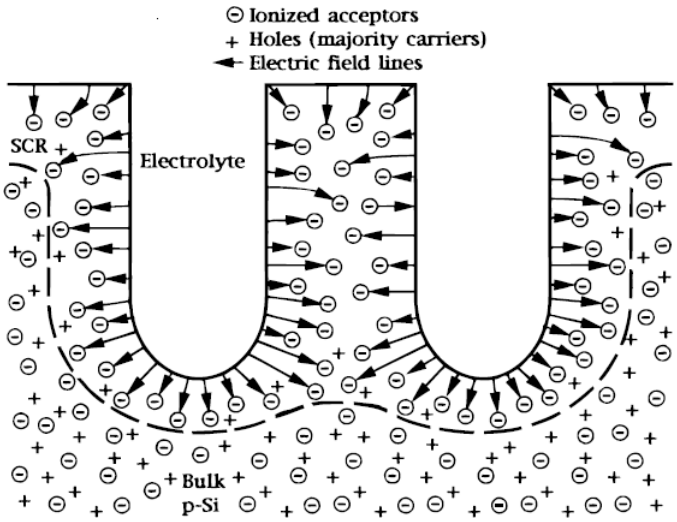


Figure 37: Sketch of the equilibrium charge distribution and the electric field around pores in a p-type semiconductor electrode.

This is sensitive to W similar to the diffusion current, but, because of the small dimensions of SCR, mesopores are to be expected.

In this model macropore formation on p-type silicon is due to the increase of the diffusion current density at pore tips, compared to flat electrode areas, due to pore tip geometry, that produces a minimum of SCR width and consequently a maximum hole concentration gradient. Besides pore walls become passivated against dissolution if their distance decreases to two times the SCR width, because *holes* which initiate the dissolution process become depleted. The process is suppressed if thermoionic emission becomes dominating. However, as Zhang argued [15] that this does not explain the formation of two PS layers with several orders of magnitude difference in pore size, nor what governs the dimension of the macropores.

2.6.12 *Kinetic model*

In 1997 Kooij *et al.* proposed a pure chemical model. This model was first developed for n-type silicon, but can be applied to p-type too. In this kinetic model, unoxidized silicon surface atoms are represented by Si(0). At the first step of the anodic dissolution these atoms capture a valence band hole according to this reaction:

$$Si(0) + h^{+}_{VB} \rightarrow Si(I) \tag{20}$$

It is assumed that the hole is captured in a Si-Si bond and the Si(I) intermediate state corresponds to a one-electro-deficient Si-Si back bond. This intermediate state is very mobile and can act as a catalyst for the dissolution reaction. These are the essential steps of the model:

$$Si(0) + h^{+} \rightarrow Si(I)^{1+} - e^{-} \rightarrow Si(II)^{2+} - e^{-} \tag{21}$$

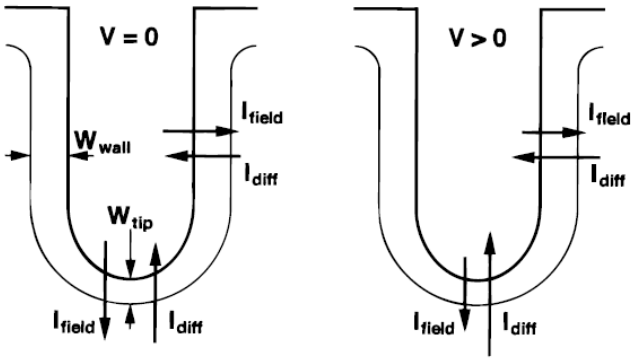


Figure 38: (a, left) Equilibrium (V=0) field currents and diffusion currents across the space-charge region for the macropore tip and wall region in p-type silicon. (b, right) Field currents and diffusion currents under forward bias (V>0). Note that due to geometric field enhancement around the pore tip the tip currents are always larger than the pore wall currents [16].

$$\downarrow$$

$$Si(III)^{3+} - e^{-} \rightarrow Si(IV)^{4+} + Si(0) \tag{22}$$

$$\downarrow Si(I)$$

$$Si(IV) + H_2 + Si(0) \tag{23}$$

It is assumed that Si(I) stimulates the chemical reaction

$$Si(II) + 2H^{+} \rightarrow Si(IV) + H_2 \tag{24}$$

This would imply that anodic dissolution proceeds much faster on surface region around an Si(I) intermediate state. This active region can be characterized by a radius which is determined by the diffusion length L of the mobile Si(I) intermediate:

$$L = (D \times \tau)^{1/2} \tag{25}$$

Where D is the surface diffusion coefficient of the Si(I) and τ is the lifetime. Inhomogeneous etching will occur if the diffusion length of the Si(I) intermediate is smaller than the average distance between this intermediates:

$$L < 1/s^{1/2} \tag{26}$$

Where s is the surface concentration of Si(I). However this model does not produce any estimations about the number of these intermediates [97, 98].

2.6.13 *Transport of holes*

Another model that tries to describe the early stages of porous silicon formation was proposed in the late 1990s by Valance [99], Kang and Jorne [100], and developed by Ozanam [96]. The model is based on linear stability analysis and incorporates the transport phenomena of *holes*, in the semiconductor and ions in the electrolyte. This model well predicts the characteristic structure size comparable with SCR width. However the model cannot be used to describe the pore growth process in a proper way. Based on the same proposals, the model developed by Kang and Jorne resulted in a different conclusion: the most likely dissolution mechanism during porous silicon formation involves the capture of two *holes* to form some intermediate silicon product Si(II), which further react with protons to produce Si(IV) and H_2 gas [97].

2.6.14 *Current Burst Model*

In the early 2000s Föll *et al*. proposed a model that try to account for all the processes of the reactive Si-electrolyte interface including current oscillations on the current voltage characteristics. Taking in account all the previous models, they proposed that the current flow across Si-electrolyte interface is spatially and temporally inhomogeneous. They consider four reaction during the dissolution of silicon:

- Direct dissolution with the net reaction:

$$Si + xh^+ - ye^- \rightarrow Si^{4+} \tag{27}$$

  where x *holes* (h^+) are consumed in the reactions (and x must be ≥ 1), while y injected *electrons* (e) account for the rest of the charge needed. Direct dissolution thus makes the most efficient use of *holes*; it can proceed if only one hole is supplied.

- Oxidation:

$$Si + 4h^+ + 2O_2^- \rightarrow SiO_2 \tag{28}$$

  Oxidation will always need four *holes*; it is thus not as efficient in the use of available *holes* as direct dissolution

- Oxide dissolution

$$SiO_2 + 4F \rightarrow SiF_4 + O_2 \tag{29}$$

  Oxide dissolution is a purely chemical process that does not need current flow or applied potentials. It essentially limits the total current that the system can process, because the oxide generation rate cannot be larger than the dissolution rate (on average).

- Hydrogen passivation of the free silicon surface

$$SiX + H \rightarrow SiH + X \tag{30}$$

  It means that whatever is sitting on the surface will be replaced by hydrogen in due time as given by some reaction constant k_{cov} as long as no other reactions take place.

Both dissolution processes must occur simultaneously, because the valence of the processes (i.e. the number of carriers flowing through the external circuit for one atom of silicon dissolved) is usually around 2.7 and a single process should have an integer as valence.

The idea of the model is that the local current start to flow where the local field strength is high enough. This current generates some oxide growth and it stops to flow at certain thickness of the oxide. The oxide is then chemically etched, and the cycle starts again. The "events" are correlated in space and time. This means that the nucleation probability of a current burst is not only a function of the surface state S(x, y, t) but may depend on what has happened before at (x, y) (interaction in time) or on what is going on in the neighborhood at t (interaction in space). Surfaces where no current bursts happened for some time are more passivated and thus less likely to nucleate a new current burst. Since the kinetics of passivation are strongly anisotropic, so is Current Burst (CB) nucleation, and CBs nucleate preferentially on (100) (and (113)) surfaces. Critiques to this model come from Vyatkin: even if it is useful in predicting frequency dependence of macropore parameter formation on external experimental parameters, it is not good to predict pore diameter, pore wall thickness, pore formation rate, and other useful in practical applications parameters[97].

2.6.15 *Other hypothesis*

Other models have been developed. In many studies, the presence of a surface layer has been suggested to be essential for the formation of PS. For example reactions involving hydrogen-bonded species were proposed to be fundamentals by Allongue and by Lewerenz. Unagami suggested that the formation of PS is promoted by the deposition of a silicic acid on the pore walls which hinders the dissolution of the walls and results in the directional dissolution at the pore tips. Alternatively, Parkhutik et al. suggested that a passive film composed of silicon fluoride and silicon oxide covers the wall and the bottom of the pores and that the formation of PS is similar to that of porous alumina where a barrier layer exists on the base of pores. Jaguiro et al. developed a theoretical modeling based on charge transfer kinetics; La Monica introduced a theory based on thermodynamical arguments.

As it can seen mechanisms involved in PS formation are quite complex, and, although lots of models have been developed, no one can describe porous all silicon morphologies formations. All the models can predict some of the properties, morphological aspects, etc., of PS, for a limited range of electrolyte, and substrate doping. Studies on PS models are far to be concluded.

3

POROUS SILICON PROCESSES CHARACTERIZATION

3.1 INTRODUCTION

This chapter gathers the process characterization data for the porous silicon layers used in this work. The optimization of the characteristics of porous silicon layers, i.e. morphology, porosity, and thickness depends on the correct choice of electrolyte type, anodization current density, anodization time and HF concentration in the electrolyte. It should be evident, from chapter 2, that no general analytical solution exists to this problem but only an large set of experimental data that can be used as starting point. The data collected in this chapter fall in two large categories:

- Mesoporous silicon layers grown of n+ and p+ silicon substrates. Data on 0.1 Ωcm wafers have been originated in previous works and are reported her because they have been used for the development of compliant contacts with the CRML technology described in chapter 6. Data on 0.01 Ωcm have been originated in this work for the test of copper deposition into PS layers.
- Macro- and micro-porous silicon layers on p- silicon wafers. The characterization of macro and microporous layers on that substrate have been carried on in this work.

Highly doped substrates have been used in the layer transfer technology described in chapter 6 because of the uniformity of the porous layer that can be obtained (see figure 31) and because no illumination is necessary for n-type silicon wafer. Lowly doped p-type substrates have been used for the study of the hydrophobicity characteristics of the macroporous surface, for the realization of multi-layer porous structures and buried cavities and as substrates for silicon interposers.

All the anodization experiments were made according to the following protocol:

1. Cleaning of the silicon wafer with RCA[1] process to remove superficial contaminants. Porous silicon is extremely sensitive to contamination and defects and a thorough cleaning step is necessary to obtain a uniform porous layer.

1 RCA clean is a standard cleaning procedure for silicon wafer involving three steps: Organic Clean, Oxide Strip and Ionic Clean. The process has been developed at Radio Corporation of America, hence the name.

PS regime	Orientation	Growth rate [nm/s]	Thickness [nm]	p [%]
1 (a,b)	(100)	44.3	886	55
2 (e,f)	(100)	64.2	963	82
1 (c,d)	(111)	40.5	809	52
2 (g,h)	(111)	46.2	693	85

Table 3: Anodization parameters for meso-PS layers on 0.01 Ωcm silicon wafers in 9% HF solution. The anodization current determines the porosity of the layer. The crystal orientation influences the growth rate of the porous layer. Porous silicon growth is slower on (111) substrates.

2. The wafer is cut in square samples squares of $3 \times 3cm$.
3. Just before anodization, the sample is dipped into Buffered Oxide Etch (BOE) to remove the native oxide.
4. The sample is inserted into the anodization cell. The active area of the cell is 3 cm^2. The sample is contacted on the back-side (the side not exposed to the electrolyte) with a graphite disk. The counter electrode is platinum wire counter-electrode (cathode).
5. The sample is anodized and then rinsed in DI for 5 minutes, dried in nitrogen and stored for analysis.

3.2 MESOPOROUS SILICON LAYERS ON HIGHLY DOPED SILICON WAFERS

Meso-PS layers can be obtained from highly doped silicon wafers of both type with two aqueous electrolytes with 9% HF and 12% HF concentrations. The first electrolyte is a mixture of HF (45 wt.%), H_2O, and CH_3H_7OH (Isopropyl alchool (IPA)) in a 1:3:1 ratio by volume. The second electrolyte is a mixture of the same compounds but in a 1:2:1 ratio by volume. For each electrolyte the porosity depends on the anodization current density as shown in figure 39, for 0.1 Ωcm wafer resistivity.

The porous ayers obtained on monocrystalline n-type (100) and (111)-oriented Si wafers with the resistivity of 0.01 Ωcm [2] are shown in figure 40 and 41, respectively. Two different anodization regimes were applied:

1. current density of 60 $^{mA}/_{cm^2}$ for 20 s,
2. current density of 120 $^{mA}/_{cm^2}$, for 15 s.

The porosity of the layer has been determined with the gravimetric method and layer thickness has been extracted from the SEM images.

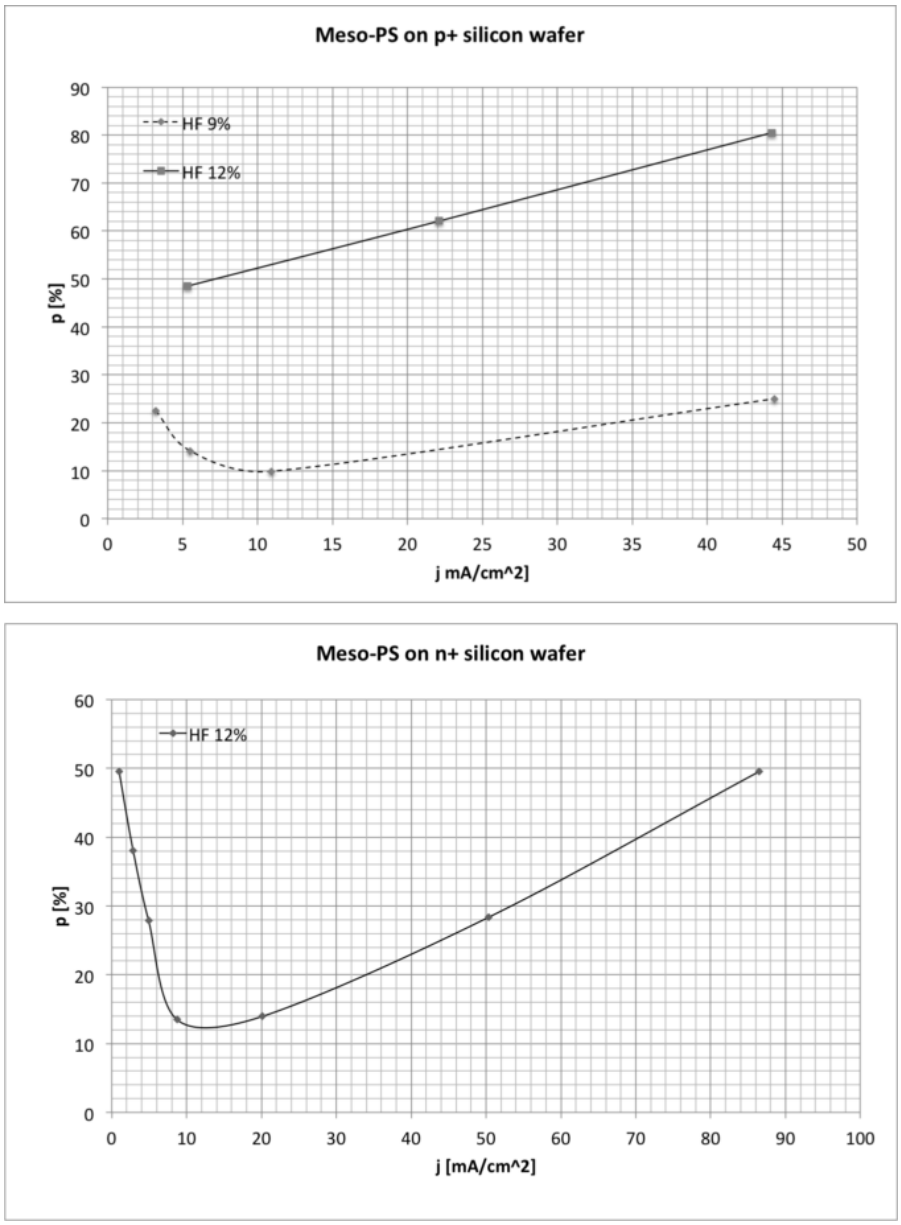


Figure 39: Porosity vs anodization current plot for n+ silicon wafer in 12% HF electrolyte (left) and for p+ silicon wafer in 12% and 9% HF electrolyte.

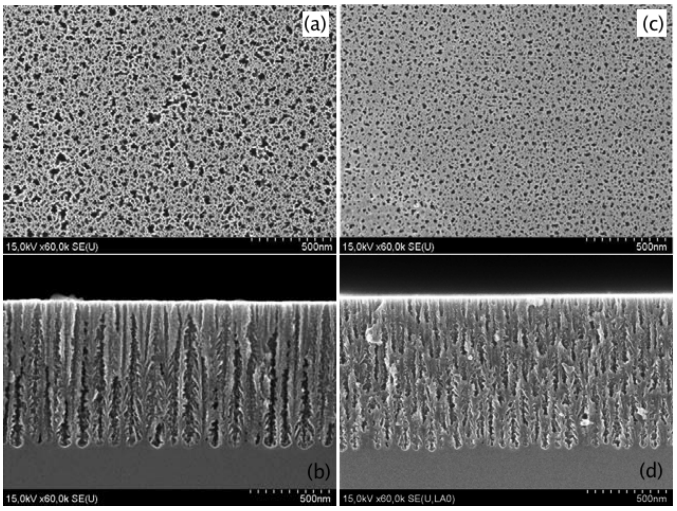


Figure 40: 50% porosity meso-PS layers on n+ type: (100)-oriented silicon wafer (left) and (111)-oriented silicon wafer (right) with resistivity of 0.01 Ωcm.

Four sets of PS templates have been prepared; table 3 reports the average parameter for each set. Figures 40 and 41 show the SEM top and cross sections of PS for the regime 1 and 2, respectively. It is seen that in all cases, porous silicon consists of a matrix of silicon and voids which are perpendicular to the substrate surface. Porous layers of 52-55% porosity look like the ordered alternation of silicon nanobranched crystals and channel voids (figure 40.(a-d)), i.e. the pores. The entrances of the channels have almost regular cylindrical shape. The porous layer is deeper in the (111) orientation than in the (100). The structure of PS layers with porosity of 82-85% might be characterized as a network of smooth silicon nanoplanes which formed the channel walls (figure 41.(e-h). The entrances of the channels are wider and have a more irregular perimeter (figure 41.(e), 41.(g)) than the ones in the layer with lower porosity (figure 40.(a), 40.(c)). It is noteworthy, that PS channel on (111) orientation (figure 41.(h)) are not parallel to each other and shorter than the one on (100) (figure 41.(f)).

3.3 POROUS SILICON ON LOWLY DOPED P-TYPE POROUS SILICON WAFERS

Lowly doped p-type (100)-oriented silicon wafers with resistivities in the 10-20 Ωcm range are readily available at low cost and constitute an interesting platform for the assembly of heterogenous system in future SiP. In this work has been developed a fabrication technique for macroporous structures suspended over a cavity using micro-PS as sacrificial layer (to create the cavity). The characteristics of macro-PS and micro-PS layers on that wafers has been thoroughly studied.

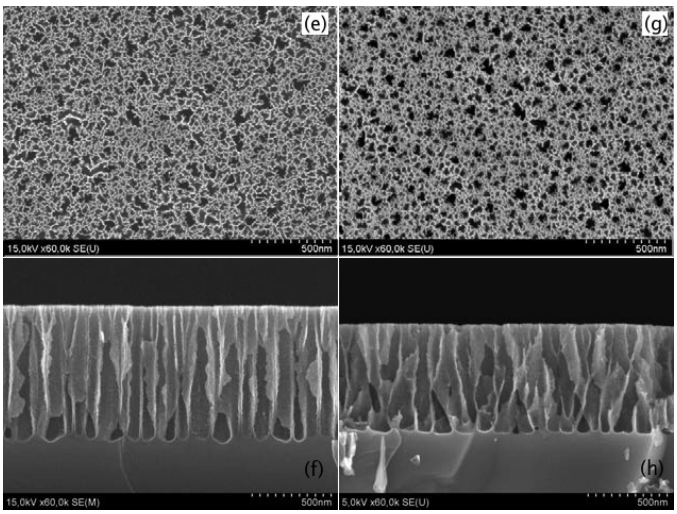


Figure 41: 80% porosity meso-PS layers on n+ type: (100)-oriented silicon wafer (left) and (111)-oriented silicon wafer (right) with resistivity of 0.01 Ωcm.

It can be recalled, from chapter 2 that macro-PS with straight, open macro-pores can be produced on lowly doped wafers using different electrolytes. It has been reported in literature that both aqueous and organic electrolytes (according to the definition given in chapter 2) can produce macropores. The two most cited aqueous electrolytes are: HF 3% (1.4 M)[16], HF:EtOH in 1:1 ratio by volume (10 M) [17]. Among the organic electrolytes, the ones based on DMSO present less safety issues than the other. DMSO-based organic electrolytes includes simple dilution of HF (4M) [101], or more complex formulation as HF:IPA:DMSO in a 1:1:3 ratio by volume (4.6M). The electrolyte that gives the best results, in terms of pore morphology and surface homogeneity on 10-20 Ωcm wafers, is the HF:DMSO in 10:46 ratio by volume (4.1 M). The characteristics of the macroporous layers have been characterized for different anodization current densities and anodization time. All the performed experiment conditions have been reported in table 4. The maximum current density is 30 $^{mA}/_{cm^2}$, the electropolishing threshold (J_{PSL}). Due to the long anodization time, the solution is agitated during the process to continuously supply fresh (non depleted) electrolyte to the silicon surface.

3.3.1 *Macro PS morphology investigation*

The morphology of representative macro-PS layer for the each of the performed experiments, excluding the 30 $^{mA}/_{cm^2}$, because no porous layer is present due to electropolishing, is reported in appendix B. SEM analysis of the porous layers (see the cited appendix and figure 42) shows, in all cases, a uniform thickness of the porous layer (in the center of the sample) with pores perpendicular to the (100) sur-

Charge density [C/cm^2]						
Time		Current density J [mA/cm^2]				
[min]	[s]	1	3	5	10	30
15	900				9000	27000
30	1800			9000		
45	2700				27000	
50	3000		9000			
90	5400			27000		
150	9000	9000	27000			

Table 4: Table of characterization experiments for macro-PS. The experiments are carried on at two charge density (i.e. the charge involved in the electrochemical reactions per square centimeter) values. The value of 30 $^{mA}/_{cm^2}$ is the electropolishing threshold.

face. Aspect ratios in excess of 30:1 have been obtained in this work, but higher values are easily achievable by increasing anodization time (due to the anisotropy of the process). Plan view of the porous surface (fig. 42 b) and, cross section (42 a) show that the surface of the porous layer present an higher density of pores than the bulk. In particular, the bulk of the porous layer seems to present an "order" in the organization of the porous structure that is not apparent from the plan view. The cause of this difference between surface and bulk is visible in figure 42 d: each fully developed pore (i.e. a pore that extends for all the thickness of the layer) is surrounded by shallow pores (often called interpores or proto-pores) that extends for a few microns only.

This cause of the interpores is that, for the first few microns of the porous layer, the SCR is not fully developed and thus, pores develop in a random order. The more the porous layer grows, the more the SCR reaches its stable thickness, as predicted by Lehmann's model, and competition between adjacent proto-pores for hole supply starts. Those pores whose distance is near the value predicted by the SCR model are at able to receive a continuos hole supply from the bottom and continue to develop, the others stop.

An high magnification SEM image (figure 43) reveals that a nanoscale roughness is present on the surface of the pores. Macropores surface is rough either on the top and inside the pore wall, as can be seen in figure 43. The presence of this roughness increases the exposed surface of macro-PS.

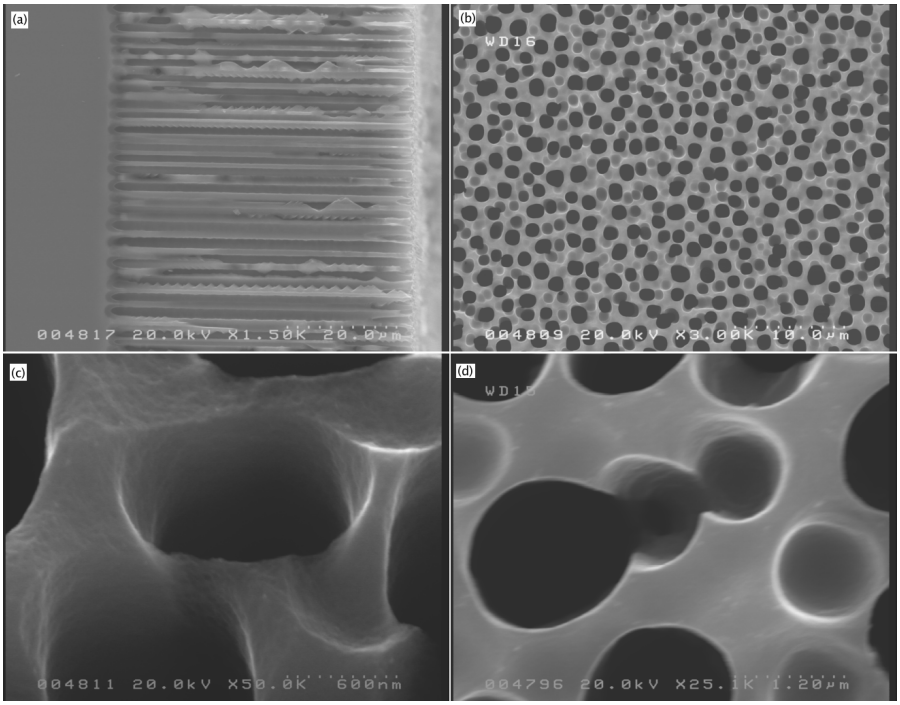


Figure 42: SEM images of macroporous silicon layer obtained on 10-20 Ωcm, p-type, (100)-orientation, with HF:DMSO (10:46) at 10 $^{mA}/_{cm^2}$ for 60 minutes, at RT. (a) Cross section of the layer (thickness of 55 μm); (b) top-view of the layer; (c) Magnification of the "entrance" of a pore; (d) magnification of a fully developed pore and two associated interpores.

3.3.2 *Macro PS layer analysis*

The statistical characteristics of the macro porous layer (porosity, pore diameter, pore distance, etc.) have been determined using the ImageJ software [63] by using feature analysis and spectral methods. The first methodology (i.e. feature analysis) has been introduced in 2.2, the other: the Radially Averaged Autocorrelation (RAA) spectral method, will be introduced here.

The methodology used analyze the image, strongly influences the results. Visual inspection of the image, like the one done (as an example) in figure 44, where false colors (ImageJ Fire Look-Up Table (LUT)) have been use to enhance the detectability of features reveals that pores have a diameters in the 0.98-1.6 μm range and interpores (usually smaller), being in the 0.74-0.92 μm range. The major drawback of this technique is the time necessary to compute the pore diameter on large images (containing hundreds or thousands of pores) and the ambiguous choice of the characteristic diameter for irregular features. This method works well for the determination of the porous

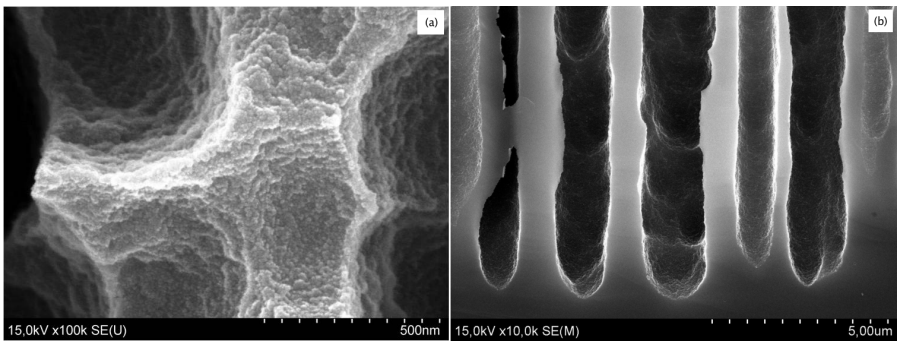


Figure 43: Roughness of the surface of macro-PS layer.

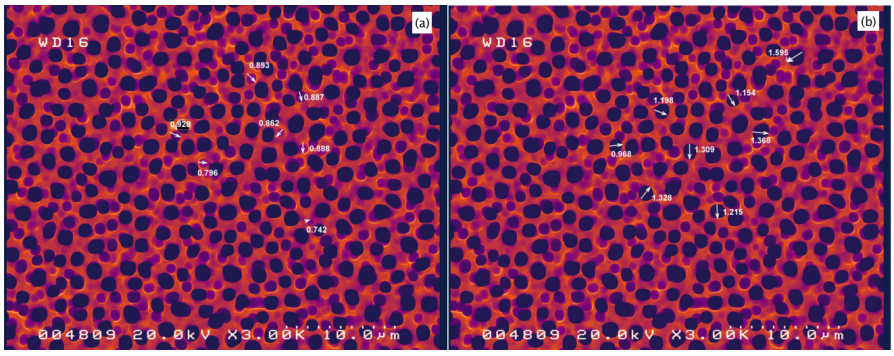


Figure 44: False colors image of the macro-PS layer in figure 42 (b). The diameters of some pores (a) and inter-pores (b) have been highlighted. All values are in μm.

layer thickness instead. Both problems can be overcome using ImageJ particle analysis tool, as described in 2.2.

The results of the analysis (values averaged over all the images) are summarized in the tables in figure 45 where it can be seen that pore diameters match with the results obtained by visual inspection. According to the results, a trend emerges in pores diameters, as they get wider with the increasing of the anodization time. This can be attributes to non perfect passivation of silicon surface during anodization or, chemical dissolution due to the long time exposure to HF. The superficial porosity, computed as defined in 2.2, is constant and in the range 50-62%. It is interesting to compare this result with the porosity computed with the gravimetric method, shown in figure 46.

Direct comparison of the two porosities shows that bot values match for higher pores depth (the ones obtained in the 27000 C/cm^2 experiments). The values reported by the feature analysis are lower, as said before, due to the influence of interpores on the surface. The anomalous value obtained from the gravimetric method for other experiments (greater than 100%) is due to a dissolution phenomenon that happens before the stabilization of the SCR. A seed layer with high porosity forms at the start of the anodization process (with a thickness less than 5 μm) where both pores and inter-pores develops

Pore depth [um]						
		J [mA/cm^2]				
Time [min]	Time [sec]	1	3	5	10	30
15	900				4.2	ep
30	1800			3		
45	2700				29.6	
50	3000		4			
90	5400			32		
150	9000	3.24	30			

Pore diameter [um]						
		J [mA/cm^2]				
Time [min]	Time [sec]	1	3	5	10	30
15	900				0.87	ep
30	1800			0.819		
45	2700				1.15	
50	3000		1.167			
90	5400			1.37		
150	9000	1.195	1.617			

Superficial porosity [%]						
		J [mA/cm^2]				
Time [min]	Time [sec]	1	3	5	10	30
15	900				50.3	ep
30	1800			60.7		
45	2700				53.2	
50	3000		54.7			
90	5400			57.2		
150	9000	59.9	61.9			

Figure 45: Results of ImageJ features analysis on the macro-PS samples realized in the experiments reported in table 4. Electropolishing (ep) is reported for 30 mA/cm^2.

Porosity gravimetric [%]						
		J [mA/cm^2]				
Time [min]	Time [sec]	1	3	5	10	30
15	900				121.65	ep
30	1800			188.21		
45	2700				50.04	
50	3000		145.45			
90	5400			53.27		
150	9000	192.82	59.11			

Figure 46: Porosity of the samples realized in the experiments reported in table 4 computed with the gravimetric method. Electropolishing (ep) is reported for 30 mA/cm^2.

Dissolution Valence						
		J [mA/cm^2]				
Time [min]	Time [sec]	1	3	5	10	30
15	900				2.2	ep
30	1800			2		
45	2700				2.28	
50	3000		1.9			
90	5400			1.98		
150	9000	1.8	1.9			

Figure 47: Dissolution valence for the macro-PS samples realized in the experiments reported in table 4. Electropolishing (ep) is reported for 30 $^{mA}/_{cm^2}$.

(random pitting). When the thickness of the layer is sufficient to stabilize the SCR, macro-pores develops and inter-pores stops. Inter-pores are what remains of the pores in that layer. This layer is not evident in SEM images because it is etched during the formation of the stable macro-porous layers, by chemical or electrochemical dissolution. Nevertheless, it contribute to the weight loss of the sample, causing the anomalous value of porosity. It has to be said that the thickness of the porous layer in figure 45 has been obtained from SEM images that do not show the missing layers (as the borders of the layer are not present in the image). The dissolution valence of the process is generally below 2 for all processes up to 5 $^{mA}/_{cm^2}$ and is 2.2-2.3 at 10 $^{mA}/_{cm^2}$, as shown in figure 47.

This increase in the dissolution valence (it is an average value over all the process) means that electropolishing phenomena start to occur at that current density. It has to be said that, due to border effects in the electrochemical cell, the current tends to crowd at border, giving rise to electropolishing phenomena. This is a known phenomena and must be accounted to avoid the breaking of the macroporous layer, especially for thick layers.

3.3.2.1 *Autocorrelation analysis*

The correctness of the data obtained with feature analysis has been verified with a spectral method based on the radially averaged autocorrelation of the image. The description, applicability and validation of this method is discussed in appendix A.

The RAA has been applied to the samples obtained with the processes in table 4. The first minimum of the autocorrelation (i.e. an anticorrelation peak) expresses the average diameter of the pores; the negative peak implies that the maximum difference in color between pixels at that distance exists, a condition that is met when a pore (dark in the image) is correlated with silicon (light grey or white). Instead the first maximum represent a similitude of pixel color at that distance, in terms of pores, this corresponds to the correlation of two pores. This is used to measure the average interpore distance (i.e. the

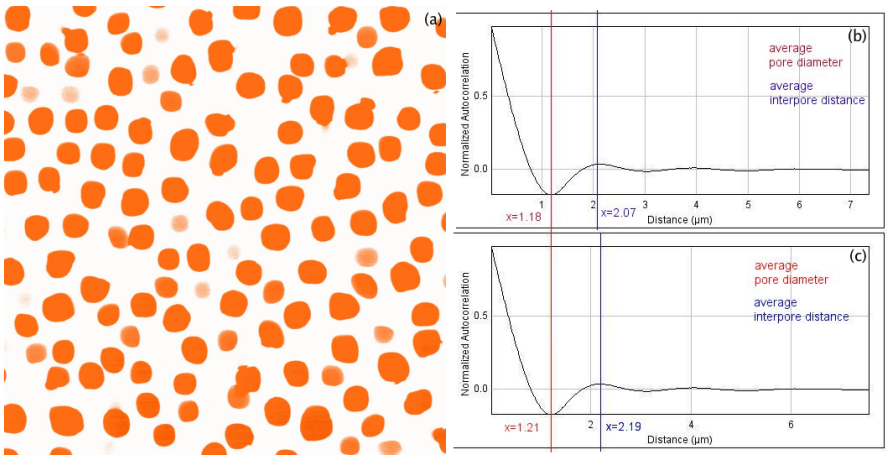


Figure 48: (a) image 42 (b) modified with false colors for autocorrelation, (b) RAA of the 42 (b), and (c) RAA of the image in false colors.

distance between two pore). Although this method is good to analyze the average pore diameter, it suffers of the presence of inter-pores. In most situation, only fully developed pores are of interests, and thus the influence of inter-pores should be eliminated. In grayscale images, pores and inter-pores diameters are, in fact, averaged together: inter-pores are darker than silicon but lighter than pores, and this translates to a shift of the autocorrelation side peak. An evidence of that is given in figure 48: the image in figure 42.(b) has been subject to the RAA process and the result is the curve in figure 48.(b). The value x (distance) of the first peak, 1.14 μm, smaller than the expected one for deep pores (around 1.3 μm according to the measures). When the image is re-colored in false colors as shown in figure 48.(a), the autocorrelation changes to the one in figure 48.(c). This coloring scheme increase contrast and the brightness of the original image, and lighten the inter-pores to reduce their weight in the autocorrelation. The resulting autocorrelation presents a shift in the peak distance of 0.07 μm, and the results better approximates the expected value (obtained with visual inspection).

The result of the RAA analysis applied to the macro-PS samples is shown in figure 49. The average pores diameters are within 20% of the ones computed with feature analysis. In particular, the RAA method provide always lower values.

In conclusion, from all the analyses carried on macro-PS samples, emerges that the dimension of pores and interpore distances cannot be controlled with anodization current density on this substrate. Electrochemical or chemical dissolution is shown to alter the surface of sample, during the anodization process. The study of the morphology of macro-PS layer has also been used to determine the pitch of pitting of the the substrate to grow orderer macropores as shown in the cross-section in figure 50.

RAA pore diameter [um]						
		J [mA/cm^2]				
Time [min]	Time [sec]	1	3	5	10	30
15	900				0.87	ep
30	1800			0.75		
45	2700				1.11	
50	3000		1.01			
90	5400			1.19		
150	9000	1	1.23			

RAA interpore distance [um]						
		J [mA/cm^2]				
Time [min]	Time [sec]	1	3	5	10	30
15	900				1.72	ep
30	1800			1.96		
45	2700				2	
50	3000		1.96			
90	5400			2.17		
150	9000	2	2.35			

Figure 49: Results of the autocorrelation analysis on macro-PS samples realized in the experiments reported in table 4. Electropolishing (ep) is reported for 30 $^{mA}/_{cm^2}$.

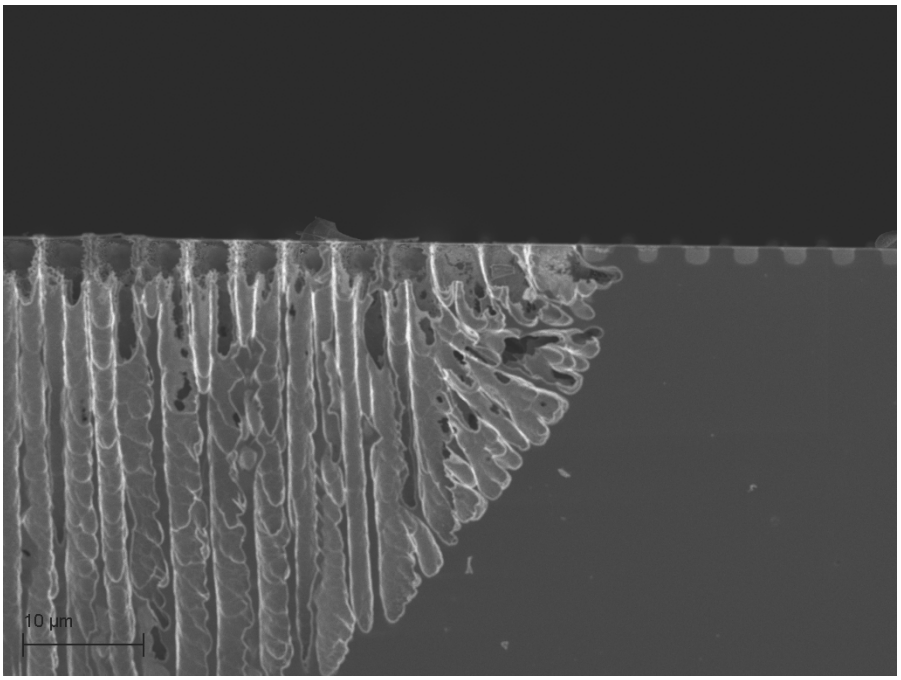


Figure 50: Ordered macropores obtained on p-type (100)-orientation silicon wafer with a resistivity of 10-20 Ωcm. The macro-PS layer has been obtained in HF:DMSO (10:46) at a current density of 10 $^{mA}/_{cm^2}$ for 45 minutes. Pre-pitting of the substrate (2 μm opening, 4 μm pitch, 1.5 μm depth) has been done with RIE.

The picture show a SEM image of a cross section of an ordered macropore layer (at the edge of the sample to show pre-pitting) obtained by masking silicon with an undoped polysilicon mask and pre-pitting the surface. The pre pitting is a regular pattern of 2 μm openings set at 4 μm pitch and 1.5 μm deep. In the image, the formation mechanism of the macro-PS layers is evident: the silicon between etch pits is dissolved in an isotropic process until the wall between adjacent pits becomes passivated and the pore start to grow. In this particular case, four pores are generated in correspondence of each pit. The average pores diameter in this sample is 2.5 μm, 25% larger that the ones measured on random sample, this is attributed to the distance between initial pits. In the Lehmans' model, the thickness of the wall, that in turns depend on SCR thickness, gives the pore diameter.

3.3.3 *Macropores growth rate*

The growth rate of Macro-PS layers has been studied for the anodic process in HF:DMSO (10:46) with a current density of 10 mA/cm^2, the one that gives the most reproducible results. The process is anisotropic but the etch rate is not equal on the whole surface and border effect characterization on growth rate has been done. The thickness samples anodized for three different times has bee measured in three different region: at the center of the sample, at a point equidistant from the center and the edge (indicated with "middle" for brevity), and at the edge of the sample, in the region where pores are vertical, with reference to figure 50.

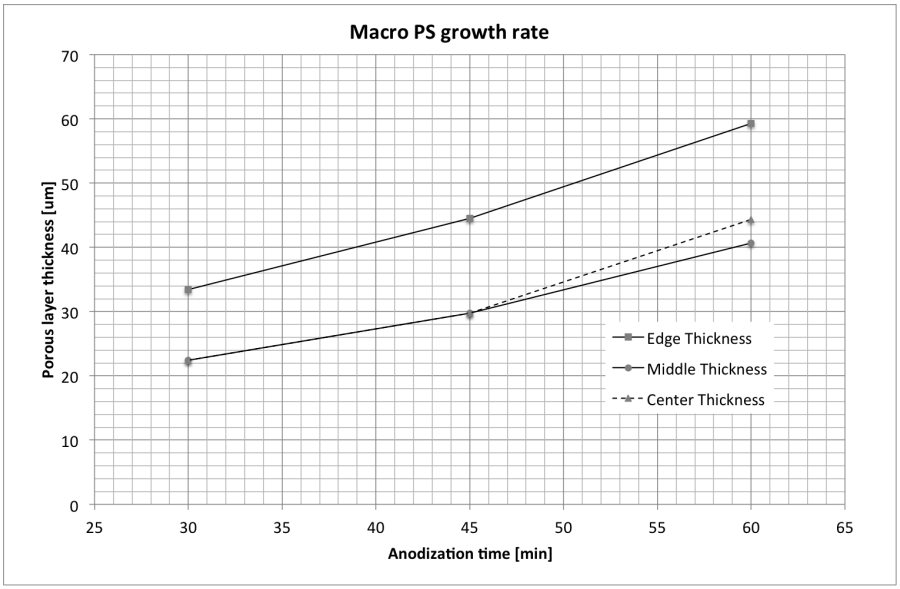


Figure 51: Macro-PS growth for HF:DMSO (10:46) on p-type (100)-oriented, 10-20 Ωcm silicon wafer. Data are sampled in three different points (see 3.3.3 for a description of the sampling strategy).

The growth is higher at the edge of the silicon wafer, due to border effects as figure 51 shows. Far away from the border (middle and center points) the porous layers has almost the same thickness after 60 minutes of anodization. The growth rates have been computed, by linear interpolation:

- Edge 0.98 $\mu m/min$
- Middle 0.67 $\mu m/min$
- Center 0.72 $\mu m/min$

Applications that will use macro-PS layers grown with the processes presented here should take border effect into account.

3.3.4 *Microporous layer morphology investigation*

The formation of micro-PS layers on low doped silicon wafer requires the use of high concentration of HF in the electrolyte, and is not always possible. It has been found that, for 10-20 Ωcm silicon wafers, concentrated HF (45 wt.% - 48 wt.%) is necessary. If possible, the HF should be diluted in IPA that will act as a surfactant and will favor the penetration of the electrolyte in the nano-pores. The anodization current density for obtaining the micro-PS morphology is 40 mA/cm^2. The characterization of the growth rate has been done with the same procedure followed for the macro-PS (3.3.3) and results are reported in figure 52.

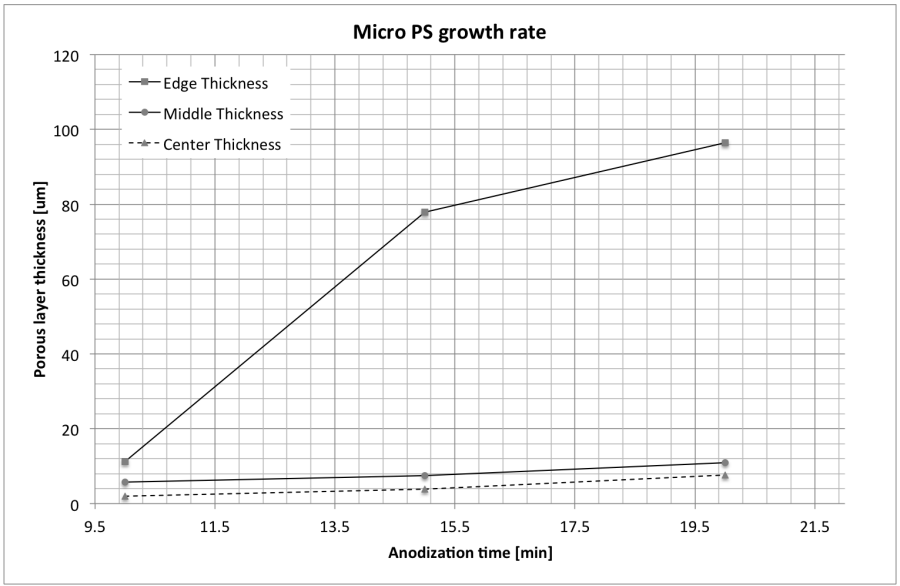


Figure 52: Micro-PS growth for HF 45 wt.% on p-type (100)-oriented 10-20 Ωcm silicon wafer, process rate. Data are sampled in three different points (see 3.3.3 for a description of the sampling strategy).

There is a larger amount of micro-PS formed at the edge. Middle and center grows at a nearly constant rate. Linear interpolation gives the following growth rate:

- Edge $5.1 \mu m/min$
- Middle $0.54 \mu m/min$
- Center $0.35 \mu m/min$

The one-order of magnitude higher growth rate at the edge is attributed to the border effects that are more pronounced due to higher current crowding than in the case of macro-PS. SEM investigation of the region (see figure 53) reveals the presence of a continuous layer whose color differs from the one of bulk silicon (darker in color) but no feature is visible (due to the small dimensions of the crystallites). The surface of this layer appears rough at high magnification (figure 53.(b)) because the cleavage cut along several crystallites with different orientation.

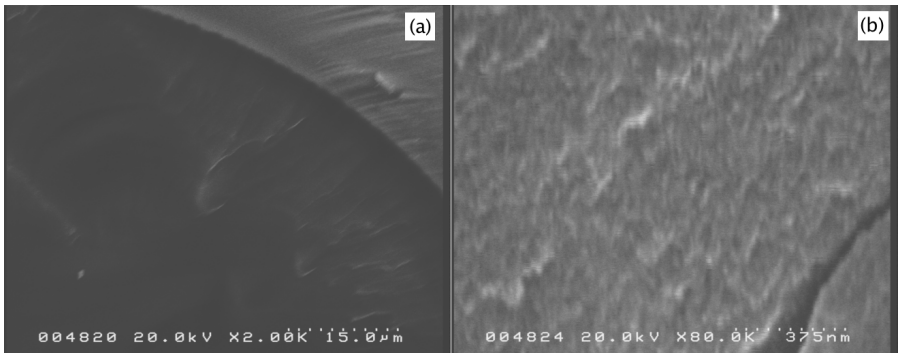


Figure 53: SEM image of micro-PS: edge (a), and its magnification (b). The sample is realized in HF 45% with current density of 40 mA/cm^2 for 5 minutes.

4

COPPER DEPOSITION INTO POROUS SILICON LAYERS

4.1 INTRODUCTION

Recently, numerous studies have been undertaken to modify PS surface with metal particles to obtain the desired properties of the porous material required for different applications [102, 103]. Recently, the nanostructured PS covered with silver nanoparticles (NPs) has been found to be an active substrate for the Surface Enhanced Raman Scattering (SERS) [104]. Extremely tempting goal is to minimize the complexity and the cost of PS based devices production. It requires cheap materials, high repeatability and simplification of the technological process. Chemical displacement deposition of copper on PS combines these requirements. Copper is characterized by the redox chemistry, thermal, catalytic, sensing properties as well as lower price than silver. Composite structure based on PS covered with copper NPs has demonstrated to improve the sensitivity of ellipsometric gas sensors to vapors of methanol [105], as an example. Copper nano-rough films deposited on PS pillars have been found to enhance the signal of SERS [106]. Copper particles of 100-300 nm have been used to form inner electrode material for multilayers capacitors [107].

The chemical displacement deposition of copper on PS has many advantages:

- simple control of the process,
- no need of special equipment,
- penetration of copper atoms in porous layer.

The method presented here is a variant of the wet chemical deposition and based on the displacement reaction of the silicon atoms by the copper atoms. Copper cations in the aqueous solution interact with silicon and PS resulting in the formation of copper NPs [108, 109, 110]. Whereas metal plating of PS is not new [33, 111] the peculiarity of this method is the simultaneous copper deposition and PS dissolution and the non-oxidation of the silicon surface. This is obtained by the addiction of fluorine ions (adding HF) to the aqueous solution of copper salt.

This chapter is ideally divided into two section. The first section introduces the immersion plating deposition of copper onto silicon electrodes reports and summarize the research done on copper displacement deposition [1, 4, 3, 2] whose focus, within the context of

this thesis, has been to produce a seed layer for the metal electrodeposition processes for the layer transfer technology described in 6. The second parts report the result of experiments of copper electrodeposition into macro-PS layer. It is important to recall that the process described here are not compatible integrated circuit technology, in the presented implementation. Copper deposition, as described in this chapter, without any pre-deposited barrier layer, will bring silicon atoms in direct contact with the silicon surface. Nickel based electroplated seed layers have been investigated in [112, 113] as a possible solution to overcome this problem.

4.2 IMMERSION PLATING

Some metals can be deposited on a substrate (silicon) by dipping the substrate into the desired metal ion solution, without the need for electric generator. The solutions used in literature contain generally a metal salt (i.e. $CuSO_4$ or $(CF_3SO_3)_2Cu$) that is mixed with water or an organic solvent to form and an acid compound like H_2SO_4 to adjust pH [32, 114]. A reaction mechanism was first proposed by Jeske *[33]*. This process involves two different redox reactions at the silicon/electrolyte interface. The first redox involves silicon oxidation and copper reduction by holes injection into the valence band:

$$\begin{aligned} &\textit{oxidation}: && Si + 2H_2O + 2h^+ \rightarrow Si(OH)_2 + 2H^+ \\ &\textit{reduction}: && Cu^{2+} \rightarrow Cu + 2h^+ \end{aligned} \tag{31}$$

The second redox involves the oxidation of silicon hydroxide (to form silicon dioxide) and hydrogen evolution (the reduction) by electrons injection into the conduction band:

$$\begin{aligned} &\textit{oxidation}: && Si(OH)_2 + 2H_2O + 2h^+ \rightarrow SiO_2 + 2H^+ + 2e^- \\ &\textit{reduction}: && 2H^+ + 2e^- \rightarrow H_2 \end{aligned} \tag{32}$$

This mechanism implies injection current multiplication, although is an electroless process. This model was criticized by Harraz in [32]. In this model the two steps of oxidation have an energy $E^\circ = -0.85V$ versus Standard Hydrogen Electrode (SHE), so any aqueous solution of metal ions with a positive equilibrium potential should deposit metal by reducing the corresponding metal ions. Instead observations showed that only noble metals can be deposited on PS by immersion plating [115]. Fourier Transform Infrared Spectroscopy (FTIR), X-ray photoelectron spectroscopy (XPS) and XRD analyses of copper deposition from MeCN and Methanol (MeOH) solutions, confirm that PS oxidation accompanies the deposition of copper metal, and that in MeCN solutions, whereas oxide forms, no metal deposition occurs. To understand this phenomenon, the *rest potential* of PS exposed to a 0.01 M Cu solution has been measured and the results are shown in 54.

Organic solvent	Rest potential (V)	Metal deposition
MeOH	−0.20	Yes
EtOH	−0.25	Yes
DMSO	−0.37	Yes
DMF	−0.41	Yes
MeCN	+0.34	No

Figure 54: Rest potentials (V vs Ag/AgCl) of PS in 0.01M $(CF_3SO_3)_2$ Cu organic solutions [32].

The rest potential value in MeCN solution shifts to a "nobler" direction (more positive) and this could explain the inhibition of metal deposition. The potential shift is adducted to complex formation with the copper ions. The the current-potential curve in a MeCN solution of copper ions is shown in figure 55.

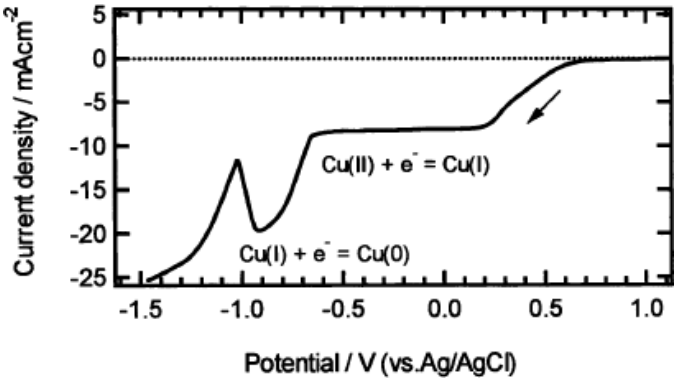


Figure 55: Current density-potential curve of platinum rotating disk electrode in 0.01 M $(CF_3SO_3)_2$ Cu MeCN solution containing 0.1 M tetra-*n*-butylammonium perchlorate as supporting electrolyte. The rotation rate and scan rate were 2000 rpm and 10 mVs^{-1}, respectively [32].

The result reveals a cathodic current plateau which is attributed to the reduction of Cu(II) to Cu(I) followed by a cathodic peak corresponding to the reduction of Cu(I) to Cu(0):

$$\mathrm{Cu(II)} + \mathrm{e}^- \rightarrow \mathrm{Cu(I)} \tag{33}$$

$$\mathrm{Cu(I)} + \mathrm{e}^- \rightarrow \mathrm{Cu(0)} \tag{34}$$

Then there is an increase in current density due to hydrogen evolution from the residual water. Further, it is shown that the recorded cathodic wave exhibits a peak current about twice that observed for the cathodic plateau current. This suggests that this plateau reduction current is the one-electron reduction from Cu(II) to Cu(I). The presence of a cathodic current plateau is indicative of the considerable stabilization of Cu(I) in MeCN solution.

Another experiment explains the importance of the rest potential in this process. Metal is deposited from a 0.01 M $(CF_3SO_3)_2$ Cu MeCN solution containing various amount of water (see figure 56).

Water content	Rest potential (V)	Metal deposition
Dehydrated MeCN,		
(~30 ppm)	+0.34	No
1000 ppm	+0.29	No
10 wt%	+0.28	No
50 wt%	−0.22	Yes

Figure 56: Rest potential of PS in 0.01 M $(CF_3SO_3)_2$ Cu MeCN solution containing various amount of water [32].

It can be seen that by varying the water content, the rest potential varies, and metal can or cannot be deposited. These results showed that copper deposition requires the presence of water; however, the effective water level varies with the organic solvent used. Another interesting result is that copper does not deposit from a MeOH solution on a non oxidized PS sample. This shows that the oxidation of PS is necessary for the deposition of metal on the surface of PS.

4.3 CHEMICAL DISPLACEMENT DEPOSITION

According to the previous section, oxidation of PS is necessary for the immersion-deposition of copper. In this section it is shown that, adding fluorine ions in the solution, it is possible to remove the oxidized layer. Experiments were carried on both n+ and p+ silicon wafers, with (100) and (111) orientations. In this section only experiments performed on n+ (111)-oriented are presented for brevity, the results can be immediately extended to the other type and, are reported in [4].

4.3.1 *Experimental details*

Monocrystalline antimony doped (111)-oriented Si wafers with a resistivity of 0.01 Ωcm were used to fabricate meso-PS according to the processes described in 3.2, using a mixture of HF (45 wt.%), H_2O, and C_3H_7OH in a 1:3:1 ratio by volume as electrolyte. The anodization has been carried on at 60 $^{mA}/_{cm^2}$ for 20 minutes, at RT. Such regime provided fabrication of PS layers 1000 nm thick with a 55% porosity (determined gravimetrically).

After anodization the porous silicon has been washed with DI without sample removing from the cell. In order to grow copper particles of different sizes two aqueous solutions were used:

1. 0.025 M $CuSO_4 \cdot 5H_2O$ + 0.005 M HF, this is the "standard" solution;

2. 0.025 M $CuSO_4 \cdot 5H_2O$ + 0.005 M HF + 0.1 M C_3H_7OH, IPA has been added as surfactant to this solution to increase wettability.

The copper deposition was carried out by the adding of 20 ml of the solution into the cell varying the time and temperature regimes. After copper deposition samples were washed with IPA and dried by the air flow at 40 C. The phase composition of the samples was studied by XRD with Cu K_α radiation, and the morphology by SEM images. The metric used to compute copper particle sizes is the *particle analysis* available in ImageJ [63]. The analysis has already been used for pore dimension computation, where a simple thresholding of the image was sufficient to extract the pore shape. In the case of copper particles, a "trainable classifier" based on neural networks has been necessary due to particles' complex geometry. The metric used to classify the particles is the usual "Feret's diameter."[1] The Feret's diameter is an accepted metric for microscopy analysis of random oriented particles. All analyzed images had an area of 4.463 μm^2 and a scale of 506.67 pixels/μm.

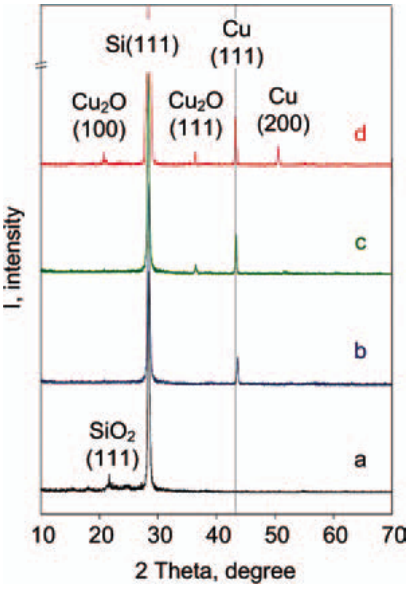


Figure 57: XRD patterns of PS immersed in $CuSO_4 \cdot 5H_2O + HF$ aqueous solution for: (a) 0 s, (b) 4 s, (c) 60 s, and (d) 180 s at 25 °C.

4.3.2 *Displacement deposition process*

After immersion of porous silicon in the solution for the copper deposition, a gradual color change of the sample surface from grey to red, is observed. That indicates the formation of the copper deposit on the PS. The process is accompanied by the release of gas. According to Morinaga [108], the cations of copper have much higher redox potential than silicon. That is the reason why Cu^{2+} reduction to atomic

1 Feret's diameter is the perpendicular distance between parallel tangents touching opposite sides of the profile.

form occurs by taking electrons from silicon in the following redox reaction equations:

$$\begin{aligned} &oxidation: && Si + H_2O \rightarrow SiO_2 + 4H^+ + 4e^- \\ &reduction: && Cu^{2+} + 2e^- \rightarrow Cu^0 \end{aligned} \tag{35}$$

The released gas has been the hydrogen in accordance to (35). A change in the deposit's color, from light to dark red, has been observed for prolonged deposition processes. This has been attributed to copper oxidation. To understand composition, phase and structure of the observed deposits XRD analysis has been done and presented in figure 57.

The figure presents the X-ray diffraction patterns of the porous silicon: (a) fresh and after immersion in the "standard" solution for (b) 4, (c) 60 and (d) 180 s. The XRD pattern for fresh PS (figure 57.(a)) shows the intensive peak of Si (111) and the weak peak of the native silicon oxide (111). However the silicon oxide peak has disappeared in the remaining XRD patterns (figure 57.(b-d)) that belong to the porous templates which have been immersed in the solution for copper deposition. As expected, hydrofluoric acid has removed native silicon oxide and provided Cu deposition on the oxide-free silicon surface according to the reaction:

$$SiO_2 + 6HF \rightarrow 2H^+ + SiF_6^{2-} + 2H_2O \tag{36}$$

Figure 57.(b) shows new peak related at the angle $2\theta = 43.66°$ after 4 s of immersion into the copper solution. It corresponds to the diffraction from the plane (111) of crystalline cubic face-centered copper; i.e. the amount of copper crystallized during the short deposition time has been enough to be revealed by XRD. After 60 s of immersions (figure 57.(c)) intensity of copper peak has increased and the angle has shifted to the position $2\theta = 43.36°$. The shift means an expansion of the lattice parameter of the copper crystals. Moreover, peak of cubic primitive Cu_2O (111) at $2\theta = 36.22°$ has appeared. The most complex XRD pattern is observed for the PS immersed in the solution for 180 s (figure 57.(d)). The intensity of the peak of Cu_2O (111) has increased. Noteworthy, several new peaks have appeared: cubic face-centered (200) copper and cubic primitive Cu_2O (100). The maximum of the Cu (111) peak intensity is observed at the angle $2\theta = 43.31°$. The deductions that can be done analyzing the results of the XRD analysis are :

1. at the initial stage of deposition crystalline copper has inherited the orientation of silicon but later it has lost the epitaxial properties;
2. copper lattice parameter has expanded with the immersion time increasing;
3. simultaneously with the copper deposition Cu_2O has formed.

4.3.3 *Surface Morphology of Copper*

To reveal the morphology of the PS samples after copper deposition SEM analysis has been performed.

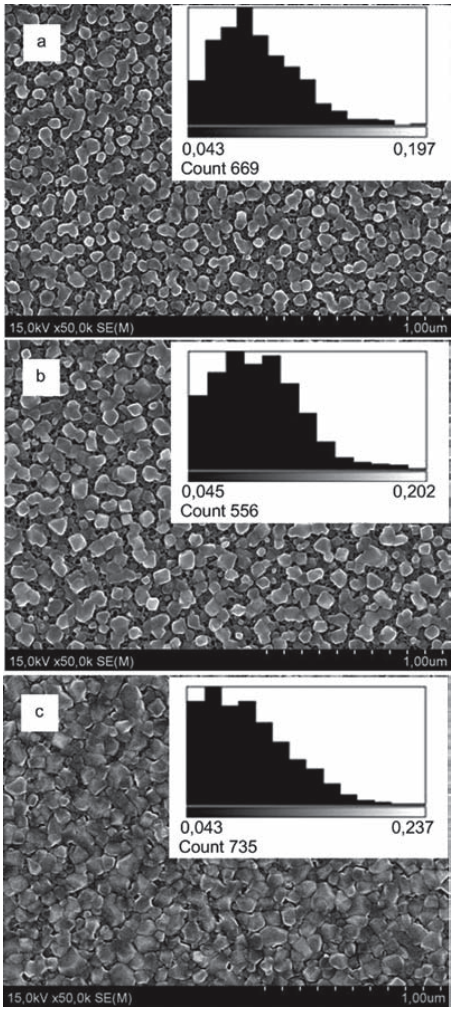


Figure 58: SEM top images and Feret's diameter histograms of PS immersed in $CuSO_4 \cdot 5H_2O + HF$ aqueous solution for: (a) 0 s, (b) 4 s, (c) 60 s, and (d) 180 s at 25 °C.

Figure 58 shows SEM top images and Feret's diameter histograms of PS immersed in the standard solution at 25 C for (a) 4, (b) 60 and (c) 180 s. The images show the layer of copper particles of different dimensions covering the porous silicon outer surface. There are quantitative characteristics of the distribution below each Feret's histogram. Common view of all Feret's histograms looks like an asymmetric bell that has right shoulder longer than left. It means irregular size distribution of copper particles. At the beginning of the process copper has deposited as separated particles of the diameter from 43 to 197 nm (figure 58.(a)). The density has been about 669 NPs per 4.463 μm^2 ($1.5 \cdot 10^6$ particles/cm^2). The increasing of immersion time has led to insignificant size growth of particles from 45 to 202 nm (figure 58.(b)). The body of the distribution bell has expanded in the area of large particles and their number has decreased to 556 (1.25 · 106 particles/cm2. That means connection of some particles has taken place. Further immersion of PS in the solution (figure 58.(c)) has resulted in the coalescence of particles into quasi-continuous copper film. Distribution "bell" has lost its left shoulder and the maximum of the dimensional range has shifted seriously to 237 nm as well as the density of particles increased to 735 per 4.463 μm^2 ($1.65 \cdot 10^6$ particles/cm^2). According to the SEM images the process of the copper deposition might be divided in two common stages:

1. copper particles nucleation and their growth;
2. copper particles coalescence into quasi-continuous film.

The density of particles has decreased between the nucleation and the formation of quasi-continuous film. This can be attributed to the image analysis method that considers the aggregates of particles as a single particle.

4.3.4 *Model of copper particles growth on porous silicon layers*

The outer surface of PS presents the alternation of silicon planes and the pore openings. Copper has deposited on the tiny areas of monocrystalline silicon (111) planes. The proposed phenomenological model of copper particles growth, on the outer surface of PS during the displacement deposition process, is summarized in figure 59.

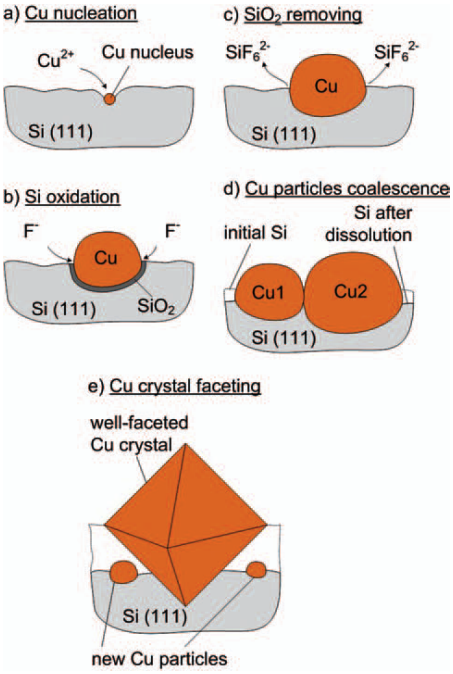


Figure 59: Phenomenological model of copperPS particles growth on PS skeleton.

At the moment of PS immersion in copper solution primary copper particles have nucleated (fig. 59(a)). Electron exchange between copper cations and silicon skeleton has been more likely to happen where defects are present, such as edge of pores, because of higher surface activity. At this point the redox reaction described by equation (35) occurs:

- Copper reduction requires two electrons from silicon, and silicon oxidation produces four electrons. The excess of electrons negatively charges the silicon skeleton that attracts copper ions (Cu^{2+}) to form a nanoparticle [108],

Simultaneously, corrosion of the oxidized silicon under copper particle takes place due the etching of silicon oxide by fluorine ions (figures 59.(b) and 59.(c)). The growth of copper particles has led to their connection (figure 59.(d)). Figure 59.(e) explains the silicon corrosion and the copper faceted crystals growth which have occurred due to the releasing of free silicon surface for the secondary particles nucleation.

Figure 59 considers the only case of copper (111) crystals formation, but XRD has shown copper (100) appearance when particles coalescence into film (figure 57(d)). Silicon and copper have the cubic face-centered structures of the lattice. Despite the difference of lattice parameters (a_{Cu} = 03615 nm, a_{si} = 0543 nm) such similarity is likely to allow epitaxial growth of copper on the monocrystalline silicon.

Figure 60 shows the different orientations of copper particles growing on different silicon planes around the pore wall, that is confirmed by experimental observations. It is known, that pore walls of PS have the branched morphology (figure 60.(a)). Walls of such pores represent extremely tiny silicon planes which are posed under different angles to each other. Figure 60.(b) shows an example of idealized silicon lattice of the pore wall in the entrance region (surface). Copper (111) has grown on the outer surface of silicon skeleton across the (111) silicon plane, while copper (200) has nucleated on the (100) edge plane of pore wall. Copper simultaneously crystallize in the different orientations on whole surface of PS from the moment of sample immersion in the solution. XRD analysis detects copper (111) only after 60 s of deposition (figures 57.(b) and 57.(c)), only because the deposited amount of copper (200) is below the sensitivity of XRD analysis. The dependence of the copper lattice parameter on the immersion time has been determined and reported in figure 61. An analysis of copper growth reveals that, at low immersion time, the lattice parameter of (111) copper particles is lower than the one of bulk copper. The parameter value increases with time up to the value of bulk copper, that is reached at 120 s. The expansion of lattice parameter with immersion time corresponds to the growth of copper particles. When the particles coalesce into a quasi continuos film, the parameter has a value of 0.3615 nm that corresponds to lattice parameter of bulk copper.

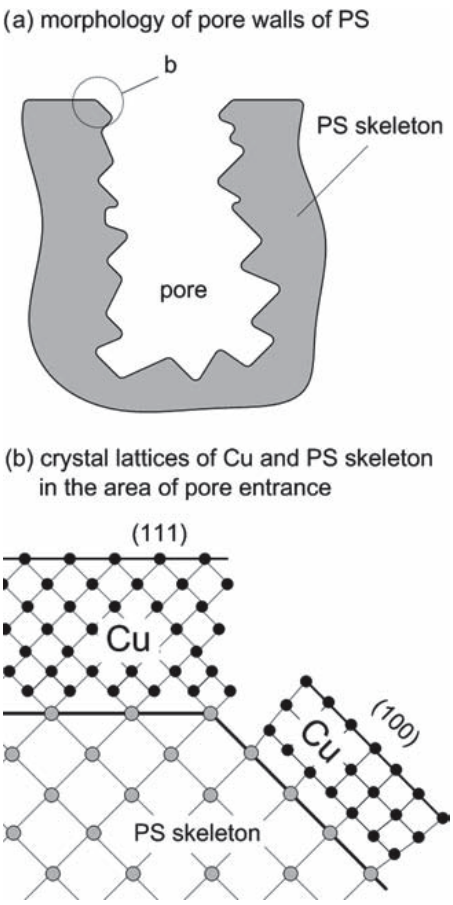


Figure 60: Growth of crystalline copper of different orientation on PS skeleton.

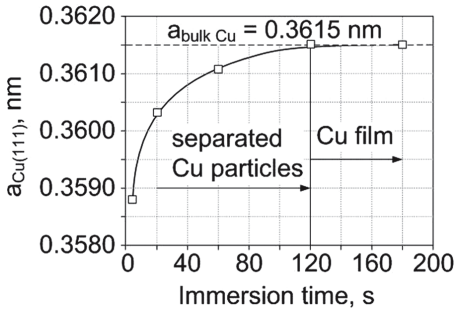


Figure 61: Lattice parameter a_{Cu} of Cu (111) vs immersion time.

The developed model explains the copper deposition onto PS layers and allows to predict the necessary conditions for depositing copper nanoparticles with assigned average dimension (e.g. for surface functionalization) or continuos film (seed layer for uniform electroplating). Additional experiments were done to evaluate the influence of temperature, in particular, experiments done at 10 C have shown a decrease of particles' average diameter for each immersion time. Observed particles average diameter range for 4 - 180 s immersion time range is 43 - 237 nm at 25 C and 23 - 128 at 10 C. The same effect of coalescence to a continuous film has been observed at 10 C. The effect of temperature is to alter the growth rate of the particles.

4.3.5 *Copper particle growth with surfactant*

The coalescence phenomenon observed preclude the possibility of growing isolated particles over a certain size. In order to grow separated copper particles of large sizes, isopropyl alcohol has been added to the solution for copper deposition (solution 2 with increased wettability). The exchange reactions have been accompanied with the hydrogen release (36). Active gas bubbling prevents coalescence of copper particles placed on the different edges of the pore. Isolated copper particles with maximum diameter of 512 nm have been grown with this solution at 25 C. IPA improves the wettability of the solution and provides fast reagent exchange inside of the pore channels, thus improving the uniformity of seed layers.

4.3.6 *I-V Characteristics of Copper-PS structures*

Analysis of the electrical characteristics of copper layer deposited with the displacement reaction has been done [1] on both (100) and (111) (n-type, 0.01 Ωcm) substrates with three different porosities: 45% (P45), 65% (P65), and 85% (P85). To obtain a continuos copper film, the immersion time has been 180 s for all samples and the standard solution have been used.

The results of the measurements are presented in figure 62. The IV characteristics present an exponential rise under forward bias condition, i.e. the Cu-PS contact forms a Schottky junction. The differential resistance grows with porosity and is higher on (100) substrates than

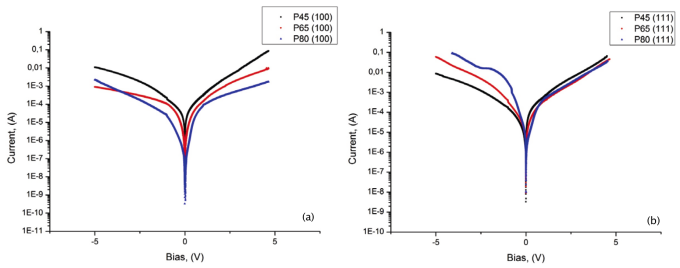


Figure 62: I-V characteristics of Cu/PS structures for (100) (a) and (111) (b) silicon substrates(n-type, 0.01 Ωcm).

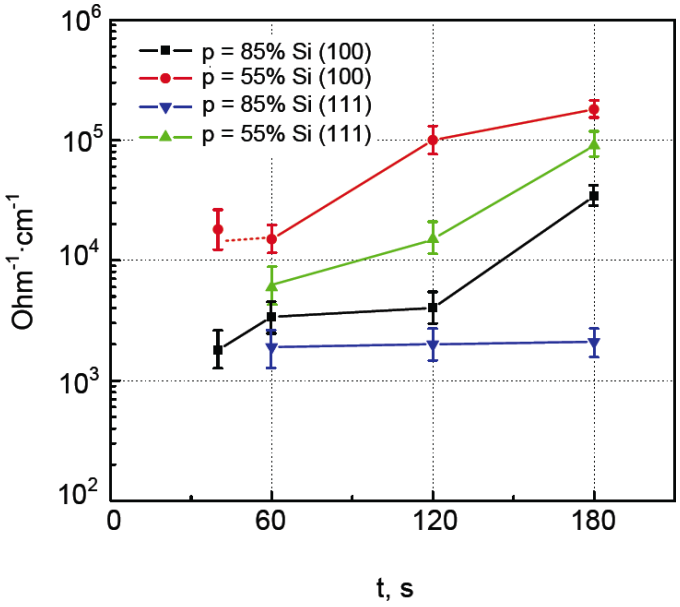


Figure 63: Conductivity of copper films deposited on PS using the immersion displacement deposition.

on (111). Reverse bias IV characteristics fit a power for voltages below -2V:

$$I = V^a \tag{37}$$

with a in the 0.5 - 2 range and then becomes linear. The magnitude or reverse current in copper to (100)-silicon contact is lower than direct current (a leaky rectifying contact has been obtained) and the differential resistance has the same values of the one in forward biasing. The differential resistance in reverse bias of copper to (111)-silicon contact decreases with the increasing porosity.

The electrical resistance of the copper film on PS surface has been measured and the results are shown in figure 63. Measurements were obtained from sheet resistance measurements (4-point probes) and the thickness of the deposited layer have been measured with optical profilometer to convert the sheet to bulk resistance.

The conductivity tends to increase with immersion time, and decreases with increasing porosity. The conductivity on (100)- oriented samples is higher than the one one (111)-oriented samples. The cause

of this difference is attributed to the oxidation of copper on that samples. XRD analysis [1] has shown the presence of the Cu_2O peak on that samples. It can be deducted that copper grown on (111) substrates tends to oxide more easily than on (100) substrates.

4.3.7 *Porous copper membrane*

Copper membranes formed on meso-PS have been studied for application in copper/polymer glares as a low cost manufacturing technology for flexible sensors [116]. The growth process is quite slow 7200 s (2 h) for a 8 μm thick membrane. The membrane was obtained from a 3 μm deep meso-PS (from 0.3 Ωcm p-type wafer) with a porosity of 60% that was totally converted to porous copper as no trace of the porous layer was present after membrane separation. The thickness of the membrane, higher than the PS template layer, suggests that copper deposition process occurred in two directions: towards the bulk of the silicon wafer, via silicon displacement and consuming the mesoporous template and, in the opposite direction, particle coalesced to form a uniform layer that continued to grow until separation from the substrate. Figure 64 shows SEM images of the cross section 64.(a), top side 64.(b), and bottom side 64.(c) of the separated membrane and related Energy-dispersive X-ray spectroscopy (EDX) point analysis which are considered in the next paragraph.

The membrane presents a two-layered structure of 8 μm thickness: the top surface (figure 64.(b)) was the sample/solution interface, while the bottom (figure 64.(c)) was connected with the substrate. The top layer has a thickness of about 5 μm and represents a tightly packed array of parallel column-like agglomerates which are perpendicular to the substrate, i.e., columns grew along the pore direction of the original PS layer. On the other hand, the bottom layer looks like a sponge of 3 μm thickness consisted of chains of small particles. Particle diameter in the two layers differs by more than one order of magnitude: particles in the spongy layer have diameters between 160 and 200 nm, and the ones on the upper layer between 2,500 and 3,500 nm (but with wider distribution as particles with 1.500 nm diameter were also found). The density of upper agglomerates is about $9 \times 10^2\ cm^{-2}$, while the density of the bottom NPs is four orders of magnitude higher ($9 \times 10^8\ cm^{-2}$ to $16 \times 10^2\ cm^{-2}$).

The most interesting characteristics of this structure is its Young's modulus. Young modulus measurements of the porous copper membrane were performed in air in the temperature range of −100 °C to 100 °C. In all experiments, the sample has been subject to an external sinusoidal stress at a frequency of 1 Hz. Measurements were conducted with the sample mounted in two different geometries in order to obtain the elastic modulus either perpendicular to the pore direction $E_\perp$, that is along the plane of the membrane, or along the

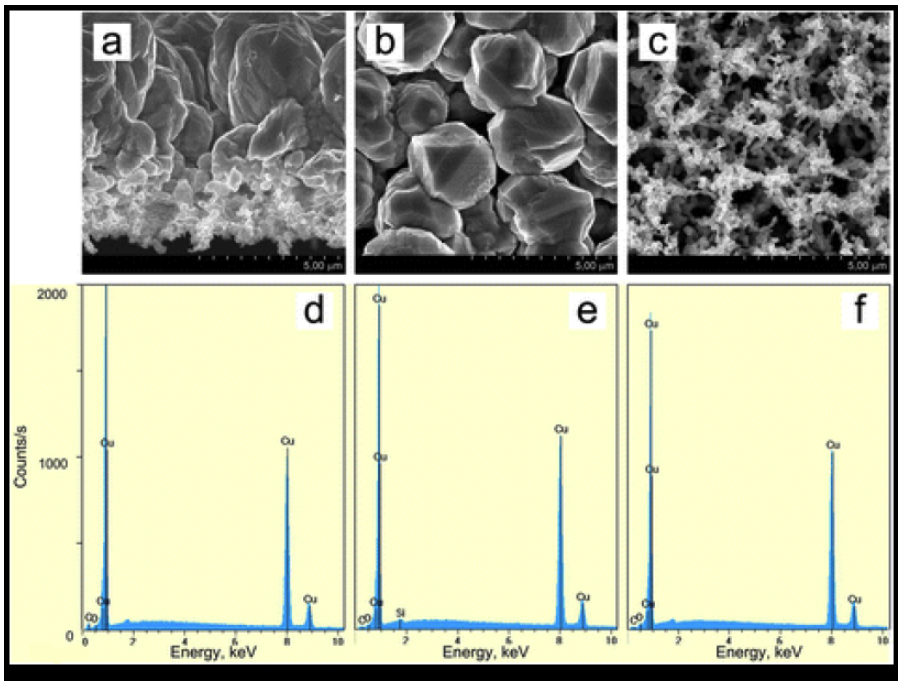


Figure 64: SEM (a, b, c) and EDX point analyses (d, e, f) of the porous copper membrane. The porous copper membrane was formed by displacement deposition of copper on 0.3 Ωcm p-type silicon for 7,200 s from the solution containing IPA (improved wettability); porous copper membrane was analyzed in cross section (a, d), top (b, e), and bottom (c, f).

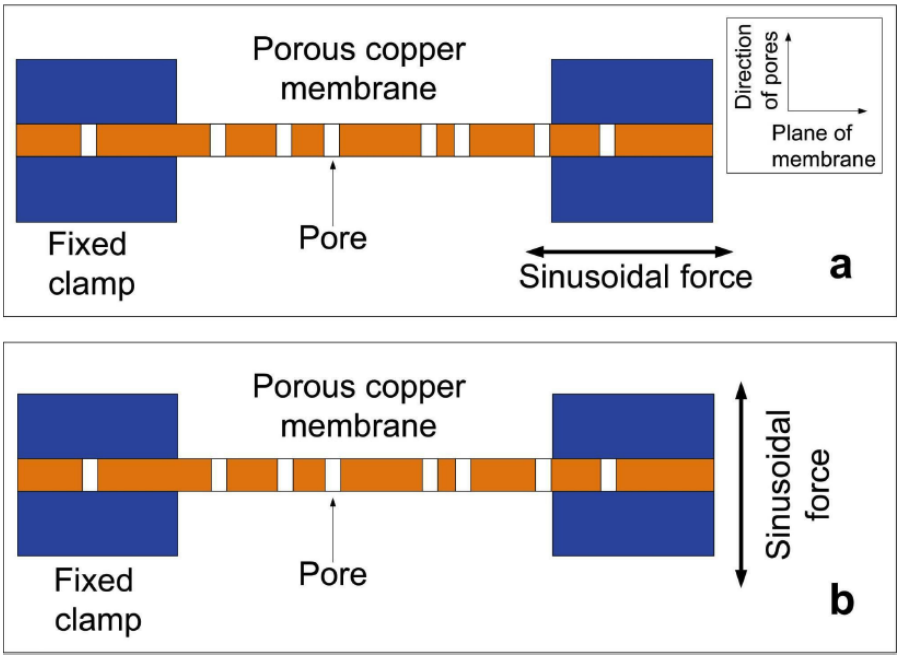


Figure 65: Schematic view of configurations for Young's modulus measurements: (a) Tensile configuration $E_{\perp}$, (b) cantilever configuration $E_{\parallel}$.

pore direction $E_{\parallel}$, that is perpendicular to the plane of the membrane. In the first case, the so called "tensile" configuration was used as it is shown in 65.(a): the sample is clamped between a fixed end and a mobile part, and an in-plane oscillating force is applied. A static load has been superimposed to the oscillating force in order to avoid buckling. In the second configuration, "single cantilever" experiment was performed: the sample was clamped between a fixed part and a mobile clamp which applies the force along the direction parallel to the pores and perpendicular to the plane of the membrane. The relative strains were kept below 1.2% and 0.4% in the tension and in the cantilever configuration, respectively. Preliminary measurements were performed identify the linear region of the stress–strain curve.

The temperature variation of the Young modulus $E_{\parallel}$ measured for the porous copper membrane during the flexural vibration and that of $E_{\perp}$ measured during the extensional vibration are reported in figure 66. In both directions, E increases at low temperatures, as usual in most solid samples. The measured values of the Young's modulus (both $E_{\perp}$ and $E_{\parallel}$) are much smaller than the value of E (110 to 128 GPa) for bulk polycrystalline copper, due to the high porosity and to the quasi-bidimensional feature of the membrane. It can also be noticed that the values of the Young's modulus along the two directions differ by a factor of 300 at low temperature and 500 at high temperature, indicating a strong anisotropy of the sample, which is stiffer in

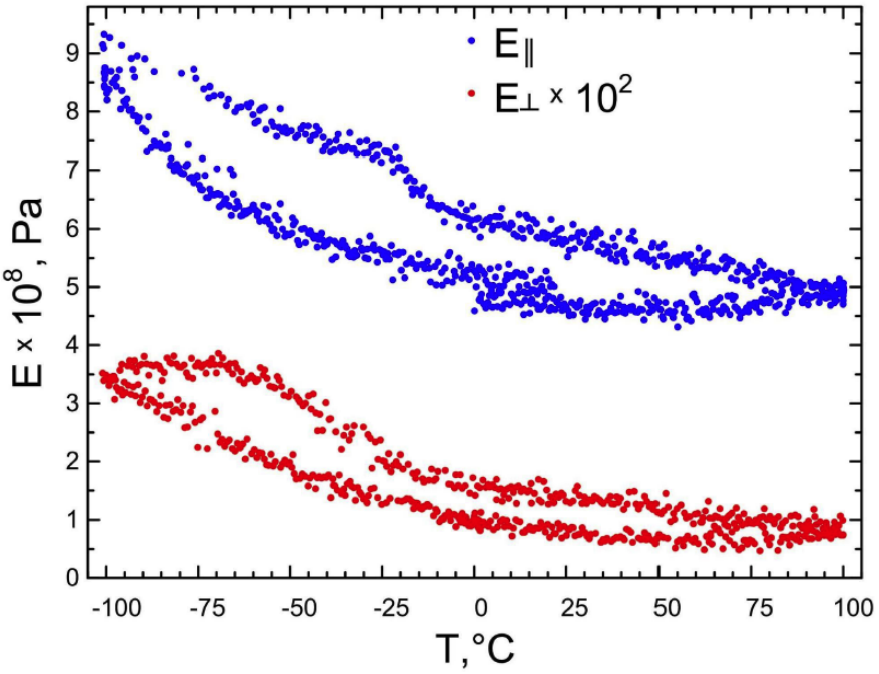


Figure 66: Temperature variation of the Young's modulus for the copper membrane. The modulus is computed in two directions: perpendicular and parallel to the porous structure.

the direction parallel to the pores, that is perpendicular to the plane of the membrane.

Recently, a systematic experimental and theoretical investigation of the elastic constants and of the Young's modulus of a block (approximately 10 × 10 × 10 mm^3) of polycrystalline copper containing elongated pores was reported in [117]. All crystallites had one crystallographic direction aligned along the [001] copper axis and another two randomly oriented in the perpendicular plane. The pores were oriented along the [001] direction, and their diameters ranged between 15 and 380 μm. In such a system, the values of $E_\perp$ and $E_\parallel$ strongly depend on the ratio of the axes of the ellipsoids associated to the pores. At low porosity (p < 20%), for pores having a high ellipticity, $E_\perp > E_\parallel$ [117]. However, both values decrease with increasing porosity and virtually reach a null value for p = 100%. However, while $E_\parallel$ decreases linearly with p, $E_\perp$ has a stronger dependence on porosity which leads to $E_\parallel > E_\perp$ for p > 20% [117] as in the case of the membrane grown on meso-PS.

Figure 66 also shows a clear hysteresis between cooling and heating in both vibration modes, which is reproduced upon subsequent cycling and could be possibly due to the absorption and desorption of gases on the porous structure.

4.4 ELECTRODEPOSITION

The realization of thick metal layer is not possible with the displacement deposition presented above. Thick, compact metal layer are needed for the realization of metal MEMS, as the compliant contacts presented in chapter 8 or the antennas presented in chapter 9. Other applications of microdeposition of metals on silicon include: catalyst, optical devices, discrete magnetic recording media [118], solar cells [119], and sensor [120].

The displacement deposition can be used to provide a seed layer to homogenize the following electroplating step. The electrodeposition of metals into PS has been studied in the past, with particular interest in deposition inside pores for the realization of Trough Silicon Via (TSV). The typical reactions involved in electrodeposition are:

$$\begin{aligned} &\textit{reduction}: && Me^{z+} + ze^- \rightarrow Me \\ &\textit{hydrogen evolution}: && 2H^+ + 2e^- \rightarrow H_2 \end{aligned} \tag{38}$$

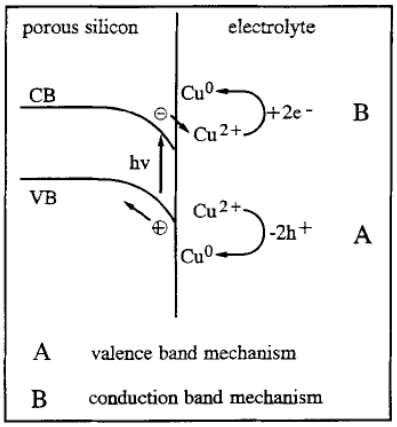


Figure 67: Reduction mechanism of copper on silicon electrodes [33].

The electroplating process is easier to control than displacement, through precise control of the electrical current flow. After a first period of nucleation the metals grows with nearly constant potential. It has been found that the electroplating over PS does not involve the oxidation of silicon like the immersion plating and, illumination of the samples increases the reaction rate. It is known, from semiconductor electrochemistry (figure 67) that reduction of Cu^{2+} ions happens only by *holes* injection into the valence band in dark, whereas under illumination it can involve electrons in the conduction band; these can migrate because of the cathodic band bending to the PS-electrolyte interface and there reduce Cu^{2+} ions [33].

Harraz [121] demonstrated experimentally that in immersion plating method, copper nucleation takes place into the entire surface of macropores, and thus the complete pore filling is not possible. On the other hand, in the electrochemical process, copper deposition takes place preferentially at the pore bottom, and from there up to the surface, thus allowing for complete pore filling. In figure 69 a cross-sectional image of macro-PS after electrodeposition, in the dark, at different process times.

The analysis of current-potential curves of the process (reported in figure 68) shows higher cathodic current (curve b) for the process under illumination, than the process in the dark (curve b). This is attributed to the generation of photoelectrons that could be transferred to the solution promoting Cu^{2+} reduction, and permitting hydrogen evolution (not possible under dark condition). Under illumination the copper deposition increases at the top-surface and around the pore walls, and not significatively at the pore bottom (see figure 70). So to fill all the pore is advisable to perform the process under dark conditions [121].

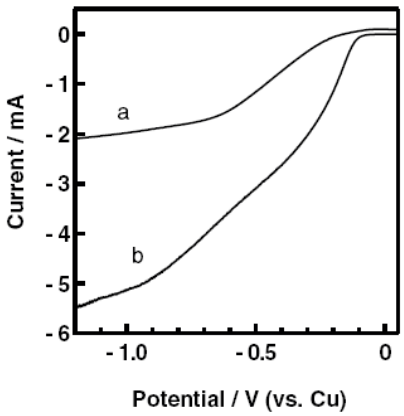


Figure 68: Current-potential curves of macroporous silicon measured in 0.1 M $CuSO_4$: (a) in the dark, and (b) under front-side illumination. The scan rate was 10 mV/s [33].

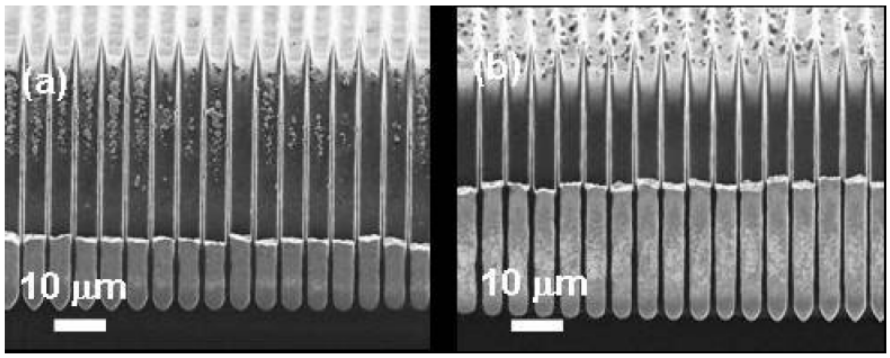


Figure 69: FE-SEM cross-sectional images of macroporous silicon after electrodeposition of Cu in 0.1 M $CuSO_4$ solution in the dark for: (a) 60, and (b) 120 min [33].

Fukami [35] extended the results obtained on macro-PS to meso-PS. With the aid of numerical simulations and experiments, he proposed that pores bottom can be a preferential current path because the pore wall acts as a series of resistances. There is difference between macro- and meso-PS processes, because of the substrate used. Silicon used for the formation of mesopores has, in general, lower resistivity. This lower resistivity makes electrodeposition more difficult in mesopores than in macropores, because high reaction rate leads to plugging at the pore opening. However it is possible to fill mesopores by depositing metal (copper) with low current. Besides he showed that mass transfer should be an important factor to control electrodeposition in mesopores. Figures 71 and show SEM images of copper electrode-

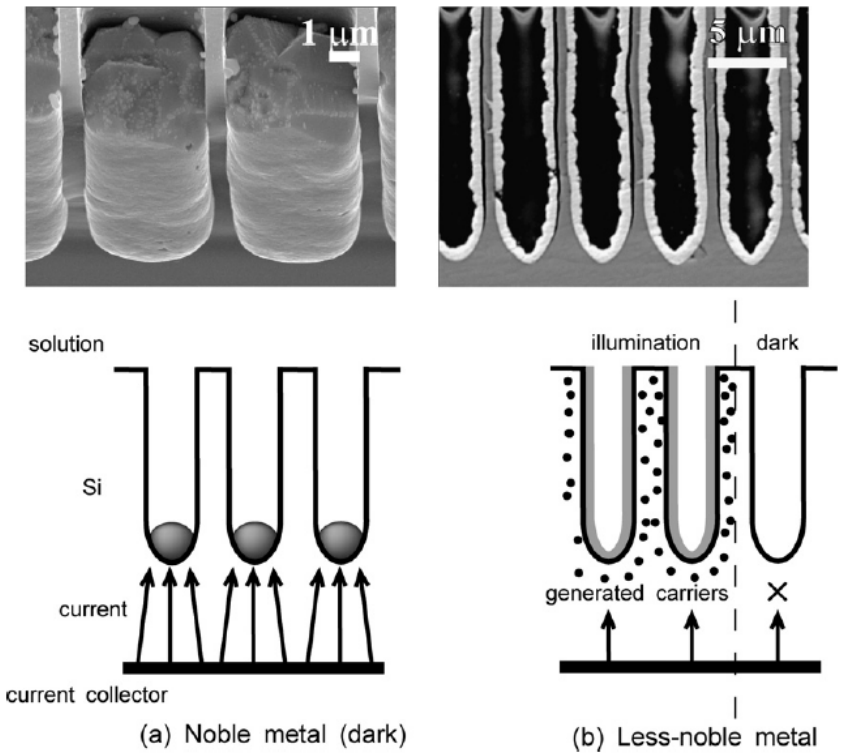


Figure 70: Pore filling with metal inside the macropores of p-type silicon. (a) Metal grows from the pore bottom in the dark when the valence band process is possible (noble metals). Preferential growth at the bottom results mainly from the current distribution. Microrods are obtained after dissolving the silicon substrate. (b) Electrodeposition does not take place for less-noble metals in the dark. Illumination generates electrons over the wall area and enables the reduction reaction on the wall leading to the formation of a microtube structure [34].

position into meso-PS. It is evident the infiltration of copper inside the mesopores for their total length (from EDX peaks) with a compact layer on the top of pores.

4.4.1 *Characterization of copper electrodeposition into macroporous silicon*

Macropore uniform filling has been obtained on samples with the morphologies presented in chapter 3 using the electrolyte

$$CuSO_4\ (10^{-2}\,M) + H_2SO_4\ (0.5\,M) \tag{39}$$

diluted in DI. Homogeneous pore filling occurs at a current density of 2 $^{mA}/_{cm^2}$ in dark. In figure 73 the characterization of the copper growth with time is shown. The main experimental problem in evaluating the homogeneity of thickness is that a cross section of the porous structure is needed and copper may jump out of the pore during cleavage.

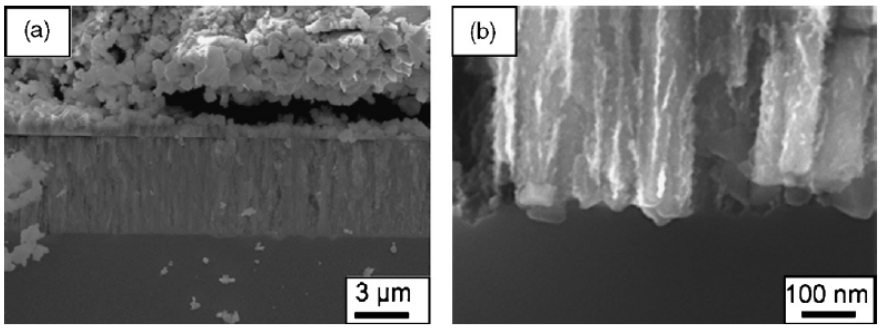


Figure 71: Cross-sectional views of the mesoporous silicon with 4 μm depth after the copper electrodeposition at $-5A$ for 2 h (sample area$0.79cm^2$): (a) low magnification image, and (b) high magnification image [35].

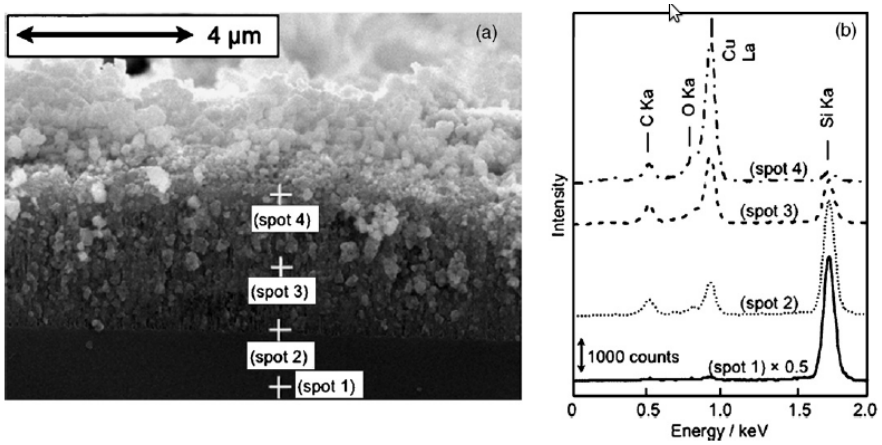


Figure 72: Copper electrodeposition in mesoporous silicon: (a) cross-sectional view of the mesoporous silicon after the copper filling (same process as in figure (71)); (b) EDX spectra analyzed at identified spots in (a). The solid, dotted, dashed and chain lines indicate the EDX spectra at the spots 1, 2, 3 and 4, respectively [35].

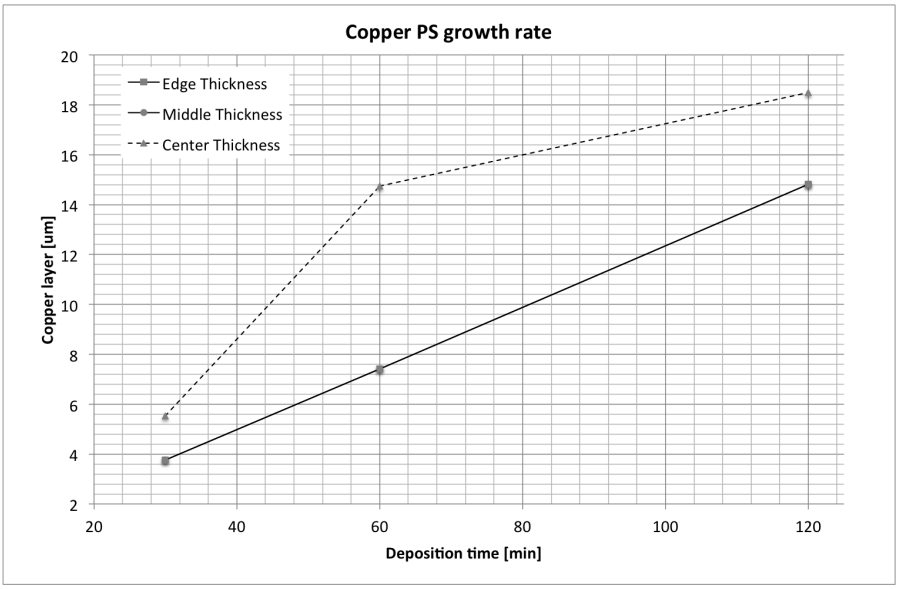


Figure 73: Copper electrodeposition process rate.

The values of copper growth rates for the three different regions of the sample are:

- Edge 0.12 $\mu m/min$
- Middle 0.16 $\mu m/min$
- Center 0.16 $\mu m/min$

The SEM image of a fracture in the macro-PS layer (see figure 74) reveal that nucleates at the pore tip and grows filling all the pore. The deposited copper follows the profile of the pores without voids.

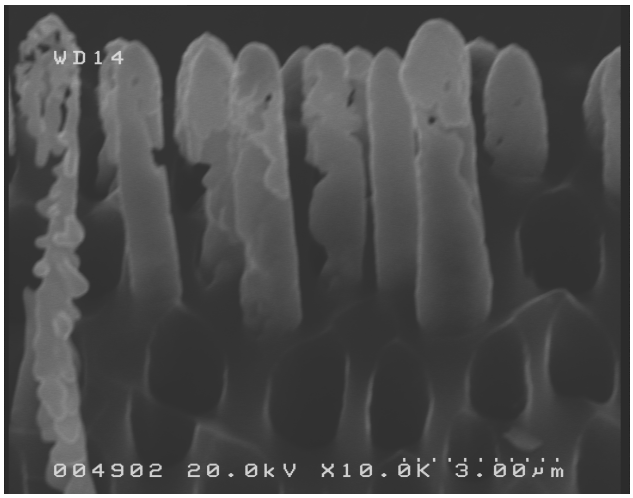


Figure 74: SEM image of the base of the pores obtained in a fractured region of the macro-PS layer.

Electrodeposition experiments were performed on both random and ordered macro-PS, as can be seen in the optical microscope images in figure 75. The images on random macropores (figure 75.(a,b)) do not give the certainty that all of pores are filled, however the one on ordered layers (figure 75.(c, d)) present a more homogeneous filling. This difference is due to the cleavage process, as introduced, before that detaches the copper from the silicon template. This phenomenon is more evident in macropores, probably because the cleaving plane cuts the pores in random positions and copper plug randomly stick to one side or the other of the cut.

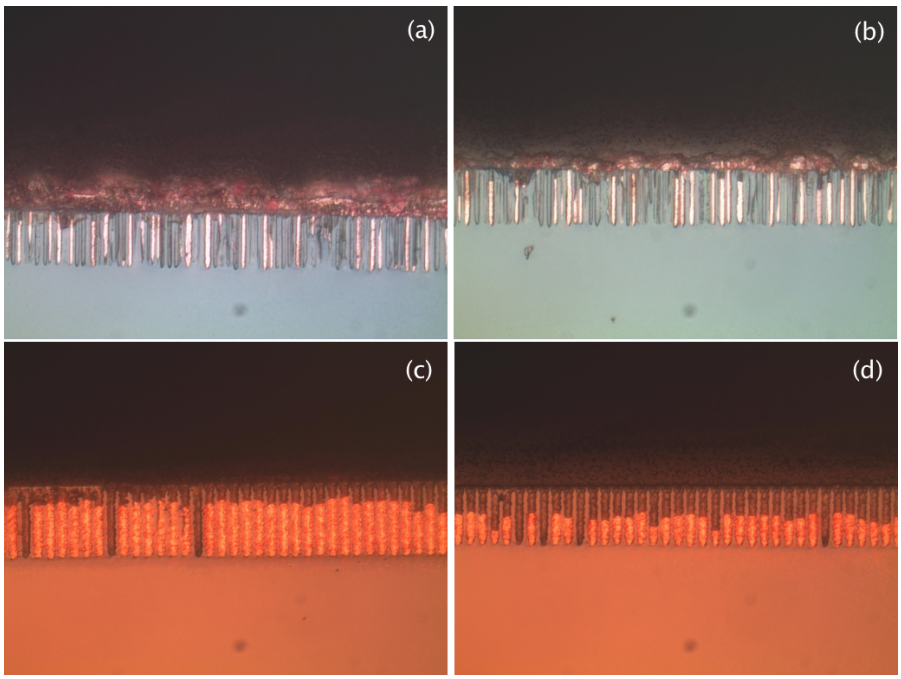


Figure 75: Examples of macroporous structures filled with copper. Both random macropore layers (a,b) and ordered have (c,d), have been filled. The macropores were grown into 10-20 Ωcm (100)-oriented, p-type wafer.

5

POROUS SILICON SUPERHYDROPHOBIC SURFACES

5.1 INTRODUCTION

In recent years Superhydrophobic Surface (SHS) [122] have increasingly attracted the interest of the scientific and technological community thanks to their self-cleaning properties and to the large wall-slippage they present for liquid water [123]. Natural Superhydrophobic Surfaces (SHSs) have been observed in plant leaves (Lotus) and insect wings and are characterized by large contact angles, low contact angle hysteresis and large slippage. The typical feature of natural SHSs is their micro/nano scale roughness where air bubbles can get trapped. The presence of the air-water interface is the cause of the surface's low contact angle hysteresis, and slippage. Several research groups have been working towards the development of synthetic SHSs capable of mimicking the roughness hierarchy of natural SHSs. The air-trapping capability of a surface alone is not enough for SHS application to microfluidics. A crucial issue, indeed, is the stability of the Cassie state [124], since trapped bubbles, under environmental fluctuations, could lead to the transition to the Wenzel state, with water filling completely the roughness elements. A strategy to fulfill this requirement is combining surface morphology modification and hydrophobic coating. The Cassie-Wenzel transition threshold is actually affected by the liquid-solid interface energy which can be significantly reduced by appropriate surface coating, e.g. silane layer deposition. A promising approach to produce robust and economical silicon SHSs is the use of macro porous silicon surfaces. The wetting properties of porous silicon strictly depend on the surface morphology, in particular on the pore diameter and porosity. Nanoporous silicon is reportedly highly hydrophilic [125], while macroporous silicon, without surface coatings, can be either highly hydrophobic [125], or hydrophilic, depending on the electrolyte and silicon doping type and level. SHSs characterized by contact angles in excess of 150° have been recently obtained from pSi surfaces by morphology modification and/or coating of the surface with a low surface energy layer [125, 126]. Macro-PS surfaces realized with the processes described in 3 have been characterized for hydrophobicity/hydrophilicity [6, 5]. The interest in these surfaces lies in their easy-to-implement and economical manufacturing process. Particular attention has been devoted to the development of a CMOS compatible process, to open the possibility of integration of SHS in standard ICs. The advantage of such an approach becomes

clear when considering the increasing miniaturization of lab-on-a-chip devices that could benefit from electronic control and actuation of microfluidic circuits.

5.2 SURFACE PREPARATION

The sample SHSs are realized, from 10-20 Ωcm resistivity, boron doped, p-type silicon wafers with (100) orientation. The organic electrolyte, HF (48 wt%):DMSO 10:46 by volume, has been used to obtain macropores. Before anodization silicon wafers were cleaned for 10 minutes in *piranha* solution (H_2O_2 (30%) : H_2SO_4 (30%) 1:3 by volume) for 10 minutes, rinsed in DI for 5 minutes and dried with nitrogen. Each wafer has been cut in square chips of approximately 2.5 cm edge. Silicon chips have been dipped in BOE solution and rinsed for 5 minutes in DI and dried in nitrogen before being processed.

Immediately after the anodization process, silicon chips are rinsed in DI water for 5 minutes and dried with N_2. The porous surfaces are then activated in an oxygen plasma (50 sccm O_2 at 200 mTorr for 3 minutes) and coated with perfluorooctyltrichlorosilane via Low Pressure Physical Vapor Deposition (LP-PVD). In addition, the effect of acetone washing on silanized samples is investigated, by performing a 4 min sonication of part of the samples.

5.3 POROUS SILICON MORPHOLOGY

Porous silicon morphology, in particular at the surface, determines its superhydrophobic behavior. The pore morphology depends in general on wafer type, doping density, crystal orientation, electrolyte type, HF concentration in the electrolyte, anodization current density, illumination intensity and anodization time. An extended survey of such morphologies is reported in chapter 2 and in chapter 3. To be effective as SHSs, macro-PS layers should have a depth greater than 10 μm, to disfavor the transition to the Wenzel state, as will become clearer in the next section.

The porous surfaces have been prepared using three different anodization current densities: named A, B and C, reported in table 5. The highest current density has been chosen to be the half of electropolishing threshold, to obtain uniform, reproducible, porous surfaces. The lowest values has been chosen to grow 10 μm deep pores with a process time of 30 minutes to reduce the effect of wall dissolution.

5.4 CONTACT ANGLE MEASUREMENTS

The the sessile drop method has been adopted to measure the Contact Angle (CA) over the porous silicon samples. Images of millimeter size

Process	Current density [mA/cm^2]	Time [min]
A	5	30
B	10	30
C	15	15

Table 5: Process parameters for the porous silicon surfaces.

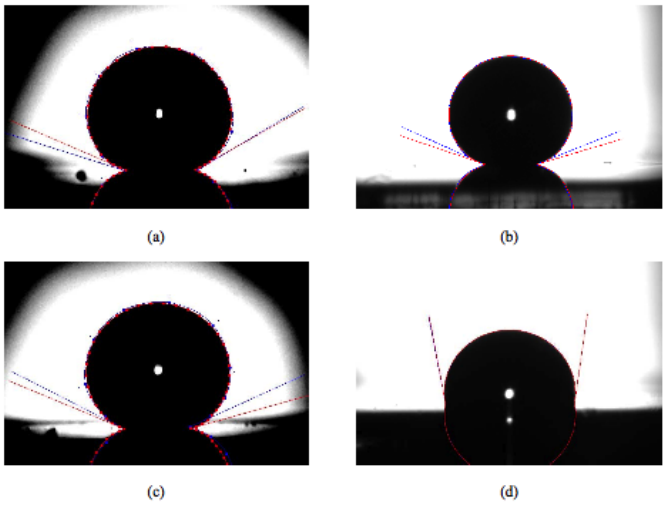


Figure 76: Contact angles on selected silanized samples: (a) sample 1, (b) sample 2, (c) sample 3 as defined in table 6, corresponding to processes A-C, respectively in table 5; (d) silanized flat silicon wafer.

sessile DI water drops, at rest over horizontal samples, were taken with a single reflex camera equipped with a 60mm lens, and processed with the freely available software Drop-Snake [127], to measure contact angles.

In figure 76 some representative results of image analysis are shown. In particular, panels (a)-(c) show drops sitting on porous silanized samples obtained, respectively with the processes A-C in table 5. The (d) panel, instead, shows a sessile drop on a smooth silane coated silicon wafer.

The Drop-Snake software requires a user-defined detection of the drop boundary (the blue solid line in the figures), which is used as initial guess for the B-spline fitting of the drop boundary. The red solid line is the final computed boundary whence the left and right contact angles are measured. Further details on the software implementation and accuracy may be found in [127]. The contact angles extracted with Drop-Snake are found to be robust to small changes in the user-defined definition of the drop boundary. The average contact angles are reported in table 6.

The averages are computed by analyzing at least 5 images of a sessile drop on the same sample, recorded after moving the drop on

Sample	Process	Acetone wash	Macro-PS	Contact Angle [°]
1	A	NO	YES	156.0 ± 1.6
2	B	NO	YES	154.5 ± 1.5
3	C	NO	YES	160.8 ± 1.6
4	B	YES	YES	152.8 ± 1.1
5	-	NO	NO	98.5 ± 1.6
6	-	YES	NO	156.0 ± 1.6

Table 6: Static contact angles on realized SHSs. The effect of surface morphology (see table 7 for pore characteristics) and acetone wash is highlighted.

Process	Pore depth [μm]	Pore diameter [μm]	Pore area [μm^2]	Pore Perimeter [μm]	Porosity [%]
A	13.2	1.88 ± 0.53	2.24 ± 0.94	5.77 ± 1.61	$55.5 - 61.6$
B	14.6	1.84 ± 0.70	1.79 ± 0.89	5.83 ± 2.50	$68.8 - 70.6$
C	14.3	2.42 ± 0.82	3.28 ± 1.44	7.47 ± 2.69	$69.5 - 69.7$

Table 7: Characterization of the superficial porosity: Diameter of the pores, area and perimeter as evaluated from top SEM images. Pore depth is evaluated from cross section SEM images.

different positions of the observed region, to average the effect of local morphology on the contact angle, that is one of the causes of contact angle hysteresis. For the same reason, right and left contact angles of drops are averaged.

5.5 SURFACE ANALYSIS

SEM images and the ImageJ [63] software have been used to characterize the porous surfaces (see figure 77). The porosity value has been computed from the surface topography by counting the percentage of pixels whose intensity is below a set threshold. As can be seen from figure 77, fully developed pores appear black with well defined perimeter while shallow pores appear as dark gray areas.

The measured porosity is the "surface porosity" of the sample, that is, the area fraction occupied by depressions. Pore depth has been computed from cross sections of cleaved samples (figure 77, right half). All the images were taken at an angle of 63° as this is the maxi-

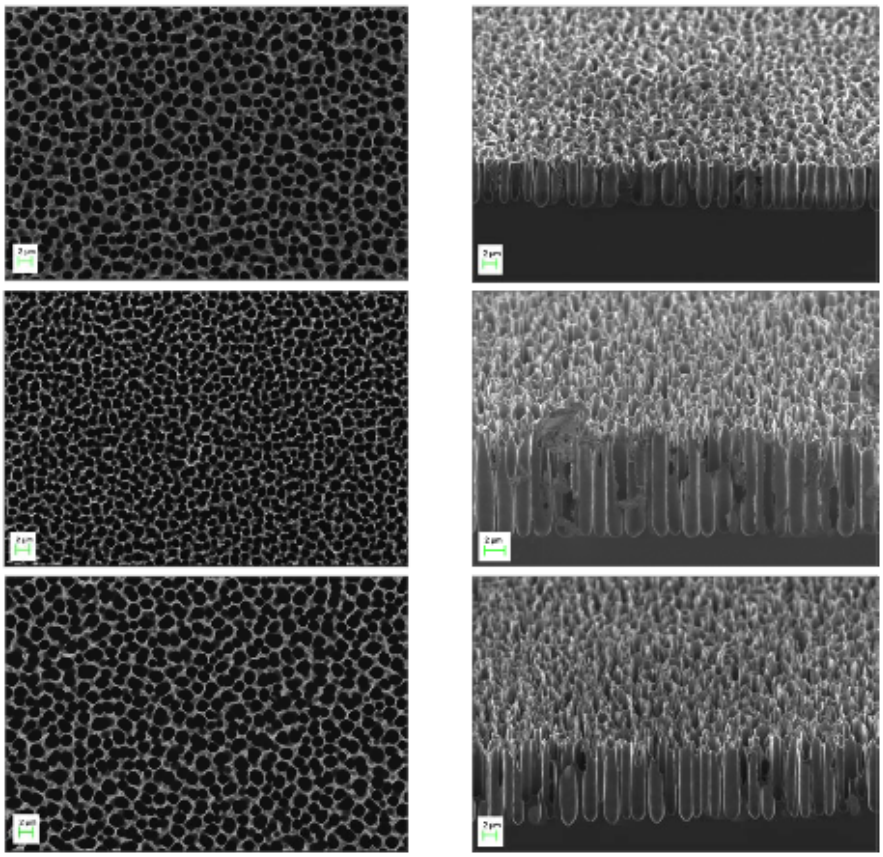


Figure 77: SEM images of macroporous surfaces (top images on left column, 63° tilted cross sections on right column) obtained with the processes detailed in table 5: images are ordered from A to C as they appear in the table. The scale on the images corresponds to $2\mu m$.

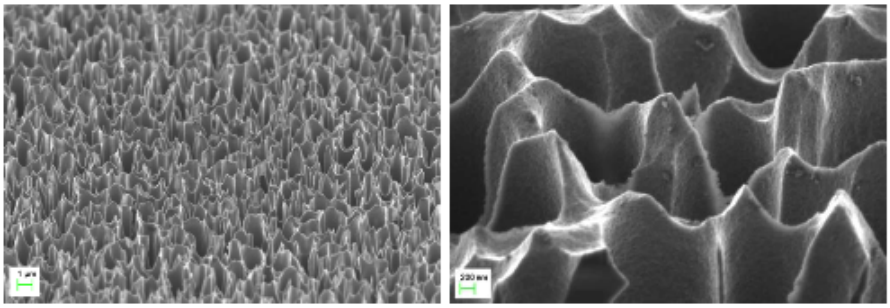


Figure 78: Surface of the sample obtained with B process (10 $^{mA}/_{cm^2}$, 30 min). Shallow inter-pores are visible as well as the partial dissolution of pore walls.

mum angle allowed by the microscope stage. Some silicon fragments are visible in cross sectional images, due to imperfect cleaving. Sample cross sections clearly show the morphology of pores. Straight, open, pores with uniform depth extend in the silicon bulk.

Cross sections show that, after the porosification process, the silicon fraction far from the surface is still relevant. Furthermore, from top view images, it is evident the continuous structure of the pore walls. Both characteristics contribute to the mechanical stability of the surface. Such an ordered situation does not exists close to the sample surface, as figure 78 clearly shows. The presence of inter-pores and the partial dissolution of pore walls confer roughness to the surface, contributing to its hydrophobicity.

Three figures have been chosen for surface characterization: pore Feret's diameter, area, and perimeter. The distributions of the parameters have been computed with ImageJ particle analysis tool. A summary of surface characteristics, as obtained with the three processes in table 5, is reported in table 7. It is noted that the inter-pores dissolution increases with increasing current densities, leading to a spiked surface and pore overlap. As a result the pore perimeter increases and circularity decreases.

5.6 SURFACE CHARACTERIZATION

Table 6 summarize the contact angle measurements under different experimental conditions, with the aim of investigating the effect of:

- surface morphology,
- low energy coating.

It has been observed that non-coated samples are hydrophilic, presenting contact angles of 75° on smooth samples and almost total wetting on porous ones. Only contact angles after silanization are reported in table 6. cases 1-3 refer to silanized porous surfaces obtained,

respectively, with the processes A-C of table 5. For instance, after anodization at 10 $^{mA}/_{cm^2}$ for 30 minutes (case 2) and silanization, the resulting contact angle is 154.5° ± 1.5°. This figure shows that the presented method is successful in providing highly hydrophobic silicon surfaces. By comparing cases 1-3, it is observed that the sensitivity of contact angles to process parameters -that is, density current and anodization time- is very low. This is due to the fact that, below the electropolishing level, the surface porosity and pore diameter vary only slightly with free parameters.

In view of microfluidic applications, the tolerance on process parameters to obtain SHS with controlled wetting properties is a positive fact. The evidence that an effective surface energy modification was prompted by the silane LP-PVD is provided by the contact angle of 98.5° ± 0.6° measured over silanized smooth silicon surfaces, corresponding to the static Young angle (case 5). This value is in line with the experimental contact angle values reported in [128] for surfaces coated with various silane types. This value is also compatible with that reported in the molecular dynamics simulations of [129] for Octadecyltrichlorosilane (OTS) coated crystalline silicon. The influence of surface morphology on the contact angle is reflected in the largely different values reported in for cases 2 and 5, and is immediately evident by comparing panels (b) and (d) in figure 76. The effect of organic solvent washing of the coated samples was tested by performing an acetone sonication of the samples. The cleaning procedure is applied to both porous and smooth silicon surfaces, corresponding to cases 4 and 6 of Table 6, respectively. Acetone wash may be effective in removing excess silane deposited physically but not grafted on the surface. However, only slight variations in contact angles were detected. A possible explanation of these small variations is the effective cleaning from surface contaminants obtained with the acetone wash.

5.7 WETTING MODELS

The two classical models are compared in order to interpret the reported experimental data in relation to the surface morphology. In particular, the increase of contact angle between porous silicon samples and smooth ones is analyzed in view of Cassie and Wenzel models. In the Wenzel model, the liquid is assumed to fill in completely the roughness profile. The variation in CA of a rough surface with respect to a perfectly smooth one is ascribed to the larger solid-liquid interface. According to the Wenzel model, the contact angle θ_w is given by:

$$\cos\theta_w = r\cos\theta \tag{40}$$

where r is the ratio of the actually wet area to the projected area of the surface and θ is the Young contact angle on the smooth surface

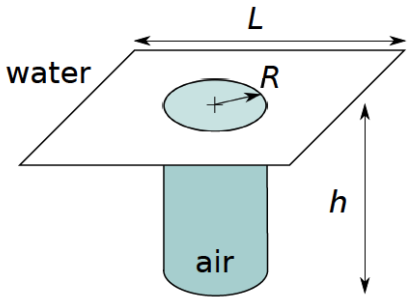


Figure 79: Idealized lattice used to model the macro-PS surface used for calculation. Air is trapped inside the cylindrical pore of radius R and height h. Water is in contact with the whole (periodic) cell of lattice constant L and area L^2.

having the same surface composition. In the experiments, the value of θ is computed as an average of cases 5 and 6 of table 6.

In the Cassie model, air bubbles are trapped within the pores and the liquid is in contact with the solid only at the peaks of the roughness. The resulting contact angle θ_C is:

$$\cos\theta_C = -1 + \varphi_S\,(1 + \cos\theta) \tag{41}$$

where φ_S is the solid fraction of the interface, i.e. the ratio of solid-liquid area to whole droplet base. Though liquid droplets can be observed in both states, the truly superhydrophobic one is the Cassie state which promotes water slippage and low CA hysteresis. Informed by the analysis of the SEM images, it is possible to provide an estimate r and φ_S. In particular, φ_S coincides with the complement to unity of the surface porosity χ, that is $\varphi_S = 1 - \chi$. The estimate of r is less straightforward. An ideal surface is considered, where each pore is perfectly circular and pores are regularly distributed on a periodic square lattice of size L (see figure 79). In this idealized scheme, the following relation between L, φ_S, and R withstand:

$$L^2\,(1 - \varphi_S) = \pi R^2 \tag{42}$$

that, after some manipulations, leads to:

$$r = \varphi_S + (1 - \varphi_S)\left(\frac{2h}{R} + 1\right) \tag{43}$$

This expression is still valid if the pores are not on a regular lattice. However, formula (43) is not appropriate in the case that pores overlap. Some overlaps actually happen as apparent in figure 78 and the surface morphology is more complicated than the ideal case we are considering, nevertheless equation (43) still provides a rough estimation of r.

Process	r	φ_S	θ_W	θ_C [°]	**Penetration** [μm]
A	17.44	0.41	non-wetting	131	1.25
B	23.12	0.30	non-wetting	139	0.55
C	17.45	0.30	non-wetting	138	1.01

Table 8: Summary of the geometrical features of the surfaces and related classical wetting models predictions for contact angles. The last column reports the wet depth d as obtained from the mixed model in equation 44

Using the geometrical characterization of the surfaces in table 7, along with the average contact angle value measured on smooth silicon surfaces computed from cases 5 and 6 in table 6, that is, $\theta = 100°$. Table 8reports the predictions for contact angle values corresponding to the models described by equations (40) and (41). For all processes, the Wenzel model leads to a left hand side of equation (40) smaller than -1. While this value has no direct physical meaning, it has to be noted that the closest physically significant case of $\cos\theta_w = -1$ corresponds to the perfectly hydrophobic state, where the surface is not wet and $\theta_w = 180°$. These considerations suggest that the Wenzel model is not adequate to explain the phenomenology on the considered morphology, and that, reasonably, the roughness profile is not fully wet. This tendency is reasonable in view of the high aspect ratio of the pores that causes the Wenzel state to be extremely energetically unfavorable. The Cassie equation (41), along with the solid fraction values of table 8 and the experimental value $\theta = 100°$, yields contact angles in the range θ_C=130° - 140° , depending on the process details, with the higher values corresponding to the lower solid fractions. However, the experimental contact angles on porous surfaces of table 6 are larger than the Cassie estimates, while smaller than the perfectly hydrophobic surface towards which the Wenzel model tends. A possible explanation of the discrepancies between the experimental data and the Wenzel and Cassie models may be found in the partial filling of the pores. This phenomenology is intermediate between the limiting cases of the fully wet surface and the "fakir" state, embodied by the Wenzel and Cassie models, respectively. A simple model for this scenario is now presented. Lets suppose that the pores in regular lattice previously introduced, are filled with water up to a certain depth d. The contact angle is then given by the weighted average of the cosine of contact angles, see [122]:

$$\cos\theta' = \sum \cos\theta_i = \varphi_S \cos\theta + \frac{p \cdot d}{A} \cos\theta - (1 - \varphi_S) \tag{44}$$

Here p is the total perimeter of the pores and A is the total area of the considered SEM image. Therefore the factor corresponds to the ratio between the lateral surface of the pores and the projected area. The first term on the right hand side of equation (44) represents the

contribution to the average of the liquid-solid interface having contact angle θ. Eventually the third term on the right hand side results from the air-liquid interface, as already seen in the Cassie equation. Substituting in equation (44) the experimental data $\theta = 100°$ and θ' as in table 6, an estimate for the wet depth d can be provided.

Results for the three process analyzed here are reported in table 8 and lie around 1 µm. This value appears reasonable in view of the SEM images reported in figure 77, but provides only a consistency check on the model.

In conclusion, it can be stated that silane coating of macro-PS surfaces roved effective in stabilizing the superhydrophobic Cassie state, allowing for persistent air trapping within the pores. Measured contact angles exceeded 150°. The resistance of the coating to organic solvents was also tested, showing good characteristics. Comparison of contact angle measurements with the available wetting models for heterogeneous surfaces suggested a partial filling of the pores, probably connected to the presence of interpore pitting.

Part II

CRML AND BURIED CAVITY TECHNOLOGIES

This part describes two technologies developed with porous silicon layers. The first is the CRML (Controlled Release Metal Layer) technology, a new MEMS technology that allows the realization of arbitrarily shaped three-dimensional free standing metal structures that can be integrated on integrated circuits by simple bonding process. The second one is a technology for the realization of buried cavities on silicon wafer, that can be exploited in microfluidics applications.

6

THE CONTROLLED RELEASE METAL LAYER TECHNOLOGY

This chapter describes the fundamental processes involved in the realization of the CRML technology. Mesoporous silicon layers are used to allow or to prevent (depending on porous layer characteristics) the release of a thick metal layer from the silicon wafer. The metal layer will form the three dimensional interconnections.

CRML is a layer transfer technology that uses porous silicon as Sacrificial Layer (SL). In a layer transfer technology (see fig. 80) a Transferred Layer (TL) is brought from a first substrate, identified as Seed or Support Wafer (SW) in figure 80 to a second substrate called Handle Wafer (HW) by a bonding/splitting process. In the first process step the TL is bonded to the HW and, subsequently, the sacrificial layer SL is removed or broken to complete the transfer. Layer transfer technologies have been developed to handle fragile layers during processing or to assemble layers grown on different substrates; there are three possible variations of such technologies, as shown in fig. 81 (showing silicon wafer as support and porous silicon as sacrificial layer).

In the first variation (A), integral layer transfer is considered, in the second, the transfer of a pattern onto an handle wafer is shown (B) and in the third (C) the embedding of the transferred layer into the handle. In the first two variations, a uniform PS layer is formed on the silicon wafer and, in the last one, porous silicon is formed only in the areas corresponding to the transferred pattern. The embedding into an handle wafer can be done, in principle, even with a uniform PS layer but this is not convenient in practice due to the porous nature of the sacrificial layer. In this case, the HW is a soft material (e.g. a poly-

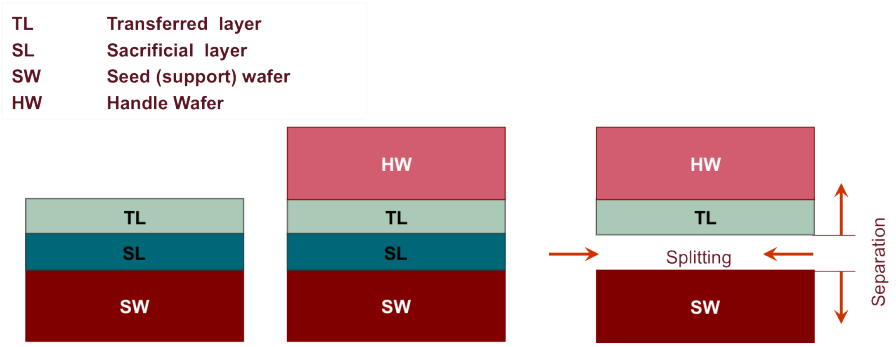


Figure 80: Layer transfer technology definitions and steps.

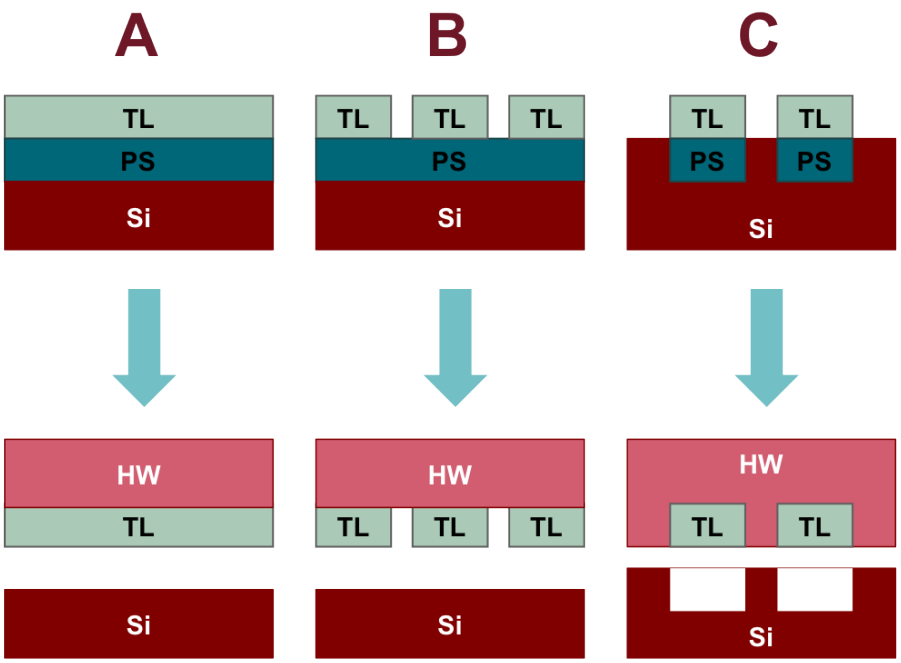


Figure 81: Three different layer transfer technologies employing porous silicon as sacrificial layer.

mer) that is pressed against the SW or if in liquid phase, dispensed over the SW. In both processes the following can happen:

- The HW material infiltrates the PS layer that is integrally transferred with the pattern,
- the HW material does not infiltrate the PS layer but copies its superficial asperities (an unwanted nano-imprinting), that will alter the surface finishing of the HW.

In the former (infiltration) a subsequent etch of the sacrificial material can be done but the resulting surface of the HW would conserve part of the porous pattern. Original surface finishing can be recovered with a polishing process, if necessary but this is an additional step that can be avoided. In both cases, a uniform sacrificial layer will interfere with layer transfer over polymers like Polydimethylsiloxane (PDMS) as they are dispensed in liquid phase. The liquid infiltrates the porous structure making mechanical splitting hard to achieve with good uniformity. Patterning of the sacrificial layer solves both problems as the surface of the silicon wafer is flat (standard average roughness of silicon wafer R_a is lower than 5 Å)

6.1 POROUS SILICON AS SACRIFICIAL LAYER

Porous silicon is the most natural choice as sacrificial layer when the SW is a silicon wafer because (but this concept can be extended to other semiconductors that can be made porous:

1. Porosification is a reliable, low-cost and high throughput process to modify the surface of monocrystalline silicon and it can be done using CMOS compatible processes,

2. porous silicon can serve as an adhesion promotion sublayer, reducing mechanical stress and lattice mismatch, increasing the effective contact surface, in particular porous silicon can be considered as the only known solution for electrochemical deposition of thick stressed metal layers,

3. mechanical properties of PS strongly depend on its structure and porosity and can be modulated over a wide range and, by varying the current density during the anodization process stacked layers with different mechanical characteristics can be realized. The ultimate strength of PS goes from the value close to that of silicon at porosities below 10% to a few tens of MPa at porosities close to 90% making possible the mechanical splitting of the porous layer,

4. etching of PS layers is possible by means of the structure-sensitive mechanism. The selectivity of PS etching in comparison with monocrystalline silicon, reaches 100000:1.

The most effective porous silicon morphology for layer transfer technology is the meso-porous with pores whose diameter is between 50 and 100 nm. This can be obtained from highly-doped wafers, of both types (p-type and n-type) and the porosity obtained from heavily doped silicon wafers. A comprehensive discussion of the porosification regimes has been presented in 2.3.2 and in 3.2.

6.2 ADHESION BETWEEN METALS AND POROUS SILICON LAYERS

The adhesion of thick metal layers onto porous silicon of different porosity have been previously characterized in [20] for n+ and p+ (0.01 Ωcm) silicon wafers. A short summary of the method employed for the characterization, with results is presented here. A two-step anodization process is employed for the PS layer:

1. in the first annotation process, a linearly varying current density is applied to the silicon substrate to form a 0.5 μm thick PS layer (the pSi1 layer in figure 82). The variable current density produces a gradient of the porosity with depth: 80% porosity on the surface and 20% at the bottom. This first layer acts as an adhesion layer for the metal and, due to the decreasing porosity, will prevent deep penetration of the metal in the next layer, the layer that will be tested for ultimate strength. Metal infiltration would cause an alteration of the measure.

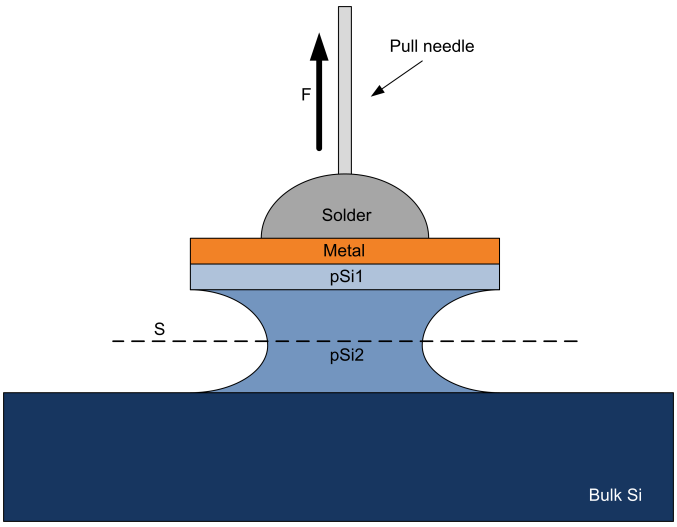


Figure 82: Test sample for measuring the ultimate strength of porous silicon layers. A two-step anodization process at different current densities produces two porous layers (pSi1 and pSi2) characterized by different porosities. A metal layer is deposited into pSi1 and a needle is soldered to it. The value of the force "F" applied to the needle that causes the fracture of the pSi2 layer is recorded.

2. In the second anodization process, the "layer under test" (he pSi2 layer in figure 82) is formed. This layer is grown at constant current density and the process is timed to achieve 10 μm thickness. The porosity of this layer is constant over all the thickness.

Once the porous bi-layer has been formed, a seed copper metal layer with a thickness of 150 nm is deposited by immersion plating, using the processes described in 4.3. A second metal layer (nickel) with a thickness that can vary from 4 to 12 μm (the thickness of this metal does not influences the measurement) is then electroplated (using industrial solutions and processes). The silicon wafer is then patterned to protect arrays of circular areas (each one with an area of 20 mm^2) that will constitute the test samples. The exposed metal etched and the porous layers are etched with KOH solution (2% to 10% depending on porosity). KOH etch stops at bulk silicon if temperature is below 60 °C and consumes only the porous layer. The final section of each test sample is the one depicted in figure 82, where PS under-etch is shown (KOH etch on mesoporous silicon is as an isotropic process).

Pull needles are then soldered on the remaining metal areas using an a low temperature solder to avoid thermal annealing of the porous layer. Tensile tests are executed on each sample and the force at which the silicon breaks is recorded. To obtain the stress value, the fracture is analyzed under microscope to compute its area, the stress value is computed by dividing the recorded force over the fracture area. The results of this analysis have been presented in chapter 2, figure 9.

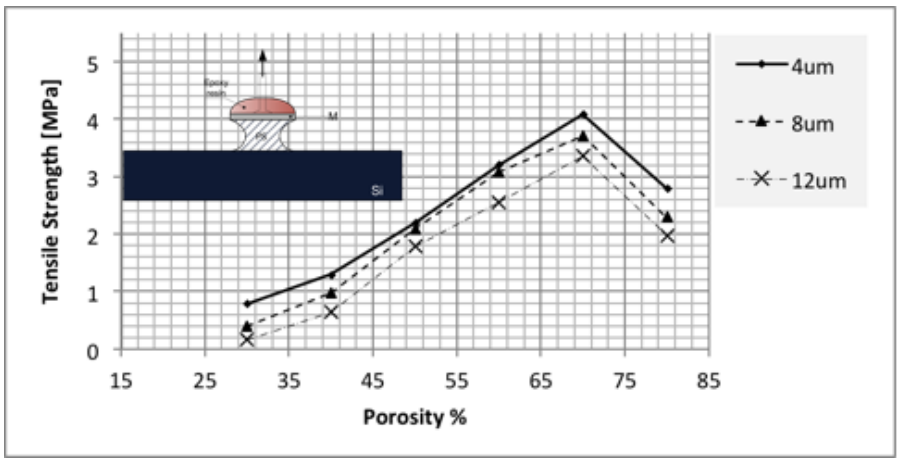


Figure 83: Tensile strength (at break) of porous silicon layers at different porosities for three different metal thicknesses. The measurement setup is shown in the top-left inset.

The tensile-test process applied to one end of a long metal line patterned on a porous silicon layer, peels the metal layer from silicon by breaking the PS/silicon interface. This is the idea a the base of the CRML technology. The porous bilayer described above is too complex to be used in practice for the technology and a simple process has been developed. In particular, the metal is deposited directly on top of the pSi2 layer, without the pSi1 barrier. This cause a dependence of the breaking strength of the porous layer from the deposited metal thickness.

Metal deposition on the porous layer follow the same protocol described for the bilayer case: immersion plating of copper to obtain a 150 nm seed layer followed by an electrodeposition. The tensile strength has been computed for three different metal thicknesses: 4, 8 and 12 μm. The metalized porous silicon samples were glued with an epoxy resin to a metal pin (as shown in the inset in figure 83) and then vertically pulled with a tensile testing machine. The "adhesion" of the metal with the porous silicon layer was considered to be the tensile strength of the porous silicon layer. Structure release, in this technology, takes place due to the breaking of the porous silicon layer. It was found (83) that the tensile strength of the porous silicon layer depends on porosity and metal thickness, and increases with increasing porosity. The main reason for this is the penetration of metal into pores (figure 84), leading to an increase of the effective contact area between the metal layer and silicon. The peak of adhesion is obtained for porosity of 70% for all three metal thicknesses. Porosity values higher than 70% lead to a decrease of adhesion due to gradual raise of the fragility of porous silicon.

The possibility to modulate the adhesion of the metal/PS interface is exploited in the **CMRL!** (CMRL!) technology to design metal structures that are only partially released from silicon:

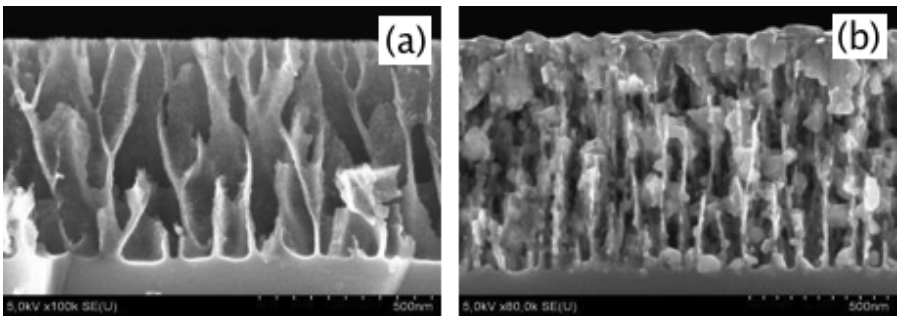


Figure 84: SEM cross section image of porous silicon as fabricated (a) and after metal deposition (b).

- a porous layer with 55% porosity is realized below the areas that should not be released (high adhesion),
- a porous layer with 35% porosity is realized below the areas that should be released (low adhesion).

This section introduced the concept at the base of the CRML technology: the modulation of the adhesion of metal over meso-PS layer. In the rest of the chapter, the technology is presented in detail through an application: the design of a MEMS contactor for wafer-level burn-in tests, the application for which the technology has been developed.

6.3 PROBE CARDS FOR WAFER-LEVEL BURN-IN TESTING

The testing step is fundamental in industrial fabrication of integrated circuits (ICs). Alongside with increasing the complexity and performance of the ICs the number of input and output pads also increases. As a result, the number of the test probes should increase at the same rate, but this is a challenging task due to the decreasing pad and pitch dimensions. According to the International Technology Roadmap for Semiconductors (ITRS), in 2013 probe technologies must support peripheral staggered pad probing with effective pitches of 20-40 μm, 45 μm pitch for dual row, non-staggered probing on all die sides. Multi-site probing support is highly desirable. The conventional needle probe card cannot fit to test the higher pad-density ICs. Several alternative probe card technologies using the semiconductor fabrication techniques have been proposed, among which a membrane probe card for high-density ICs that still has some limitations due to non-uniform contact force and high contact resistance. A cantilever-type MEMS probe cards can not endure nor produce the force required to break the oxide on a pad surface. Currently there is no available probe card technology on the market that meets simultaneously all of the future technology requirements such as low contact and low series resistances, high scalability, exact positioning of tips, versatile chip pattern, low cost per touchdown. This is why different probe-

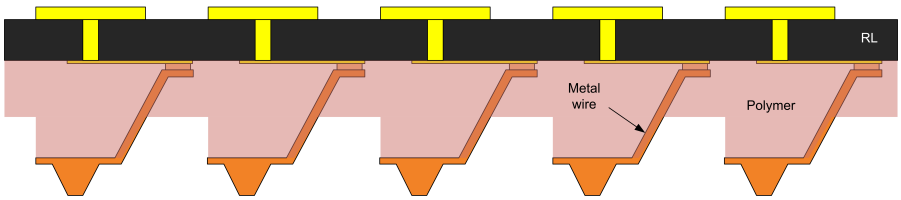


Figure 85: CRML implementation of the contactor for the probe card.

card constructions are used for different applications. The CRML technology has been used to build a contactor part of a probe card for wafer-level burn-in. The contactor is the part of the probe card that enters in contact with the die and provides electrical contacts to the rest of the probe card assembly. It is the most critical part of the entire probe-card assembly because its dimensions and its physical properties must closely match that of the IC device under test.

The schematic view of the developed contactor structure is depicted in figure 85. It consists of pyramid shape probes connected to a signal ReDistribution Layer (RDL) by means of metal wires. Metal wires are partially embedded into a polymer layer that adds the mechanical stability and provides the compliance to the assembly. Compliance is necessary in probe cards technology to compensate the non-uniformity in pads' height and planarity error between tested wafers and probe head. The realization of the contactor structure leads to the development of the CRML technology based on silicon micro machining processes and using of nano-structured materials. The technological steps of the contactor fabrication are schematically presented in figure 86.

Standard thickness (460 μm) 4 inches silicon wafer is used as a carrier substrate. The pyramid shape probe is realized first (figure 86.(a)) by etching the silicon wafer in a two-step process. The surface of the silicon wafer is protected by the silicon nitride mask. The openings are made in correspondence to each contact of the die under test. At the first step, the pyramid wide base is created by 2.5 μm Reactive Ion Etching (RIE) process through the openings. BoroSilicate Glass (BSG) mask is then deposited and patterned to create the lateral walls and the base of the pyramid by standard KOH anisotropic etching for desired depth. The exposed silicon is anodized in hydrofluoric acid solution to obtain the first porous silicon (pSi1) layer (figure 86.(b)). The "high adhesion layer", and contact metal are then deposited (figure 86.(c)) forming the tip of the compliant contact. The BSG mask is then removed and the silicon nitride is opened again to define the wire structures (figure 86.(d)). The second porous silicon (pSi2) layer is formed playing the role of the "low adhesion layer". The metal layer,

5 to 10 μm thick, is then deposited to grow the wire and fill the contact probe (figure 86.(e)). After a subsequent lithography step, the "pulling pad" area is plated with a joining material (e.g. Sn60Pb40 solder, figure 86 (f)). After completing this step the contacting structure on the wafer was aligned and bonded to the RDL substrate via the "pulling pad" (figure 86.(g)) using standard die bonding equipment. The assembly is then moved to a pulling machine where two substrates are separated and kept at a prescribed distance (figure 86.(h)). The partial release of the wire is possible due to the controllable adhesion of the metal onto the porous silicon layers. The space is filled with a polymer (figure 86.(i)) and the original wafer is removed by a XeF_2 dry etching (figure 86.(j)). The polymer is then etched by RIE to obtain independent polymer columns for each electrical contact (figure 86.(k)). The different adhesion of metals onto porous silicon allows to modulate the adhesion of metal to silicon and to obtain partially releasable structures that can be pulled away from the substrate to form freestanding 3D structures.

The partial release process is fundamental for carrying on the polymer filling process without tip displacement. The filling process is necessary to obtain the desired mechanical characteristics of the compliant contacts. The technology, thus, relies on two key challenges: the ability to modulate the adhesion of metals to silicon and, on modulating the mechanical characteristics of the polymer.

The porosity values chosen for two porous silicon layers in this technology are 55% for pSi1 and 35% for pSi2. SEM images in figure 87 show the cross sections of the wire region (figure 87.(a)) and contact tip (pyramid) region (87.(b)). The different morphology of porous silicon is evident in the images; the brighter porous layer in the pyramid region corresponds to a higher porosity region that the darker layer in the wire region.

6.4 BONDING AND PULLING PROCESSES

The carrier silicon wafer hosting the metal structures must be bonded to the RDL to obtain the contactor assembly. The RDL is a double-sided ceramic circuit board that gives mechanical stability to the contactor assembly and re-distributes the electrical signals to the rest of the probe card.

The RDL used in this technology is an alumina substrate 380 μm thick with 10 μm thick copper traces finished with Electroless-Nickel, Immersion Gold (ENIG). The probe side of RDL has 50 μm pads; the backside has 300 μm pads for probe card connection.

This substrate is aligned and bonded to the carrier wafer by means of solder bumps deposited onto the probes metal wires. Solder bumps diameter is in the 20-40 μm range. Larger bumps will cause shorts due to the small pitch of the probes. Smaller bumps may prevent uni-

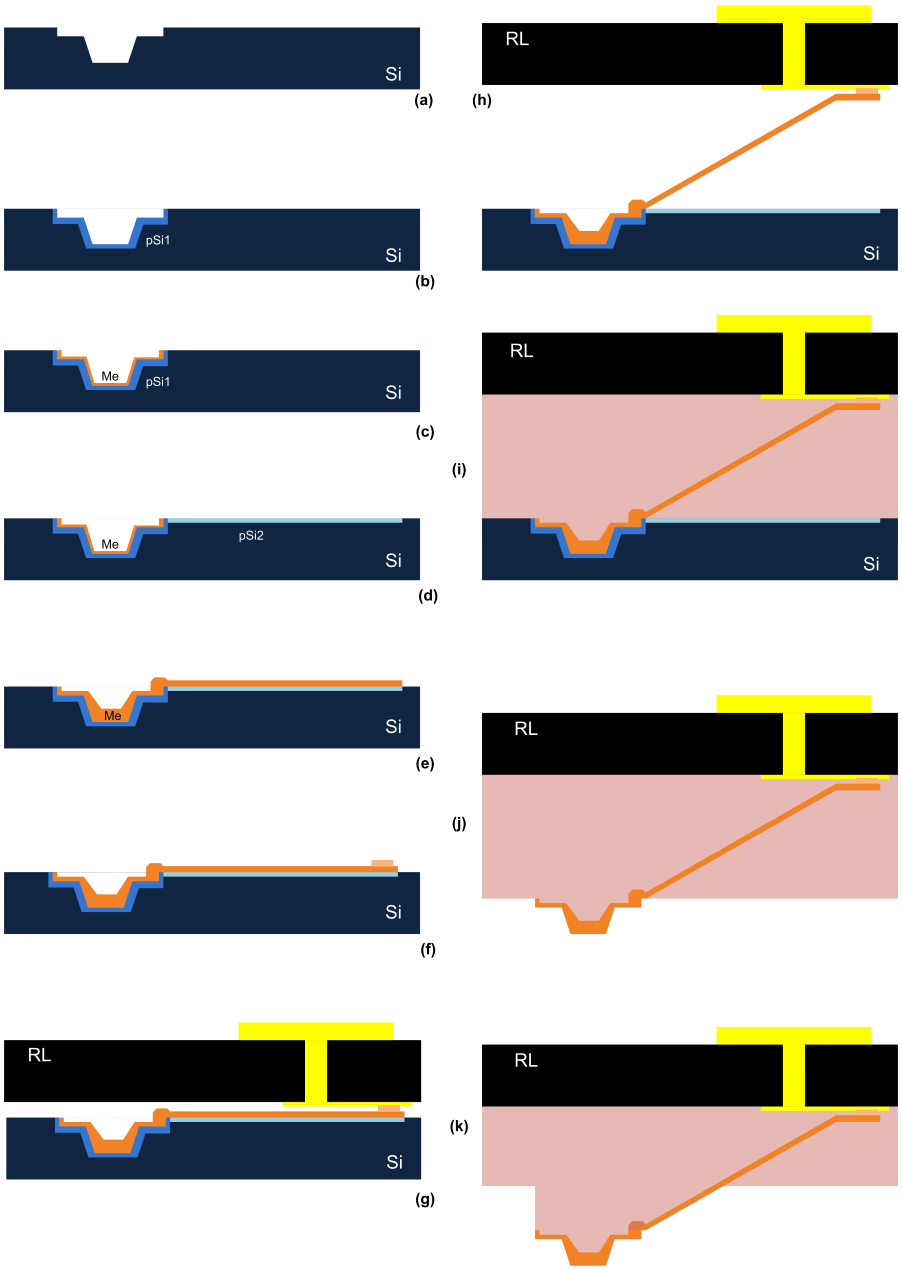


Figure 86: Main technological step for the realization of the electrical contact: (a) etching of pyramid pattern, (b) realization of the high-adhesion porous silicon layer, (c) deposition of contact metal, (d) realization of the low-adhesion porous silicon layer, (e) deposition of wire meal, (f) deposition of the "pulling-pad" metal, (g) alignment with the RL substrate, (h) pulling process, (i) polymer filling, (j) silicon wafer separation, (k) polymer etch for contact definition.

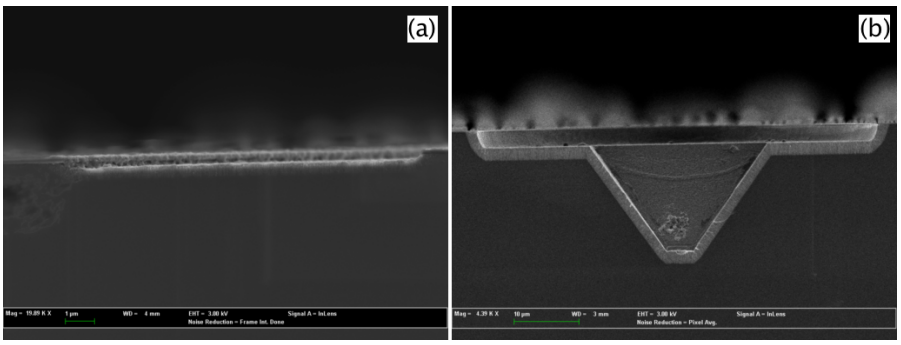


Figure 87: SEM cross sections of low adhesion porous silicon layer (a) below the pyramid region, and high adhesion porous silicon layer (b) below wire region.

form bonding. Thermo-compression bonding was used as bonding process for this technology due to the low dimensions of the bumps. In thermo-compression bonding, a compressive force is applied to the assembly during the reflow process. This compressive force is needed to break the thin oxide layer of the solder bump, and to compensate the height variation of the bumps that is typically in the range of 10% in electroplating process.

In this technology, fluxing agents are not applicable because the residues cannot be cleaned without the risk of releasing the structures or interfere with the polymer injection process in case of no-clean flux.

The force applied during the reflow process was found to be the critical parameter of this technology due to small bump dimensions. The force must be kept small to not squeeze the liquid solder and at the same time must be sufficient to break the oxide layer over the bumps and wet the substrate pad. The highest yield for all the vehicles was obtained with constant force application. Process atmosphere is also an important issue when no flux is used in the soldering process. The use of formic acid has been studied [130] as improvement factor in the chip bonding and has proven to be necessary in this technology to achieve the total wetting of substrate pads at lower forces, thus reducing the risk of solder bridges. Formic acid flow of 10 lt./min at 200 °C has been used to process the samples. The optimal process parameters determined experimentally are summarized in table 9.

The bonded assembly is moved to a pulling machine (a laboratory-scale custom machine has been built) that pulls the RDL away from the substrate for a prescribed distance. At this point the wires are partially released from the silicon substrate and are kept in position by the pyramid tips (still inside the wafer) and the solder joints on the RDL. Once the needed distance is reached, polymer filling and curing is carried on. The result of the bonding and filling process is shown

Force	0.3 - 0.72 g/bump
Preheat temperature	150 °C
Peak temperature	240 °C
Dwell time	5 sec
Heating rate	2 °C/s
Cooling rate	2 °C/s
Time above liquidus	75 s
Atmosphere	Formic acid 10 lt./min @200 °C

Table 9: Optimal bonding process parameters for Sn60Pb40 soldering with 20-40 μm bumps without the use of fluxing agent.

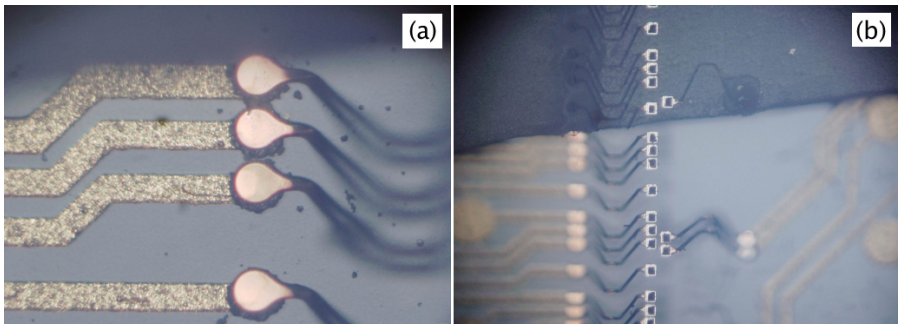


Figure 88: Optical microscope image of pulling pads bonded to the RDL (a); contacting assembly half-filled with a transparent polymer, pyramidal probes are visible in the center (b).

in figure 88 (the right part of the figure shows the sample half filled with polymer).

6.4.1 *Solder joint failure analysis*

Solder joints reliability issues emerged during the development of CRML technology [9]. SEM and EDX analyses have been performed on failing joints to classify defect typologies and investigate failure causes.

Two classes of defects were found:

1. Incomplete wetting by the solder of the gold pads.
2. A constantly higher failure rate (percent number of failing joints) has been observed on gold finished surfaces.

Analyses proved that such unusual rate was due to contamination of gold surface left by additives in the plating bath and to the embrittlement caused by gold diffusion into molten solder. Plating additives contamination reduces the wettability of gold surfaces. Concentration values of 3 wt.% for gold, considered safe for surface mount applications, caused embrittlement in solder bumps of 20-40 μm diameters.

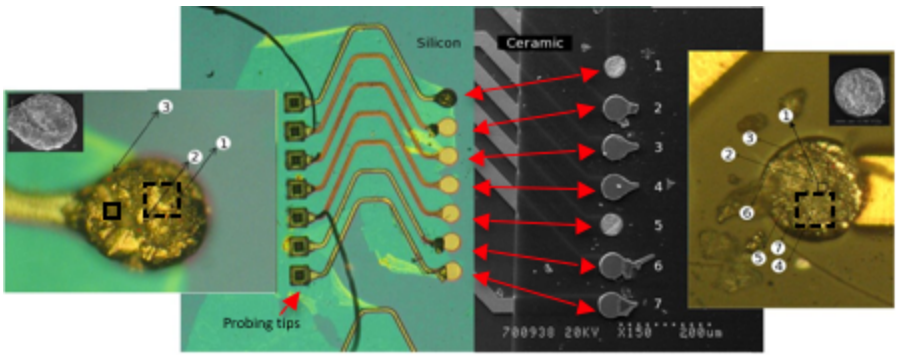


Figure 89: Detail of a gold finished sample (silicon left, ceramic right) after pulling process. Pad 1 (both sides) is magnified to show micro and quantitative analyses areas. The visible film on optical photo (left) is a residue of flux used for solder reflow. The probing tips (at the left) are still attached to the surface even if corresponding wires have been completely released.

The gold wettability issue was attributed to the plating additives; Auger spectroscopy revealed the presence of thallium oxide (thallium is an additive used in gold plating baths). This thin oxide layer (extending for 5 nm) has been removed by ion milling prior to bonding and this resulted in an increase in yield, but to a value still lower then the one of preformed solder finishes. This difference has been the subject of an in-depth study to discover the causes and find a possible solution, as gold finish was preferred over preformed solder. Figure 89 shows part of a sample, where is possible to see all the revealed defect mechanisms that affected the bonding and pulling processes. Arrows in the center shows matching pads, and arrows in the magnifications mark the areas (1x1 μm^2) where EDX analysis has been done. Squares (solid and dotted) correspond to 3x3 μm^2 and 10x10 μm^2 areas where the average quantitative analysis of the Au (gold), Sn (tin) and Pb (lead) has been computed. The analyses results are presented in figure 3 and figure 4.

All examined defects fall in 3 categories:

1. solder joint failure without release of wire from the silicon substrate (pad 1);
2. solder joint failure with release of the metal wire (pad 5);
3. silicon cratering with or without wire break (pads 2,6,7).

The missing metal wires (on pads 3 and 4) are not classified as failures as the wires broke during handling of the samples.

Pad number 1 is representative of the most frequent failure encountered during testing and has been object of SEM and EDX analysis to reveal the microstructure and composition of the failing joint. The SEM photos in figure 90 show the fracture on the ceramic side, (a) and (b) and silicon side, (c) and (d). The fracture is located between 3 and

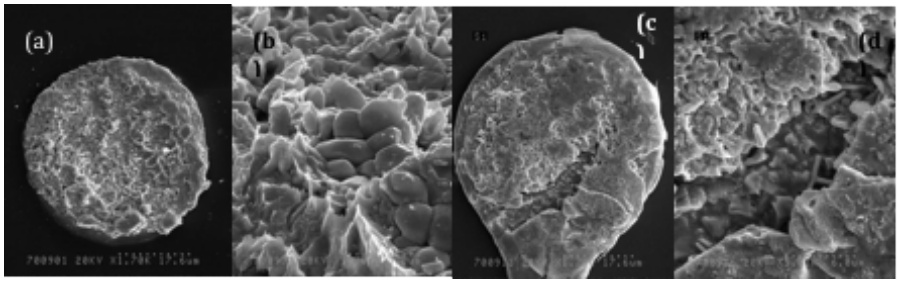


Figure 90: SEM images of pad 1; ceramic side (a), magnification of pad1 to reveal intermetallic compounds (b); silicon side (c) and magnification of fracture on silicon side (d).

6 μm from the pad surface and the cause is attributed to solder contamination by intermetallic compound that embrittle the joint. The morphology of AuSn InterMetallic Compounds (IMC) is evident [131] in both sides of the fracture (figure 90.(b) and 90.(d)). Whereas EDX data cannot be readily used to quantify the concentration of material in the specimen, it is evident that a ductile fracture happens where Au is absent (e.g. position 1 on silicon side and position 3 on ceramic side) and brittle fracture happens at high Au concentrations (positions 2 and 3 on the rim of the pad). EDX data in figure 91 (ceramic side), reveals the presence of Au on the entire surface, indicating that gold has diffused into solder, concentration in the dotted square is >35 wt.%. Position 3, where the fracture appears ductile, corresponds to a Pb-rich area. EDX on silicon side of pad 1 (figure 92) reveals that Au concentration is >28 wt.% inside the brittle fracture (3x3 μm^2 area) where the AuSn intermetallics can be recognized in the morphological analysis (figure 90.(d)) and <6 wt.% in the ductile Pb-rich fracture (10x10 μm^2 area). Analyses run on other pads show similar results.

The cause of low yield is the gold poisoning of the solder joint. Gold finish, used to protect lower metal layers from oxidation and contamination, is known to influence the soldering process and joint reliability when tin rich (e.g. 63Sn-37Pb or 60Sn-40Pb) solder is used.

The concentration of Au affects tin lead solder in the following:

- fluidity,
- wettability and spread,
- mechanical properties (solder ductility is drops rapidly as the Au concentration exceeds 7 wt.%),
- microstructure (at concentrations greater than 1 wt.% solder becomes detectable in the microstructure as needle-shape phase).

There is no general agreement on the maximum Au concentration that can be tolerated in a solder joint, with the most restrictive constraint set to 3 wt.% and most of the authors suggest to test Au influence in every specific case.

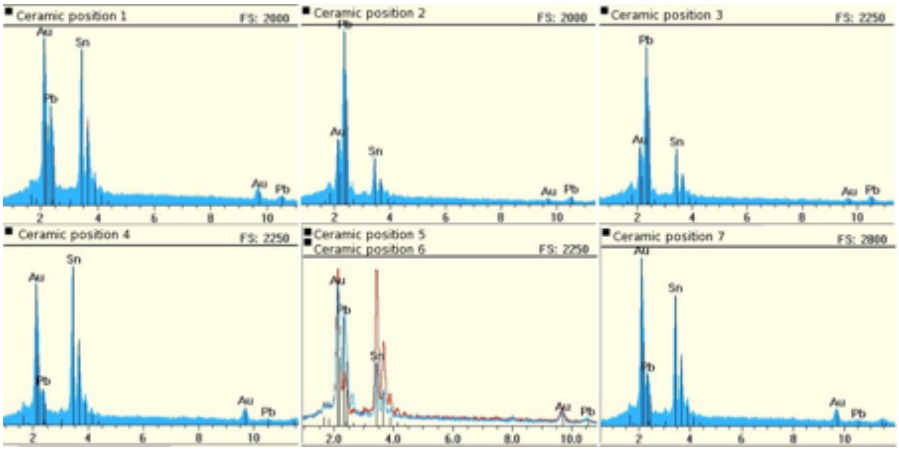


Figure 91: EDX analysis on pad 1(ceramic). Position numbers reflect the one in figure 89. The normalized results are: Pb 29 wt.%, Au 36 wt.% and Sn 35 wt.%.

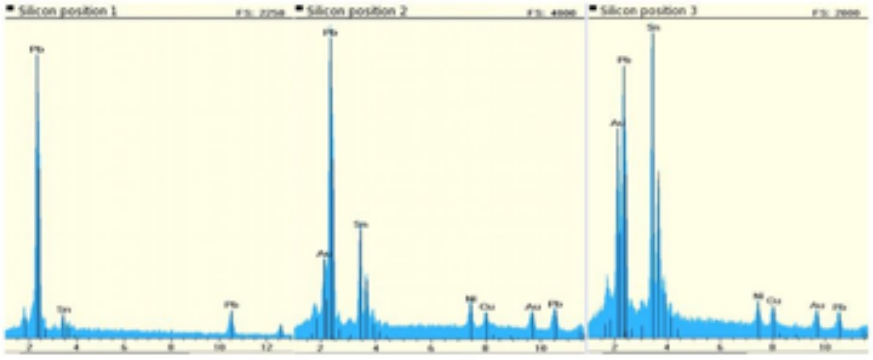


Figure 92: EDX analysis on pad 1 (silicon). Position numbers reflect the one in figure 89. The normalized results are: Pb 76 wt%, Au 6 wt.%, Sn 18 wt.% in the 10x10 μm^2 area and, Pb 26 wt.%, Au 28 wt.%, Sn 46 wt.% in the 3x3 μm^2 area.

When the content of Au is excessive, the following phenomena may happen:

- solder joint fracture due to embrittlement,
- void creation (Kirkendall voids),
- and microstructure coarsening.

In this specific case, the 3 wt.% threshold is not applicable and the cause of this additional detrimental effect lies in the interface kinetics of Au with solder where both dissolution of Au into solder and interfacial reactions, contribute to the formation of brittle AuSn intermetallic compounds. The solubility of Au is 7.8% at 220 °C, according to the data in [132].

In this technology, the 250 nm gold finish is readily consumed into molten solder and the intermetallic compound starts to form, causing

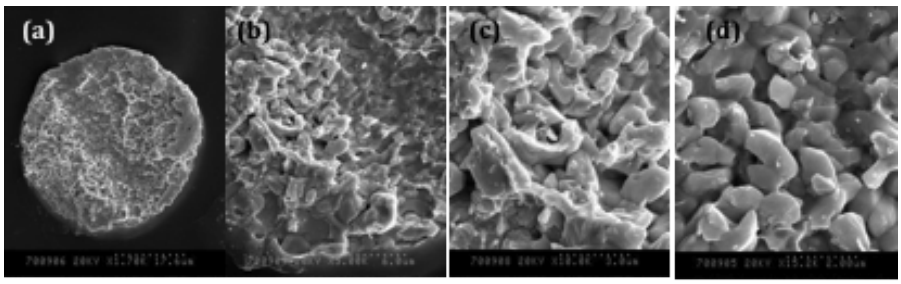


Figure 93: SEM analysis of pad 5 on ceramic substrate: (a) full pad view, (b) particular of the bottom left area, (c) and (d) intermetallics.

embrittlement of the joint. In this case gold diffuses faster in tin. As the gold diffuses in tin it forms intermetallic and as the concentration of gold increases more Sn is incorporated in the intermetallic and the concentration of Pb will increase forming a pro-eutectic and the resulting structure will be a highly concentrated part of Pb with AuSn intermetallic. The difference in diffusion coefficients of gold into tin and lead is the main mechanics of void formation. This is known as Kirkendall effect and seems to be the cause of the degraded yield and tensile strength of solder joints.

The photo of pad 5 in figure 93 shows the voids. It is evident the AuSn phase embedded into the solder made the joint brittle with presence of voids between the intermetallics as can be seen in figure 93 (c) and figure 93 (d). This will happen for concentration of gold going from 3 to 75 wt.%. In order to overcome this problem it would be necessary to stay under 3% or move to a solder that will form the eutectic 80Au-20Sn where all the above-mentioned problems are not observed. It was not possible to analyze the corresponding pad on silicon because the wire was released and the pad is standing in air. A tentative solution to reduce the gold issue is to keep the time above liquidus at minimum, without affecting the wetting, increasing the cooling rate. Above 4°C/s another problem has been found, the silicon cratering under the silicon pad.

6.5 DRY ETCHING OF SILICON WAFER

The silicon wafer onto which pyramid-shaped probes are built must be removed to expose the contacting probes. The removal of the silicon wafer was found to be a critical step of the technology as standard silicon wet etchants (acidic and basic) deteriorate the metal structure. Wet and dry etching of silicon was attempted. Acidic etchants, in particular, corrode the metals, and KOH etching, while being safe for the metals, generates hydrogen gas that raise the pyramids from the polymer base. RIE dry etch was found to be too slow for removing 460 μm of silicon. RIE etch with a mixture of SF_6/O_2 (flows: 50 sccm for SF_6

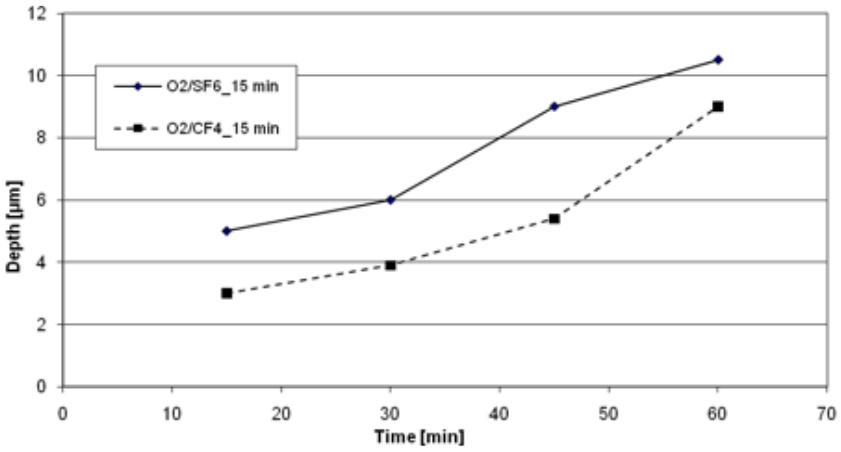


Figure 94: Etching rate of polyurethane in RIE with SF_6/O_2 and SF_6/CF_4 gases.

and 2 sccm for O_2), power level of 300W and pressure of 460 mTorr, has been measured to have an etch rate of 1.2 $\mu m/min$.

Moreover, the selectivity to polymers of the SF_6 etch is only 7.5:1 (as shown in figure 94), and is not sufficient to guarantee a flat polymer surface due to inhomogeneity of silicon etching. The XeF2 etching of silicon [133] was found to be the only reliable process as it shows higher etching rates and high selectivity between silicon and polymers. Moreover it was found that the polymer used is not etched in this gas and only a change in color is observed that has been attributed to fluorination of its surface. Contamination of polymer surface is of no importance because it is removed during the polymer etching process. Considering that the XeF2 etching is an exothermic reaction precaution must be taken not to overheat the sample over the polymer softening temperature. It was found that the optimum etching process is an impulsive one in which the process gas is loaded in the chamber where it reacts with the silicon for a controlled time and then purged to let the sample cool. Then the process gas is loaded again in a repetitive load/purge etch process.

The optimal process time was found to be 10 sec, allowing to maintain the temperature lower than 74 °C. The normalized etching rates are presented in figure 95. The etching rate is the value considering process time only (i.e. the time the silicon sample is exposed to process gas), and effective etch rate is calculated considering the total time, adding the purge time between process steps.

6.6 POLYMER LOADING AND ETCHING

The polymer that embeds the contacting structures gives the contactor its mechanical properties. In compliant contacting technologies

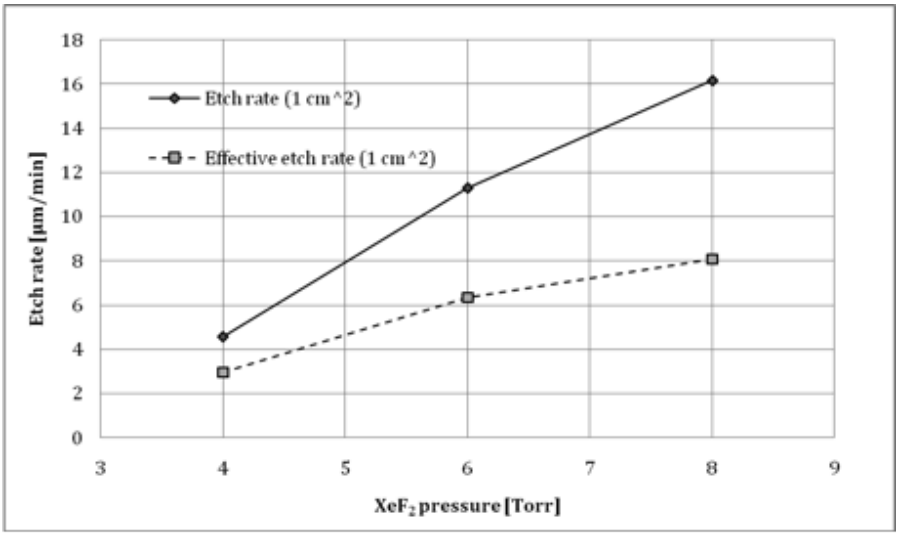


Figure 95: Etch rates for a 1 cm^2 surface of silicon. Effective etch rates take into account the purge time between two consecutive etch steps.

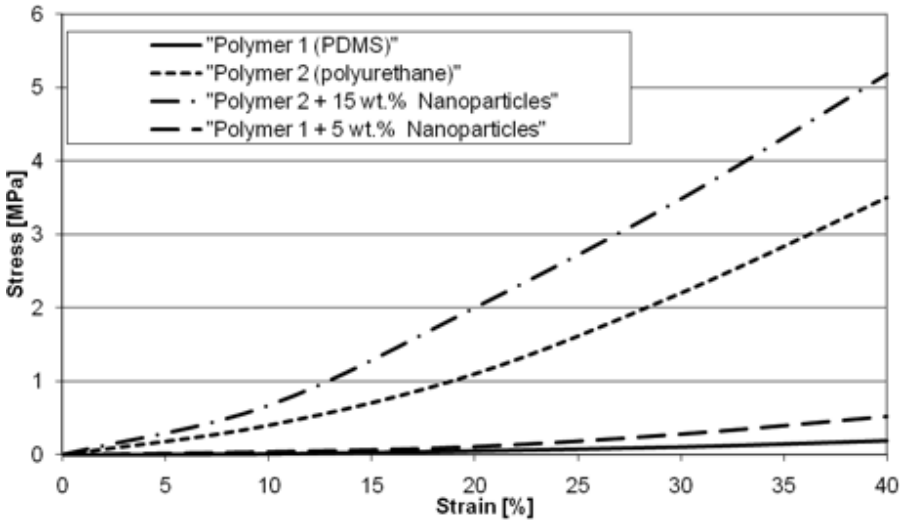


Figure 96: Stress strain diagram for different polymers.

the critical parameter is the contact force (i.e. the force between probe and test pad) and according to Holm's theory [15], the electrical contact resistance as its stability depend only on the force and not on its surface contact. Fine-tuning of the force is possible by changing the polymer mechanical characteristics by loading it with controlled quantities of nano-particles. Figure 9 summarizes polymers that have been tested for this technology. The effect of loading with nanoparticles is evident from figure 96: the load necessary to deform the material increases.

Two different types of polymer are presented: polymer 1 is PDMS and polymer 2 is polyurethane. The nanoparticles were silica nanoparticles 10 nm in diameter. It was found that, the polymer must be degassed, prior to filling the gap between substrates, otherwise micron sized bubbles, trapped between the two surfaces, render the contact unusable. After the XeF_2 process, the polymer is etched to create columnar structures below each probe. The columnar structures are needed to allow independent movement of different probes to compensate non-uniformity in the tested circuits and non-planarity between probe card and wafer. The process employed to create columnar structures is anisotropic RIE etch. The gas mixture used was a mixture of CF_4/O_2 gas (flows: 4 sccm of CF_4, 50 sccm of O_2) at a power level of 125 W and process pressure of 86 mTorr.

The measured etch rate of polyurethane is shown in figure 94. The etching depth depends on the maximum allowed compression of the contact. It is advisable to keep compression length below 40% of the total column length, as the stress/strain curve is not linear. The forces necessary to obtain deformations over 40% are usually higher than the one that can be applied to an integrated circuit without causing damage to the fragile low-k dielectric layers below the test pad. Example of the etching is presented in figure 97.

6.6.1 *Contact shape and mechanics*

To obtain the correct contact force, Finite Element Method (FEM) simulations of the actual geometry are required and must involve extensive characterization of the materials employed. The contact in figure 97 has been simulated to determine the displacement under load (see figure 98). This technology uses pyramid-shaped contacting tips, realized by anisotropic etching of silicon (figure 97), on top of a column of polymeric material. When the tip is pressed against a plane, the polymer column deforms and generatea a reaction force . The normal component of the reaction provides the stable contact; the tangential one produces a displacement that performs the scrub action (useful to remove the oxide in the contacted area). The scrub movement, generated by the mismatch between the centre of mass of the tip and the application point of the reaction, can be controlled with masses

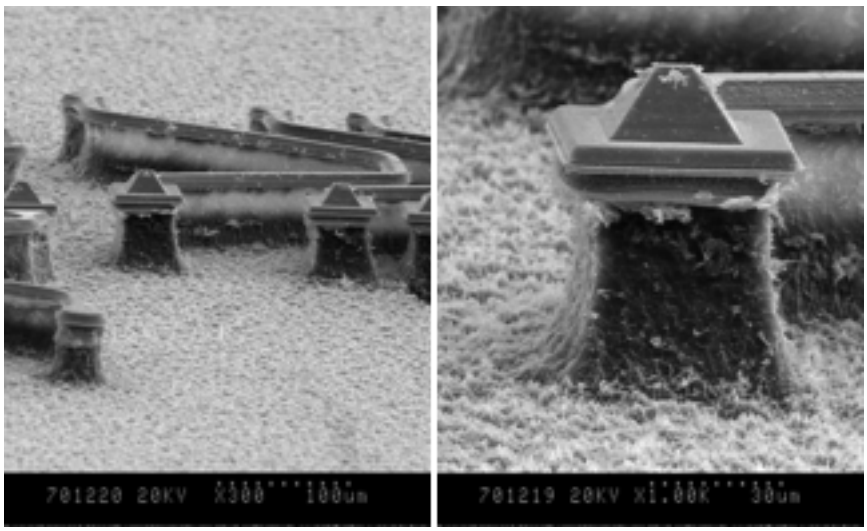


Figure 97: Contact probe (RIE etching testing samples). The wires are all above the polymer in this sample. It is evident the masking effect of the metal wires on the polymer.

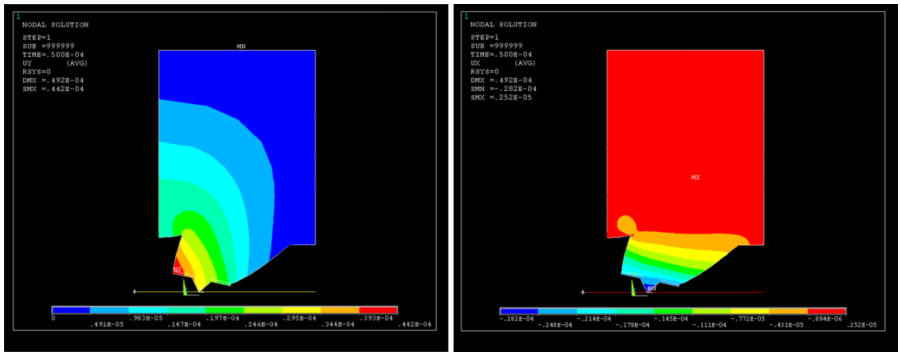


Figure 98: FEM simulation of the electrical contacts realized with the CRML technology. The vertical (left) and lateral (right) displacement fields are shown.

distribution. All designed tips are designed to present a lower inertia in the wanted direction of scrubbing.

The value of the reaction force at a given displacement is an important parameter for this application and can be controlled, in this technology, by tuning the mechanical characteristics of the polymer (see figure 96).

7

MACROPOROUS SILICON MULTILAYERS, CAVITIES, AND MEMBRANES

7.1 INTRODUCTION

The possibility of controlling macro-pore shape with illumination in n-type wafers has not an analogous in p-type. The supply of holes in p-type wafers is not altered by illumination and, thus pore modulation does not occurs. It has also been found and reported in that, pore modulation with current density alone is not possible. In this chapter an effective way to modulate macro-pore morphology on p-type wafer is presented. It requires both a change in the electrolyte and in the current density. The technological steps described in this chapter can be used to obtain macroporous multilayers, buried cavities and macroporous membranes.

7.2 MACROPOROUS SILICON LAYERS WITH DIFFERENT PORE WALLS THICKNESS

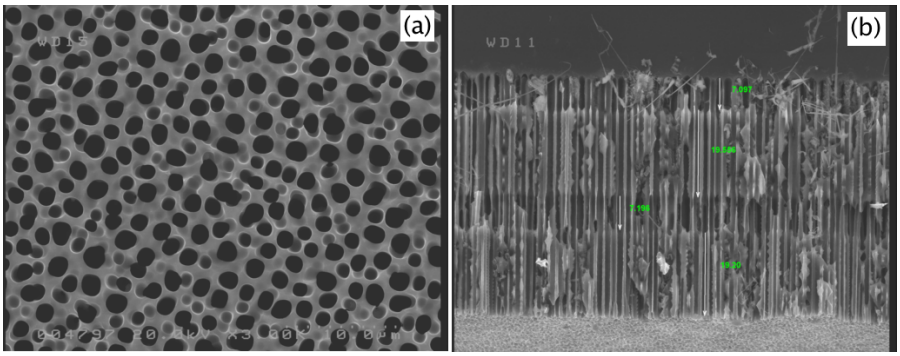


Figure 99: a) SEM image of a multi-layer macroporous silicon structure. The sample has been realized with two steps of organic/aqueous electrolyte alternation: 45 min for HF : DMSO and 5 min for HF : DI : EtOH, for 100 min total process time, at RT.

It is possible to modulate macropores wall thickens on (100) p-type silicon wafers with a 10-20Ωcm resistivity, using a combination of an organic electrolyte and an aqueous electrolyte, with different process conditions. This dual macro-PS morphology has been obtained by accident while trying to grow a layer of micro-PS below the macro one. The two electrolytes and current densities are:

- HF : DMSO(10:46) with 10 mA/cm^2

- HF : DI : Etoh(1:1:2) with 200 mA/cm^2

After the process the sample has been rinsed in IPA and dried with nitrogen. Figure 99 shows the obtained morphology from the top (figure 99.(a)) and in cross-section (figure 99.(b)) after 4 process steps (two alternations of the electrolytes). The difference in pore morphology is evident is the cross section. Several silicon wires detached from the macro-PS layer are visible in the cross section, a clear evidence that this macroporous structure is more fragile than the one realized with organic electrolytes only. It is interesting to observe the continuity of the pore wall along the section, the pore conserves its integrity, only the wall becomes thinner.

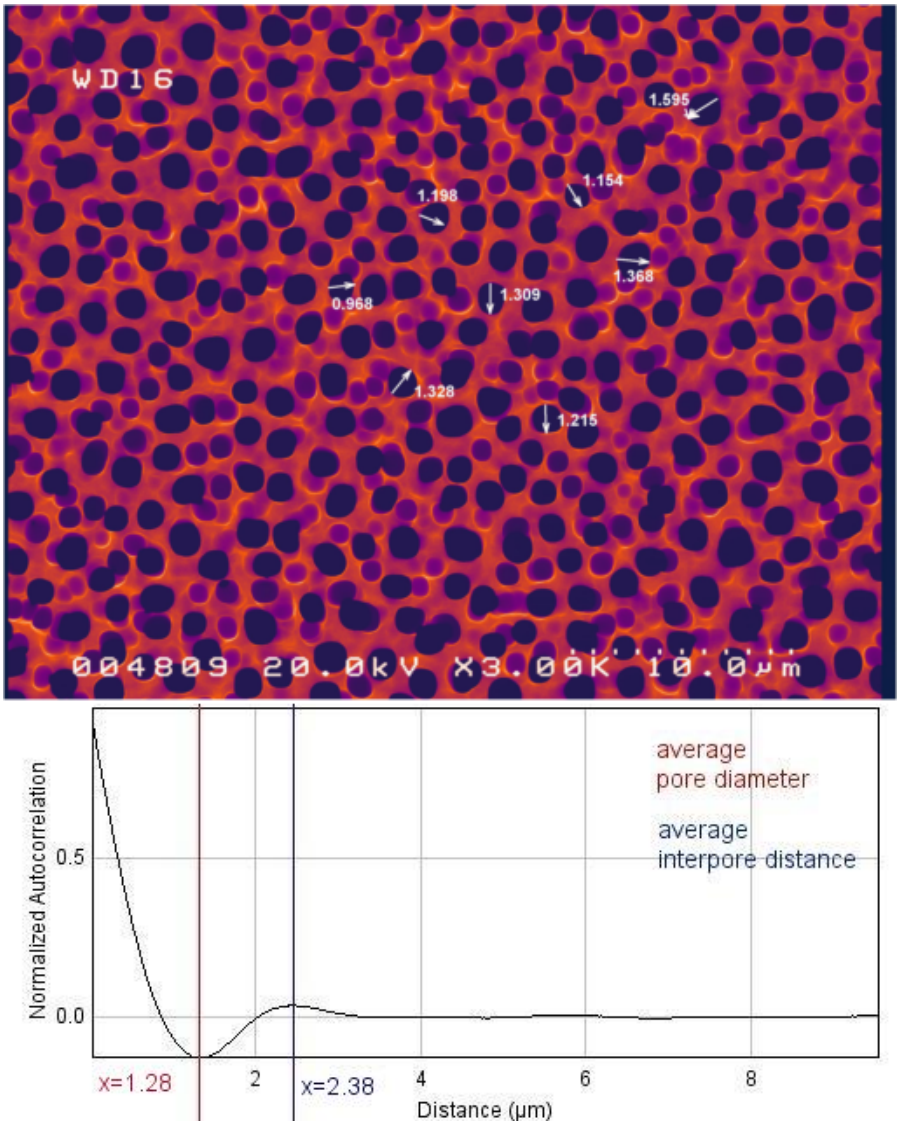


Figure 100: RAA analysis of the multilayer macroporous surface.

Pore analysis has been carried on the surface of the multilayer structure with imageJ [63] to identify dimensional changes. The RAA analysis carried on figure 99.(a), using a false color palette to reduce the

weight of the intepores, confirmed an increment in the average pore diameter (figure (100)), with respect to the one obtained with the organic electrolyte only. A possible explanation is that chemical dissolution occurs at the pore walls during the anodization steps in aqueous electrolytes, due to a width reduction of the SCR that allows *holes* to reach pore walls.

In figure 101 (upside-down) shows part of multilayer that detached from silicon after cleavage. The layer obtained with the aqueous electrolyte is easily broken during cleavage. A careful analysis of the image shows that the two macroporous layers are split, again caused by a failure of the weakest layer. In analyzing pore morphology on internal layers, it has to be observed that the each macro-PS layer acts as a masking layer for the next one. It is known that it is possible to produce wider pores (wider than the average diameter of the ones on a random surface) by etching pits with a regular pitch on the substrate. Each pore tips acts as an etch pitch and a seed point for a new pore. As predicted by the Lehmann's model, the new pore grows in diameter until the walls are depleted of *holes*. This will explain the "pore continuity" and, since the width of SCR is narrower for the aqueous electrolyte, the hypothesis of slow dissolution of previous layers seems (verified by image analysis), seems confirmed.

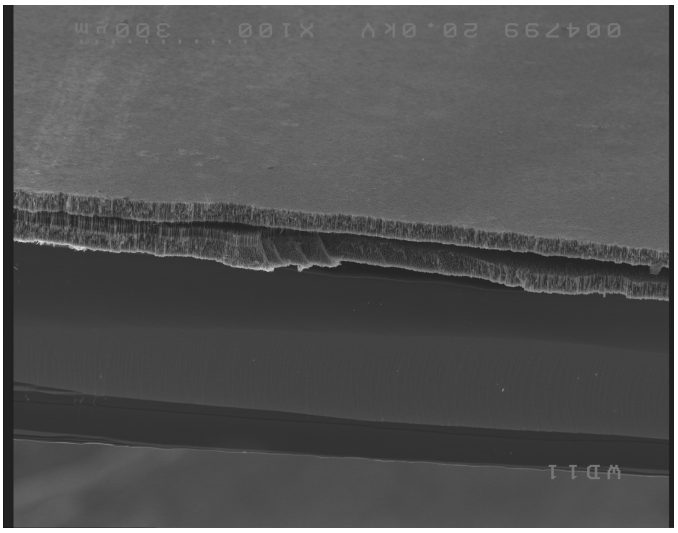


Figure 101: Multilayer macroporous structure detached from silicon.

7.3 BURIED MICROPOROUS LAYER

Growing micro-PS layers on low doped silicon wafers requires an high concentration of HF in the electrolyte. Micro-PS layers have been obtained, in this work, by anodization in stock HF (45 wt.% or 48 wt.%). The use of such high concentration of HF poses compatibility prob-

lems with photoresist masks that tends to peel off. The anodization conditions to obtain a buried micro-PS layer are:

- HF : DMSO (10:46) with 10 mA/cm^2
- HF 45% with 40 mA/cm^2

The first step produces a macro-PS layer with vertical pores and the second a micro-PS uniform layer conformal to the previous, homogeneous and compact. Figure 102 shows the result of such process (50x objective, each mark corresponds to 7.4 μm) where the macro-micro dual structure is clearly visible.

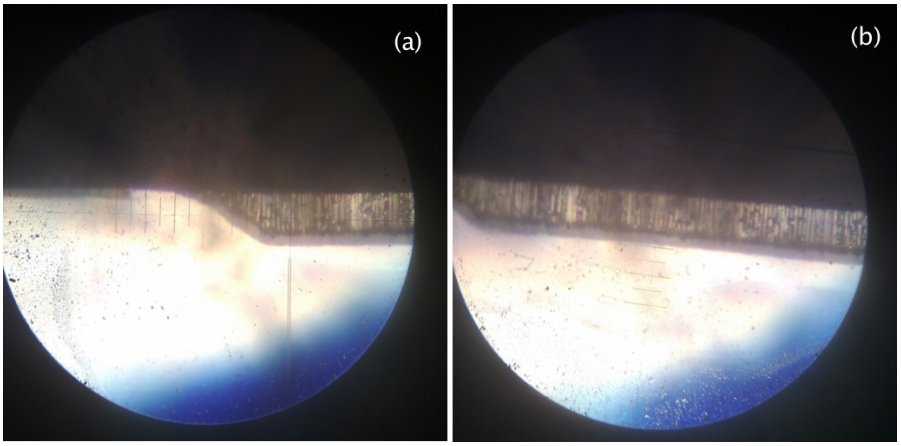


Figure 102: Edge (a) and center (b) image at the optical microscope (50x objective, each mark is 7.4 μm) of a sample realized with: HF:DMSO (10:46) with 10 mA/cm^2 for 30 min, and HF 45% with 40 mA/cm^2 for 20 min, at RT. Silicon was masked with SU-8 photoresist, under-etching due to peeling if the photoresist at the edge is visible.

Both macro- and micro-PS layers shows under-etch. The under-etch of macro-PS is 43.3 μm (for an 22 μm thick layer). This values suggests that photoresist peeled off during macroporous layer formation. A possible solution to remove the edge effects is to grow a uniform macroporous layer, transfer the pattern for the microporous layer, exploiting photoresist penetration inside macropores, and perform the anodization step to grow the microporous layer.

Figure 103 shows the result of this technique. A thick microporous layer is clearly visible below the macroporous morphology. The profile of microporous layer shows pronounced under-etch at the edges (the top inset of 103 show an optical microscope view of the edge area). The round shape of the under-etch area suggests a isotropic process, the thickness of the microporous layer is 40 μm, as the lateral penetration under mask. Figure 104 shows a magnification of the interface between the two porous morphologies: the microporous layer totally surrounds the bottom of the macropore and part of the lateral

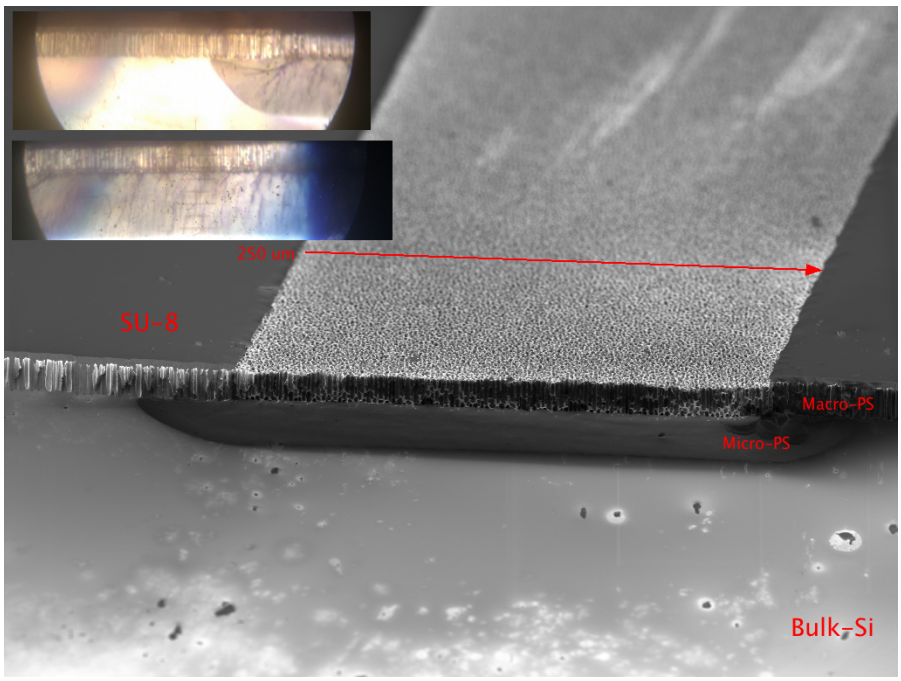


Figure 103: SEM image of micro-PS layer grown below macro-PS. The insets shows optical (50x objective, 7.4 μm mark) images of the edge (top inset) and center (bottom inset) of the microporous layer., a) center, b) edge. The sample is realized in HF:DMSO (10:46) with 10 mA/cm^2 for 30 min, and HF 45% with 40 mA/cm^2 120 min, at RT.

wall. This suggests that micro-PS formation starts from the macropore tip and proceed isotropically toward the bottom of the wafer. No microporous morphology is visible in the lateral walls of the macropores. This technique make possible the fabrication of even and thick microporous (37 μm have been demonstrated) layers below a macroporous structure.

The RAA analysis of the top surface (macroporous layer), shows a widening of average pore diameter (see figure 100) caused by the additional etching process with a different electrolyte.

7.4 BURIED CAVITIES BELOW MACROPOROUS SILICON

Selective etching of microporous layers buried below macropores produces a cavity. Selective etching of micro-PS layers has been obtained, in this work, by immersion of the sample in the HF:DMSO (10:46) electrolyte (without applying current). The oxidizing nature of DMSO has been reported first by Song and Sailor [134]. The combination of an oxidant (DMSO) with HF, produces a continuos oxidation and dissolution of the highly reactive surface of micro-PS. Silicon dissolution of macro-PS is not evident due to kinetic reasons: reaction rate is significantly higher on micro-crystallites than on macro pore walls.

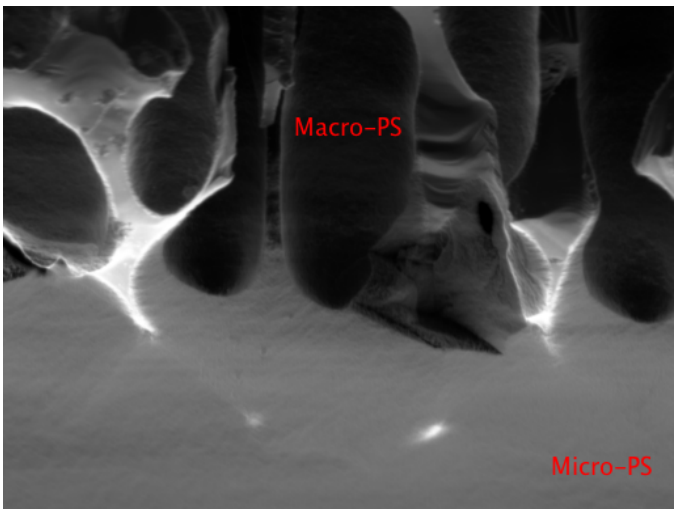


Figure 104: SEM image of the interface between macroporous layer (top) and microporous layer (bottom). The interface is continuous with microporous layer surrounding the bottom of the macropores.

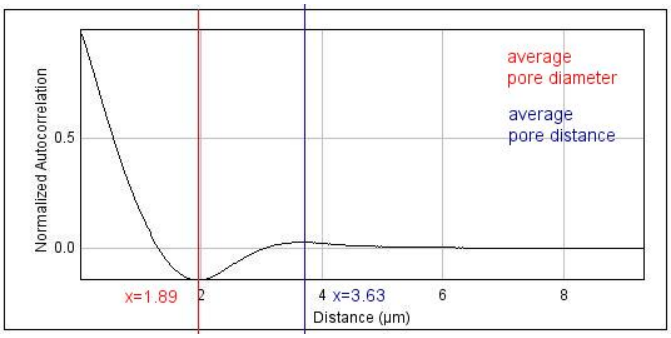


Figure 105: RAA of the macro-PS surface for the buried microporous layer samples.

The dissolution of silicon is confirmed by hydrogen evolution visible during the immersion. The process stops when all the microporous layer has been dissolved as the electrolyte does not etch bulk silicon. The volume previously occupied by micro-PS now is a buried cavity enclosed by macropores at the top and bulk silicon at the edges and at the bottom, as can be seen in figure 106. The picture shows the cross-section of a cavity obtained from a rectangular on the silicon wafer masked with SU-8. In 106.(c) the microporous layer extends below the entire macroporous layer and, reaches the silicon surface. In this case, dissolution of micro-PS caused the detachment of the macroporous layer and make impossible the realization of a closed cavity. The solution to this problem is the use of a different mask (undoped polysilicon or an HF resistant metal like gold) or, as demonstrated in this work, the transfer of the pattern after the growth of the macroporous layer. This would prevent the under-etch as the SU-8 infiltrates macropores and acts as a "vertical" mask to stop silicon dissolution

at the border of the cavity. The penetration depth of SU-8 determine the maximum depth of the buried cavity. It would be interesting to realize a cavity totally surrounded by macro-PS, exploiting the super-hydrophobic characteristic of silanized macro-PS, as described in 5 in microfluidics applications.

This type of cavity (see figure 107) can be obtained by performing an anodization step with the organic electrolyte after the microporous layer has been formed. Microporous silicon would naturally dissolve in HF:DMSO (10:46) and the application of an electric current increments the reaction rate and will form a second macro-PS layer at the bottom.

The technological step for the realization of a buried cavity are summarized in figure 111 at the end of the chapter.

7.5 SEPARATED MACROPOROUS MEMBRANE

When no lithography is used, as outlined above, the border effects at the edge of the electrochemical cell causes surfacing of the microporous layer. When this condition occurs, the macropore membrane is completely isolated from bulk silicon by micro-PS. Selective etching of the microporous bed will cause the detaching of the macroporous layer. The process steps are:

- HF:DMSO (10:46) at 10 mA/cm^2
- HF 45% at 40 mA/cm^2
- HF:DMSO (10:46)

The thickness of the membrane is determined by the first step. The second step determines the thickness of the microporous layer that, in this application is not important. Two minutes of anodization in concentrated HF are sufficient for the surfacing of the layer that will cause the detachment of the membrane at the next step. An example of the detached membrane is shown in figure 108. The fabricated membranes can be used in applications like molecular separation [135], or as filters.

7.6 MICROPOROUS LAYER FORMATION BELOW MACROPOROUS LAYER

The morphology of both sides of a buried cavity obtained with the double macro-PS, is visible in figure 107 and, at higher magnification in figure 109. In all the realized samples, different morphology of macroporous surfaces is observed:

- pore bottom of the upper macroporous layer show sharp pointed tips,

- pore top of lower macroporous layer show depressions that have the shape of a spherical cap (particularly evident in figure 109).

This difference in morphology gives insight in the microporous layer formation mechanism (see figure 110).

Microporous silicon formation is a isotropic process starting in correspondence of pore tips, because of the current crowds in this region due to the higher concentration of the carriers [30] (*holes*). In a simplified growth model, it can be thought that microporous silicon grows from each tip spherically. The microporous layer grows in all direction, toward the bottom and the top of the pore. This is visible in figure 104 where the microporous layer (that appears as a rugosity) extends upward, until the equilibrium thickness of pore wall is reached. According to Lehmann's model further dissolution should be precluded in that direction by the SCR.

Downward growth of microporous layers continue with the spherical front until spheres merges. The interface where sphere merges is sharp and constitute a new nucleation site for the microporous layer; *holes* should concentrate at these new sites, increasing the local growth rate. The final profile of the microporous layer is shown in figure 110, in the right panel. The gray region is the remaining silicon and it perfectly matches the morphology visible in the SEM image in figure 109.

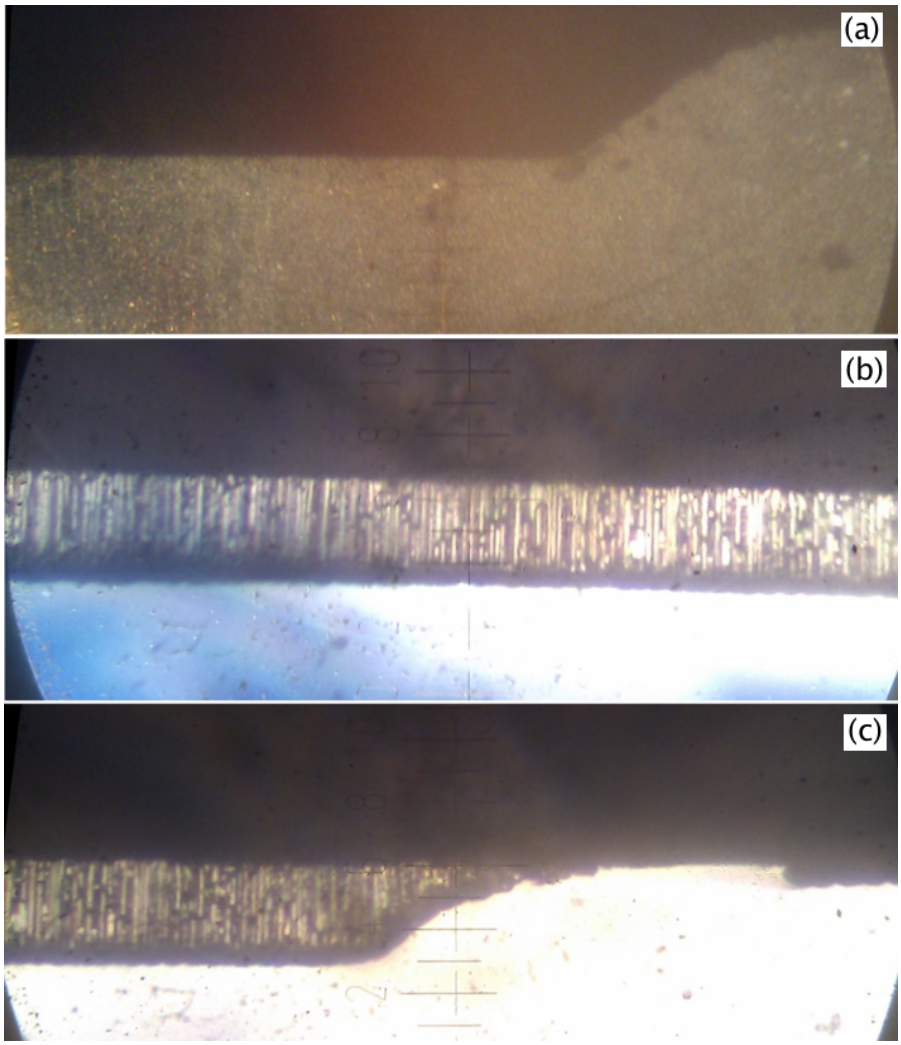


Figure 106: Buried cavity below macroporous layer. (a) Optical microscope image of bulk silicon after dissolution of micro-PS and detaching of macro-PS; (b) optical microscope image of the central area of a macro-PS membrane over a air cavity; (c) optical microscope image of the edge of the macro-PS membrane. The micro-PS over the membrane and, causes its detachment after dissolution. All images have been obtained with a 50x objective, each mark is 7.4 μm. Sample has been realized in HF : DMSO (10:46) at 10 mA/cm^2, for 30 min, HF 45% at 40 mA/cm^2 for 20 min, and HF : DMSO (10:46) for 1 min.

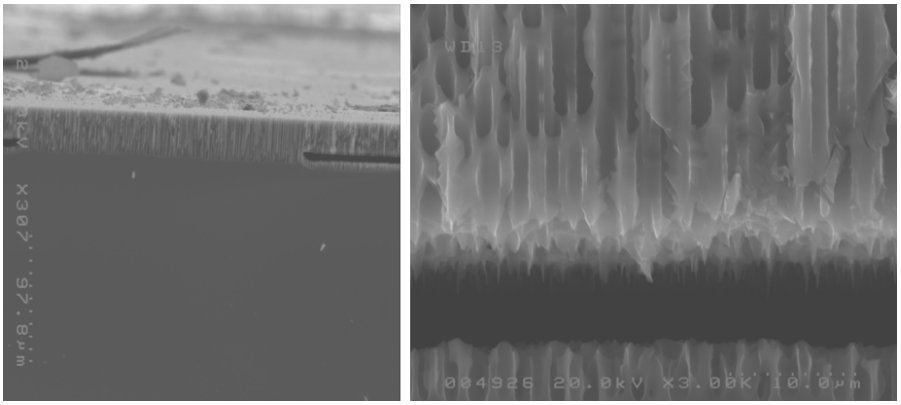


Figure 107: Cross-sections of a buried cavity surrounded by macro-PS on all sides. Sample has been realized in HF:DMSO (10:46) at 10 mA/cm^2 for 30 min, HF 45% at 40 mA/cm^2 for 20 min, and HF:DMSO (10:46) for 1 min at 10 mA/cm^2, RT.

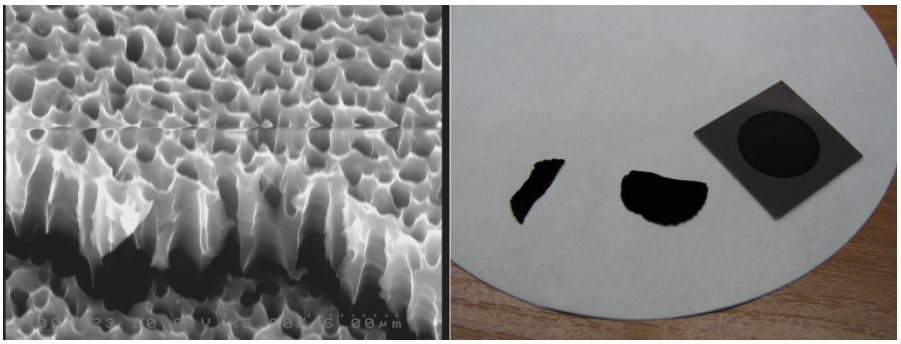


Figure 108: Detached macroporous membrane. The SEM image shows the membrane morphology in a region corresponding to a crack. The photo shows the an example of a separate membrane (broken in two pieces) and a membrane is still on a silicon wafer. Sample has been realized in HF:DMSO (10:46) at 10 mA/cm^2 for 30 min, HF 45% at 40 mA/cm^2 for 10 min, and HF:DMSO (10:46) for 1 min.

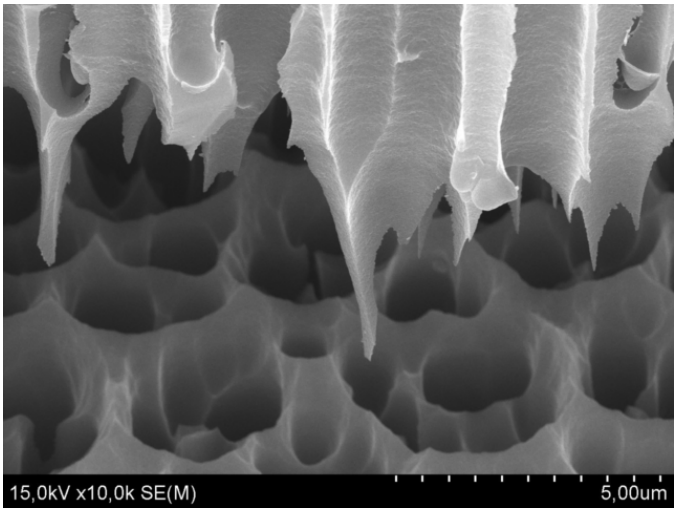


Figure 109: Magnification of sharp tip of upper face.

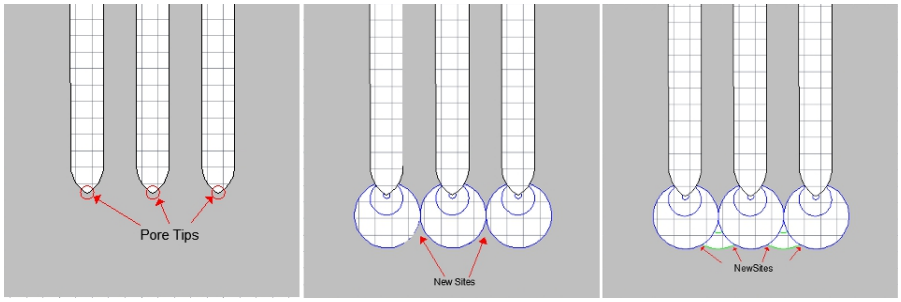


Figure 110: Growth model for microporous silicon layer below a macroporous layer: growth starts at pore tips (left), and proceed with a spherical front in all directions until two spherical front touches (center) forming a new sharp tip facing upward in correspondence of the contact point. A new nucleation site starts in correspondence of the contact point and the growth proceeds (right).

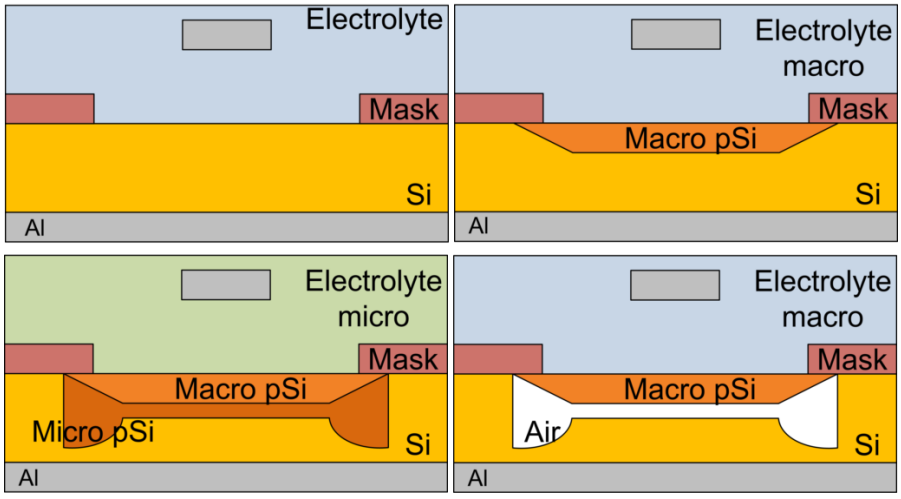


Figure 111: Summary of the technological steps for the realization of buried membranes (left to right, top to bottom).

Part III

APPLICATIONS

This part describes two applications developed with the CRML technology: compliant contact for high density probe cards and, on-chip integrable helical antennas.

8

COMPLIANT CONTACTS USING CRML TECHNOLOGY

8.1 INTRODUCTION

The ITRS predicts the main trends in the semiconductor industry spanning across 15 years into the future. Off-chip interconnections will soon constitute the bottleneck to the further scaling of IC technology. The integration of heterogeneous thin dies (thickness <50 μm with projections down to 15 μm) in SiP technologies, over organic interposers, will pose severe reliability issue of solder joints. The difference between silicon die Coeffiecient of Thermal Expansion (CTE) (i.e. coefficient of thermal expansion between 2.6 and 3.2 ppm/°C) and organic substrate (in the range 11–16 ppm/°C) induces enough stress to cause solder fatigue during thermal cycling, primarily in the outermost solder-bump interconnects.

Epoxy based underfill is used to mechanically couple the die and the substrate to evenly distribute the stress across the entire die area, reducing the differential motion of die and substrate, and dissipating the stress. The main drawbacks of this technology are:

- underfill delamination and degradation of mechanical properties at working temperature higher than 150°C;
- not applicable in case of substrate-to-die gap smaller than 5 μm (due to filler particle dimensions);
- ohmic losses at radio-frequency.

In all situations where underfill or, in general, adhesive contacts, cannot be used, compliant contacts are the only solution.

Figure 112 summarizes the state of the art of compliant contacts and the requirements of the ITRS 2010. The main limitations of metallic compliant contacts are the 3D-shapes that require complex manufacturing technologies, the minimum spacing of 0.1 mm and the high parasitic inductance. Compliant contacts are also used in the IC testing industry to provide temporary electrical connection between the dies on the wafer and the testing system. In this chapter, the application of the CRML technology to the realization of compliant contacts is presented.

8.2 THE COMPLIANT CONTACT

The single compliant electrical contact realized with the CRML technology is shown in figure 113. It consists of a metal wire, embedded in an

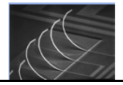
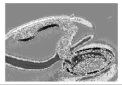
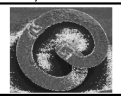
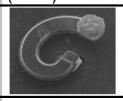
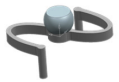
Technology	Adhesives		Metallic compliant contacts						ITRS 2010	
	Anisotropic conductive film (ACF)	Fine Pitch ACF	J-springs (2002)	Sea of Lead (2003)	Beta Helix (2003)	G-Helix (2004)	FlexConnect (2008)	Multi-Path (2011)	Flip Chip Array	Flip Chip peripheral
Type	Gold-coated polymer	Poly-Ni-Au								
Particle size [μm]	30	3								
Thickness/Height [μm]	45	20	NA	90	110	78	<70 (estimated)	NA		
Min. spacing [μm]	100	12	6 (not array)	100	100	100	100	NA	95	35
Min. pad area [mm^2]	0.5	0.0013	NA	NA	51.4	42.7	40.9	37		
Resistance [$m\Omega$]	20-100	25-50	2.50E+05	20	32	43.63	40.94	>20 (est.)		
Inductance [pH]	NA	NA	NA	100	102	92.7	36.5	37		
Peel Strength [g/cm]	>700	NA	NA	NA	NA	NA	NA	NA		
Compliance [mm/N]	NA	NA	10000	0.91	11.1	11.5	6.47	3		
Fatigue Life [cycles]	NA	NA	NA	NA	>3000	3118	1000	>1000		

Figure 112: Summary of the state of the art of compliant contact for off-chip interconnections and requirements from the ITRS. Missing or not applicable parameters for each technology have been marked with NA.

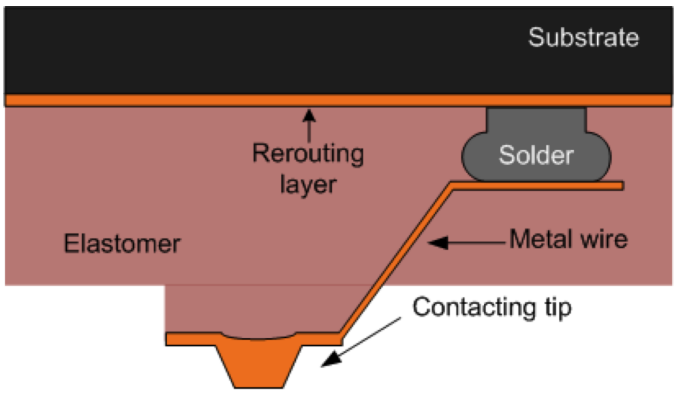


Figure 113: The compliant contact realized with CRML technology.

elastomeric matrix, ending with a pyramid shaped tip and soldered to an inorganic substrate where single or multiple routing layers can be patterned to establish the necessary electric connections to the rest of the system. The tip provides the electrical contact with die I/O pad and creates an electrical path to the substrate. The technological steps required to fabricate this structure have been presented in 6. To create a stable electrical contact, a force must be applied and kept during all the operating life of the contact, i.e. the contacting tip must be pressed against the I/O pad. The value of the force that must be applied to obtain a stable contact depends on the mechanical characteristics of the materials involved. The figure of merit is the contact total resistance, defined as [136]:

$$R_{tot} = \rho_1 \frac{l}{S} + \frac{\rho_1 + \rho_2}{4} \sqrt{\frac{\pi H}{F}} + \frac{\sigma_{film} H}{F} \tag{45}$$

where the left hand side represent the total resistance. The value of R_{tot} depends on materials parameters: bulk resistivity of tip and pad metals (ρ_1 and ρ_2, respectively), the length and section of the wire connecting the tip to the substrate (l, S respectively), the hardness H (Vicker's or Knoop) of the softer material, the resistivity of pad oxide film σ_{film} and the force F applied to the contact. The equation 45 is based on the assumption that, due to the micro roughness of surfaces, the true contact area is not the visible surface but a series of micro-contact spots whose number depends of the deformation of surfaces that, in turns, depends on hardness and applied force. The first term on the right hand side is the bulk wire resistance, the second the constriction resistance and the last one, the tunneling resistance of the oxide covering the probed pad surface:

1. the bulk resistance of the metal: $\rho_1 {}^{l}/_{S}$
2. the constriction resistance: $\left[{}^{(\rho_1+\rho_2)}/_{4} \right] \sqrt{{}^{\pi H}/_{F}}$
3. the tunneling resistance of the native oxide: ${}^{\sigma_{film} H}/_{F}$

Layout	B	A
Type	Array	Staggered Quad
Width [mm]	12.0	16.0
Length [mm]	12.0	16.0
Contacts	4325	345
Minimum pitch [mm]	0.135	0.068

Table 10: Summary of the characteristics of the test vehicles realized with the CRML technology.

The contact's self-inductance is the other important figure of merit because of the wire embedded in the polymer. The self inductance of a wire with a rectangular cross section, can be computed according to the formula [137]:

$$L_{self} = \frac{\mu_0}{2\pi} l \left[\ln \frac{2l}{w+t} + \frac{1}{2} - 0.2235 \frac{w+t}{l} \right] \tag{46}$$

where L_{self} is the wire self inductance, w and t the width and thickness of the metal, respectively, and l the total length.

8.3 TEST VEHICLE DESIGN AND CHARACTERIZATION

Two different test vehicles for testing the compliant contact have been designed. The principal layout characteristics are reported in table 10. The two testing vehicles are contactors for wafer-level burn-in probe cards for digital ICs. The "B" contactor consists of 4325 contacts evenly distributed on a 1 cm^2 area and the "A" contactor of 345 pad distributed at the periphery of a 16x16 mm die in two staggered rows. The purpose of the contacts is to provide power, ground and I/O signals to the tested IC.

The electrical specifications for probe cards in such application, that influence the design of the contactor, include the maximum steady current (often called "probe current capacity"), the signal path resistances, probe inductance and probe leakage. Probe current capacity is limited by power dissipation and electro-migration. In the design of the contactors, the maximum current for each probe is 250 mA. The wires are designed according to section 3.5.5.3 of the MIL-M-38510 standard using the following equation:

$$I = Kd^{3/2} \tag{47}$$

where I is the rated current (in Ampere), k is a constant described in the standard and d is wire diameter (in inches, being an american standard). The MIL standard refers to the maximum current in bondwires, i.e. metal wires embedded in an epoxy molding compound,

Bulk resistivity [Ωm]	Copper 1.68×10^{-8}
	Aluminum 4.00×10^{-8}
Film resistivity [Ωm^2]	Alumina 1.00×10^{-12}
Hardness [g/m^2]	Aluminum 1.30×10^{10}

Table 11: Material parameters required to compute R_{tot} from equation (45) for the materials used for the contactors.

like in the presented technology. According to the standard, the constant k, for copper or gold wires shorter than 1 mm is 30000 that lead to a wire diameter of 10.4 μm, corresponding to a cross section of 84.9 μm^2.

Contactors wires have a square cross section of 10 μm edge, corresponding to an area of 100 μm^2. The path resistance is the total resistance of a signal, power or ground path, from the probe tip to the tester interface and represent the total resistance budget that must be met. Typical total resistance requirement for power and ground lines is 0.5 Ω and for signal lines, 3.0 Ω. The contactor resistance contribution should be low enough to leave sufficient margin for the rest of the probe assembly, which usually consists of an interposer and a multilayer **PCB!** (PCB!).

The contactor contribution to the total path resistance, is given by equation (45). The values for the materials used in the two contactors are reported in table 11.

Figure 114 shows the values of the contactor resistance for different values of contact forces where it is evident that approximately at 0.3 gf the resistance is dominated by the wire resistance.

The contact forces in probing applications are above that value thus is it possible to assume that the resistance is 130 $m\Omega$ for contactor A and 92 $m\Omega$ for contactor B. Such values are low enough to provide flexibility in the design of the remaining probing structure.

The contact resistance on actual samples has been measured using a three-point techniques on a probe station by connecting 3 adjacent contacts soldered on a uniform metal layer (on the backside) embedded in PDMS as shown in figure 115. Probe needles are contacted over the three contacts as shown in figure 116.

This technique allows measuring the resistance R_b of the central contact (B in figure 116). Each needle is modeled as an ohmic resistance R_{pa}, R_{pb} and R_{pc}. A known steady current I_{DC} flows in the loop formed by the current generator, contacts A and B, and the resistances R_{pa}, R_{pb}. The voltage drop on the center branch is:

$$V_B = I_{DC} \left(R_b + R_{pb} \right) \tag{48}$$

The voltage drop is measured on the loop formed by the voltmeter, contact B and C contacts and their resistances. Since negligible current

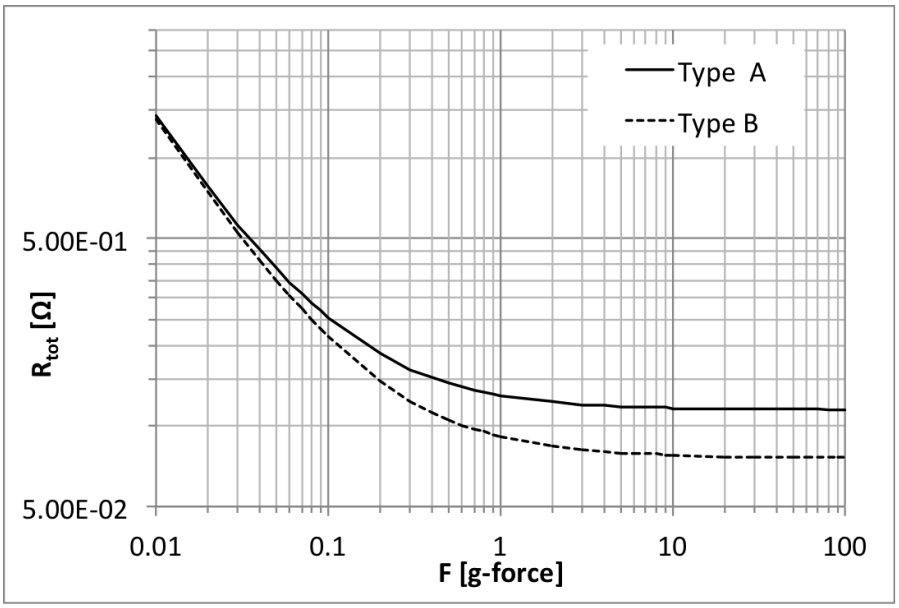


Figure 114: Total resistance of the single probe for both types of contact structures for contact forces between 0.01 and 100 grams-force on a log/log scale.

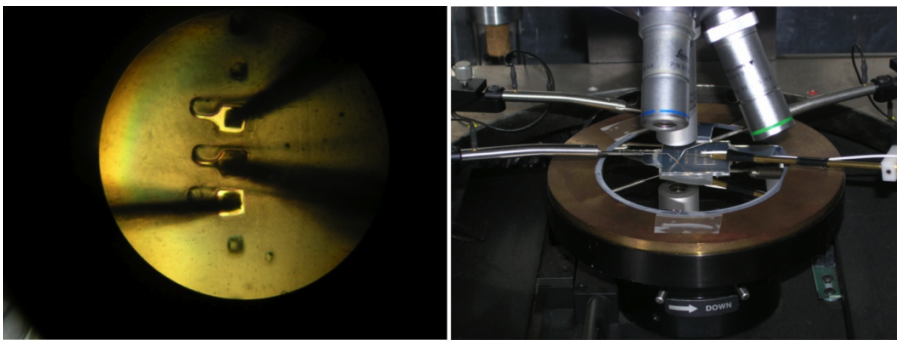


Figure 115: The measurement setup for the contact resistance. The panel on the left shows the three probes contacting the tips. The panel on the right shows the set-up.

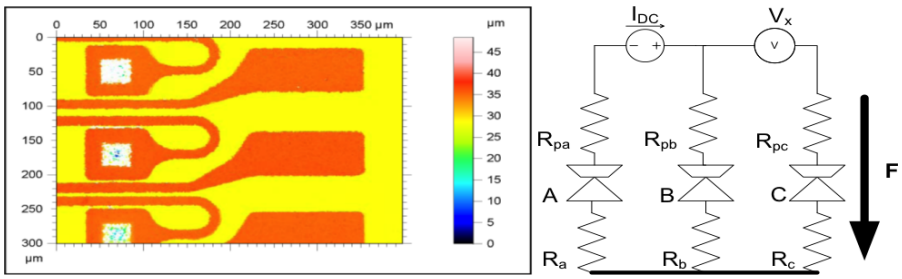


Figure 116: Profilometer images of three test pads (left) and three-points measurement technique (right).

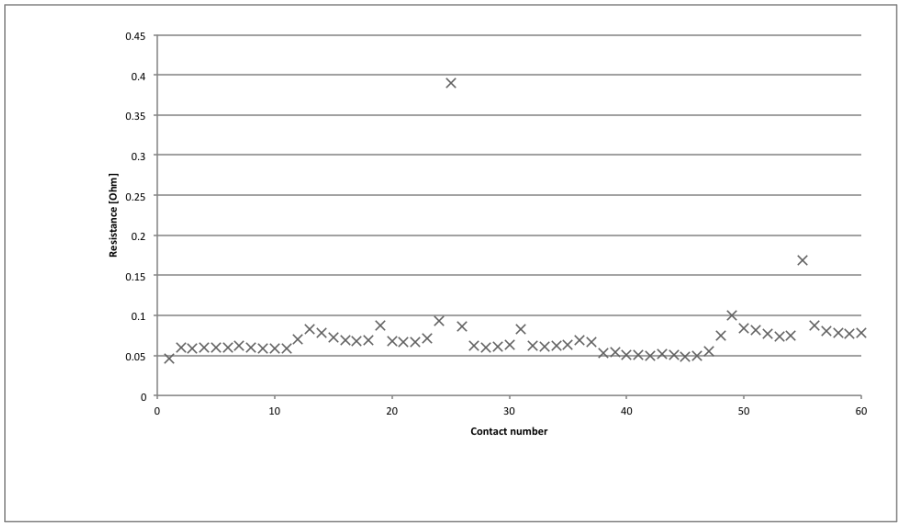


Figure 117: The resistance values measured for contactor A over 60 different pads.

flows in the voltmeter loop, and no voltage drop occurs in the metal, it is possible to determine the resistance of B branch:

$$R_b = \frac{V_b}{I_{DC}} - R_{pb} \tag{49}$$

To eliminate the probe component to the resistance, a preliminary measurement is done with probes shorted over a metal layer to extract R_{pb}. All measurements were performed using the current reversal method to eliminate the contribution of thermoelectric (electro motive forces) EMF due to differences in temperature and materials used in the set-up at a contact force of 0.5 grams.

The results of resistance measurement over 60 different pads for contactor A are reported in figure 117. The average measured value is 74 $m\Omega$, lower than the one computed. The variability depends among the contacts depends mainly on the used set-up that cannot establish identical contacting conditions in each test.

The inductance of the single probe, from the tip to the bonding pad, has been computed using equation (46). The formula can be applied to straight wires of rectangular cross-section and gives results of 0.641

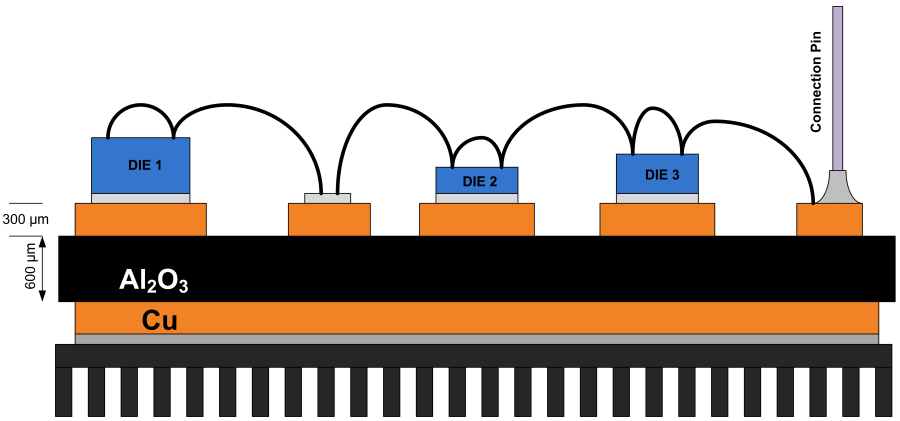


Figure 118: Representation of an Integrated Power module (IPM). Power devices (DIE1, DIE2 and DIE3), of different heights are soldered over a DBC substrate (300 um thick copper bonded on 600 µm alumina) and connected with thick (300 µm) aluminum bond wires. On the backside an heat sink is soldered for thermal dissipation. Connection pin brings control signal to an external control electronics.

nH for contactor A and 0.387 for contactor B. The "straight wire" approximation holds, as wires are designed to assume a straight shape at the end of the pulling process.

Leakage between adjacent probes is a typical specification of probe cards and acceptable values are below 10nA. In this technology the wires are embedded into a polymer matrix (eventually loaded with nano-particles) that posses a finite conductivity. The leakage between adjacent probes has been measured on actual samples and the value is less than 5nA.

8.4 COMPLIANT CONTACTS AS WIRE-BONDING REPLACEMENT

Wire bonding, in power electronic devices is one of the major failure causes. The thermal fatigue generated by the CTE mismatch of thick aluminum wires and silicon causes de-bonding and early failure of the device. The compliant contacting technology presented can solve this problem and can favor the reduction of the footprint of Integrated High Power Modules. Integrated power modules consist of a Direct Bond Copper (DBC) substrate holding power dice, mounted on a heat sink for thermal dissipation and a separate **PCB!** hosting the control circuits (see figure 118).

The control electronics is usually hosted on a side compartment of the Integrated High Power Module (IHPM) assembly, therefore increasing the dimensions of the enclosure. Reliability of IHPM is the other important issue that must be considered. The bond wires that connect silicon dice are made by aluminum and have a thickness of 300 μm. The difference in the CTE of the two materials, silicon and

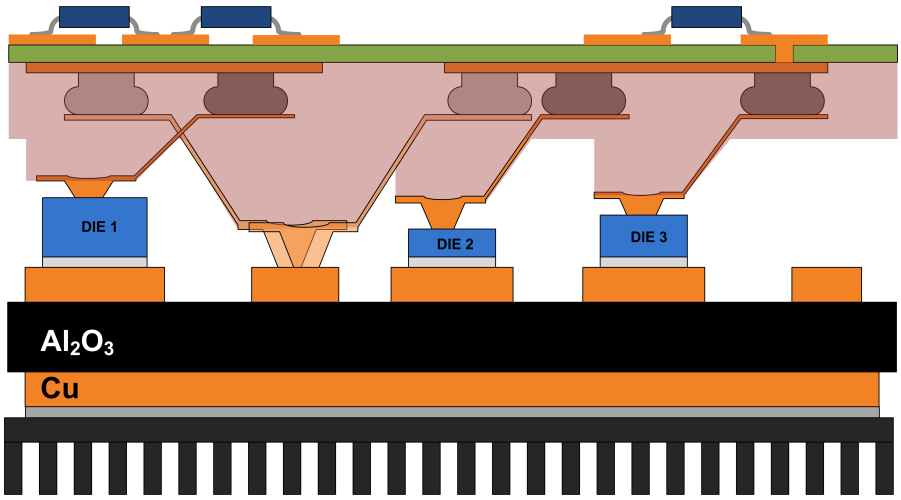


Figure 119: An improved IHPM with the same connectivity exploiting the top board to replace two long wires contacting the substrate.

aluminum (2.6x10-6 /K and 23.1x10-6 /K, respectively), exposes the bonding area to strong thermo-mechanical stress that can cause debonding during module operation. The solution to this reliability issue is the replacement of wire bonding with an alternative technology. The monolithic integration (in a single integrate circuit) of power devices with control electronics has proven to be not efficient for technical and cost reasons, therefore, new contacting technologies have been developed. Among these, the spring contacts technologies are particularly interesting because there is no need for a rigid bonding between the silicon die and the contacting wire eliminating the debonding problem. The compliant contact developed with the CRML technology fits to this purpose.

The possible integration of the assembly in an IHPM is shown in figures 119 and 120. In figure 119, a solution that can directly replace the wire bonding is presented. The connectivity between dice is the same as in figure 118, this to demonstrate that this technology can be used to retrofit existing modules. New modules can be designed with greater flexibility because some contacts can be routed on the multilayer control board (as in figure 120) to reduce traces length and improve the performances of the module, further reducing its footprint. Again the connectivity in figure 120 is the same of figure 118 but the long loop connecting to the DBC has been replaced with a shorter trace on the top **PCB!**.

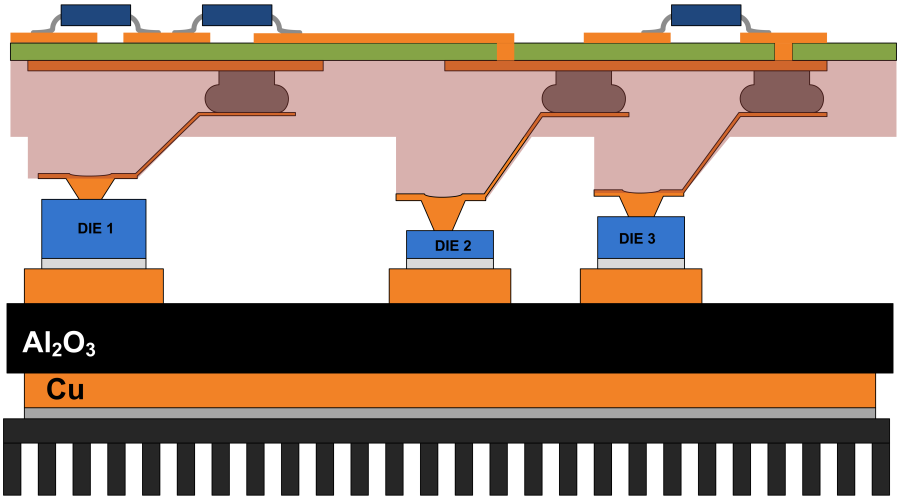


Figure 120: An improved IHPM with the same connectivity exploiting the top board to replace two long wires contacting the substrate.

9 U-HELIX ANTENNAS

9.1 INTRODUCTION

The integration of RF ICs (radio frequency integrated circuits) and antennas to form true single-chip radio [138] and, recently, focal plane arrays for THz imaging applications [139] has been made possible by the aggressive scaling of the CMOS technology. Transistors with maximum operating frequency fmax > 135 GHz [140]have been used to design 40 and 60 GHz CMOS amplifiers, and in THz radiation detectors [141]. The integration of antennas on the silicon chip is very appealing for THz imaging detectors and, it reduces the costs of packaging of single-chip radios for applications above 10 GHz.

In most of the published designs a planar antenna is built on the topmost metal layer available in the used technology. Conventional on-chip antennas are planar, since they are fabricated with the same processes used for the integrated circuit. The most common choice for the fabrication of CMOS circuits is a low resistivity substrate (10–20 Ωcm) because of the necessity to overcome the latch-up problem. However, the efficiency of planar antennas is heavily limited by high ohmic and dielectric losses in underlying silicon substrate. The efficiency of a dipole over a 10 Ωcm silicon substrate is below 10% [142]. Laying planar antennas on a polymer substrate, over an air cavity, or at the edge of the chip, have been considered as possible solutions to increase radiation efficiency. The use of three-dimensional (e.g. vertical) antennas, to reduce substrate coupling have only recently attempted, as in [143], with a monopole.

Following the same path, the CRML technology (described in 6) has been used to implement the design of a short helical antenna that can be integrated onto integrated circuits. The u-helix (micro-helix), described here, is a short inverted conical antenna fed by the external arm operating in axial mode (i.e., with end-fire type radiation pattern) and nearly-circular polarization. The u-helix is particularly interesting for applications requiring higher gain than the ones of planar antennas, operating in frequency bands where wavelength imposes micrometrical tolerances. The CRML technology allows the realization of complex geometries with tolerances defined by state-of-the-art lithographic processes on wafer scale. Antennas filling a silicon wafer with micron-size feature can be realized on a laboratory-scale mask aligner and exposure system with tight (less than 10%) tolerances on physical dimensions variability. Fire 121 shows the preliminary design of u-helix antennas, used to optimize the processes. The

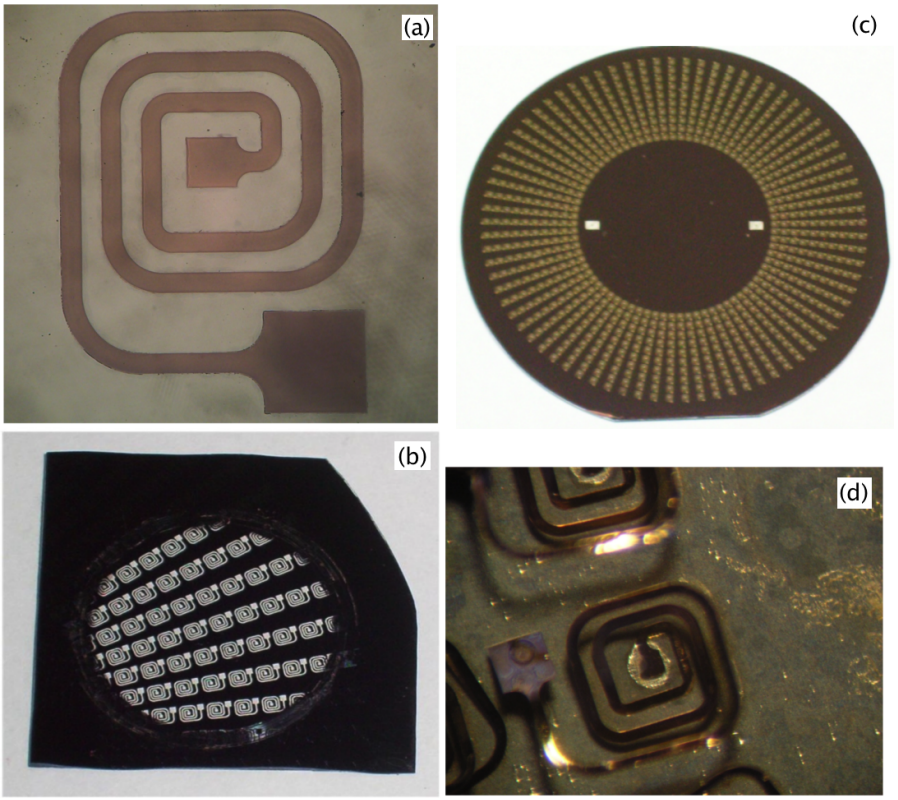


Figure 121: First prototypes of the u-helix antenna design: (a) planar structure of a single antenna; (b) quarter of a silicon wafer for testing processes for the realization of an array of u-helices; (c) full 4 inches wafer with a circular array of more than 300 antennas; (d) u-helix antenna after the pulling process, stabilized in a transparent polymer.

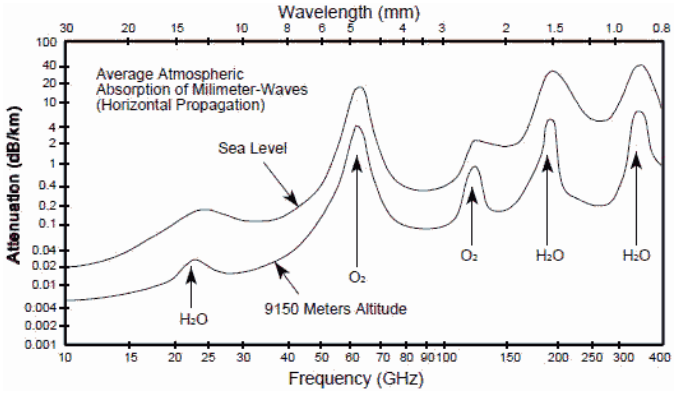


Figure 122: The average atmospheric absorption in the 10 to 400 GHz frequency range (without fog or rain contributions) at sea level and 9150m of altitude.

single u-helix, is shown, still in its planar shape on the silicon wafer in figure 121 (a): in this design, large square bond pads have been used to simplify alignment and bonding process. CRML processes have been optimized on this design to obtain a full 4 inches wafer circular array of u-helices (figure 121 (b) and (c)). The result of the bonding and pulling process is visible in figure 121 (d), where solder spreading below the bond pad is visible. In this series of experiments, the antennas were stabilized in a rigid transparent polymer.

9.2 U-HELIX APPLICATIONS

The most interesting deployment scenarios for u-helix antennas antennas are:

- *60 GHz wireless communication*: Wireless Personal Area Network (WPAN) operating in the 60 GHz band have been recently deployed and communication protocols standardized in IEEE802.15.3c. The oxygen high absorption peak at 60 GHz exploited in those systems to limit interferences, must be accounted for in the link budget to provide reliable communications. The use of an high gain antennas (as u-helix) in such system, helps in lowering power requirements of operating devices (at a fixed Bit Error Rate (BER)), improving batteries' life of mobile devices. The free-space wavelength at 60 GHz is 5mm, making very attractive the realization of an in-package antennas or antenna arrays, the latter to provide additional directivity and interference immunity in indoor applications.

- *76 GHz automotive RADARs*: integrated antennas can help in reducing the costs of short-range collision avoidance RADARs for the automotive industry, a device that could reduce the num-

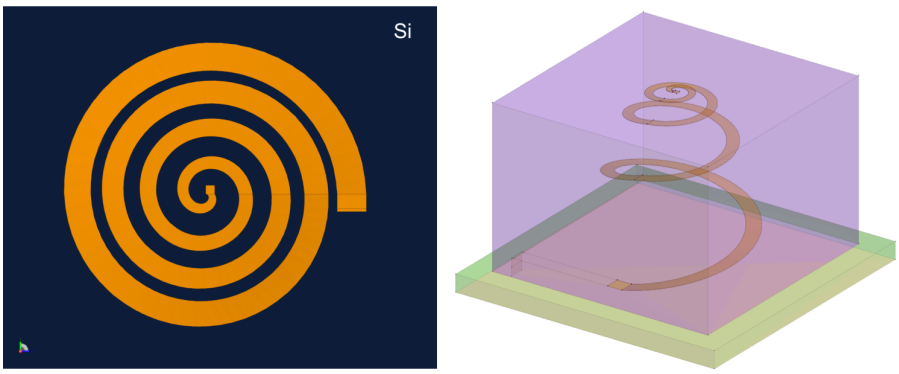


Figure 123: Top (left) and perspective view (right) of the actual design of the u-helix antenna. The perspective view shows the antenna conductor is embedded in a polymer and placed over a dielectric substrate and fed with a microstrip.

ber of car accidents. The circular polarization of u-helix helps in minimizing the detection of rain in such applications.

- *THz communications and imaging*: electromagnetic radiation in that range penetrates non-conducting materials like paper, plastics, masonry and ceramics and is stopped from metals and water. Scientific and industrial application are emerging: terahertz spectroscopy currently employed in medicine, non-destructive testing and, surveillance systems, and high-capacity communication links. The free-space wavelength in this region is between 3mm (0.1 THz) and 0.3 mm (1 THz) and IC (or MEMS) technologies are essential to fabricate antennas. Moreover, due to the small dimensions, entire focal plane arrays can be realized on CMOS chips to produce low-cost THz imaging sensors. The u-helix technology allows for the wafer-level fabrication of high-gain antennas that can be bonded on THz sensor chips.

9.3 THE U-HELIX ANTENNA

U-Helix is a monofilar short conical helical antenna with variable pitch angle. The antenna feed is connected to the largest loop at the bottom and the wire is embedded into a polymer block to guarantee mechanical stability.

The proposed antenna is similar to constant-pitch conical helices studied by Chatterjee and Nakano [144, 145, 146, 147] since 1953, and differs from them by the feeding side (the aforementioned antennas were fed from the smallest loop) and by the variable pitch angle (a limitation of the design and of the technology). The antenna metal conductor is defined by an Archimedean spiral function:

$$r = a + b\theta \tag{50}$$

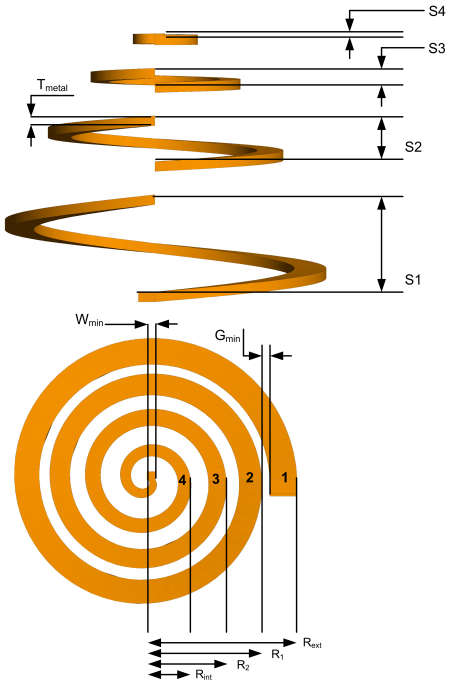


Figure 124: The u-Helix antenna with dimensional parameters in lateral and top views. In the top half of the antenna the four loops (each loop isolated for clarity) are shown, with the definition of spacings (S1 to S4). In the bottom half, the top view of the spiral is shown, with the arms radii defined (R_{ext} , R_1, R_2, and R_{int}).

where (r, θ) are the polar coordinates, and a, b the parameters that define the spiral. In this u-Helix differs from most of the conical helices whose arms follow a logarithmic spiral function. The reason behind this choice is the possibility of packing in the same space more turns, thus increasing antenna gain, given the same antenna footprint. The major drawback is that u-Helix cannot be considered true "frequency-independent antennas" (according to Rumsey's principle) so their bandwidth is usually lower than standard conical helices. The operating mode of interest in u-Helices is the axial mode.

The design procedure of a u-helix is based on an optimization that results from the combination of FEM mechanical simulations and Method of Moments (MoM) electromagnetic simulations (see figure 125). The initial guess for geometrical parameters optimization is given by the *lower-frequency helical approximation*. The lower operating frequency of the antenna is specified and, the radius of the largest arm of the spiral (see figure 124) is set equal to the one of the loop of a cylindrical helical antenna operating in axial mode at the same frequency [148]:

$$0.75\frac{\lambda}{2\pi} < R_{ext} < 1.33\frac{\lambda}{2\pi} \tag{51}$$

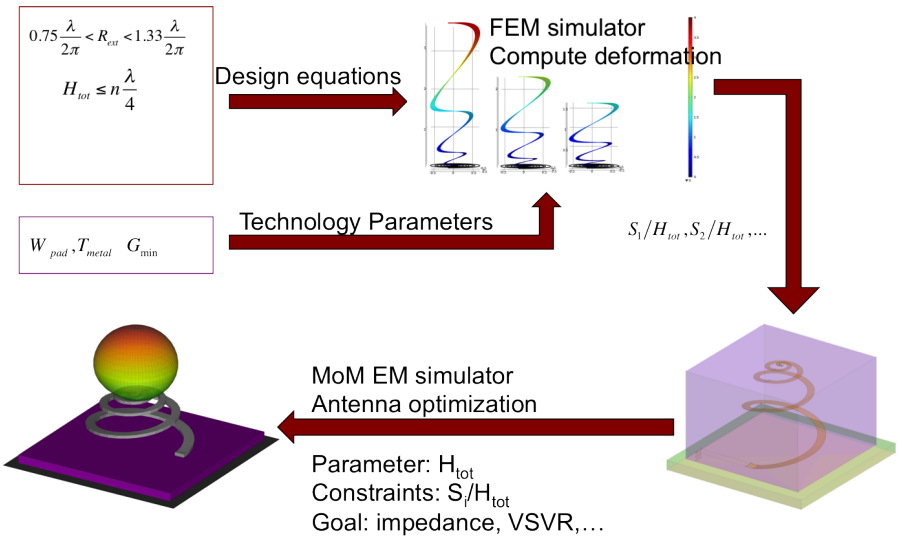


Figure 125: Design procedure for u-helix antennas is a combination of mechanical and electromagnetic simulations to optimize the final geometry.

The total height of the antenna H_{tot} (corresponding to the sum of S1 to S4 in figure 124) is set equal to the height of the helical antenna with loops spacing of $\lambda/4$ [13]:

$$H_{tot} = 4\frac{\lambda}{4} \tag{52}$$

The wavelength λ in the equations (51), (52)should be chosen equal to the wavelength in the medium surrounding the antenna. This condition becomes not essential for low permittivity materials ($\epsilon_r < 3$). The usual starting value employed for R_{ext} is $\lambda/2\pi$. Technological parameters are the constraints of the optimization procedure: in particular, due to the small dimensions of the antennas for mm-waves, W_{min} and G_{min} (with reference to figure 124), corresponding to the minimum value of metal width, and the to the minimum gap between metal traces, respectively, are the most important (metal thickness T_{metal} is considered equal to W_{min}). They influence cost and yield of the manufacturing processes.

9.3.1 *U-helix design procedure*

The u-helix antenna is implemented using the CRML technology, by controlled release of a metal conductor from a silicon wafer. In this process the metal undergoes a deformation that defines the final shape and its electromagnetic characteristics.

The u-Helix is first designed as a metal spiral according to the equation (51) with four turns. The section of the metal conductor is a square ($W_{min} = T_{metal}$) unless technological constraints (photoresist thickness, achievable aspect ratio) imposes different geometries. U-

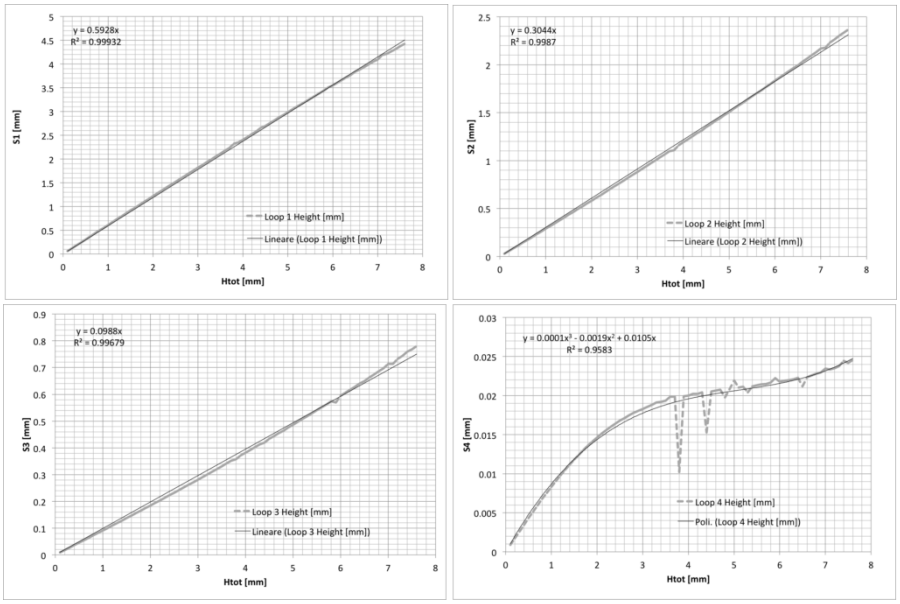


Figure 126: Analysis of the S1 to S4 parameters for the scaled model antenna (10 GHz).

Parameter	**Height [fraction of H_{tot}]**
S1	0.6
S2	0.3
S3	0.1
S4	0

Table 12: Spacings computed by FEM for the 10 GHz scaled model.

helix for different frequencies are obtained by scaling the geometry in figure 123 (top view). The geometry is transformed in a 3D model of T_{metal} thickness extruding the shape. The pulling process of the resulting model is simulated with a FEM simulator to compute the deformation that the antenna conductor undergoes when the one side is pulled by a height of H_{tot}. An example of the procedure to compute S1 to S4 is reported in figure 126, for a scaled model of the design designed to operate above 10 GHz.

The parameters S1 to S4 in figure 124 are computed at different extensions (pulling heights) to derive constraint relations that will be used in the electromagnetic simulator. The linear fit parameter describes the height of each loop for different heights, up to H_{tot}=7 mm. It can be seen from the image that the three larger loops follows a linear relationship, while the fourth a cubic one.

The evolution of conductor shape, from the planar spiral to the fully extended u-Helix is shown in figure 127 (for the 10 GHz antenna sample), where a comparison with the result of a FEM simulation is also shown. The different pitch angle is evident.

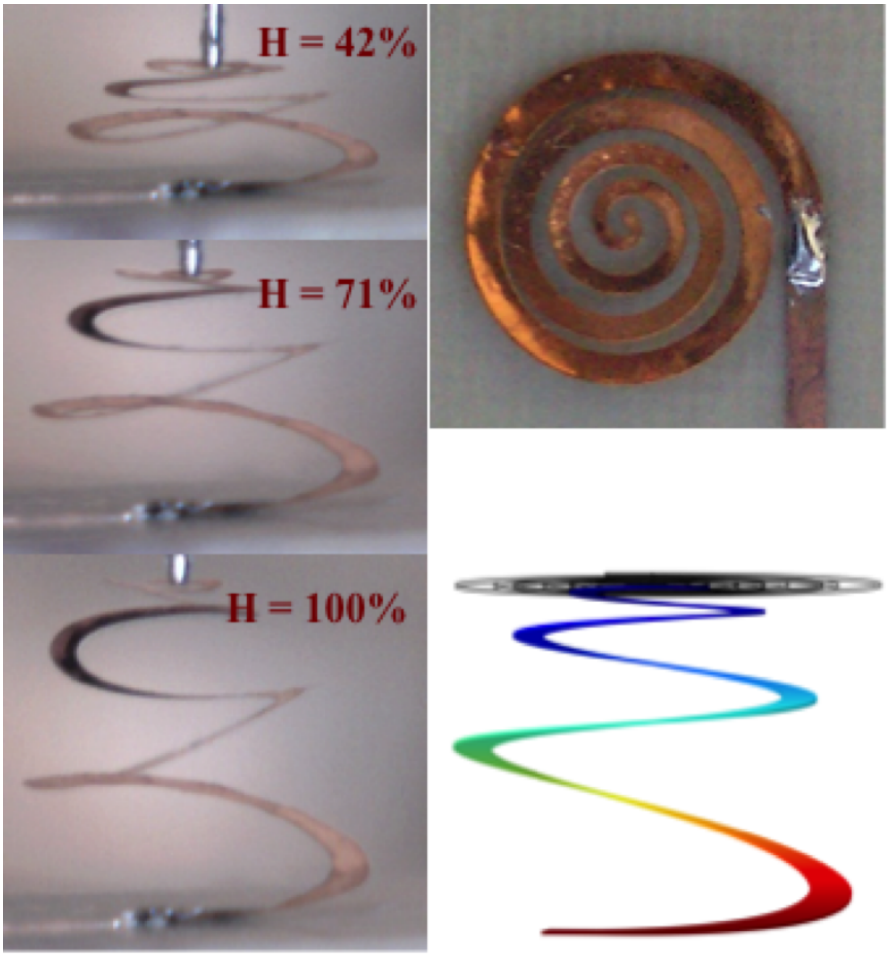


Figure 127: Analysis of the pulling process on a scaled model of the u-Helix antenna (the planar spiral is shown on the top right). In the left part of the image, the evolution at three different height (the numbers represent the % of total extension for each photo) is shown. The computed deformation, corresponding to 100% of extension is shown on the bottom right.

Table 12 reports the spacings S1 to S4, obtained by FEM simulations; the value of S4 is set to zero. The deformation of the fourth loop, in this design is neglected in the electromagnetic simulator. The values represent the fraction of H_{tot} that each turn of the spiral takes. I The region of validity of the computed is for deformations up to $H_{tot} = 1cm$. Performing simulations up to the total height defined by 52, while correct in principle, presents the drawback that non-linear phenomena due to the stress imposed to the metal wire (metal undergoes plastic deformation) reduces the accuracy of fitting parameters. It is know that u-helix are short antennas and that, the optimum values of total height are, in the 0.1λ - 0.4λ, so FEM simulation are carried on in that region.

The computed parameters are imported into an electromagnetic simulator (u-Helix have been simulated with MoM) as constraints, and the structure optimized by varying to height of the antenna. The optimization goal is the maximum gain at the design frequency. The results of simulations of this scaled model are presented in section 9.7.

9.4 U-HELIX ANTENNA FOR WPAN APPLICATIONS

The most prominent application of millimeter-wave communications is data transfer between personal digital devices (smartphones, personal digital assistant, mobile computing devices, etc.). The term Personal Area Network (PAN) has been coined to describe this kind of communications. Devices in a PAN typically use short-range, high-bandwidth links to exchange data between them (i.e., multimedia file transfer between mobile devices) and medium range links to transfer data to remote sites via a central infrastructure. The atmospheric propagation limits the inter- device communications to a few tens of meters and the device-infrastructure communication to few-hundreds. This is not a drawback in PAN as the concept of "personal area" suggests that communications should occur in an area under the control of the single person. For such applications, carrier frequency should be centered on absorption peaks to reduce interferences from nearby devices and, to provide some form of security against eavesdropping. The second application by importance is short-range RADARs, mainly collision avoidance radars for the automotive industry. Automotive RADARs are studied since the 70s of the past century [149] and only recently have been installed on high-end cars, and their general deployment is not yet foreseeable. On board millimeter-wave RADARs are used to inform the driver about potential collision risk with the preceding vehicle, to reduce the braking time by pre- tensioning brakes, to deploy the passive restraint systems, to reduce the risk associated to blind-spots in lane change and to provide information to station-keeping for automatic cruise-control.

Automotive RADARs should operate under all atmospheric conditions (e.g., heavy rain or fog) when severe additional absorption (with respect to the values shown in figure 122) is present, therefore the operating frequencies should be chosen around the absorption minima. The contrasting needs of the two different applications (communications and ranging) imply that they cannot share the same frequencies. Regulatory agencies share at least 5 GHz of continuous unlicensed bandwidth between 56 GHz and 66 GHz, assigned to WPAN applications, centered on the O_2 absorption peak. All share the 76 GHz - 77 GHz band for the automotive RADARs, near the minimum of absorption. International Telecommunication Union (ITU) and Mimistry of Post & Telecommunications (MPT) (Japan) have assigned the 60 GHz - 61 GHz band to RADAR service and Federal Communication Commission (FCC) the 46.7 GHz – 46.9 GHz band, where absorption is lower. It is evident that there exists a continuous frequency range of 21 GHz bandwidth (i.e. from 56 GHz to 77 GHz) that can be exploited for combining communication and ranging systems in automotive applications. Such combination is the essence of the Intelligent Transportation Systems (ITS) applications, in which the vehicle is required to react to stimuli coming from the environment, co-operate with its neighboring vehicles and with the road traffic-control systems. In this view the concept of WPAN can be extended to include the car in the "personal digital devices" in the network and the traffic-control systems in the infrastructures. In this work we present a high gain antenna that can operate across the entire (21 GHz) bandwidth and can be integrated into the package of an IC. The antenna can be used in a combined communication-RADAR system for inter-vehicle WPAN communications and ranging or in base stations form WPAN communications (e.g. road traffic control system, indoor multimedia-streaming hubs, etc.).

9.4.1 *The design of a u-helix antenna for WPAN applications*

The design procedure of a u-helix antenna follows the procedure highlighted in section 9.3.1. Here a 55 GHz to 85 GHz antenna is designed and analyzed for combined WPAN/RADAR applications. The u-helix is designed under the lower-frequency helical assumption at the frequency of 55 GHz and, according to equation (51):

$$0.427\,mm < R_{ext} < 0.756\,mm \tag{53}$$

The value chosen for R_{ext} has been 0.72 mm, to allow for larger conductor width. The technology-dependent constraint, for this particular implementation of the u-helix have been chosen for compatibility with packaging processes of the semiconductor industry because the intended integration of this antennas is on a SiP.

Feature	Limit Value	Limit
Minimum trace/gap width (W_{min}, G_{min})	$> 40\ \mu m$	Lithography, yield, bonding
Maximum metal thickness (T_{metal})	$< 20\ \mu m$	Photoresist thickness

Table 13: Technological constraints for 55 GHz u-helix antennas for in-package integration.

Arm	Radius	Metal Width
1	0.72 mm (R_{ext})	0.13 mm
2	0.55 mm (R_1)	0.11 mm
3	0.38 mm (R_2)	0.08 mm
4	0.21 mm (R_{int})	0.06 mm

Table 14: Radii and metal widths for 55 GHz u-helix antenna.

Table 13 reports the technological constraints for this class of antennas. In this case, conductor section is not square due to the limited photoresist thickness. Metal width of the external spiral has been set to 0.13 mm to reduce the accuracy requirement for the alignment procedure with the substrate. The minimum gap (G_{min}) between the different arms of the spiral and the minimum trace width (W_{min}) have been both set to 0.04 mm, and the metal thickness (T_{metal}) to 0.01 mm. The dimensional parameters of the antenna are summarized in table 14.

The total height of the antenna, computed by the return-loss minimization driven optimization procedure is 1.3 mm. FEM simulations, were carried for displacements up to 3.57 mm displacements (see figure 128) to evaluate the evolution of loops' height (S1 to S4 parameters) and passed to the MoM simulator to optimize the structure in the desired frequency range and for the actual operating conditions.

The electromagnetic model includes the surrounding medium (silicone in this case with $\epsilon_r = 2.33$, dissipation factor @10GHz 0.02) and the substrate below the antenna. The substrate consists in a 5mm x 5mm, 0.127 mm thick, dielectric substrate with the characteristics of Arlon 25N (permittivity $\epsilon_r = 2.22$, dissipation factor @10GHz 0.0025). Ground plane is placed below the substrate and the antenna is centrally fed by a metal arm. The largest loop of the antenna is bonded to one extreme of the metal arm and the other arm is connected to the feed through a via hole in the substrate (as shown in figure 129).

The MoM simulator is used to simulate the antenna in the frequency range of interest and optimized to minimize S11 (return loss). Sensitivity of the radiation characteristics to the H_{tot} parameter have been estimated by performing simulations at $H_{tot} \pm 10\%$. The values

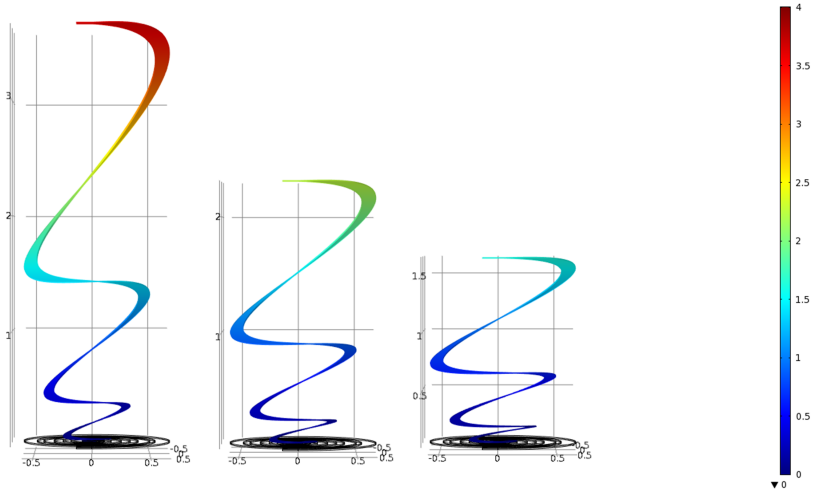


Figure 128: FEM simulation form the 55 GHz u-helix antenna. Deformation and spacing between arms of the metal conductor at three different displacements (from left to right: 3.57 mm, 2.25 mm and 1.6 mm) for a 0.01 mm thick copper metal layer. All dimensions are in mm and the color scale represents the displacement.

of the spacings S1 to S4, for the nominal value of H_{tot} are: 0.78 mm, 0.385 mm, 0.123 mm, and 0 (S4 is always zero).

The results of the simulations are shown in figure 130.

9.4.2 *U-helix WPAN antenna characteristics*

The u-helix antenna is essentially a conical helix, a class of antennas that has been thoroughly studied. The characteristics of the conical helix are usually derived from the circular helix for which Kraus (its inventor) made a thorough analysis. The circular helix is a traveling wave antenna that can radiate in three different modes: normal mode (broadside), axial mode (end-fire) and conical mode (dual lobes). The operating mode is a function of the pitch angle and the radius (compared to the wavelength) of the helix and the different modes arise from the current distribution along the helix. In the case of the WPAN u-helix antenna, the axial mode is of interest and the target is to obtain a single lobe for frequencies between 55GHz and 85 GHz, therefore covering the 60GHz communication band and the 76 GHz RADARs band. In [144], it is reported that, to obtain the axial mode in the conical helix, at least one of the loops should satisfy (51). In the case of the u-helix the largest loop is designed to meet this requirement.

In figure 130(a, b) the axial mode is evident, with an Half Power Beam Width (HPBW) (Half Power Beam Width) of 62° and a gain of 8.4 dBi. The radiation pattern at 85GHz shows a tilt and a slight reduction of gain (this is evident in figure 130 (a, b)). The frequency

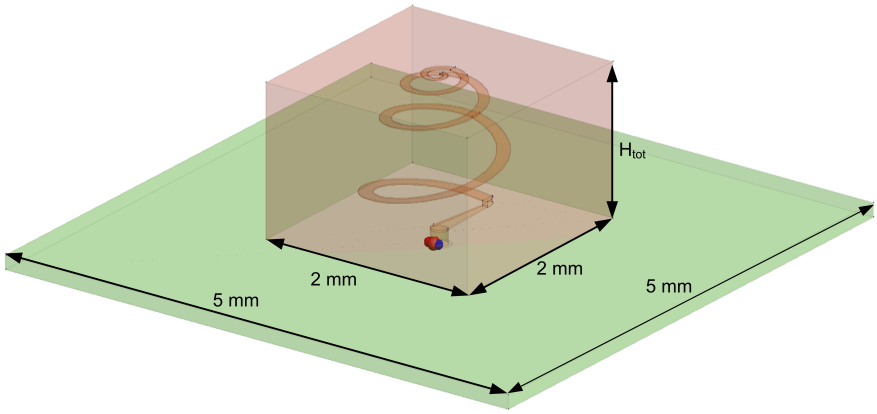


Figure 129: Model for the MoM simulator of the 55 GHz u-helix antenna. The antenna is embedded into a 2mm x 2mm x H_{tot} dielectric cube made of silicone, $\epsilon_r = 2.33$) and over a 0.127 mm dielectric substrate. Ground plane is at the bottom and the arm visible in the figure centrally feeds the antenna (through a via hole in the substrate).

at which this tilting start is 76 GHz, as the axial gain plot in figure 131 shows. Figure 130 (f) shows that the radiation pattern is insensitive to a ±10% change in the height of the antenna (antenna0_9 corresponds to -10% and antenna1_1 to +10%). The antenna real part of the impedance (figure 130 (d)) is in the range 63 Ω to 42 Ω (corresponding to a variation of 50% in 21 GHz) and the imaginary part (figure VSWR (e)) shows that the antenna is inductive. These results are largely due to the effect of the via-hole in the substrate (0.15 mm diameter, 0.127 mm thickness). The Voltage Standing Wave Ratio (VSWR), shown in figure 130 (c), is always below 1.5 in all the simulated range, and the reflection coefficient is always below -14dB (see figure 132).

9.4.3 *U-helix applications for WPAN*

The u-helix antenna, being a high-gain directive antenna, can be effectively employed in base stations of indoor WPAN communication systems operating at 60 GHz or, in phased array in automotive RADAR/W-PAN systems, where the same antenna is used for both communication and ranging. Figure 133 shows an "in-package" application of a u-helix array. The silicon system is placed on the bottom of an organic substrate (like the one simulated here) and connected to the substrate with Controlled Collapse Chip Connection (C_4) bumps (flip-chip). The u-helix array is realized, as described before, on the top layer where the feeding arms are realized. The connection with the silicon chip is done through via-holes. The bottom layer constitutes the ground plane for the antennas array and isolates the radiating structures from the lossy, high permittivity silicon substrate. The an-

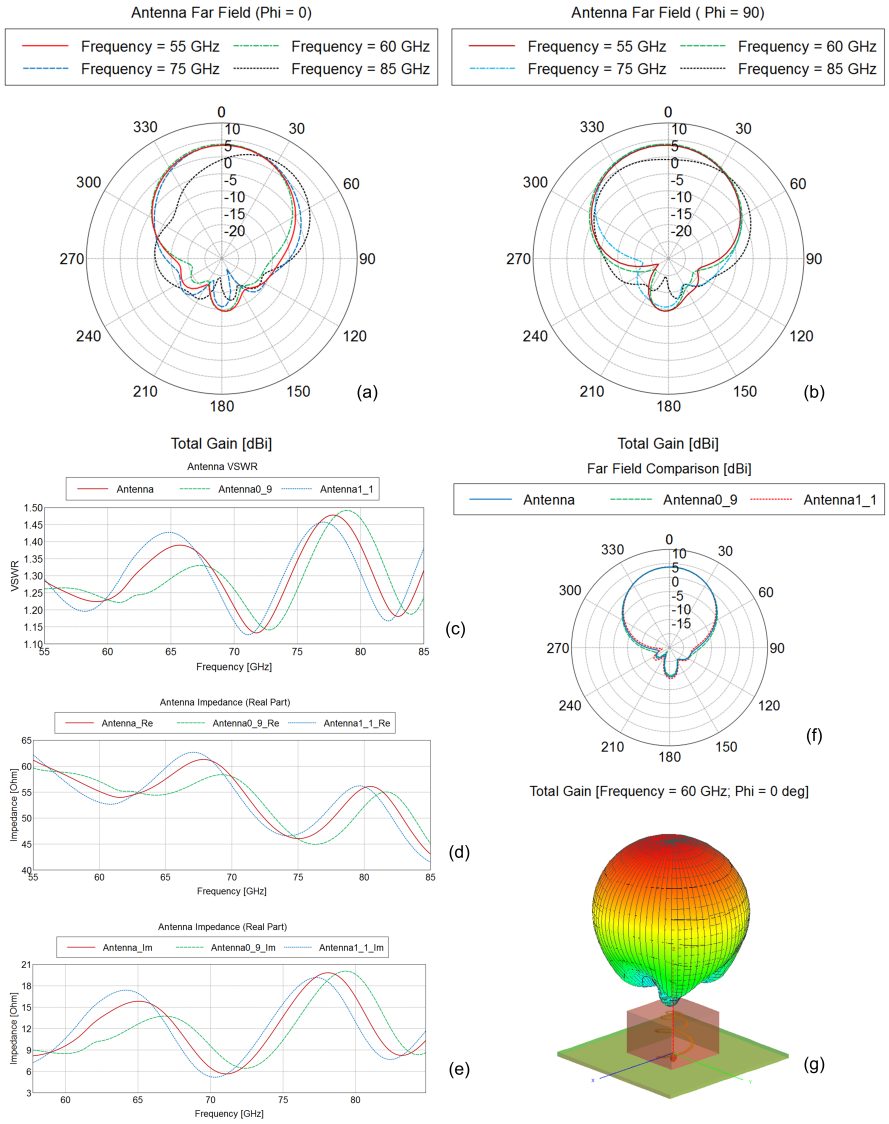


Figure 130: 55 GHz u-helix antenna characteristics for three different heights: H_{tot}, $H_{tot} + 10\%$ (identified by 1_1), and $H_{tot} - 10\%$ (identified by 0_9). Far field gain for the optimized antenna (a, b); VSWR for the three different heights (c); real and imaginary part of the antenna impedance for the three heights (d, e); comparison of the far field gain at 60 GHz for the three heights (f), and solid of radiation of the antenna at 60GHz (g).

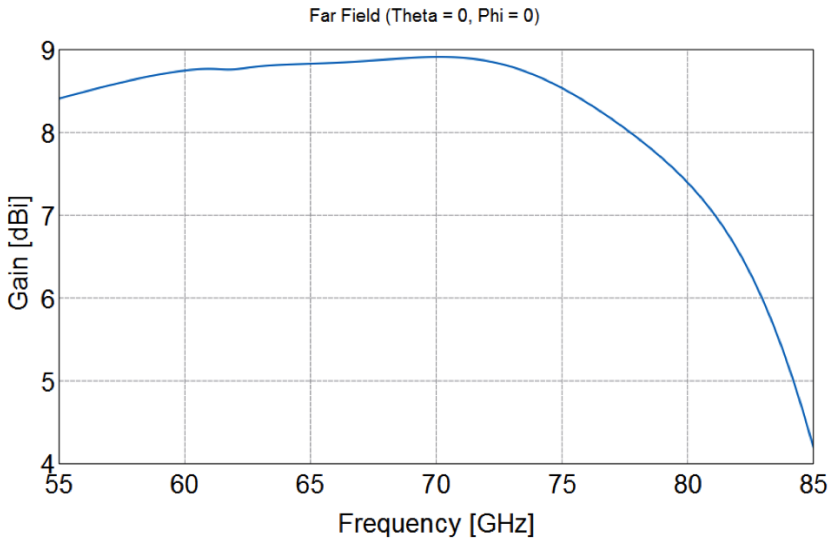


Figure 131: The gain of the 55GHz u-helix antenna in the axial direction in the frequency range of interest. The gain reduction after 76 GHz is due to the tilting of the radiation pattern (see figure 130(a, b)).

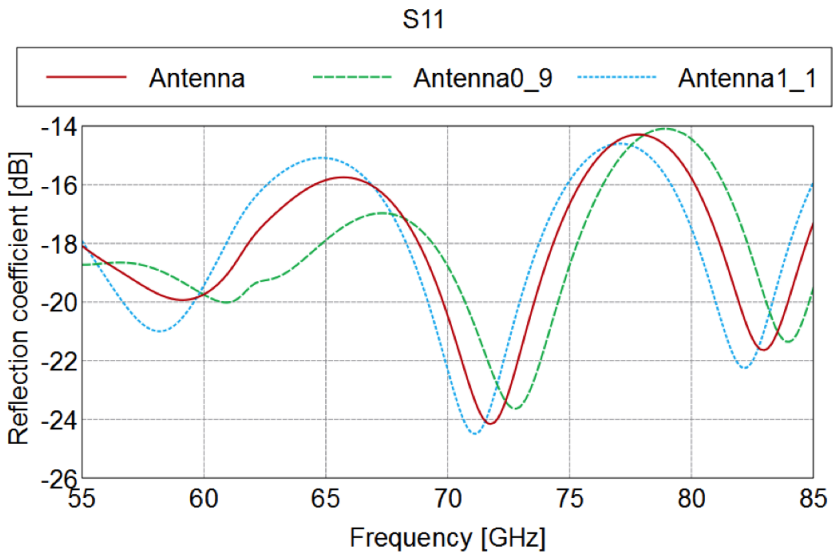


Figure 132: Return loss (S11) for the 55GHz u-helix antenna (at nominal height and for ±10% variations.

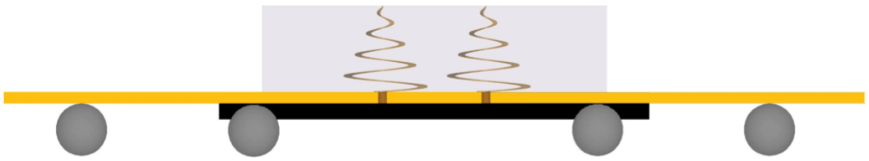


Figure 133: In package integration of the 55 GHz u-helix antenna. The RF integrated circuit is placed below an organic substrate and an array of u-helix is bonded on the other side and connected to the IC by via structures.

tennas are embedded in a polymeric material for mechanical stability as described before. If solder balls are placed on the lower side of the organic substrate, the entire assembly constitutes a SIP (System in Package) that can be installed on standard Printed Circuit Boards (PCBs).

9.5 U-HELIX ANTENNAS FOR MILLIMETER WAVES

The terahertz region of the electromagnetic spectrum extends, conventionally, between 0.1 THz and 10 THz (corresponding to wavelengths between 3 mm and 30 μm, respectively) or, between 0.3 THz and 3 THz (corresponding to wavelengths of 1 mm and 100 μm, respectively), to be consistent with the definition of "submillimeter radiation". The interest in such electromagnetic radiation in that range comes from its ability to penetrate non-conducting materials like paper, plastics, masonry and ceramics and to be stopped from metals and water. Typical applications for THz radiation are spectroscopy (eventually with imaging capabilities) and communications. Terahertz spectroscopy is currently employed in medicine, non-destructive testing and in surveillance systems. Biomedical spectroscopy exploits the excitation of vibrational modes of the water molecule caused by irradiation with THz frequencies. The strong absorption peak around 5.6 THz of water, the most abundant constituent of biological tissues, is used in Terahertz Pulsed Spectroscopy (TPS) to reveal difference in its concentration in tissues. TPS used in conjunction with imaging, can generate a contrast map, corresponding to different water concentrations that can be used to isolate tumor from healthy tissue or, muscles from adipose tissue. The advantages of THz radiation are its non-ionizing nature and the highly attainable spatial resolution (250 μm lateral resolution). Such characteristics, combined with possibility to penetrate fabrics, make THz imaging important for surveillance systems like body-scanners, to reveal objects concealed on the human body. In TPS the transient electric field is measured and the complex permittivity of a material can be determined. This offers the possibility to distinguish different materials from their permittivity, like ceramic knives hidden on a human body or, difference in material

composition or the presence of inclusions in non-destructive testing and non-destructive quality control.

High throughput data communication is the other important application for THz frequencies, as in the indoor transmission of uncompressed high-definition multimedia streams. The advantages of THz communications should be evaluated in comparison with either microwave or millimeter wave links and infrared links, for which the THz region constitutes the separation region. THz links, potentially, have higher bandwidth capacity than microwave or millimeter wave links, and, due to the less free-space diffraction, the link is more directional. On the other hand, the higher free-space attenuation (102 dB for a 10 m, 300 GHz link) translates to the need of employing high-gain (33 dB for the 10 m link) antenna, therefore limiting the communication to line-of-sight path. Even if free-space attenuation poses a severe limitation to the distance that can be covered by a THz links, they are less sensitive than infrared to atmospheric conditions like fog and therefore they can be more reliable for outdoor communications. Industrial, large-scale exploitation of the terahertz region requires the availability of cost-effective, portable, sources and detectors. The common component of both is the antenna, the interface with the free-space. The challenges in designing an antenna at such frequencies lies in its small dimensions that, being connected to the wavelength (300 μm at 1 THz in free space), impose tight manufacturing tolerances. Radiating structures having sub-millimeter dimensions and micron tolerances are not easily produced by conventional methods (e.g., drilling, cutting and milling) and require the use of micro-fabrication techniques developed for the realization of MEMS structures on silicon wafers. Such techniques are based on photolithography to define structures with accuracy of 1 μm with high repeatability, and to anisotropic etch processes like DRIE or KOH (Potassium Hydroxide) to create 3D structures. Antennas for millimeter and sub- millimeters waves, realized with these technologies, have been presented in the past [150, 151, 152, 153, 154, 155]. The high resolution and low dimensional tolerances of the **CMRL!** technology makes it attractive for the design of physically small antennas. A class of 6 u-helix antennas operating in the 0.1 THz to 1 THz region has been designed and simulated.

9.5.1 *U-helix NEC2 simulations*

Preliminary simulations of 1THz u-helix antenna have been performed with a simplified model with NEC2 simulator (using 4NEC2 code implementation). The model consists of a constant pitch angle conical helical antenna with only three loops (like the preliminary design presented in121) with: $R_{ext} = 95\mu m$ (corresponding to $1.2\lambda/2\pi$ in equation (51) for $\lambda = 0.5$ mm, i.e. 600 GHz), H_{tot} =0.38 mm (corre-

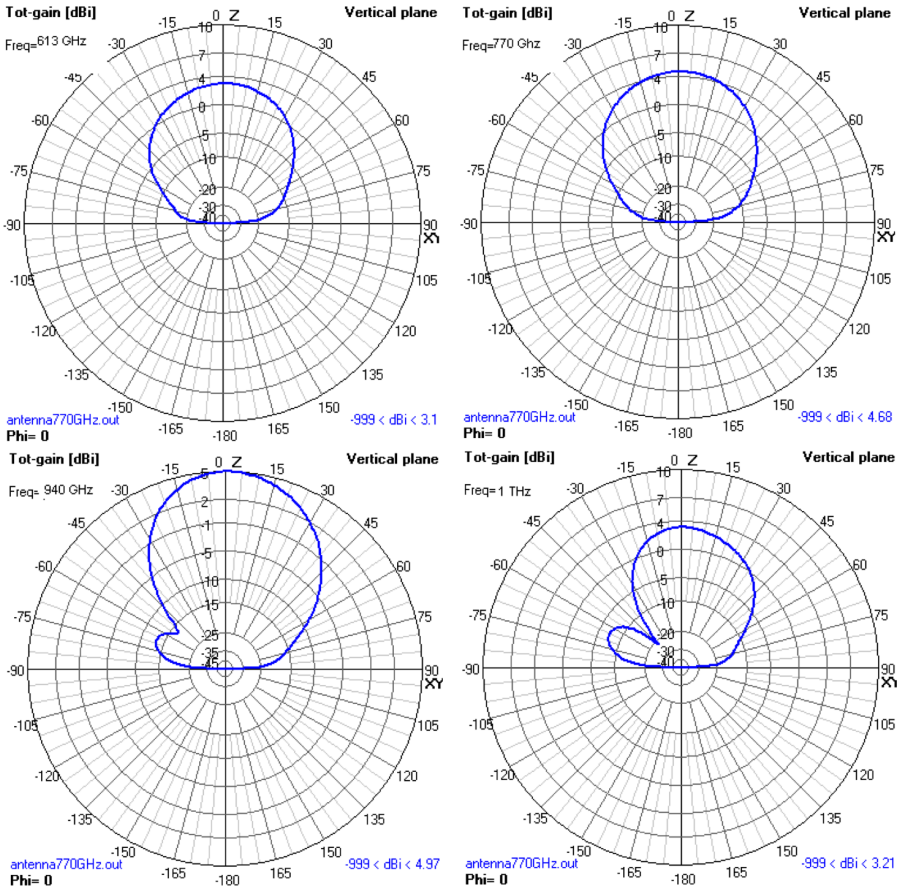


Figure 134: Radiation pattern of the 1THz u-helix antenna simulated with NEC2.

sponding to three loops spaced at $\lambda/4$ at 600 GHz), $W_{min} = 10\,\mu m$, and $T_{metal} = 5\,\mu m$. The antenna has been simulated in free space over an infinite ground plane and fed from the external arm.

The antenna structure characteristics have been simulated with 4NEC2 numerical electromagnetic code in the 0.6-1 THz band. The key parameters for defining the antenna's working bandwidth were:

- HPBW $\leq 70°$,
- $R_{in} \gg X_{in}$ (real part of the input impedance greater than the imaginary part),
- $\Delta R_{in}/R_{in} < 10\%$,
- side lobes lower than 20dB.

Simulations results (see figures 134 and135)show that the antenna radiates in axial mode up to a frequency of 770 GHz, where it presents a gain of 4.68 dBi. The gain at 940 GHz is still above 4dBi but a sidelobe with a a gain of -15dBi (-2dB with respect to the maximum gain) appears, indicating the starting of normal mode of radiation. The gain of the antenna reduces at 3.21 dBi at 1 THz and the sidelobe has reached -7 dBi (-10.2 dB with respect to the maximum gain). The input impedance presents a real part greater than the imaginary and has a value near 140 Ω, close to the theoretical value of an helical antenna radiating in axial mode:

$$Z_{in} = 140\frac{2\pi R_{ext}}{\lambda}\ [\Omega] \tag{54}$$

The antenna presents an inductive behavior for frequencies above 770 GHz. An inductive antenna is particularly interesting for on-chip integration because the output of MOSFET stages it typically capacitive. According to the specifications given, the u-helix antenna has a fractional bandwidth of 51% (from 613 GHz to 940 GHz). This result demonstrate the achievable performance of the u-helix antennas, despite is clearly an over-estimate the actual bandwidth of the antenna, because of the ideality of the model.

9.5.2 *U-helix antennas in the low terahertz region*

The design procedure described in 9.3.1 has been applied to six different u-helix design to covering the frequency band between 0.1 and 1 THz. Table 15 shows the results of MoM simulations for the six u-Helix antennas. The frequency in the table is the one that sets the radius of the largest arm in the *lower-frequency helical approximation*. The external radius (R_{ext}) and total height (H_{tot}) after the optimization procedure are shown. The quantities in parentheses are the coefficient in (51) and the total height as fraction of the wavelength, respectively. The conductor dimension for the antenna at 1 THz required it to be

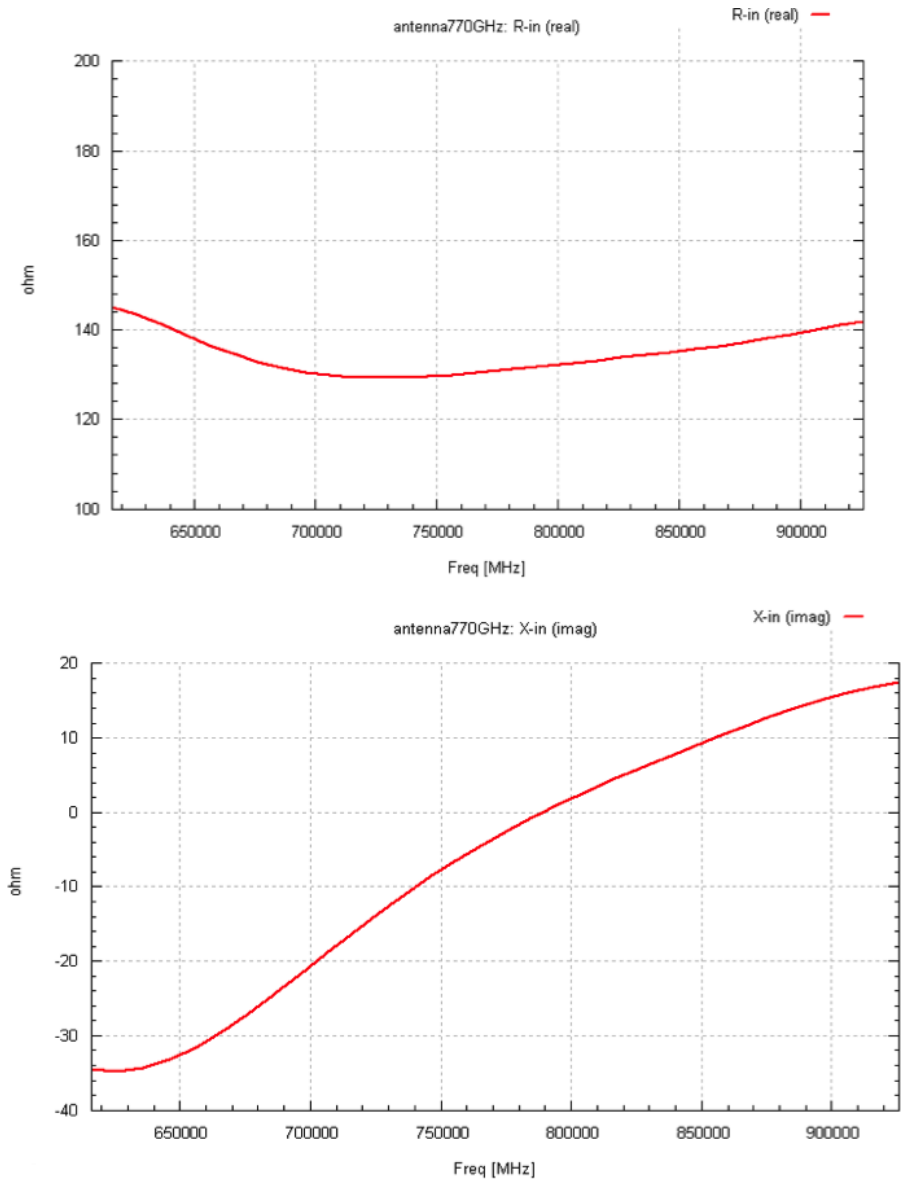


Figure 135: Real and imaginary part of the input impedance of the 1 THz u-helix antenna simulated with NEC2.

f [Hz]	Dimensional characteristics				Performances		
	Rext [µm]	*Wint [µm]*	*Tmetal [µm]*	*Htot [µm]*	*Gain [dBi]*	*VSWR (50 Ω)*	*|Zin| [Ω]*
1.0e11	480 (1.01)	26	20	640 (0.21)	4.96	< 2	30 -100
2.0e11	240 (1.01)	13	10	550 (0.37)	5.56		
4.0e11	120 (1.01)	7	7	255 (0.34)	6		
6.0e11	80 (1.01)	4	4	209 (0.41)	6		
8.0e11	60 (1.01)	3	3	90 (0.24)	5.1		
1.0e12	55 (1.15)	3	3	48 (0.16)	7.6		

Table 15: U-helix antennas for the low-THz region.

slightly larger (with respect to the wavelength) than the others. The dimensions of the antenna conductor (W_{int} and T_{metal}) reported have been chosen according to technological limitations: the upper limit depends on the availability of thick photoresists and the lower one by the resolution achievable on proximity/contact exposure system for photolithography and, from reliability issue in the release process of CRML technology.

In the MoM simulations the antennas have been simulated over an 8 μm thick finite dielectric SiO_2 layer ($\epsilon_r = 3.9$) that models the stack of inter-layer dielectrics in the integrated circuit. The optimizer in the simulator varied the H_{tot} to maximize the gain at the design frequency with the constraints in table 12. The maximum gain obtained for each antenna design is shown in table 15. The VSWR over a 50 Ω impedance is always below 2 and the magnitude of the impedance is in the 30 to 100 Ohm range in a fractional bandwidth of 40%.

9.5.3 *On-chip integration of u-helix*

U-helix antennas can be integrated in standard integrated circuits by standard bonding processes. Moreover, all designed u-helix fits inside $\lambda/2$ cell (1.5 mm at 0.1 THz and 0.15 mm at 1THz) and can be easily arrayed, including the one designed for WPAN applications in 9.4, where an in-package integration was favored. Integrating antennas and phased array directly over the silicon chip, not only reduces the overall system costs, but reduces the losses associated to the interconnect. All u-helices presents, in their operating band, a range of frequency where their impedance has an inductive component. This is favorable for connecting such antennas at the output of MOSFET, that have a capacitive output.

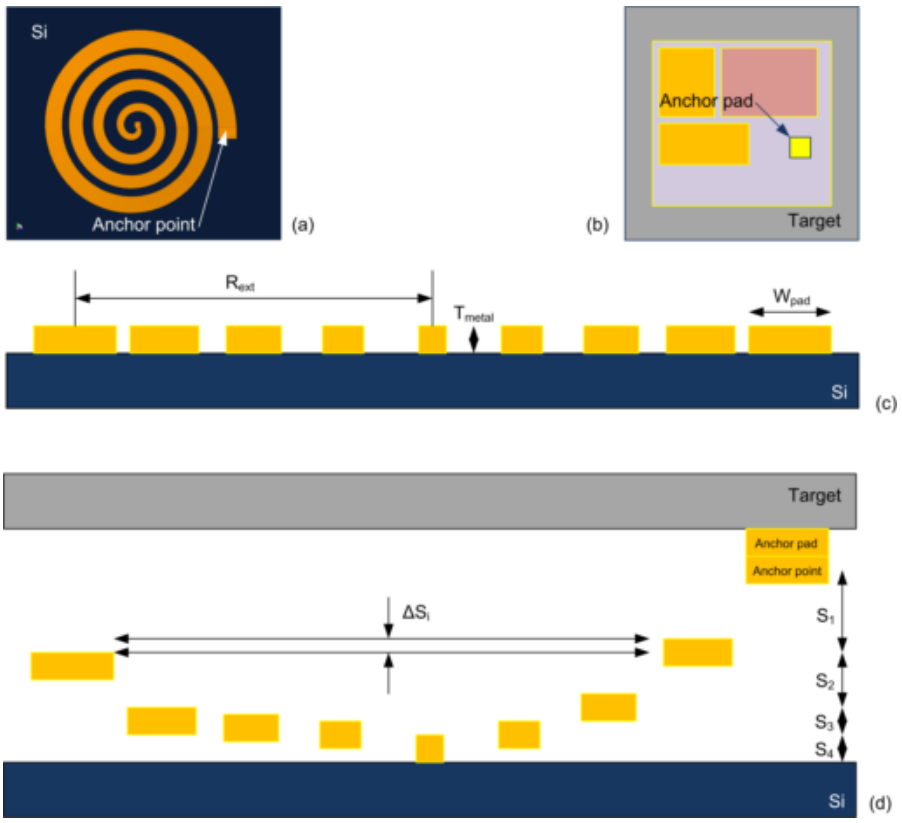


Figure 136: On-chip integration of u-helix antennas. The substrate hosting the antenna is bonded to an I/O pad of the RF IC using a suitable interconnection technique: copper pillar, gold-to-gold bonding, etc.

On-chip integration of u-helix is back-end process at packaging stage after chip passivation. The area where u-helix antennas are bonded must be free from I/O pads, otherwise the embedding polymer will prevent further chip connections. Several packaging strategies can be used like interconnect fan-in, reconstituted wafer etc. The most economical one would be to deposit a redistribution layer to connect the antennas at the center of the chip, leaving bond-pads on the periphery. In some processes, TSV structures can be used to connect antennas from the backside of the wafer. To reduce losses, integration of focal plane arrays for THz imaging should be done without chip passivation on gold-plated bond pads. In this particular case, the first step in the process outlined below is not necessary. In figure 136 a die-scale process is outlined:

1. connection structures taller than passivation layer must be realized on the silicon wafer. The usual structure used in Tape Automated Bonding (TAB), copper pillar, or solder bumps can be used,

2. the host wafer containing u-helices is aligned to silicon wafer so that the feed point of the u-helix coincides with the anchor pad on the chip,

3. the bonding process is carried on to join the antenna to the silicon chip,

4. the two substrate are pulled away one from the other, causing the release of the metal wire,

5. an encapsulant is dispensed in the gap between the two substrates. Due to capillary forces, the encapsulant will fill the gap and, by controlling the dispensed volume, it can be kept in the area between the substrates,

6. once cured, the silicon wafer where the antennas were initially patterned is removed by lapping/grinding to expose the antennas.

All other electrical connections to the chip can be done peripheral pads not covered by the polymer. It must be mentioned that this is only one of the many possible integration strategies, higher throughput processes will require wafer scale processing and the use of through wafer interconnect, because the embedding polymer must be dispensed all over the wafer preventing access to I/O pads.

The integration procedure has been tested, at laboratory scale on the preliminary design of u-helix. The result are shown in figure Phased array of Arrayed configurations to increase the overall gain In the aforementioned frequency range this translates to 1.5 mm at 0.1 THz to 0.15 mm at 1 THz. U-Helix antennas have shown high-gain

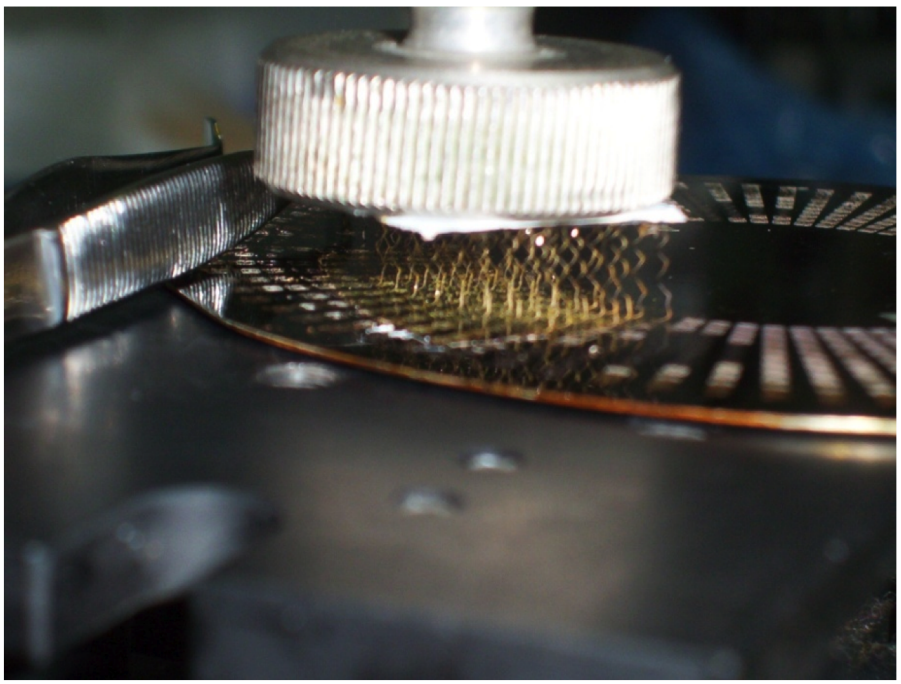


Figure 137: On-chip integration of u-helix test. Part of the circular array (bottom) has been bonded to a dummy die consisting of pads only (top). Pulling is done on a manual setup. The antennas have been extended beyond the optimum height photographing purposes.

properties (maximum gain >5dBi) and their footprint is the diameter of the largest arm that, for axial mode of operation, is $(1.33/\pi\lambda) = 0.42\lambda$.

antennas that can be arrayed and thus must fit inside a $\lambda/2$ cell. In the aforementioned frequency range this translates to 1.5 mm at 0.1 THz to 0.15 mm at 1 THz. U-Helix antennas have shown high-gain properties (maximum gain >5dBi) and their footprint is the diameter of the largest arm that, for axial mode of operation, is $(1.33/\pi\lambda) = 0.42\lambda$.

9.6 1 THZ U-HELIX ANTENNA

The performances of the 1 THz antenna, part of the six antennas of table 15 are detailed here.

The results of the simulation reported in figure 138shows that the u-Helix meets the condition on the input resistance between 1.1 THz and 1.3 THz (corresponding to a fractional bandwidth of 17%). This is the most restrictive condition for this class of antennas and the one that sets the bandwidth. An analysis of the radiation pattern shows that on the lower end of the simulated range the gain decreases by 3dB. On the opposite side, while the resistance condition is still met, the maximum of the radiation pattern starts to deviate from the axis.

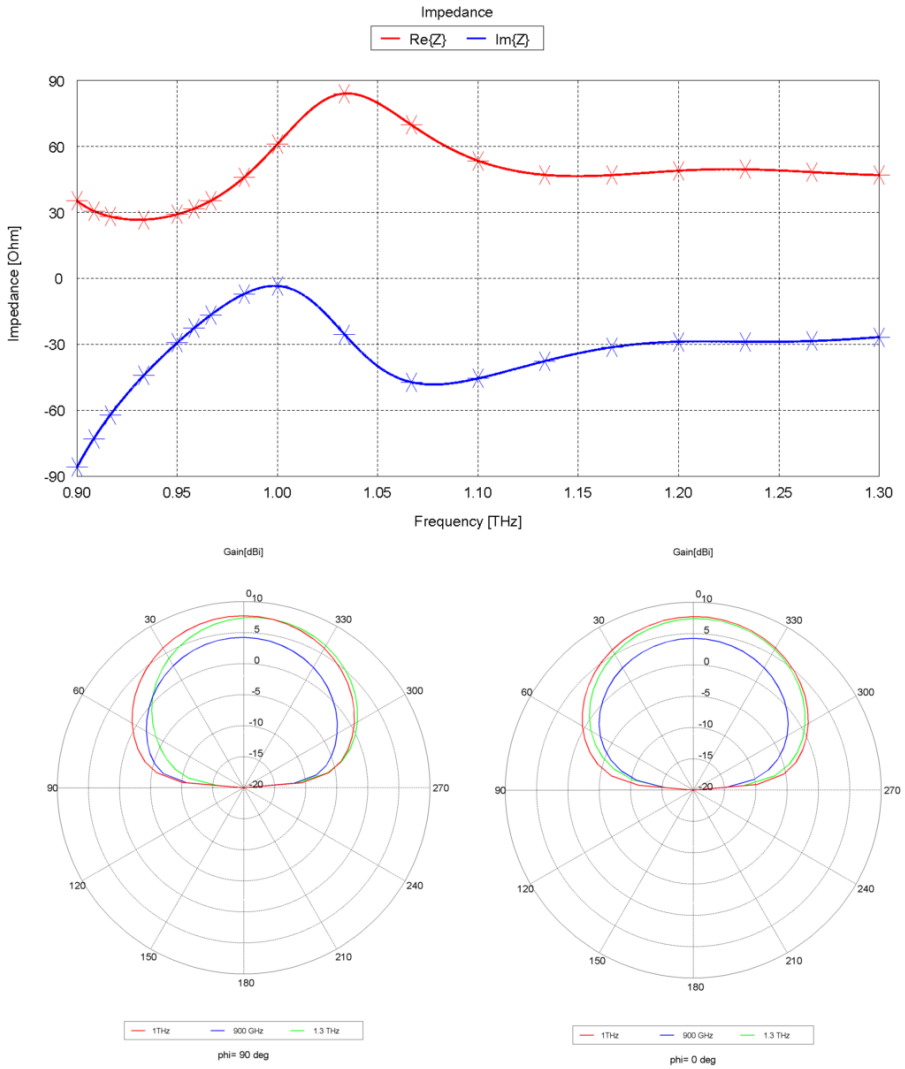


Figure 138: Simulated U-Helix antenna impedance (top) and radiation pattern (bottom) for two different φ angles (0 and 90°).

f [Hz]	Dimensional characteristics				Performances		
	Rext [mm]	*Wint [mm]*	*Tmetal [μm]*	*Htot [mm]*	*Gain [dBi]*	*VSWR (50 Ω)*	*|Zin| [Ω]*
1.0e7	3.58 (0.76)	0.35	20	13 (0.43)	7.6	<2	70

Table 16: 10 GHz u-helix antenna

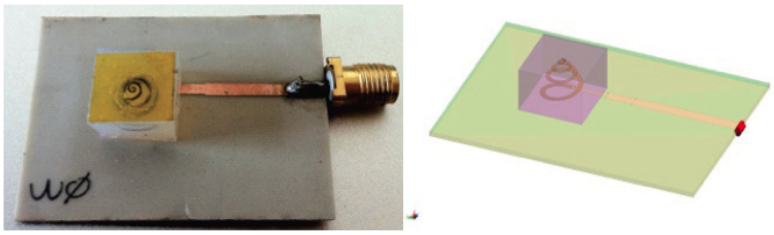


Figure 139: 10GHz U-Helix prototype realized (left) and MoM simulation model (right).

This behavior has been observed on all the simulated antennas. No sidelobe (due to the peripheral feed) appears in this band. The inductive impedance characteristics, shown in NEC2 simulation has not been verified for this design. This u-helix design shows capacitive input impedance, typical of short antennas.

9.7 SCALED MODEL

A scaled model, designed to operate above 10 GHz of the u-Helix antenna has been realized and measured. The design procedure outlined above has been applied to this model to compute optimal height (figure127 shows three different steps of the pulling process). The antenna parameters are reported in table 16.

The antenna has been realized onto a 127 μm thick Arlon substrate ($\epsilon_r = 2.22$, dissipation factor @10GHz 0.0025) and Room Temperature Vulcanizing (RTV) silicone has been used as embedding polymer ($\epsilon_r = 2.33$, dissipation factor @10GHz 0.02). The feeding structure consists of an impedance transformer to match the simulated 70 Ω antenna impedance to the 50 Ω microstrip line connected to the SMA (3.5 mm) connector. The bottom of the substrate is the ground plane. Figure 16 shows the simulation model and the actual prototype realized.

9.7.1 *Reflection coefficient measurement*

The reflection coefficient of the antenna has been measured on a vector analyzer. The measured S11 parameter (see figure 140) of the prototype remains below -10 dB from 11 GHz up to 25 GHz and a negative peak of -24.7 dB at 13.16 GHz. Further analysis of the radiation

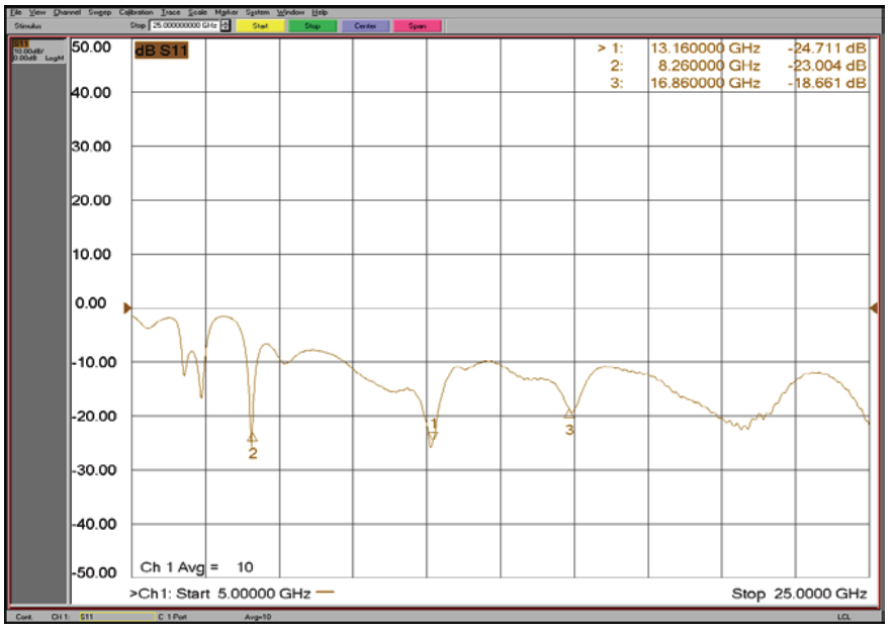


Figure 140: Measured S11 for the 10 GHz prototype.

characteristics of the antenna will be done at 13.16 GHz, where the S11 has the lowest reflection coefficient.

9.7.2 *Gain measurement*

The methodology employed to measure the radiation pattern of the antenna is depicted in figure 141. It is a comparison methodology that is robust against environmental effects consisting in comparing the measurements obtained with two calibrated antennas with known gain, with measurements in which one antenna is replaced with the Antenna Under Test (AUT) [156].

The procedure followed in the measurements is:

1. A transmitting antenna (there is no need to use a calibrated antenna at transmission side) is connected to a RF generator tuned at the frequency of interest. A calibrated receiving antenna is connected to a power measurement instrument (spectrum analyzer) and placed at distance and orientation specified in the calibration sheet. In these conditions, the receiving antenna measures the intensity of the radiated field of the transmitting antenna. This value is set as reference on the spectrum analyzer.

2. Keeping the set-up stable the receiving antenna is replaced by the AUT (keeping the same impedance matching and position of step 1) and the antenna is moved until the maximum reception condition is reached. In this condition, the value on the spectrum analyzer is read.

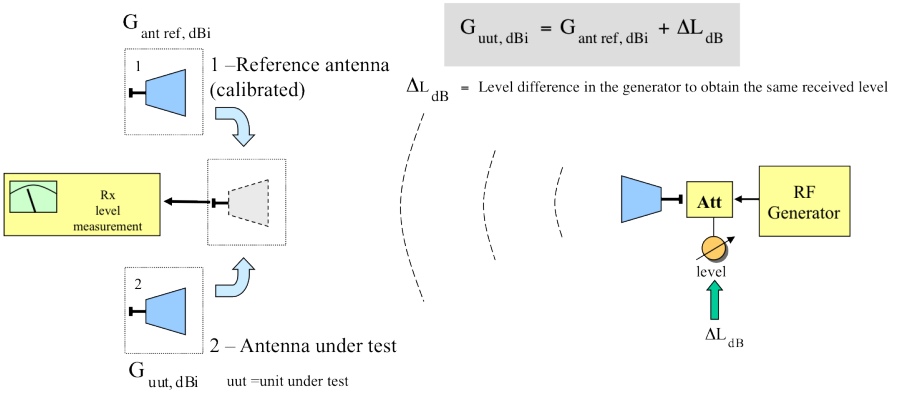


Figure 141: Antenna measurement methodology. A comparison measurement methodology has been employed to measure the gain of the u-helix antenna.

3. The value read on the spectrum analyzer is positive if the AUT gain is higher than one of the calibrated antenna (that it replaces), negative otherwise. The algebraic difference of the read value and the calibrated antenna gain (tabulated on the calibration sheet) is the gain of the AUT.

The same method can be applied replacing the transmitting antenna with the AUT. The measurement method employed here is a variation of the metrologically correct comparison method. In the latter, a precision variable attenuator is used to adjust the level in condition 2 until the same reading of condition 1 is obtained. There is no significant error introduced by the procedure followed as the spectrum analyzer used introduces non-significant error in the read levels.

The radiation pattern along φ=0 has been measured at 13.16 GHz (the frequency where the S11 has a dip) in a semianecoic chamber (an indoor site) and compared with the MoM simulations (see figure 142). The measured radiation pattern differs from the simulated in shape and maximum gain. The difference in the shape is attributed to the mechanical tolerances of the laboratory-scale manufacturing processes. The difference in maximum gain (7.6 in simulation and 5.1 in the measurement) is due to the polarization loss introduced by the antenna gain measurement technique. The u-Helix is a circularly polarized antenna while the horns are linear and this can explain the difference in measured maximum gain.

9.7.3 *Antenna efficiency measurement*

The lower gain and low directivity radiation pattern measured for the u-helix prototype suggests a low antenna efficiency. Whereas this can be attributed to the feeding structure and laboratory scale processes, its efficiency has been evaluated in a reverberation chamber with the Holloway's method [157, 158]. The method is based on the compari-

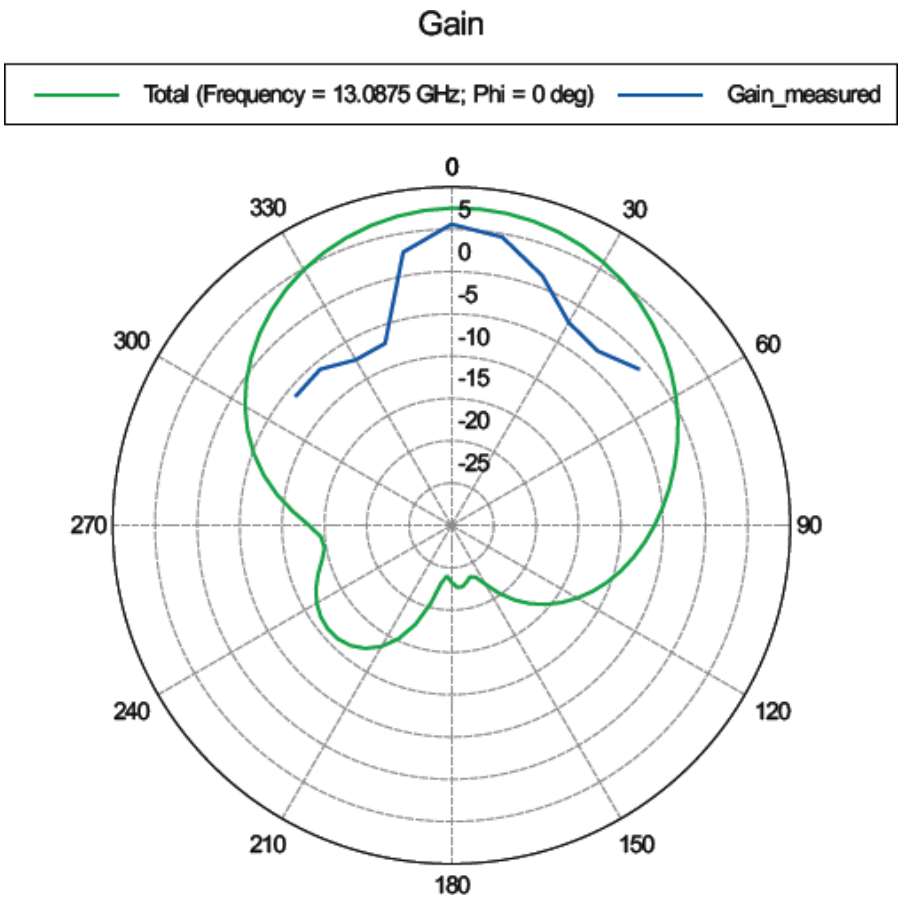


Figure 142: Comparison between measured and simulated radiation pattern.

son of scattering parameters measured by connecting the AUT at one port of the network analyzer, with the other one connected to a reference antenna (a total of two measures) with the scattering parameters measured by connecting reference antennas at both ports.

The efficiency of the scaled model, at 13.16 GHz, with the Holloway's method reported a radiation efficiency of 63%.

10 CONCLUSIONS

The main achievement of this work has been the definition of the CMRL technology. This technology, based on porous silicon allows the integration of arbitrarily shaped three dimensional structures on silicon wafers. This technology is based on wafer scale, low-cost processes and can achieve high throughput if implemented at industrial level. Two application of this technology have been presented:

- probe card contactors
- u-helix antenna.

The probe card contactors demonstrate how the CMRL technology can be effectively used for the realization of off-chip interconnections at wafer scale, eliminating the bottleneck of off-chip interconnect for next generation of ICs. The interconnections realized with CMRL have a density greater than 4000 contacts/cm^2, have a pitch of 135 um and each contact can carry 250mA. The same technology has been used to replace wire bonding in Integrated High Power Modules and increase their reliability.

The u-helix antenna is a short conical antenna that can be bonded on a standard CMOS IC, providing high gain (>5dBi) and efficiency, reducing substrate coupling problems. The high resolution achievable by the CMRL technology allows to scale down this antenna for low-THz operations. Moreover this antenna can be arrayed to further increase the gain or, can be used in focal plane array in THz detector chips.

In particular, the first application has reached the pre-industrialization phase.

Superhydrophobic surfaces and electrochemical etching of through silicon via, using macroporous layers obtained with CMOS compatible processes have been demonstrated and optimized over p-type silicon substrates, overcoming the problem of obtaining porous layers with controllable characteristics on that substrate type.

Porous silicon have proven, after 50 years from its discovery, to be still an interesting material for the electronics industry. Its porosity-dependent propitious, the low-cost and high-throughput of its formation processes, and its nature: it is silicon, make this material the ideal candidate for heterogenous integration of next generation systems-on-package.

Part IV

APPENDIX

A

COMMENTS TO THE SURFACE ANALYSIS METHOD

The analysis of statistical properties of porous silicon random surface has been introduced in 2, where the feature analysis based on the ImageJ "particle analysis" tool has been presented. In this appendix a second methodology is introduced. The new methodology allows to identify pore diameter and mean distance by using spectral analysis. Statistical analysis of non-ordered porous silicon surface is necessary because of the randomness of the features. Pores diameters and pores distances are important parameters connected with pore formation kinetics. In this appendix, the two methods are applied to a synthetic image (that resembles a metallic sheet with punched holes) with regular features at constant distances. The results of both analysis methods will be compared to identify the weaknesses of each one.

A.1 TEST CASE

The proposed method has been applied to the test image in figure 143 to verify its consistency.

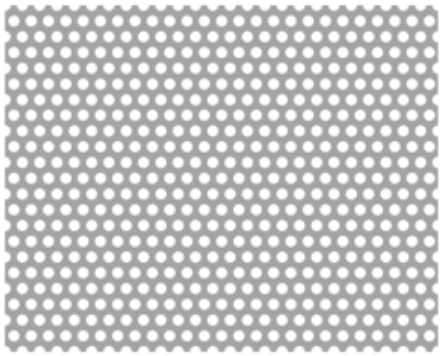


Figure 143: Artificially generated test image.

The use of a regular and ordered pattern allows to unambiguous comparison between extracted data and direct measures. The image consists of a regular array of circular (white) holes on a metal (gray) sheet. Circular holes pitch (center to center) has been set to 1 μm (by artificial scaling on ImageJ [63]. The original image must be binaries to isolate the features from the background. In this case this is trivial because all the features have the same color (intensity) the differ from the background color. Simple thresholding segmentation returns a noise-free binary image like the one in figure 144, where only the "internal" holes have been kept to remove the contribution of the white border on the analyses.

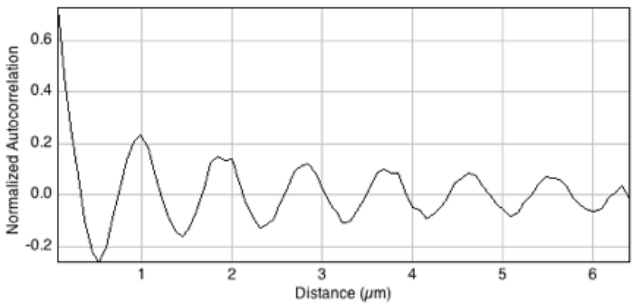


Figure 145: RAA analysis of the test image.

A.2 RADIALLY AVERAGED AUTOCORRELATION

The RAA technique is used to extract the average features size and pitch on binary images. The exact nature of the features, depends on the image. In this test case, the features are the white holes in a perforated metal sheet (the synthetic image in figure 143).

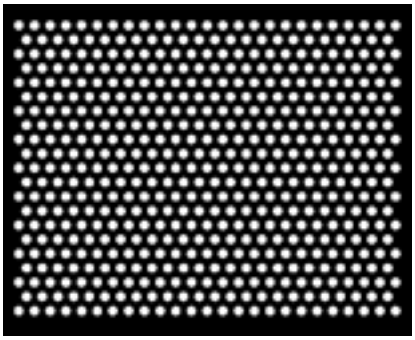


Figure 144: Binarized test image

The tool used to extract data is the "Radially Averaged Autocorrelation" ImageJ macro [159] that implements the RAA method for binary images. The macro calculates the two-point correlation of the pixels of the image as a function of distance. This method is based on the Fourier's transform of the image but does not suffer from the artifacts generated by the periodicity of its nature. The method assumes to work on a random part of a much larger image with the same autocorrelation to correct artifacts that would be introduced by the finiteness of the analyzed image. The results are scaled to give 1 for perfect correlation. A value of 0 indicates no correlation at all, and a value of -1, a perfect "anticorrelation". The interesting information are contained in the position (distance in figure (145)) of the first minimum and of the first side maximum of the RAA. The former corresponds to the hole average dimension, the latter to the average distance between two holes.

The result of RAA on the test image is shown in figure 145 where it is evident that maximum correlation is equal to 1 (the macro does not output the value in zero as it is always 1 due to the chosen normalization) and is in the origin (as expected) because every image is identical to itself. The first minimum in the correlation graph happens at distance 0.54 μm, close to the Feret's diameter (corresponding to circle diameter in this case) of circular openings, which is 0.57 μm

(the error is below 1%). The second maximum is situated at $1\mu m$, the exact distance between the holes. The image shows other peaks that are related to the high degree of regularity of the structure and their spacing not equal to 1 μm is due to the non radial symmetry of the image.

The significance of this analysis for porous materials is demonstrated in [160], where it is applied to estimate the permeability of porous rocks. In particular, in that work, a difference scaling of the RAA allows to compute the porosity of the sample from the autocorrelation graph. The porosity ϕ is defined as:

$$\phi = \hat{S_1} = \langle f(\mathbf{x}) \rangle \tag{55}$$

as the volume average over the spatial coordinate x of the characteristic function $f(x)$, that assumes the value of 1 in feature region (i.e. pores) and 0 elsewhere. The two-point correlation function is defined as

$$\hat{S_2}(\mathbf{r_1}, \mathbf{r_2}) = \langle f(\boldsymbol{x} + \mathbf{r_1}) f(\mathbf{x} + \mathbf{r_2}) \rangle \tag{56}$$

The above formula can be simplified for statistically homogenous and locally isotropic porous media. Statistical homogeneity implies that the value of the two-point correlation depends on the distance between the two spatial coordinates:

$$\hat{S_2}(\mathbf{r_1}, \mathbf{r_2}) = \hat{S_2}(\mathbf{r_2} - \mathbf{r_1}) \tag{57}$$

Local isotropy implies that the averages do not depend on the orientation of the argument:

$$\hat{S_2}(\mathbf{r_2} - \boldsymbol{r_1}) = S_2(|\mathbf{r_2} - \mathbf{r_1}|) \tag{58}$$

Under these assumptions the following is derived, with $r = |\mathbf{r}|$:

$$\begin{aligned} S_2(0) &= \phi \\ \lim_{r \to \infty} S_2(r) &= \phi^2 \\ S_2'(0) &= -s/4 \end{aligned} \tag{59}$$

The value assumed in zero by the two point correlation is the porosity, the value at infinity is the porosity squared and the first derivative in the origin is proportional to the specific surface area s (the internal surface area per unit volume). This particular scaling is not implemented in the macro but it can be recovered by the following formula:

$$S_2 = \phi^2 + RAA(\phi - \phi^2) \tag{60}$$

A.3 RADIAL DISTRIBUTION FUNCTION

A second procedure can be used to verify the results of RAA. The Radial Distribution Function (RDF) $g(r)$, used in statistical mechanics,

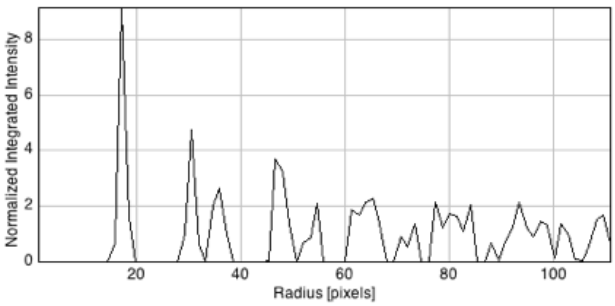


Figure 147: RDF analysis of the test image.

describes how the atomic density varies as a function of the distance from one particular (reference) atom. Given an atom in the origin O, and $n = {}^{N}/_{V}$ the average number density of atoms (the ratio of the number of atoms N and the volume V), the local density at distance r from O is $ng(r)$. ImageJ implements a macro to compute the RDF [161] that requires the use to extract the centroids of the features. This can be done using the "Process->Find Maxima..." command in ImageJ on the binarized image (figure 144). The result is shone in figure 146.

Figure 146: Image of the extracted centroids for the holes in the test image.

The graph obtained in the case of this picture is in figure 147 where distances are reported pixels. The scale is: 17.333 pixel/μm. The first peak is centered at 17 pixels, which corresponds to 1 μm. This method is able to identify the lattice constant of the image. Subsequent peaks have no readily apparent significance. This method, of course, does not give any information about morphology (diameter) as every feature is collapsed into a single point.

A.4 MORPHOLOGICAL ANALYSIS OF THE FEATURES

The morphological analysis has already been introduced in 2.2. In this appendix only the validation of the method on the test image is presented. The Feret's diameters and areas of the holes in the test image have been extracted using the particle analysis tool in ImageJ (using the procedure outlined in 2.2) and histogram plots have been generated. The computed values should fit, in principle, in a single bin for the sample image as all holes have the same dimensions. In practice this is not verified because of pixel-level differences (e.g. the use of an-

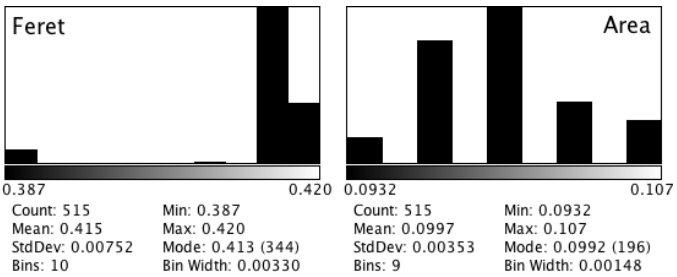


Figure 149: Distribution of the Feret's diameters and holes areas.

tialiasing), differences introduced by the thresholding algorithm and, by the image resolution. Figure 149 shows the histogram plots for Feret's diameter (values in μm) and hole's areas (values in μm^2). The observed mean Feret's diameter 0.415 μm, smaller than value 0.54 μm reported above. The sources of this error (27%) is due to the chosen threshold (that is observer' dependent) and the limited resolution of the image. In the test image, one pixel corresponds to 60 nm, the average feature is 7 pixel wide, and a two-pixel error (due to incorrect thresholding caused by anti-aliasing) will cause an error of 120 nm, that if added to the average value reported above, will give a diameter of 0.534 μm (very close to the previously reported one). The same problem applies to the computation of holes' areas: a circular hole with a diameter of 0.415 μm should have an area of 0.135 μm^2 (computed by the $\pi\,(d/2)^2$ formula, where d is hole's diameter) but the mean area is 0.1 μm^2. This is caused by the limited resolution of the image.

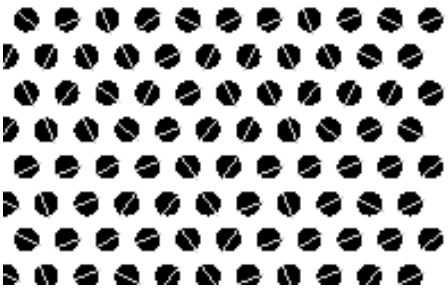


Figure 148: Feret's diameters extracted for the holes in the test image. The image represents only a part of the original image to make visible the Feret's diameters.

A.5 GENERAL CONSIDERATIONS

The set of algorithms used for evaluating the dimensions of SEM images features tends to underestimate the dimensions of such features. Among the two presented methods: RAA and particle analysis, the former is more robust and produces more accurate results, the latter tends to underestimate features dimension due to the limited resolution of the image and the observer's judgement in the thresholding algorithm.

B

MACROPOROUS SILICON CHARACTERIZATION

This appendix contains the images acquired for the characterization of macroporous silicon in chapter 2.

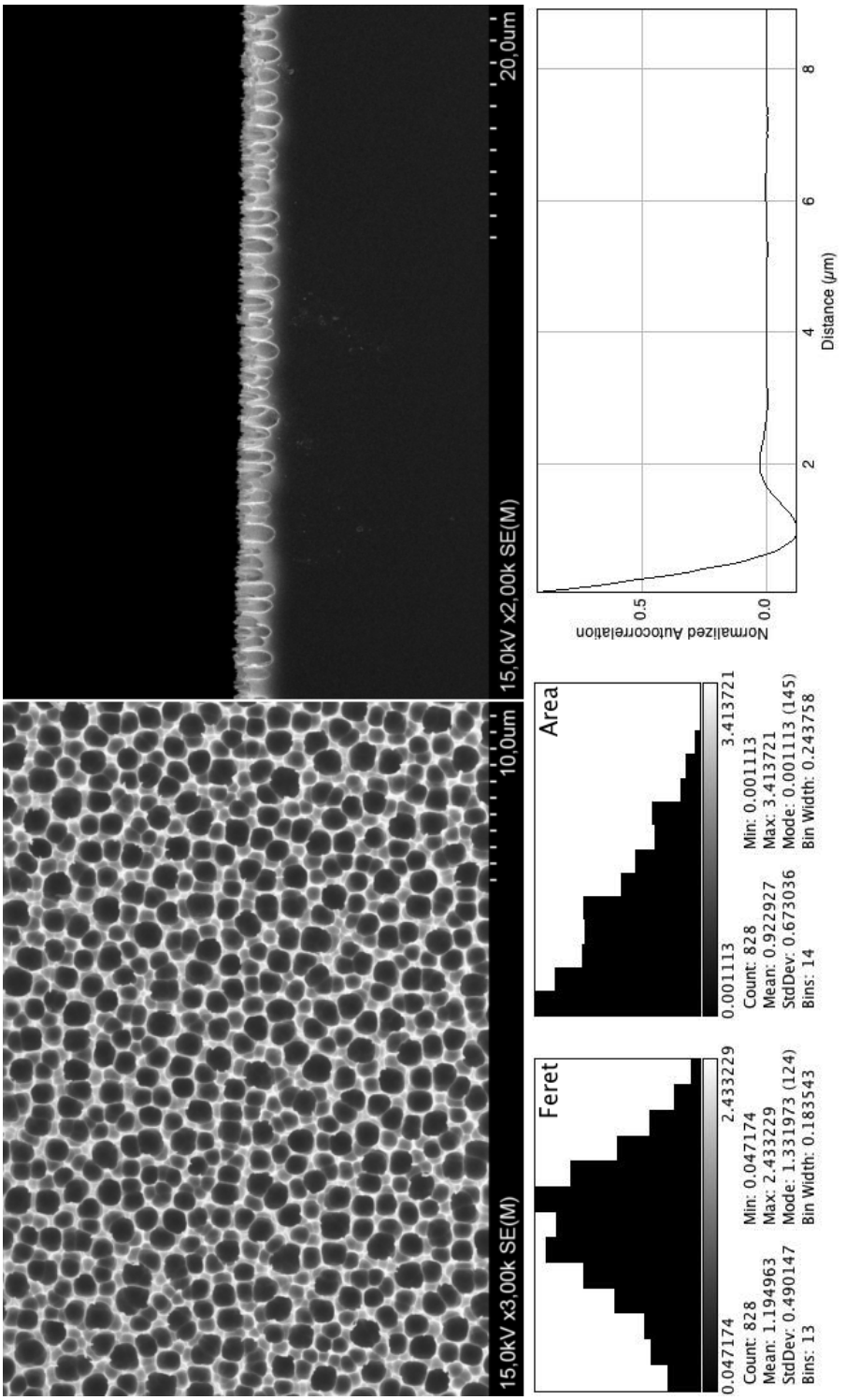


Figure 150: Macroporous silicon on (100) 10-20Ωcm p-type (Boron doped) silicon wafer anodized in HF:DMSO=10:46 at $1mA$ for 9000 *sec*.

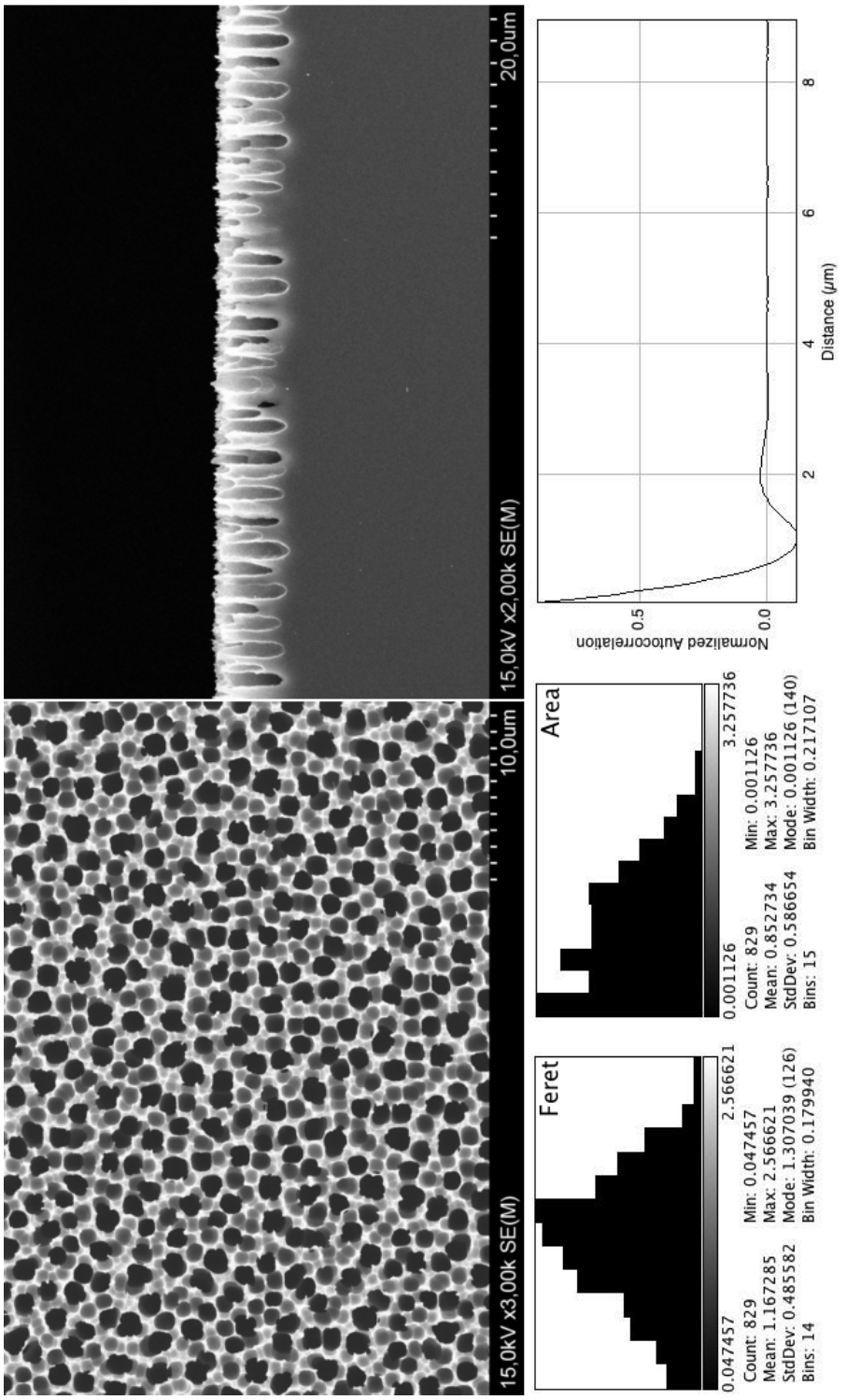


Figure 151: Macroporous silicon on (100) 10-20Ωcm p-type (Boron doped) silicon wafer anodized in HF:DMSO=10:46 at 3mA for 3000 sec.

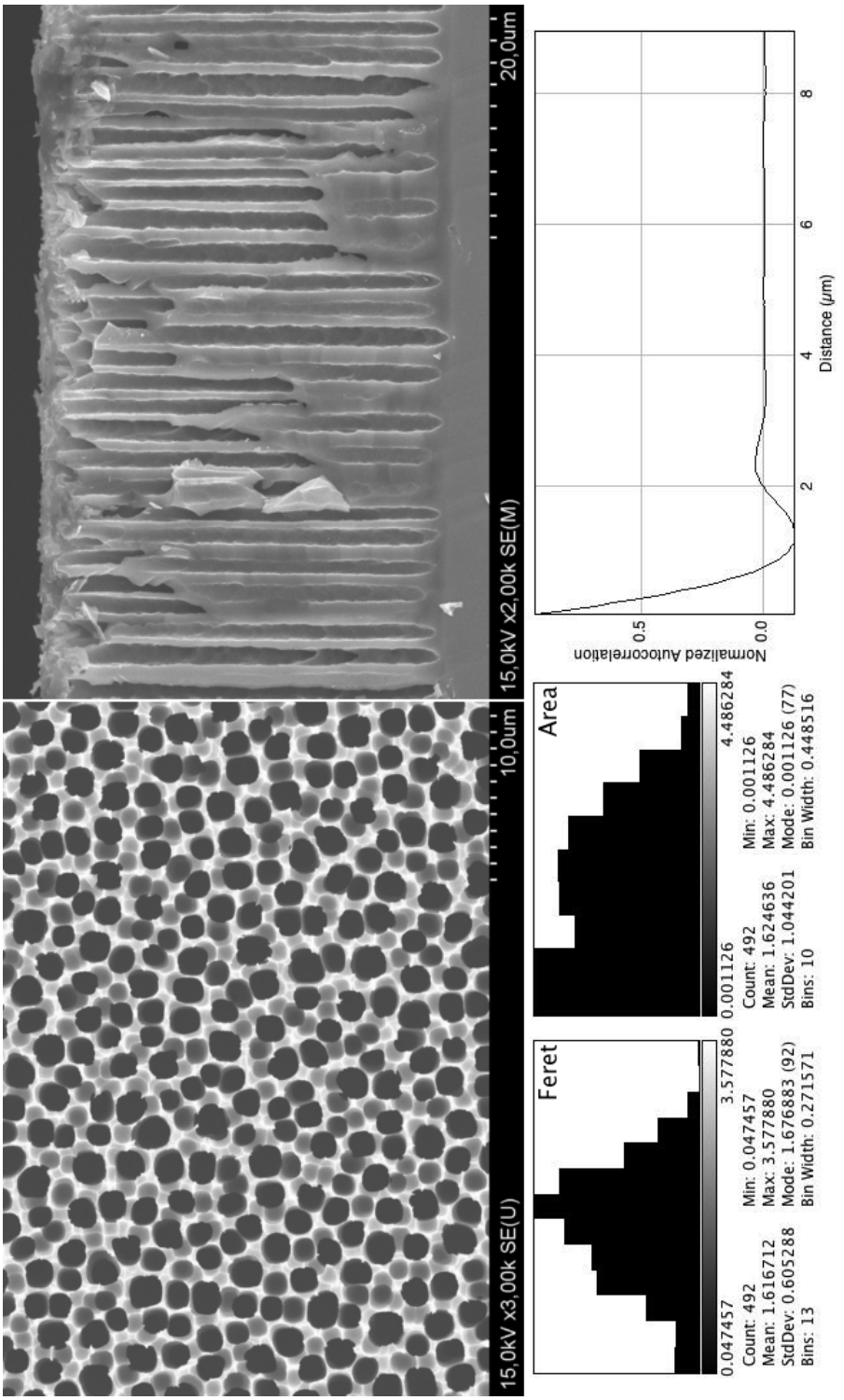


Figure 152: Macroporous silicon on (100) 10-20Ωcm p-type (Boron doped) silicon wafer anodized in HF:DMSO=10:46 at $3mA$ for 9000 *sec*.

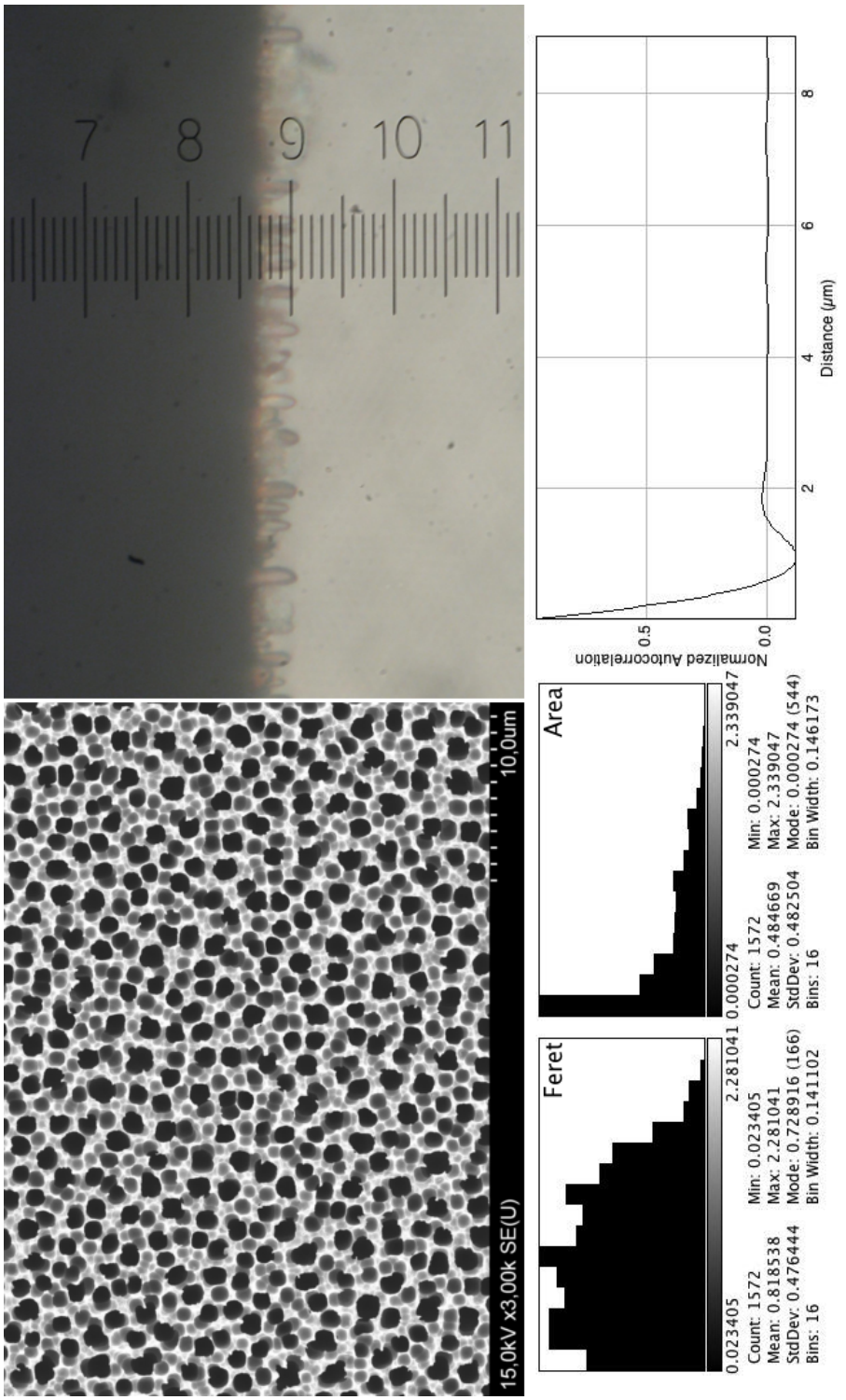


Figure 153: Macroporous silicon on (100) 10-20Ωcm p-type (Boron doped) silicon wafer anodized in HF:DMSO=10:46 at 5mA for 1800 sec.

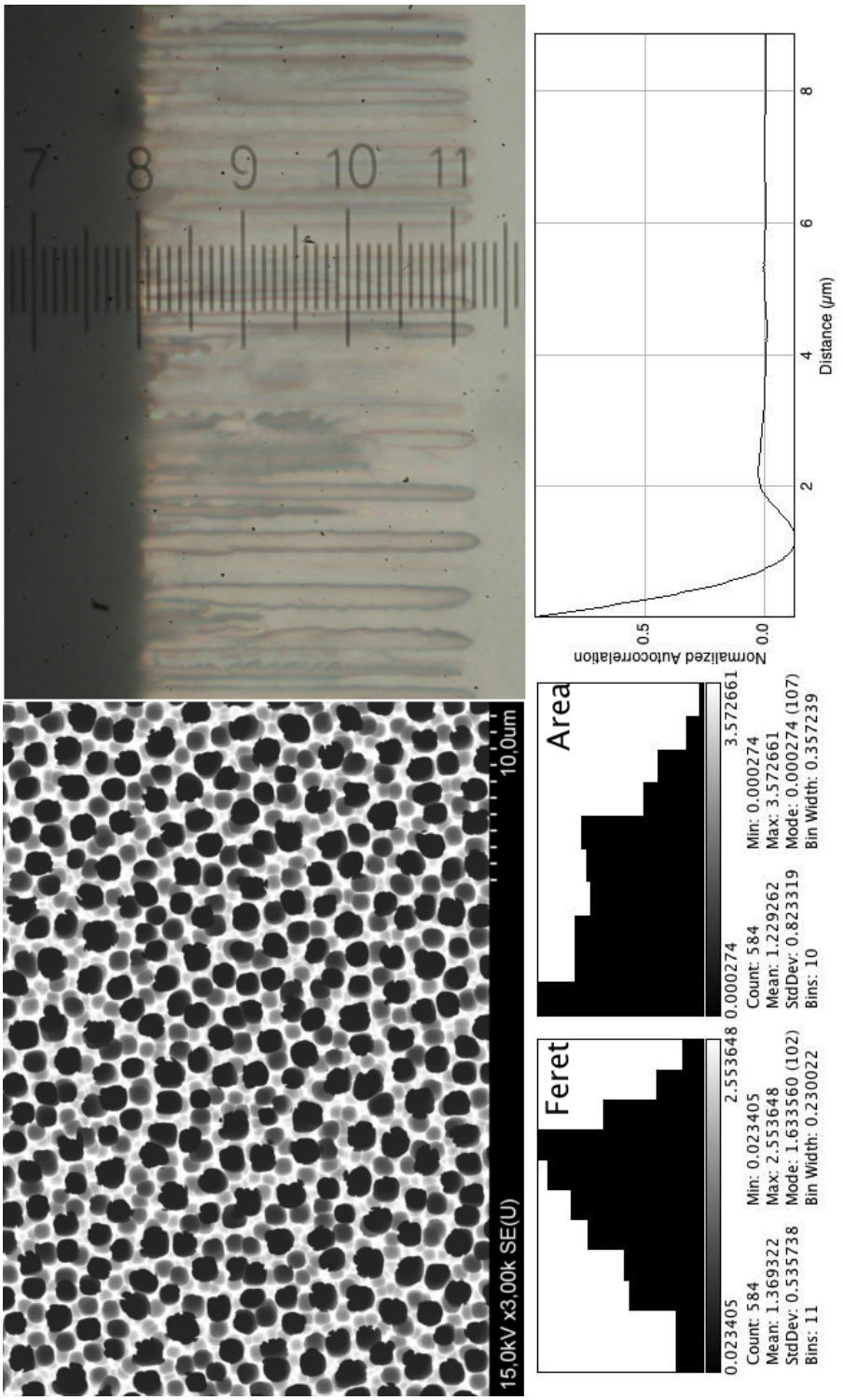


Figure 154: Macroporous silicon on (100) 10-20Ωcm p-type (Boron doped) silicon wafer anodized in HF:DMSO=10:46 at 5mA for 5400 sec.

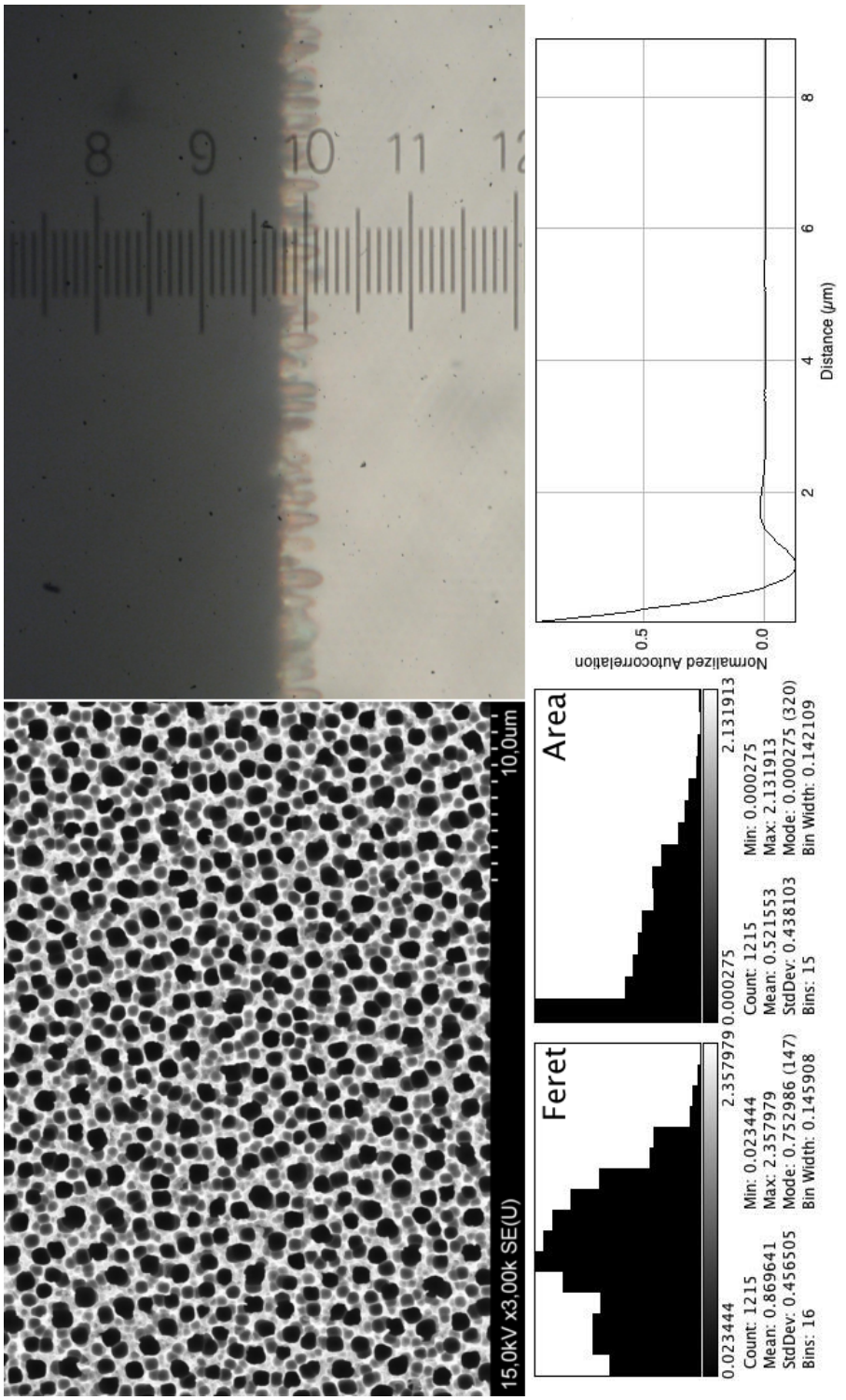


Figure 155: Macroporous silicon on (100) 10-20Ωcm p-type (Boron doped) silicon wafer anodized in HF:DMSO=10:46 at 10mA for 900 sec.

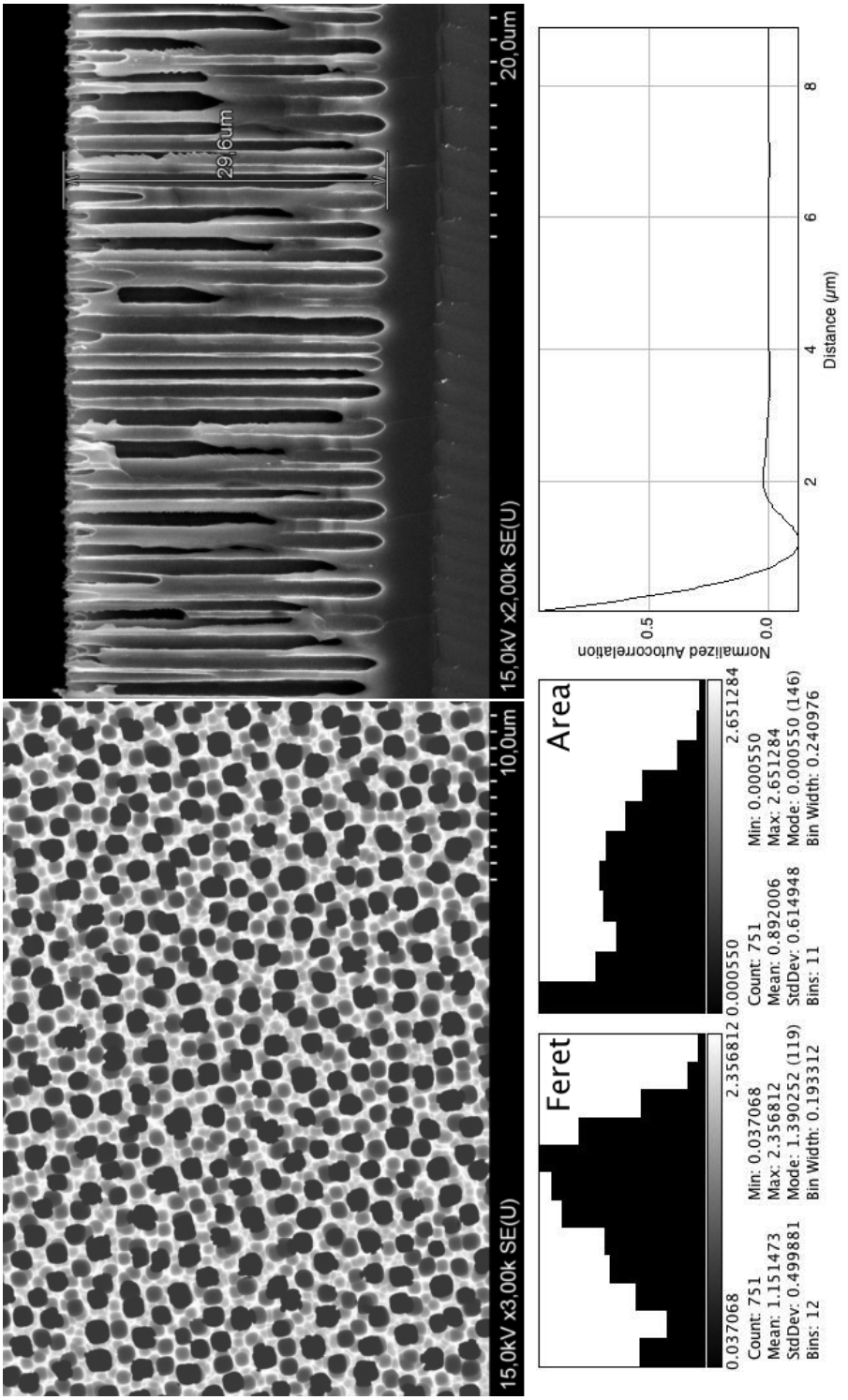


Figure 156: Macroporous silicon on (100) 10-20Ωcm p-type (Boron doped) silicon wafer anodized in HF:DMSO=10:46 at 10mA for 2700 sec.

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