6T-SRAM 1Mb Design with Test Structures and Post Silicon Validation

by

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ABSTRACT

Static random-access memories (SRAM) are integral part of design systems as caches and data memories that and occupy one-third of design space. The work presents an embedded low power SRAM on a triple well process that allows body-biasing control. In addition to the normal mode operation, the design is embedded with Physical Unclonable Function (PUF) [Suh07] and Sense Amplifier Test (SA Test) mode. With PUF mode structures, the fabrication and environmental mismatches in bit cells are used to generate unique identification bits. These bits are fixed and known as preferred state of an SRAM bit cell. The direct access test structure is a measurement unit for offset voltage analysis of sense amplifiers. These designs are manufactured using a foundry bulk CMOS 55 nm low-power (LP) process. The details about SRAM bit-cell and peripheral circuit design is discussed in detail, for certain cases the circuit simulation analysis is performed with random variations embedded in SPICE models. Further, post-silicon testing results are discussed for normal operation of SRAMs and the special test modes. The silicon and circuit simulation results for various tests are presented.

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CHAPTER 1. INTRODUCTION

1.1. SRAM 1Mb in TC25 Overview

Conventional six transistor static random access memory (SRAM) design has been used as L1, L2 and further deeper level caches for microprocessor designs. These SRAMs are designed with robust peripheral circuits that control the write and read functions. In this work, we discuss the SRAM 1Mb design in TC25, the top-level fabricated die image of TC25 with 6t-SRAM 1Mb (highlighted) is shown in Fig. 1.1.

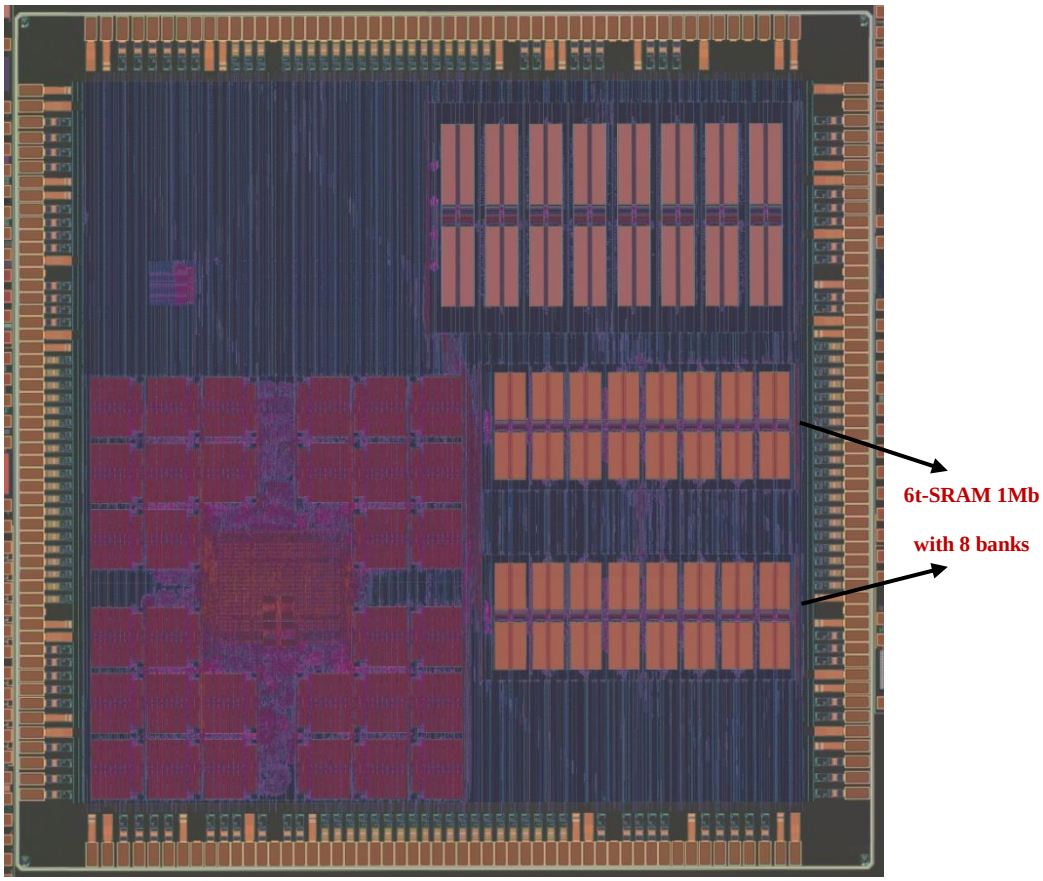

Fig. 1.1 TC25 Top-level Die Image Showing Layout till Metal2 [Fujitsu17].

Architecturally, the TC25 chip has a microprocessor, DDR clock recovery block and an SRAM block. The SRAM block further consists of two 6t-SRAM 1Mb and 8t-SRAM 1Mb. The 6t-SRAM 1Mb has eight banks which each have 16KB bit-cell storage. The write and read operations are synchronous to clock, in a clock cycle either a write or read operation is allowed. Each 16KB block has its own control circuit that manages the timing synchronization of these tasks. One out of eight banks are selected in a clock cycle and the data in and out from the selected bank is multiplexed through the data multiplexer. The datain from TC25 pad is 32-bits wide, this word is copied to the other word at SRAM block level to generate 64-bit wide input data. The clock given to the SRAM block are generated from outside the chip, this is achieved by an IO pad dedicated for clock signal. Because of the low power sub-threshold operation of SRAM, the dataout generated need to be reinforced to a nominal voltage level, this is achieved through level shifters [Wooters10] [Zhou15] placed in SRAM 1Mb block.

The design uses a Fujitsu 55nm low power process triple well process which provides good control of device threshold voltage through body-biasing.

1.2. Test Structures Overview

Fig. 1.1, shows that SRAMs occupy a majority of the chip area in this design. Traditionally, circuit designs embed special test modes for yield and manufacturability analysis in these SRAMs. We have also designed embedded test structures in SRAM to measure the offset voltage of sense amplifiers on chip. In total, there are eight banks in each SRAM 1Mb block, each bank having 64 sense amplifiers. All the circuits in SRAM are digital except the analog sense amplifier used for differential voltage-sensing in memory read operation. The differential voltage development at the sense amplifiers is critical to the read operation of an SRAM. This sense-amplifier signal is an analog voltage internal to the SRAM and cannot be determined directly from the digital dataout

from memory, without an additional circuit. In past, several methods have been proposed to directly measure the sense amplifier offset, ours is similar to [Chen12]. In this method, we create a separate path from sense amplifiers to external DC voltage pins that set input differential voltage. The sense amplifiers are trigged by the sense enable signal, resulting in digital dataout generation. The dataout flips to desired value when the differential nodes satisfy the required offset voltage. This voltage is a function of random and systematic variation caused by line edge roughness (LER), random dopant fluctuation (RDF), channel length modulation and other environmental noise factors.

The mode embedded in the SRAM design is physically un-cloneable function (PUF) detection from the inherent mismatch property of SRAM. The aforementioned variation sources in transistors are utilized to generate fingerprint that ideally remains same over time. In some work, the power-up state of embedded SRAM is used to produce a unique fingerprint [Holcomb09]. This is advantageous in terms that the SRAM inherent property without any additional circuit can be used to generate special ID. We have used this method mentioned in [Chellapa11] to de-stabilize the SRAM, which brings them to a preferred state after coming out of meta-stability. The SRAM bit-cell value is then read through the conventional read operation.

1.3. Post Silicon Validation of SRAM and SA Test Mode

Post silicon validation of SRAM is performed to determine actual silicon results. We performed basic functional test for fault detection using digital test patterns [Pavlov06]. In one test, memory is sequentially written and read in a specific address order. To give coverage of memory fault check, variety of tests are performed in silicon validation.

In this work, we also briefly show the PUF mode test-bench pseudo code. The focus of this work is on the sense amplifier offset characterization through the SA Test mode.

1.4. Thesis Outline

In this report, chapter 2 discusses the 6t-SRAM array design. The design components such as bit-cells, decoder, control and write/read IO logic are presented in detail. The timing of these circuits is further shown in the chapter. Chapter 3 describes the 1Mb bank design which has eight bank macros and other logic paths. The abstract generation and corresponding memory characterization was performed for of SRAM 16KB banks using Cadence Abstract Generator and Cadence Liberate static timing analysis tools. The generated hard macro abstract and liberty were thus used for SRAM 1Mb RTL synthesis and APR, which is also discussed in the chapter. In chapter 4, the special sense amplifier test (SA Test) and PUF mode are described. The focus of this chapter is to check the sense amplifiers for offset measurement, whereas the PUF mode is briefly described with respect to circuit design and simulation results. The details of SA Test mode setup, measurement from silicon and comparison result are presented. In this, results from Monte Carlo simulation on the sense amplifier circuit to measure offset are compared with the silicon offset measurement results.

CHAPTER 2. SRAM BANK DESIGN

2.1. Overview

The SRAM bank discussed in this chapter is designed as standalone data storage element and serves as a data memory for microprocessor HERMES in the test chip TC25. The bank has 16KB storage space and has read and write logic that are operated by control unit and decoders as shown in the Fig. 2.1.

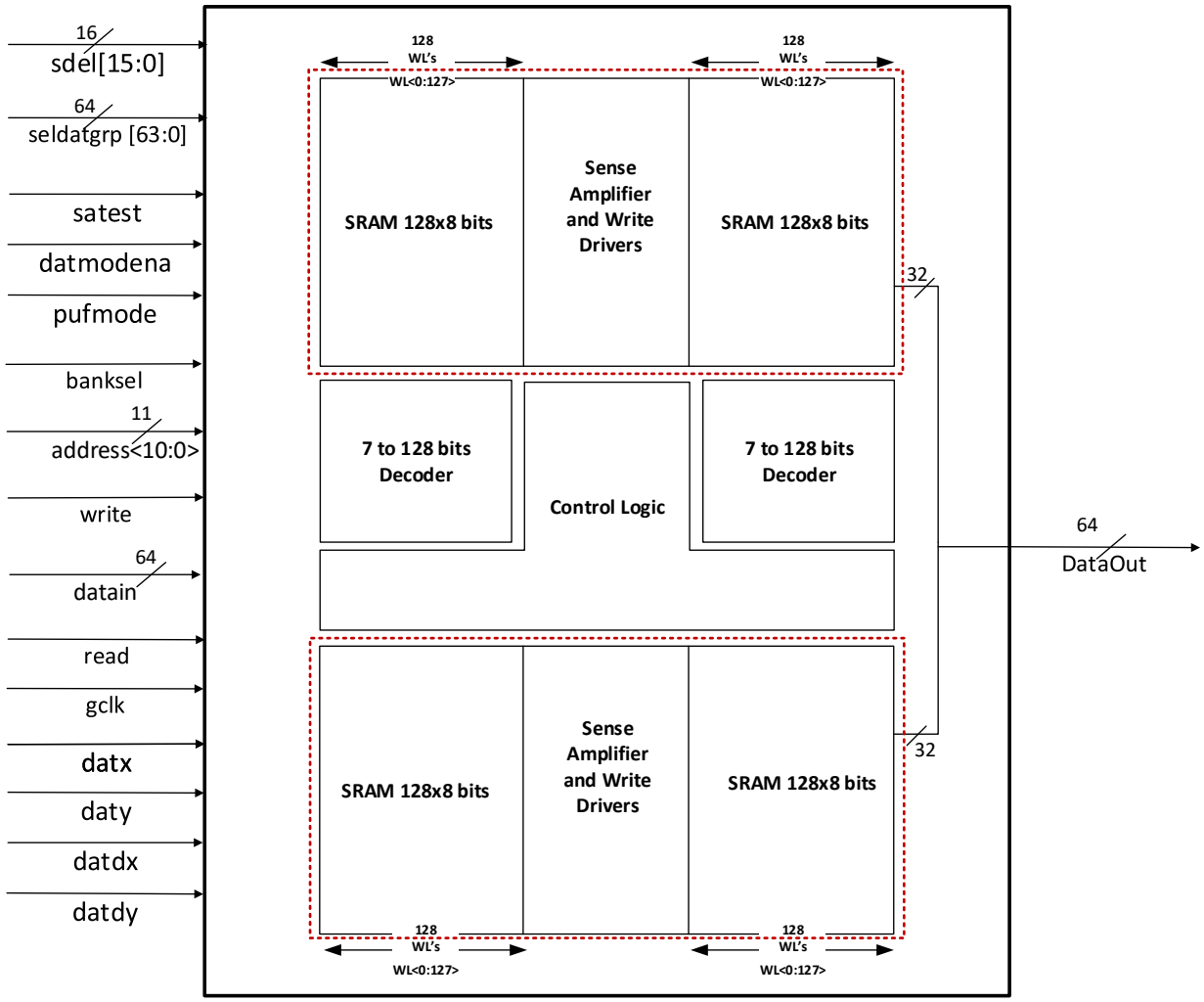

Fig. 2.1 6T-SRAM 16KB Block Diagram.

As shown in the figure, there are four bit-cell arrays which are combined in 64 column groups each having 2x8x128 bit-cells. The block diagram shows two X-decoders used to enable the column word lines. The bit lines to access each bit cell for read and write are controlled through sense amplifier and write driver circuit of each column group. The top and bottom arrays, shown in dotted red box in Fig. 2.1, generate dataout<63:32> and dataout<31:0>. The control logic is placed in between the memory arrays and decoders, they provide good accessibility of all the signals and hence capacitance matching for all the control signals running across decoders and SRAM arrays. The custom layout of completed design is shown in Fig. 2.2, it has a substantial height of ½ mm that makes 1Mb physical design floorplan critical to maintain aspect ratio of 3.5mm by 3.5 mm chip.

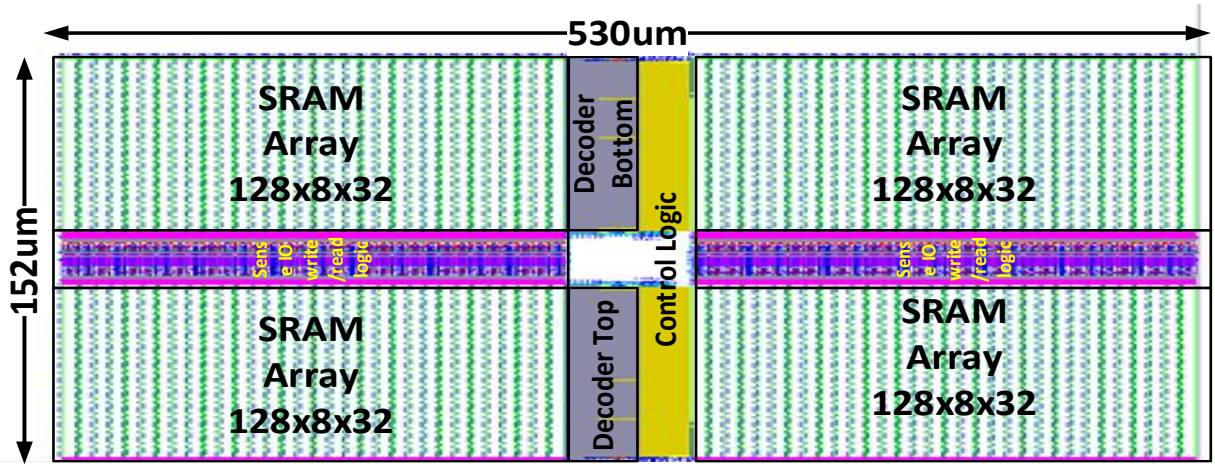

Fig. 2.2 6T-SRAM 16KB Custom Layout.

2.2. 6T-SRAM 16KB Bank Design

In this section, the basic units of 6T-SRAM bit-cell, read and write logic circuit, column group, control unit and decoder design is discussed. The read and write timings along with the functioning of each block is discussed in detail.

2.2.1. 6T-SRAM Bit-cell

The bit-cell has six transistors, two NMOS pass-gate, two pull-up PMOS and two pull-down NMOS. All these transistors have high threshold voltage as compared to other transistors used in TC25, this makes them less leaky.

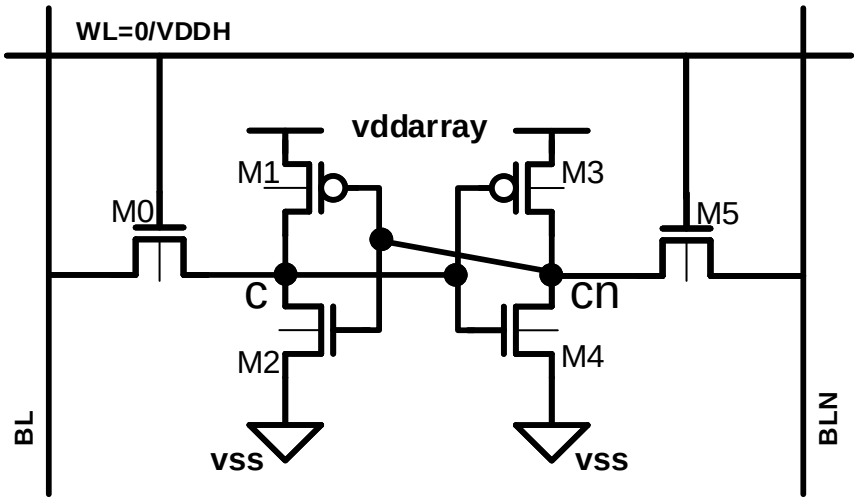

Fig. 2.3 Schematic of 6 Transistor SRAM bit-cell.

In addition to the body biasing voltages, word line, bit line and supply voltages in SRAM are also separated through different power pads in TC25. The list of all the voltages used for 6t-SRAM operation is shown in Table 2-1. Bit-cell has SRAM ULL transistors provided in the Process Design Kit (PDK). These cells are designed by the foundry considering the pull-up and beta ratio required for write and read operations.

Supply Name	Nominal Voltage	Supply Type
VDDarray	0.9V	SRAM PMOS Source
VDDH	0.9V	SRAM Word Line Voltage
VDDS	0.9V	SRAM Bit Line Voltage
VSSA	-0.4V	NMOS RBB
VDDA	1.3V	PMOS RBB
VDDAarray	1.3V	SRAM PMOS RBB

Table 2-1 Supply Voltages for 6t-SRAM.

2.2.2. Bit-cell SNM and DRV

The SRAM bit-cell stability is defined in terms of static noise margin [Seevink87], which is explained the maximum value of noise under which the bit-cell sustains the value stored in its latch. Graphically, read SNM is represented by the maximum possible square, in Fig. 2.4, between the voltage transfer characteristic (VTC) curves of the back-to-back inverter nodes.

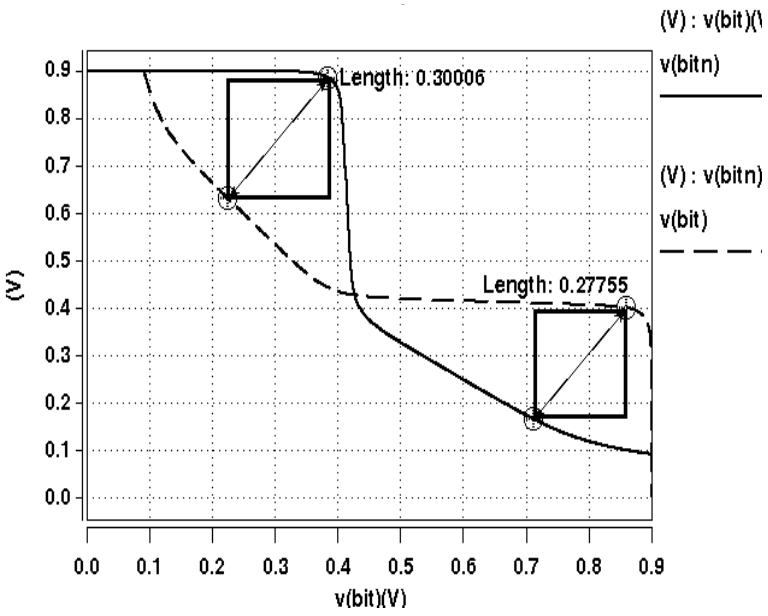

Fig. 2.4 Read SNM Curve of SRAM Bit-cell in TT Corner at Nominal Temperature and Voltages.

The analysis in Fig. 2.4 is performed at nominal voltages with the impact of variation that modifies the threshold voltage of each device. Memories are extensively used in modern chips resulting in huge power consumption; also, their access activity is low, which can be leveraged for

power saving. Different methods such as power gating, frequency reduction and dynamic voltage scaling are used to reduce static and dynamic power. In common, during the low activity time, power dissipation in caches is controlled by scaling down V_{DD}, this is done while retaining data and hence this voltage is known as data retention voltage (DRV) [Qin05]. It is the minimum voltage at which the SRAM cell preserves the stored bit value under some noise and variation. With the DRV analysis, the leakage reduction in chip can be achieved during the standby/drowsy mode of SRAM cells. To find the DRV of a bit-cell, the c and cn node are initially set to complementary logic levels whereas the WL is turned-off to bring the access transistor to off mode.

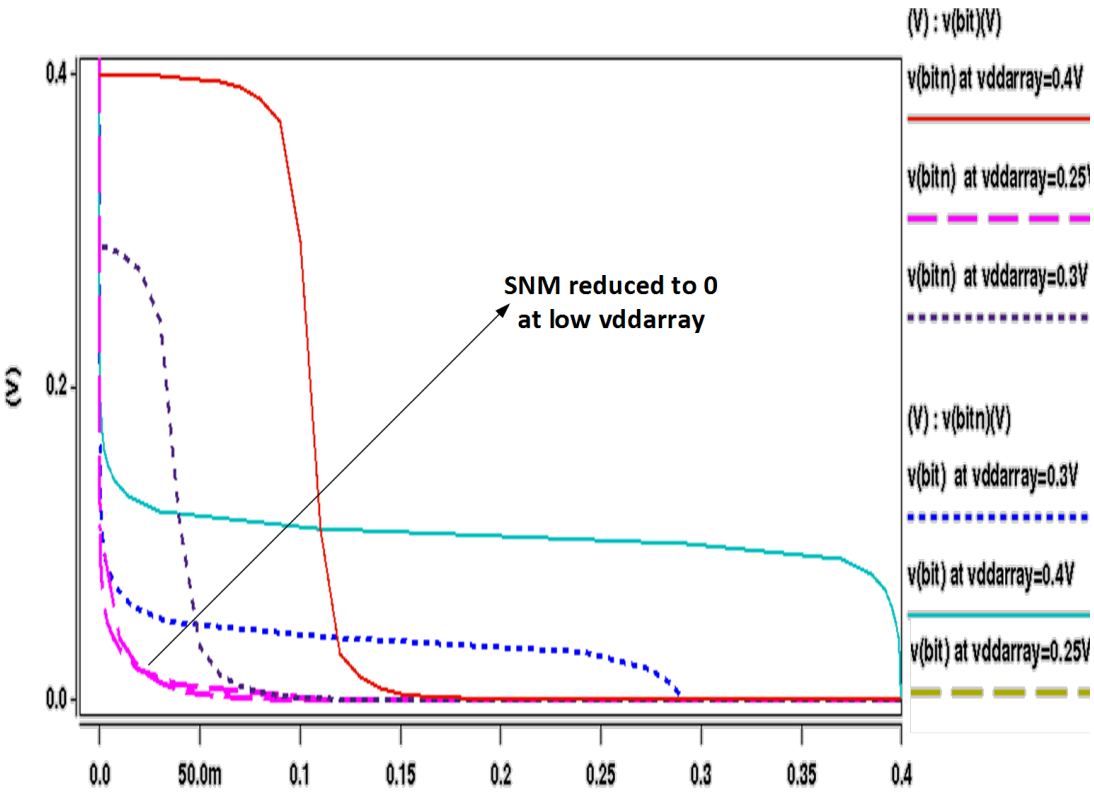

Fig. 2.5 SRAM Bit-cell SNM for V_{DD}=0.4/0.3/0.25 V with No Noise Impact in Cells. At Voltage Lower than DRV, SNM is zero.

The cross-coupled inverters in bit-cell should have loop gain greater than one to preserve the stored data. Under low V_{DD}, the VTC of the internal inverters degrade to make the loop gain equal to one; at this point, SNM of the bit-cell reaches zero, in Fig. 2.5. The method to find SNM and DRV becomes challenging with SPICE simulations under variation impact that brings mismatches in device threshold voltages [Cheng04]; hence, [Seevink87] method is adopted to find the value of minimum diagonal in the VTC. In the simulation, with the transformed axis, the V_{DD} is swept from 300 mV to 270 mV at TT corner across 50 variations in devices; Fig. 2.6 illustrates that the SNM is reduced to as close to 18 mV for 300 mV and zero at 270 mV. This does not consider the impact of layout which should add 20% margin. Even at 300 mV, there are cases which are very close to zero, hence a 350 mV DRV is considered that could retain the stored bit value.

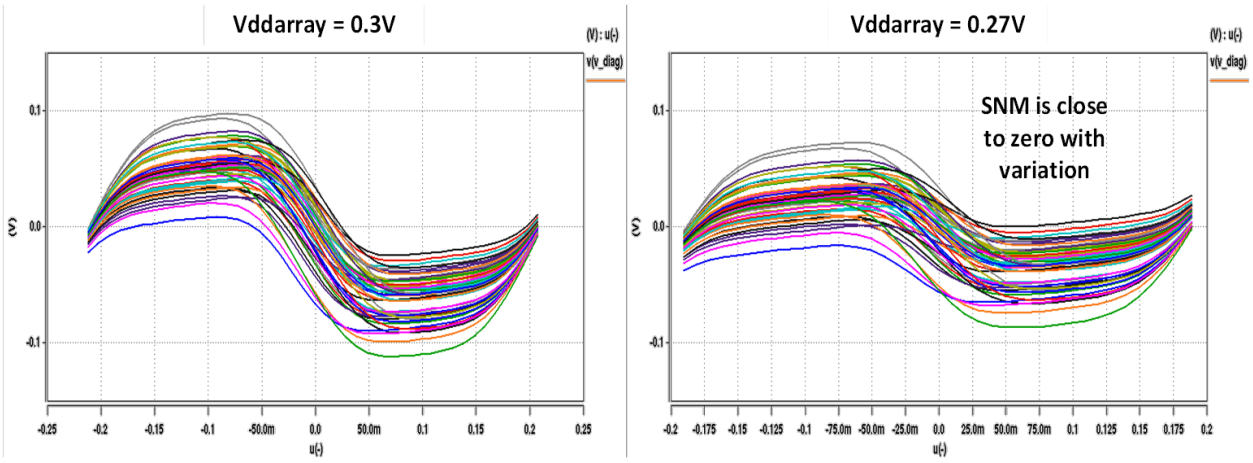

Fig. 2.6 SNM of Bit-cell for 300 mV and 270 mV at TT corner and Nominal Temperature. Right Curve Shows Zero SNM at Voltage Lower than DRV.

2.2.3. SRAM Column Group Design

The column group is designed with two 128x8 bit-cell array and read and write circuits.

Fig. 2.7 shows detailed circuit of column group top; sense amplifier read and write blocks.

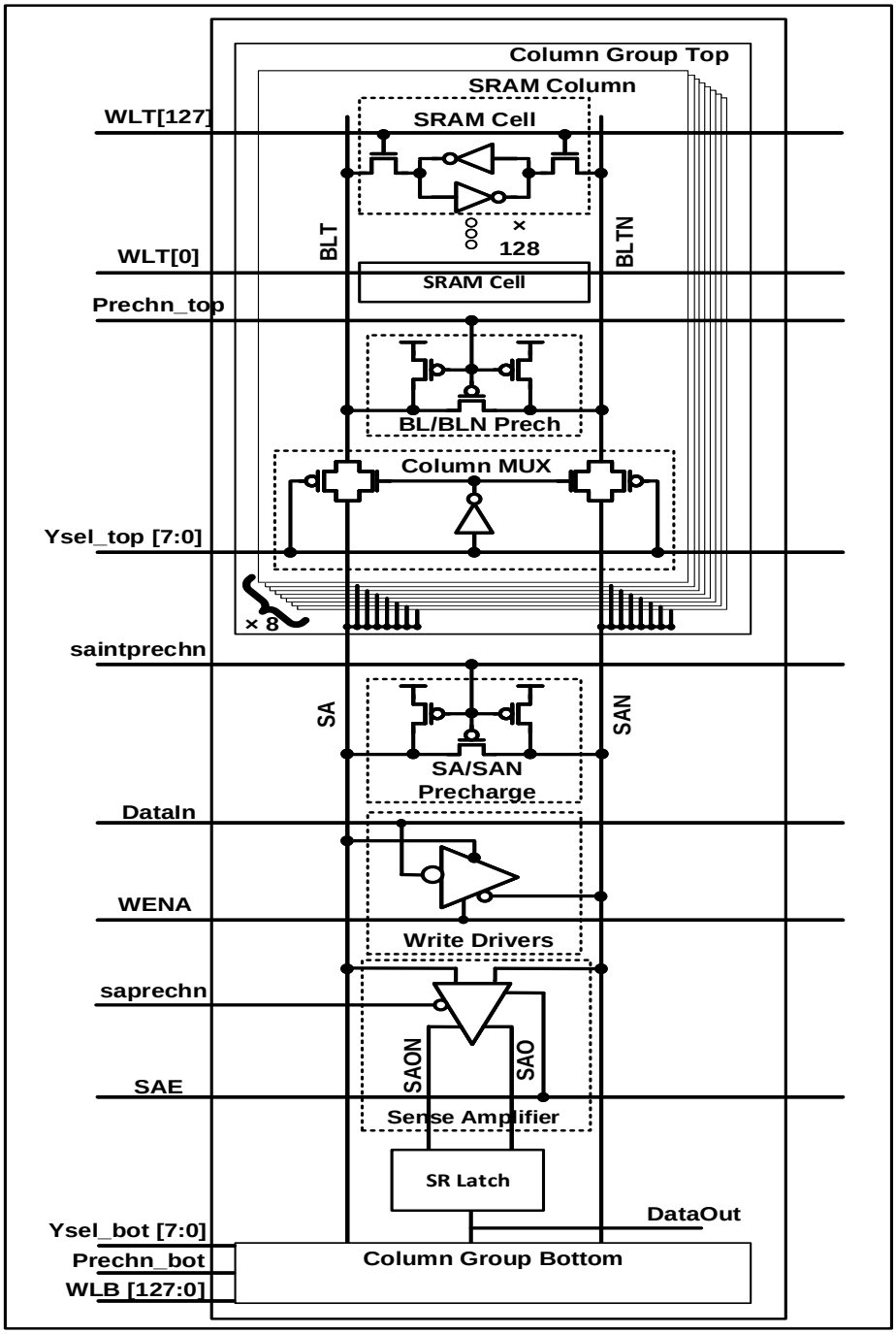

Fig. 2.7 SRAM Column Group with Top and Bottom Column Arrays and Write/Read Circuit.

In the Fig. 2.7, the bit-cell array has 8 cells stacked one over other and 128 cells connected in other direction. One of these 8x128 cells is accessed in a clock cycle for read or write operation which is performed by read/write circuits. In a full column group, there are 2048 (2x128x8) bit-cells.

2.2.3.1. Write Circuit

This circuit in Fig. 2.8 is made up of buffers and tristate driving inverters which generate inverted SA and complementary SAN signals. These signals are connected to BL and BLN to write data on the bit-cell when the y-multiplexer are ON.

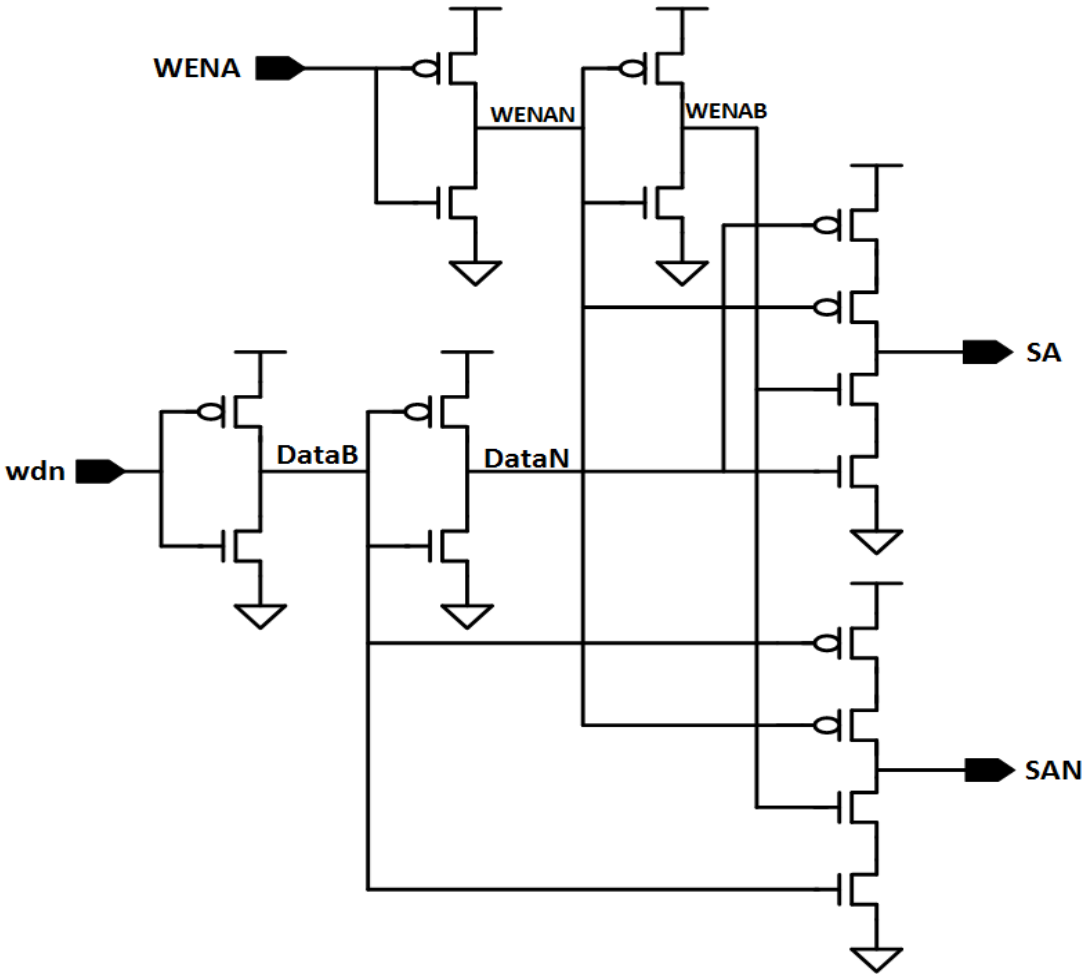

Fig. 2.8 SRAM Column Group Write Driver Circuit.

The same driver writes to both top and bottom array of column depending on the top or bottom selection. This selection is controlled by address<10> bit of the 14-bit address given to TC25. When address<10> is logic "1", top of column group is selected and on logic "0", bottom is selected. Upon the WENA signal assertion, tristate logic behaves as inverter and inverted data on *wdn* node is generated on SA node, whereas the same polarity signal to wdn is copied on SAN. The power supply voltage on SA and SAN is V_{DDS} which is enforced through pre-charge circuit.

2.2.3.2. Read Circuit

This consists of a pre-charge circuit that charges the BL and BLN to V_{DDS} in the low phase of clock. The y-multiplexers that read the BL and BLN signals are open after certain delay that includes the time required for bit-cell to change the value on bit-lines. The sense amplifier enable signal SAE is fired after the required offset voltage is developed on BL and BLN. A detailed analysis on sense amplifier offset is performed for signal delay calculation in chapter 4.

To turn the output dynamic signals of sense amplifier into static signal, an SR-latch is connected to the dual-ended output of sense amplifier. The output of SR-latch is buffered to the dataout port. Fig. 2.9 shows the layout of column group in which WL run in vertical direction on M2 and BL/BLN run in horizonal direction.

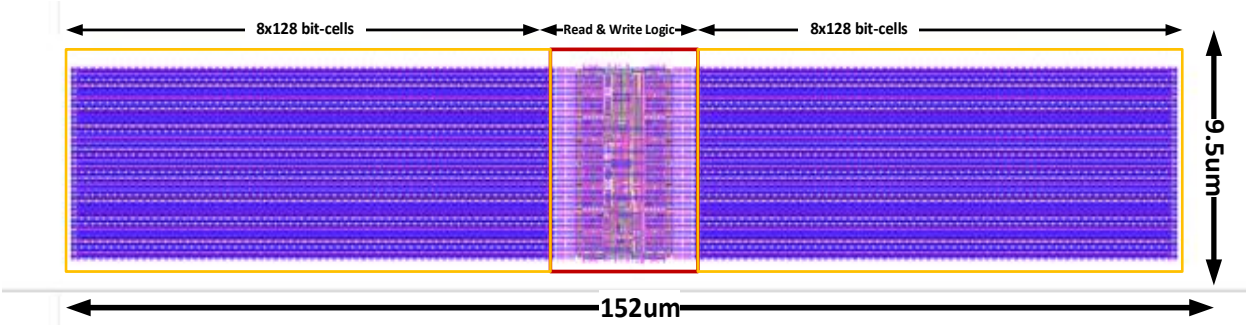

Fig. 2.9 SRAM Column Group (2 x 128 x 8 Bit-cells) Layout.

2.2.4. 7-to-128 Decoder Design

To fire the WL of one of 128 bit-cells, a 7-to-128 lines static 1-hot decoder is designed. The decoding scheme is divided in two parts, viz, pre-decode and post-decode. The pre-decoder decodes the 7-bit address lines to generate PA, PB and PC signals as shown in Fig. 2.10.

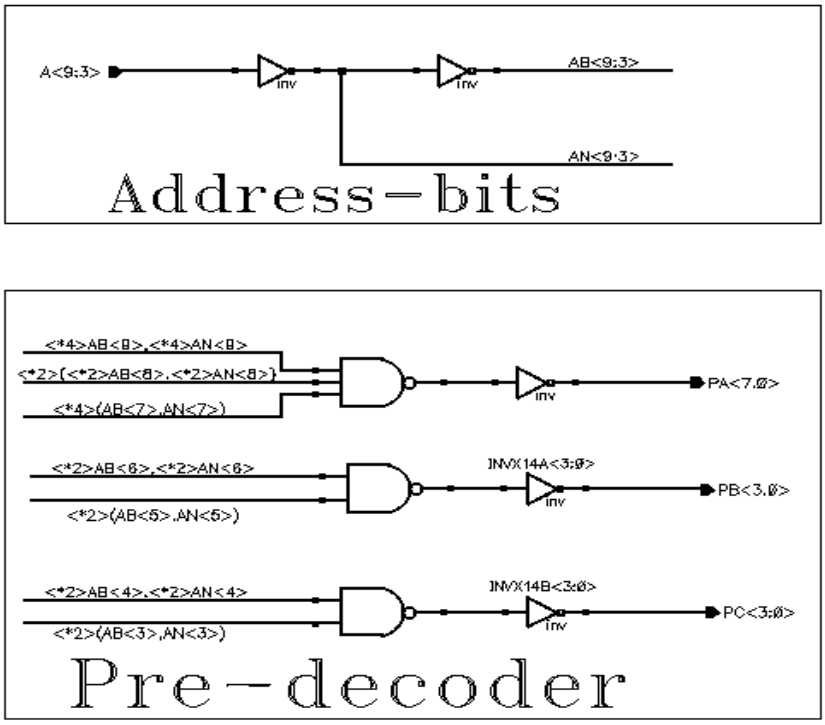

Fig. 2.10 7-Bit Address to 128-Bit WL Row Pre-decode.

These pre-decoders have small area as compared to the post decoding scheme. Each bit of PA, PB and PC signals from pre-decode is multiplied with each other to generate 8x4x4 (128) combinations of WL. The NAND gate signals are clock gated with the word line enable (WLENA) signal as shown in Fig. 2.11. There are 32 units of post decodes, one unit shown in Fig. 2.11, that generate the WL<127:0>. The WL have large capacitive load since they run across the width of array and hence while calculating the wire load for WL, both access transistor and wire capacitance with some guard-band were used. Due to the load cap, the WL driver inverters have 25.24 um (p:n

= 15.16 um:10.08 um) total transistor size. The five inversion stages before the driver inverter, are designed with ULL transistors which have low leakage but high threshold voltage. The final driver inverters are designed using LVT transistors to achieve a faster speed with comparatively small size devices.

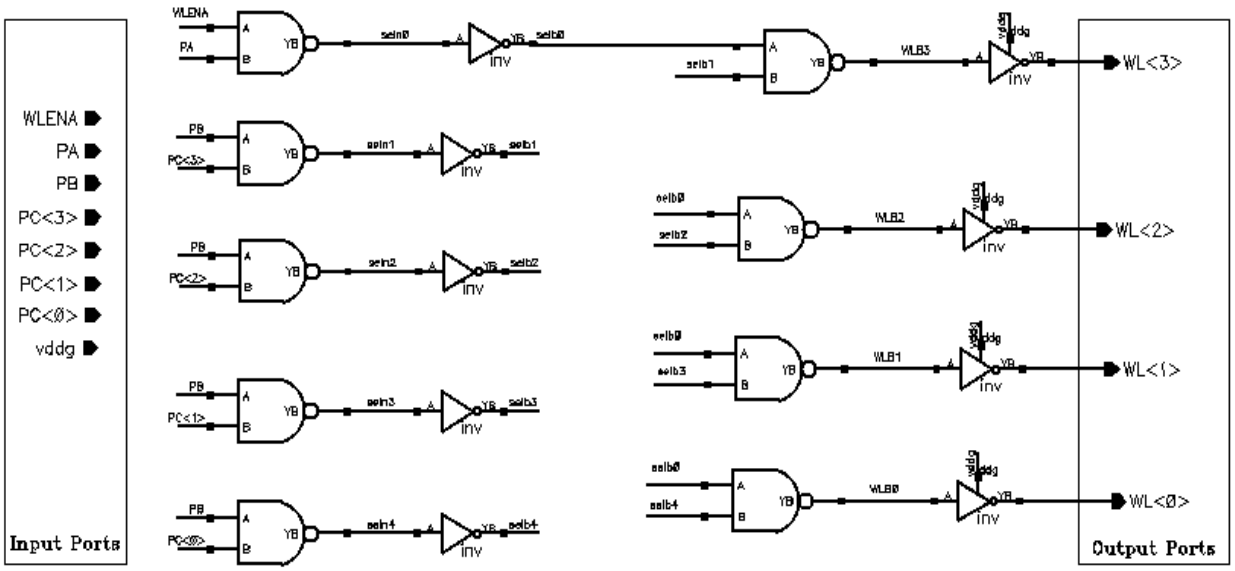

Fig. 2.11 7-Bit Address to 128-Bit WL Row Post-decode Unit.

Access transistor gate capacitance is calculated through a single bit-cell layout extraction. To find the size of word line driver inverters, the load capacitance on each line is calculated. The total transistor capacitance is calculated by multiplying the no. of column groups to the no. of bit cell in each column group and further to the no. of transistors in each bit cell and capacitance of access transistor gates. The resultant transistor capacitance is 108.8 fF (64 x 8 x 2 x 1.063 x 10^{-16} F).

The WL metal wire capacitance is calculated by extracting wire parasitic capacitance, includes cross-coupling capacitance as well, from column group and further estimated as no. of column groups multiplied by single column group WL capacitance. The resultant value is guard

band for additional length that consists of wire running across the height of decoder. The total wire capacitance is calculated to be 303 fF (64 x 3.949 x 10^{-15} x 1.2).

This value is then used to back calculate the logical effort of each stage and hence size each transistor in the signal path. The WL metal tracks run parallel to each other which could be a cause of coupling capacitance. While routing these wires, we leave double spacing between these routes to reduce coupling effect that can cause signal integrity issues. This is one of the reason that a decoder has huge width which is equal to SRAM array width.

2.2.5. Decoder Power Gating

The WL driving inverters in decoders are gated by a Power Gater. This circuit shown in Fig. 2.12 is controlled by bank select and top/bottom selection address<10> bit.

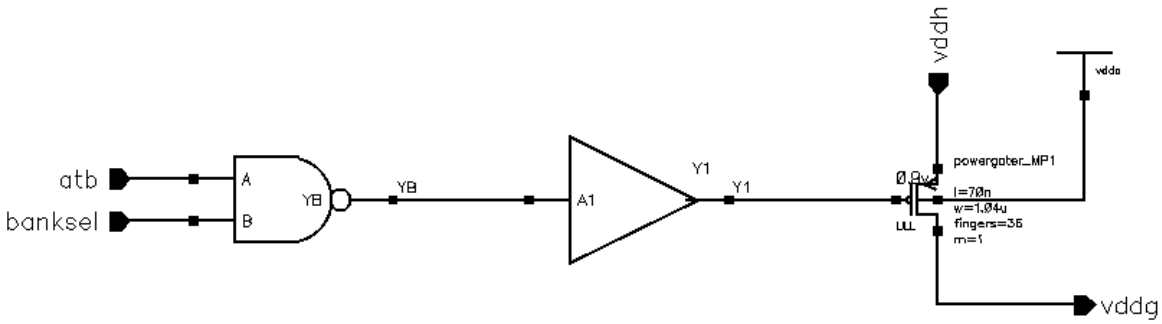

Fig. 2.12 Power Gater Circuit to Control Decoder Driver Inverter Power Supply.

A big PMOS, as shown in Fig. 2.12, is used to turn the power supply of long inverter rail. This reduces the WL leakage and in turn helps to control the leakage induced coupling capacitances on the metal wire parallel to WL. We performed simulations of power gater PMOS that shows required current of ~100 uA with 0.9 V vddg supply.

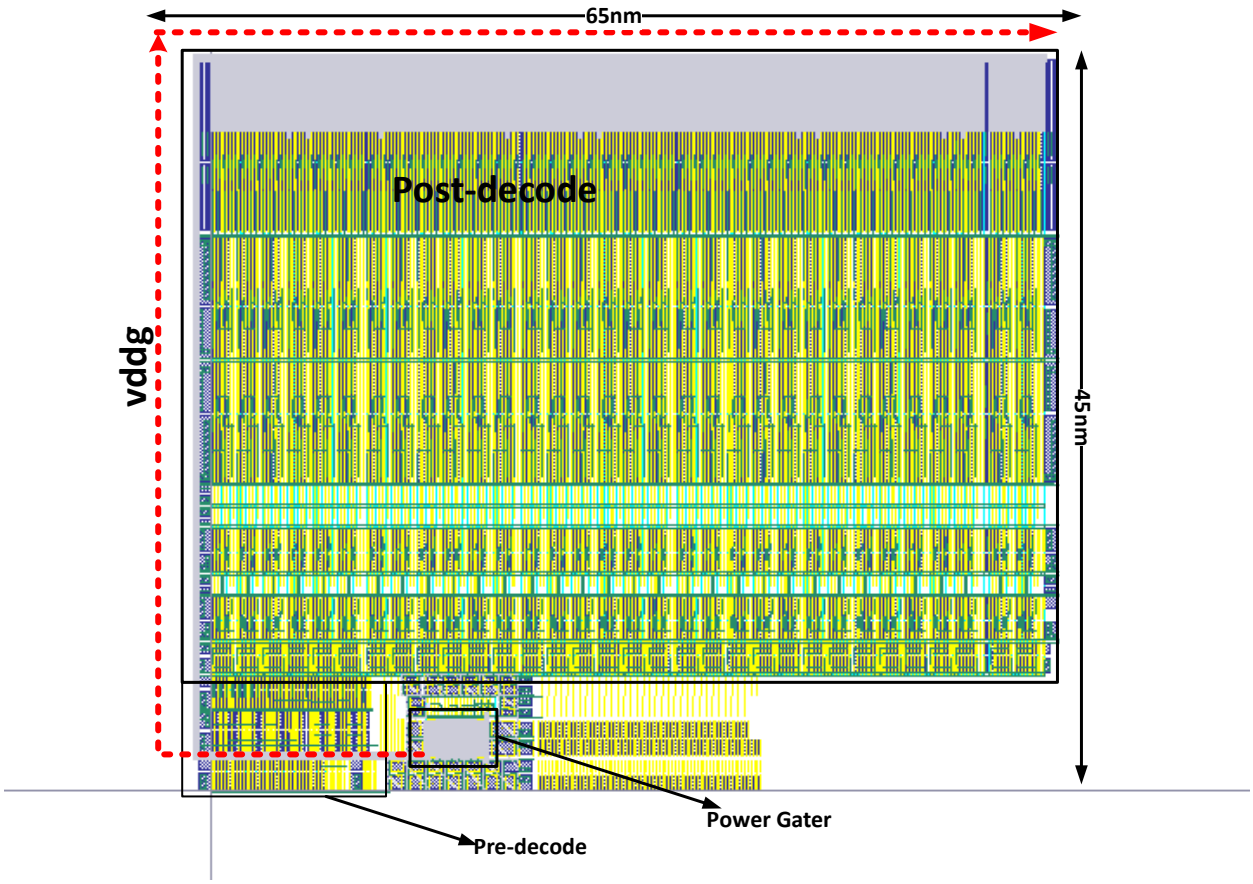

Fig. 2.13 Decoder and Power-gate Layout Designed for 16KB Custom SRAM Block.

The power-gate is integrated in decoder as shown in Fig. 2.13, the decoder width is matched with the SRAM 128x8 array, can be observed in Fig. 2.2.

2.2.6. Control Logic Design

SRAM has certain critical races such as WL to BL pre-charge, sense pre-charge to SAE and address to WLENA. A robust control circuit is designed to generate the enable and clocked signals for read/write logic. All the timing conditions w.r.t to clock are met satisfactorily through this circuit. The timing graphs related to control signals are shown in next Section 2.2.6.

Unlike other custom units in SRAM 16KB, this is a standard cell only design which is laid out using a new methodology to Auto Place and Route (APR) a standard cell based schematic

design. This kind of flow can be used for quick Place and Route turn-around time. In this we generate Verilog netlist from your Schematic Design through Virtuoso Composer. This generated Verilog netlist with other collaterals such as LEF and DEF are taken to Cadence Innovus (newer version of Encounter Digital Implementation) to place and route the design.

2.2.6.1. Schematic Design

The circuit is designed in custom schematic design platform such that the logic gates are chosen as per the required drive strength and delays. Most of the logic gates are chosen from the standard cell library, few of the modified cells are maintained to have same foot print as standard cells. This is done to ensure that in the Verilog netlist, each modified cell would have standard cell substitute whose other collaterals such as macro and Verilog function are available.

2.2.6.2. Verilog Netlist Generation

This is performed through the NC_verilog Environment Integration utility [NC-Verilog15]. The Verilog environment reads specialized simulation run control file “simrc” to generate Verilog netlist from schematic. The snippet of run control file is shown in Fig. 2.14, variables used in “simrc” file are specific to hierarchical netlist generation through Open Simulation System (OSS) [OSS17].

```
 8 simNotIncremental = 't
 9 simReNetlistAll = nil
10 simViewList = '("behavioral" "functional" "system
   mbol")
11 simStopList = '("verilog" "pld_verilog" "lai_veri
12 simNetlistHier = t
13 simVerilogLaiLmsiNetlisting = 'nil
14 verilogSimViewList = '("behavioral" "functional"
   ic" "symbol")
15 simVerilogAutoNetlisting = 't
16 simVerilogNetlistExplicit = 't
17 hnlVerilogTermSyncUp = 'nil
18 simVerilogFlattenBuses = 'nil
19 simVerilogPwrNetList = '("VDD!" "vdd!")
20 simVerilogGndNetList = '("GND!" "VSS!" "vss!")
21 vtoolsifForceReNetlisting = 'nil
22 vlogifInternalTestFixtureFlag = 'nil
23 simVerilogBusJustificationStr = "U"
24 simVerilogTestFixtureTemplate = "All"
25 simVerilogDropPortRange = 'nil
26 vlogifCompatibilityMode = "4.2"
27 simVerilogEnableEscapeNameMapping = 'nil
28 hnlSupportIterInst = t
29 vlogExpandIteratedInst = t
30 hnlVerilogPrintSpecparam = nil
```

Fig. 2.14 Snippet of Simulation Run Control (simrc) File.

2.2.6.3. Design Floorplan and DEF Export

Create a floorplan (a placement plan) for the control block with estimated area such that we will have fixed pin locations as in Fig. 2.15 and bounded area for the block. The floorplan with SRAM, Decoder and Control looks like the block shown in Fig. 2.15, in the beginning of this chapter. It important to create a place and route (PR) boundary that is understood by the APR tools as design boundary, no placement or routing would be performed outside this area.

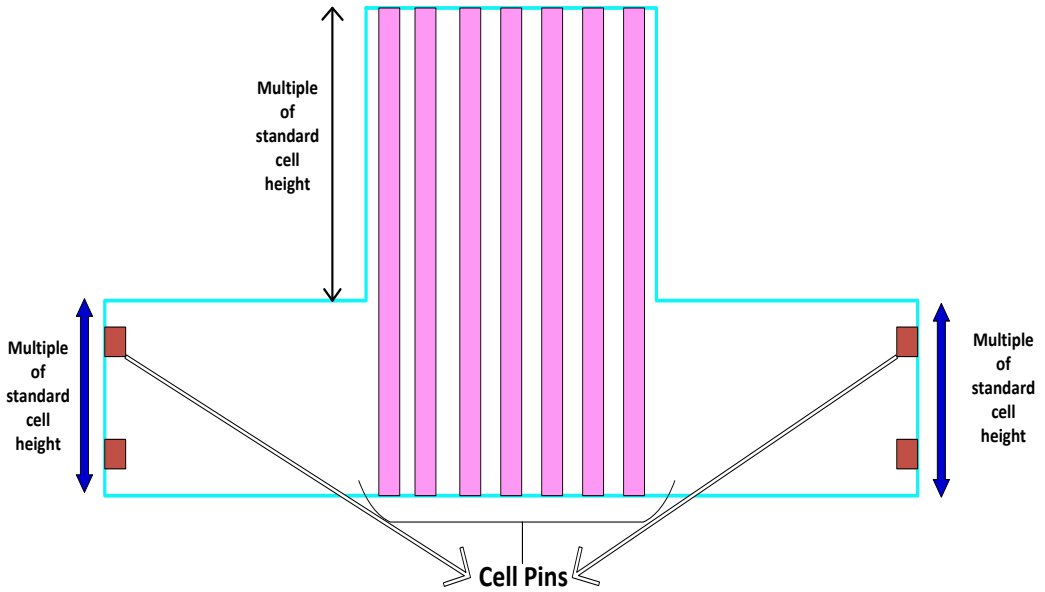

Fig. 2.15 Control Block Custom Floorplan with PR Boundary and Pins

Innovus [Innovus16] requires power, ground and clock signal types which are not generated by default from Virtuoso. Hence, a Cadence SKILL language code, shown in Fig. 2.16, is written to automate the signal type definition on ports in the design.

```
19 procedure(setSigType(@optional (power "vdd") (ground "vss") (clock "clk"))
20
21 let((d_cvId d_netId)
22         ;; Get Cell View Id
23         d_cvId = geGetEditCellView()
24
25         ;; get the power net Id
26         d_netId = dbFindNetByName(d_cvId power)
27
28         ;; set the net signal type to supply
29         d_netId~>sigType="supply"
30
31         ;; get the ground net Id
32
33         d_netId = dbFindNetByName(d_cvId ground)
34         d_netId~>sigType="ground"
35
36         ;; get the clock net Id
37
38         d_netId = dbFindNetByName(d_cvId clock)
39         d_netId~>sigType="clock"
40
41         printf("\n Signal type for %s, %s and %s pins is set\n" power ground clock)
42 ); let
43 ); proc
```

Fig. 2.16 Cadence SKILL Language Code for Signal Type Definition.

2.2.6.4. APR in Innovus and Design Back-ported to Virtuoso OA Format

The generated Verilog netlist and DEF file along with other collaterals are used in for automated place and route in Innovus [Innovus16]. The design is placed and routed, shown in Fig. 2.17, without optimization to keep the circuit same. The completed design is exported to DEF format file which is read in Virtuoso for SRAM 16KB design assembly.

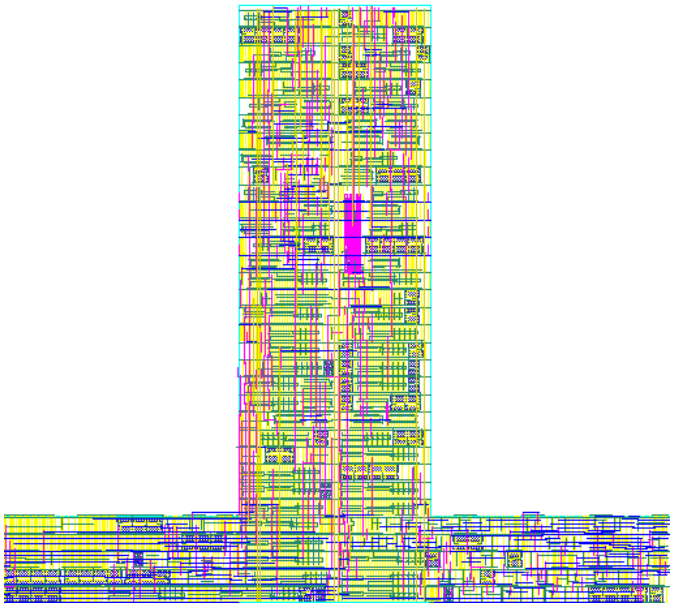

Fig. 2.17 Control Block Placed and Routed Design.

2.3. SRAM 16KB Bank Assembly

The 16KB bank has 64 column groups, divided into two groups, which each generate 32-bit word. Input data (datain) of width 64 bits can be written in the SRAM in one clock cycle. All the signals inside this block are flopped at the negative edge of clock that gives enough setup margin for write and read operations. The two decoders enable top and bottom word lines. Wide rails are laid out on Metal 4 to tap power connection later by APR tool for 1Mb power rails.

2.4. Timing

In this section, the write and read operation timings are discussed. For both write and read operations, the X and Y decoders are enabled; timing for these common paths are discussed.

2.4.1. Address Decode Timing

All the signals to 16KB bank are flopped at negative edge of the FF clock. The x and y decoding have divergence point from the flopped outputs, hence timing between the two paths is important. Before the WL asserts (by x-decoder), the write driver should have already passed the signal to SA and SAN. For this, the syn (from y-decoder) should be asserted when the SA and SAN signals are updated, to promptly open the y-multiplexer to pass the signal value on to the BL and BLN (complementary bit-lines). Hence, this critical timing of the WL assertion and syn (y-select) should be synced as shown in Fig. 2.18.

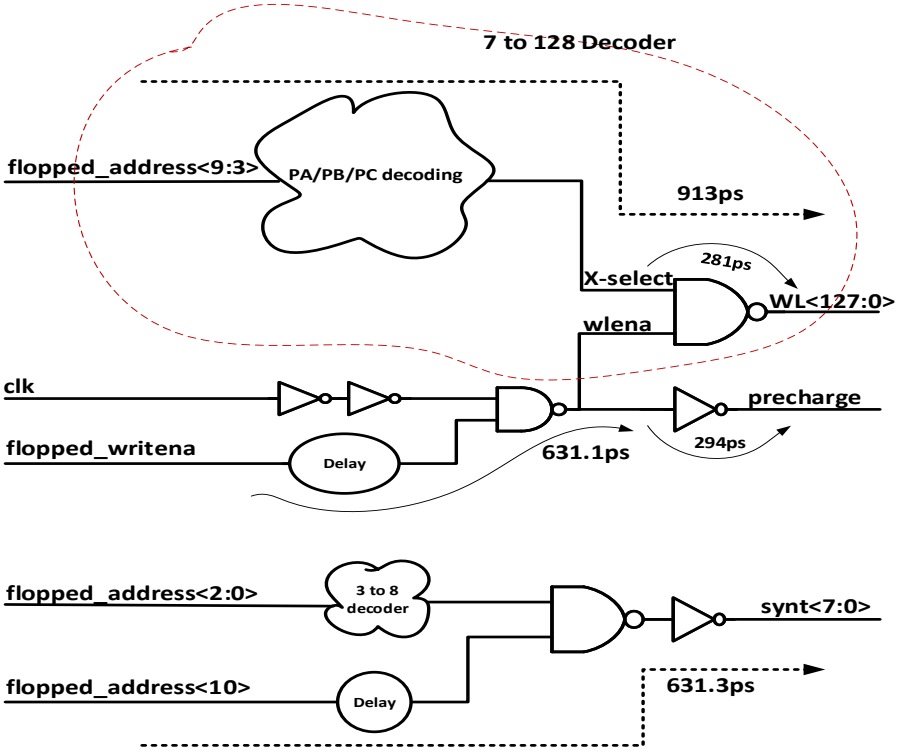

Fig. 2.18 SRAM 16KB X and Y Decode Timing for Write and Read Operation.

When the write enable and clock signal assert, the wlenat/wlenab goes high; setup time margin of 50 ps left between clock and write. From Fig. 2.18, the wlenat signal is asserted when the address is decoded, similarly the WL fires after two gate delays of 281 ps. The simulation results in Fig. 2.19 are from analysis on TT corner at nominal room temperature; this is performed by UltraSim (a fast spice simulator) in mixed-signal mode. We also performed analysis on SS and FF corner. At SS corner, the propagation delay become ~1.8x of TT whereas at delays in TT corner are ~1.8x of FF corner. Since all the sub-systems are assumed to be at one corner at time, the impact of delay is compensated through the circuits tracking each other at all the corners.

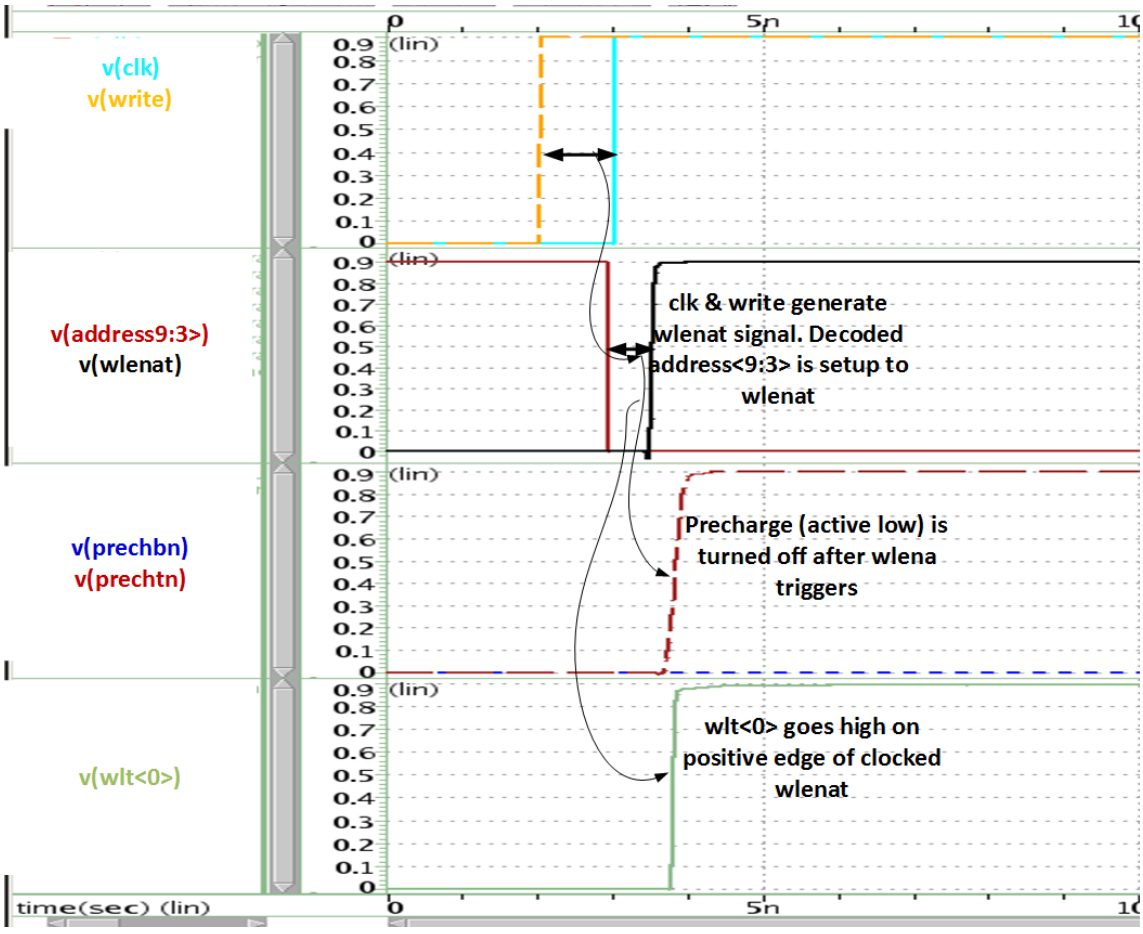

Fig. 2.19 Circuit Simulation Waveform Showing Assertion Sequence of WL and Pre-charge Signal.

2.4.2. Write Timing

The write operation timing is pre-dominated by the write enable signal generation and time required for the bit-cell to change the internal nodes bit and bitn, the path delays observed on circuit at TT corner are listed in Table 2-2.

Path	Propagation Delay (ps) at TT corner
WENA to SAN	544
Synt (y-mux select) to BL	477
Blt to bit	132

Table 2-2 Critical Path Delays for Write Cycle.

It takes 132 ps to flip the data value in the bit-cell, the timing sequence is shown in below Fig. 2.20.

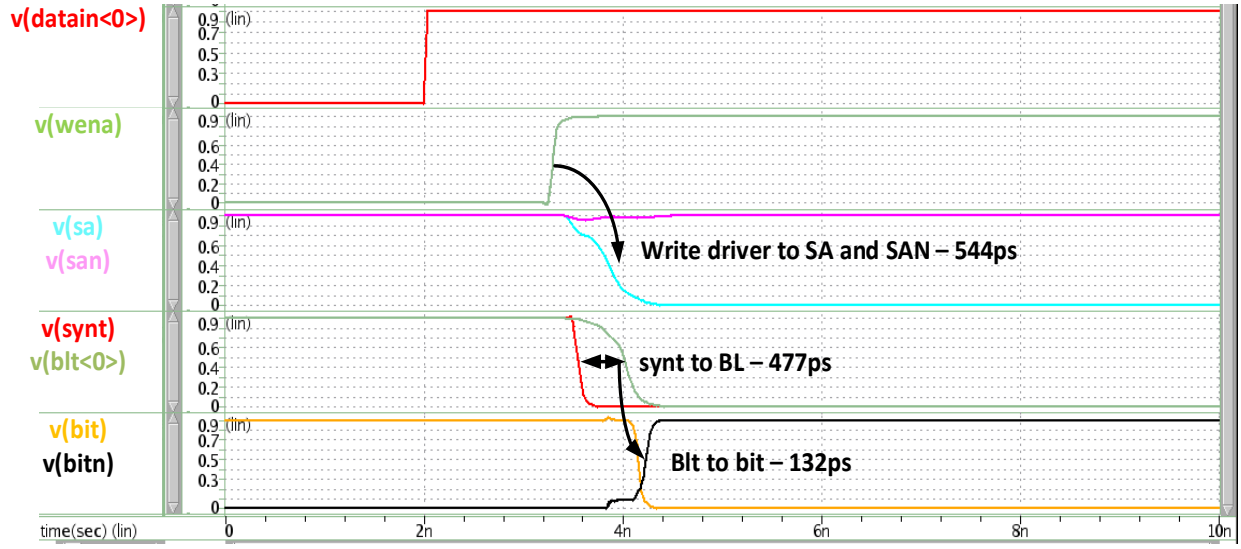

Fig. 2.20 Simulation Waveform for Write Operation in SRAM 16KB at TT Corner with Delays.

2.4.3. Read Timing

For read operation, the sense amplifier and pre-charge timing is critical and is synchronized with the clock operation. When the read enable is asserted, in addition to the y-multiplexer selection signal, SAE is fired just after the SA and SAN nodes reach the offset voltage required by the sense amplifier. Also, the pre-charge signal should be disabled just after the WL de-asserts, as shown in Fig. 2.21.

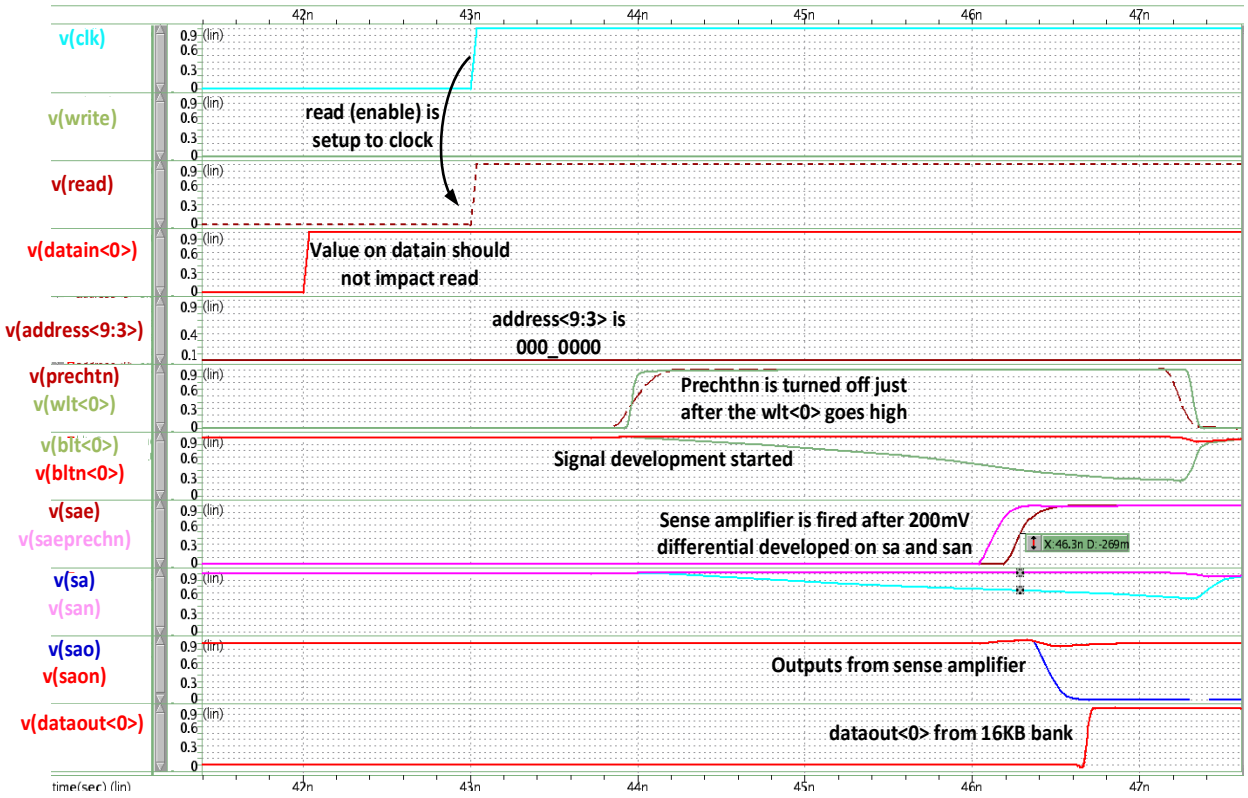

Fig. 2.21 Simulation Waveform of Read Operation on SRAM 16KB Bank at TT corner. Data is Read-out from Address<10:0>=11'b1_0000000_000.

The sense pre-charging is done locally to first equalize the dual inputs and hence avoid any previous data be sensed. After the bit-line pre-chargers are off and the y-multiplexers turned on, the BL/BLN voltage starts developing on SA and SAN. To control the sense amplifier sae firing, a programmable delay control logic is used which is configured by special registers at the top level.

Sense amplifier enable is nominally fired 100 ps (section 4.2.6) after the sense pre-charge is turned off, this leaves good margin for sa and san development. The SR-latch and a giant buffer takes 229 ps to send the output to the dataout node.

CHAPTER 3. SRAM 1Mb SYNTHESIS AND APR

3.1. Architectural Overview

SRAMs and RFs are used as caches in a microprocessor design. In TC25, there are 3 SRAM Arrays, two 6T-SRAM 1Mb blocks and one 8T-SRAM 1Mb block. The SRAM Array is selected by a block select BLK_SEL<1:0> select IO signal from TC25. Another signal SRAM_SEL<1:0> is sent to select one of the SRAM 1Mb blocks out of the three. SRAM Array block receives clock from external XOR_CLK0 which is sent from outside the TC25 through an IO pad. The SRAM 1Mb consists of eight banks of 16KB each. The signals to this block are given directly through IO Pad in TC25. These signals are not flopped till they reach SRAM Array block.

The SRAM-1Mb has eight banks, each of these sample the input signals at the negedge of clock. All the banks receive the address<10:0>, the 64bit dataout from the selected bank is multiplexed to the output port. The 1Mb design also has four level shifters, each of which converts the 16 bits low voltage dataout signal from SRAM to the core voltage of VDDH 0.9 V or above. This signal is further level shifted by the level shifter in the IO pads. The level shifter design is based on that described in [Zhou15]. Also, there are eight power multiplexers to choose between dummy supply or core voltage supply to each bank.

3.2. Bank Abstraction

Abstraction or simply abstract creation is a technique of representing a standard or macro cell such that only its pin geometries, obstruction, size, orientation and other physical features are visible for the user. The Fig. 3.1 shows eight abstracted banks of SRAM 16KB blocks inside core.

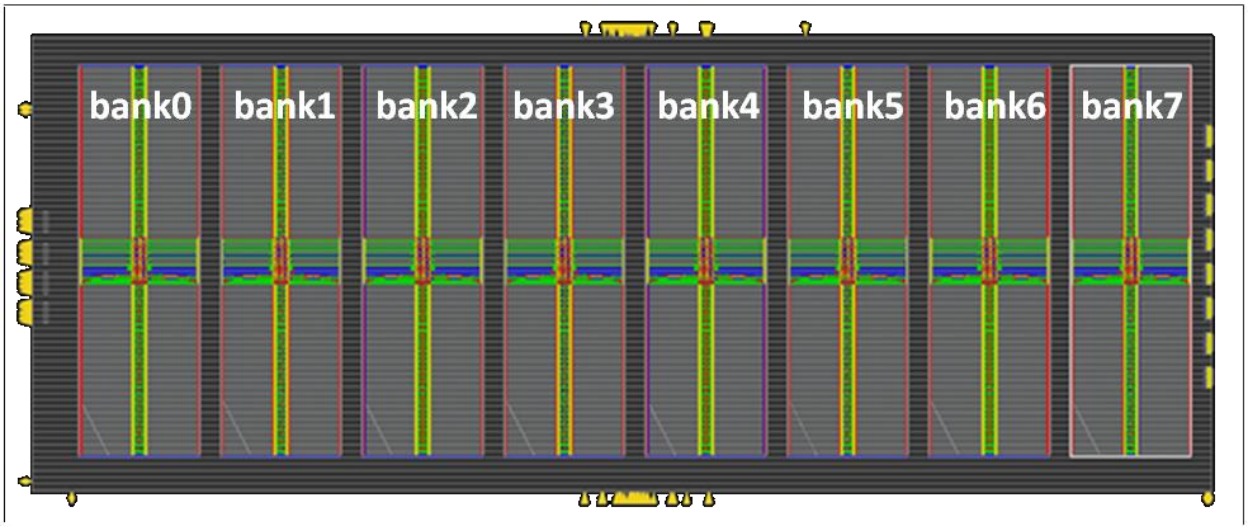

Fig. 3.1 Placed Abstracts of 8 SRAM 16KB Blocks Inside the Core Region.

The colored geometries are the pins and obstructions extracted from the layout which generating the abstracts. This is an essential step in running automatic place and route (APR) flows. As APR is done on multi-million gates designs, a macro cell representation of a standard cell having a limited number of features helps speed up the design cycle. The abstract of a cell is represented in a Library Exchange Format (LEF) file. The abstract for the SRAM 16KB is created using Cadence Abstract Generator. The abstract generation requires the layout representation of the standard cell or macro intended to characterize as input. It also requires specific user defined constraints that enable the appropriate abstract generation of the macro. For SRAM 16KB abstract creation, the power and ground (PG) nets were extracted only for the layers which had explicit labels. Shape chasing was disabled for PG nets, as this results in an overwhelmingly detailed abstract. A highly-detailed abstract causes huge runtime impact and defeats the purpose of using abstracts instead of layouts during APR. For signal nets, shape chasing was enabled as signal nets are localized and there are limited number of geometries associated. Enabling shape chasing for

signal nets also helps get a detailed geometry for signal pins, which assists the APR router during pin accessibility.

The size of the macro is determined by the PR boundary of the macro specified in the layout. For quick APR turnaround time, cover blockages were used for lower metal layers such as Metal 1 and Metal 2. For pins on Metal 1 and Metal 2, cutouts were created such that the pins are accessible by the router during APR. The custom design was carefully done and most of the IO ports were routed on upper metal layers like Metal 3 and Metal 4. Detailed blockages and pins were extracted for Metal 3 and Metal 4 such that the pins are easily accessible by the router and least number of DRC's are left out for the final fix. One of the important geometries extracted by abstract generator is the obstruction. An obstruction is an intermediate route that is not an IO pin. In case of detailed abstraction, such as for Metal 3 and Metal 4 in case of SRAM 16KB, the obstruction must be extracted. In an abstract, an obstruction is a metal geometry that must be considered while routing during APR. In case of absence of appropriate obstruction inside the abstract, the space as treated legal for APR level routing. This may lead to a huge number of DRC's during final DRC fix.

3.3. Bank Library Generation

Custom designed macros such as the SRAM 16KB blocks need to be characterized for timing, power, rise and fall transition time, setup time, hold time and pin capacitance, as this information is not provided by the foundry. The SRAM 16KB required to be characterized to be used in full chip static timing analysis (STA) flows. Accurate characterization of the SRAM 16KB blocks is important for accurate timing and power analysis at the chip level. The characterization of the SRAM 16KB block was done using Cadence's Liberate MX [Liberate16].

Liberate MX uses a fast spice simulator to gauge the activity of the design to be characterized, based on the input vectors. Based on netlist simulation and input vectors, Liberate MX identifies the input storage elements, like latches and flip flops. Each input to output arc is identified and analyzed for a range of input slews and output load capacitances specified by the user. Identification of each arc is important in accurate characterization of the SRAM as the APR stage uses these arcs and associated timing numbers from the timing library to estimate the path delay during STA. Arc based delay, power and rise/fall transition times are written in a Liberty (lib) file. These parameters depend on the operating conditions such as process, voltage and temperature (PVT). Any change in the PVT impacts the delay, power and rise/fall output transition times, and requires a new liberty file. The SRAM 16KB was characterized for typical process, 0.9 V operating voltage and 25-degree Celsius temperature. These were typical operating conditions that were used for standard cell as well.

3.4. SRAM 1Mb RTL Synthesis

As the cell level timing and physical information is available, this information is used to synthesize the RTL and generate a gate level netlist. Synthesis is a process of converting the RTL code into logic gates that mimic the functionality of the code. The SRAM 1 Mb block RTL having 8 SRAM 16KB macros and peripheral standard cells was synthesized using Cadence's Encounter RTL compiler. Synthesis is always performed targeting a specific technology. In this case, we used the Fujitsu 55-nm process standard cells, and timing libraries along with the characterized timing library of the SRAM 16KB for synthesis. RTL synthesis uses this information and maps the RTL code to its corresponding logic gate or a combination of gates. For instance, a case statement in the RTL maps to a multiplexer. Best quality results are obtained when the input standard cell library is exhaustive. This enables the tool to pick the exact cell based on the functionality required

instead of building its own logic using many standard cells. Another important parameter required to run the RTL synthesis are the timing constraints. Timing constraints are boundary constraints which provide important information about the IO ports in the design to be synthesized. For example, input and output delay, clock definition. For the SRAM 16KB block, the input and output delay constraints were determined by analyzing the path delay from the top-level ports to the IO's of the SRAM 1Mb block.

Based on the boundary constraints RTL compiler performs STA and estimates worst timing paths in the design. The worst timing path is one which has the worst negative slack among all the timing paths in the design. The tool estimates the cell or macro delays using the delays characterized in the timing library and the wire delays using wire load models. Wire load models are estimate resistances and capacitances based on the area of the design. For the SRAM 16KB block, the worst timing path estimated during synthesis was reported between from flopped output address[10] to the input port of the SRAM 16KB bank instance. This path was also marked as the most critical path during APR. This path had 0 ps slack with a clock period of 15 ns (66.66Mhz clock frequency) at the synthesis stage.

3.5. 1Mb APR

After synthesizing the design, a gate level netlist is generated for the SRAM 1Mb block. The gate level netlist is functionally equivalent to the RTL code. The RTL compiler also generates a Synopsys Design Constraint (SDC) file which lists the boundary constraints to be used in the APR flow. These constraints are optimized version of the ones specified during synthesis, as they are updated at each step during synthesis. APR flow requires the technology LEF, macro LEF, timing libraries for all PVT corners, extraction tech file, gate level netlist and an SDC file as input.

We use the characterized lib file generated using Liberate and the macro LEF file generated using Abstract Generator during APR.

The design of the SRAM 1Mb block is done carefully to optimize for optimum power consumption, fast operation and high density. The floorplan size of the 1Mb is 899064um^2, it has 8 SRAM 16KB macros, 4 level shifter cells, 8 power multiplexers and 3254 standard cells. The power grid design of the SRAM 1Mb block is meticulously done to be robust in case any voltage-drop. Metal 1 is used for building the follow rails that give power and ground signals to the standard cells. The follow rails also connect to the vertical stripes on Metal 5 and the horizontal stripes on Metal 6 (METS1). The SRAM 1Mb block contains 5 power supplies, each of them for a different purpose. Detailed description of the usage and the connectivity of each PG net is given in section 5.3 of this thesis report. Each of the PG net in the SRAM 1Mb block is gridded using horizontal and vertical stripes. A snapshot showing the power grid connections of the SRAM 1Mb block is shown in Fig. 3.2.

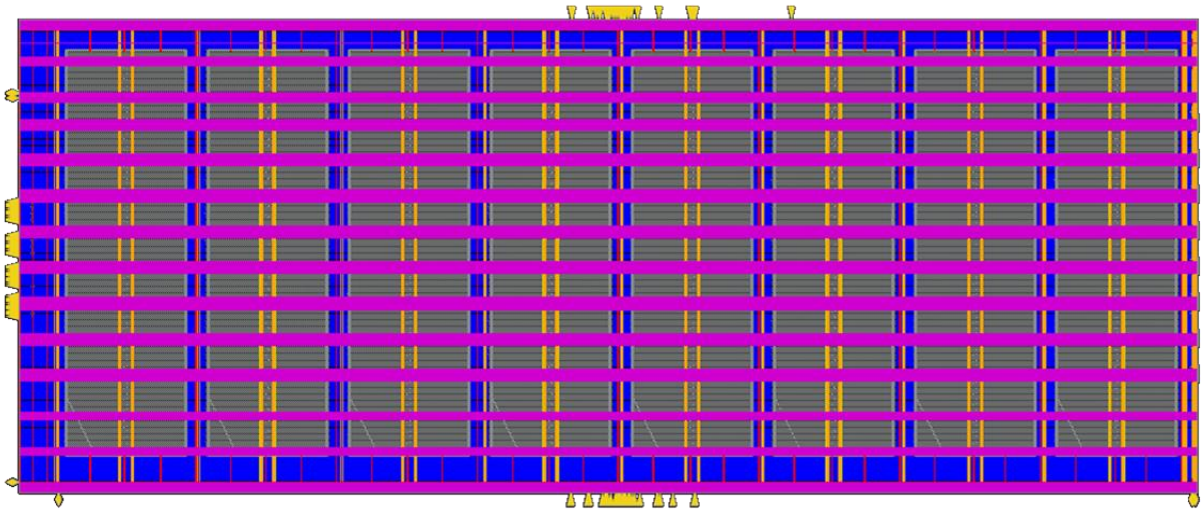

Fig. 3.2 Power Grid of the SRAM 1Mb Built During Automatic Place and Route.

After power planning, the standard cells are placed and the design is analyzed for worst timing paths. The worst timing path seen at the APR stage is from the flopped dataout[10] to the dataout[10] pin at the SRAM 16KB level. Before optimization, the worst negative slack is -128 ps at a clock period of 12.2 ns having 50% duty cycle. The worst path is analyzed and fixed during data path optimization stage.

Now, the SRAM 1Mb block is taken through Clock Tree Synthesis (CTS). We set the skew target of 100 ps, maximum latency of 400 ps and a maximum transition time (slew) target of 40 ps. SRAM 1Mb block uses special clock buffers and inverters specified to build the clock tree. This is essential to meet max transition targets. Clock buffers and inverters are usually larger in size, as they have larger PMOS and NMOS devices. This allows sharper rise and fall transition times and aids in meeting the transition targets. The large size on the other hand incurs higher power consumption compared to regular buffers and inverters. To optimize the design for power consumption, we implement clock gating. The clock propagation is turned off when the data is not expected to change. This reduces the overall toggling activity and hence improves dynamic power consumption. After multiple trials and optimizations, the SRAM 1Mb block ends with a worst skew of 102 ps and a worst-case latency of 365 ps across the setup-late corner.

The balanced clock tree is illustrated in Fig. 3.3 along with the worst skew and latency (Max Delay) for worst case scenarios. In the figure, the clock source pin is shown in yellow which connects to a fanout tree showing clock cells in blue and green. The leaf cells or clock end points are shown in red. After the CTS stage, the design is clock routed using Nanoroute and is DRC clean. The signal nets are concurrently routed during this stage for skew balancing.

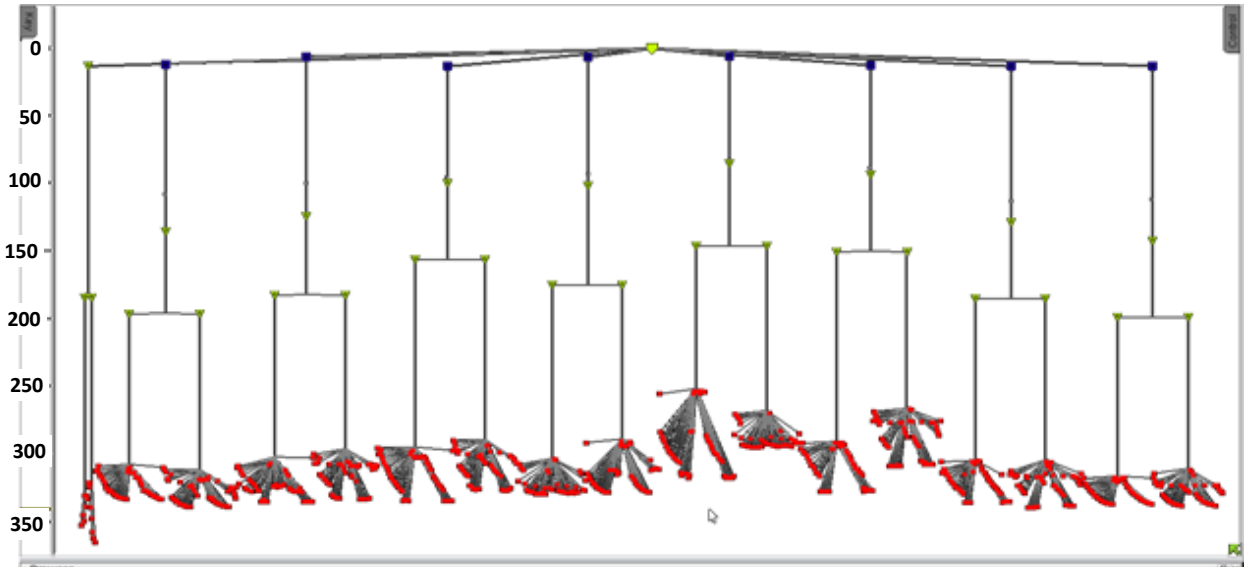

Fig. 3.3 Balanced Clock Tree Synthesis. Worst Skew of 102 ps and Max Latency of 365 ps in All Analysis Views.

As seen in Fig. 3.3, the SRAM 1Mb block has a single clock source which fanouts to multiple leaf cells. After completing CTS, the design is analyzed for worst timing paths, and data path optimization is performed. The data path optimization does not disturb the clock paths and its cells, but optimizes the data path combinational logic cells to obtain best setup and hold slack. After optimization, we observe that the SRAM 1Mb block recovers all the critical slacks and ends up with the 0 ps or more. Now, the design is taken to the next stage, where the signal nets are routed using Nanoroute.

In the route stage the un-routed or trial routed signal nets are detailed routed. The tool uses the technology LEF and the macro LEF file to refer to the foundry provided DRC rules for routing. It is mandatory for each route to honor the DRC rules to end up with a cleanly manufactured design. Any leftover DRC violation may lead to incorrect manufacturing and a functionality failure or bad quality of results. For SRAM 1Mb, the top routing layer used for signal and power routing is Metal 6. The top metal layer is densely used for power routing only. As the total number of

instances in the design (excluding physical only cells) is only 3254, hence they are mostly routed using lower metal layers.

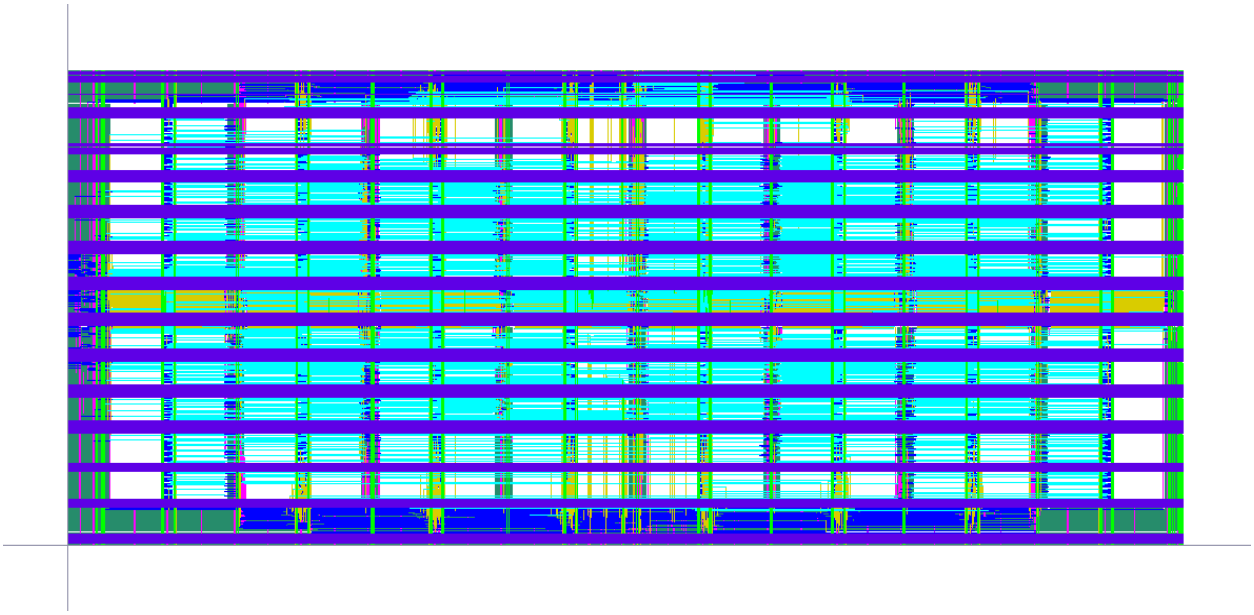

Fig. 3.4 Post Routed Design of SRAM 1Mb Block.

After routing is performed, the design is analyzed for timing. The post routed design is shown in Fig. 3.4, it shows all the PG, signal and clock routes along with instances instantiated in the design. At this stage, it is not expected to see major changes in the timing results unless, the routing is very different compared to the trial routed signal nets (from previous stages). On the SRAM 1Mb block, we see that the worst path remains the same and ends up with minor negative slack for hold time check after routing. A post route optimization step clears these timing violations, and the design is taken for final DRC fix. The final few DRC's are cleared using Calibre DRC as this is considered as the signoff check for the in our design flow in Fujitsu 55-nm technology.

CHAPTER 4. SRAM SPECIAL MODES OF OPERATION – PUF AND SA TEST

4.1. Physically Un-cloneable Function (PUF) Mode

4.1.1. Overview

Physical unclonable functions are unique identification number that are derived from the complex random properties of integrated circuits. No complex circuitry is involved in generating these unique ID [Suh07]. The ID is a secret number that is generated in a way that cannot be replicated through attacks. For security purpose, the generated ID must not be accessible to the world. Historically, random number generator logic circuits are used to generate unique identity but those logics are easy to breach through reverse engineering. The idea of using CMOS manufacturing process induced mismatches in transistors has been explored and implemented [Chellapa11].

We performed the power-up read test to get the unique ID but there are certain bits that flip back and forth between each test because of balanced nature of SRAM variation that is over-powered by the noise induced in the circuit. In the SRAM here, we used the method proposed by [Chellapa16] to generate the fingerprint from SRAM bit-cells. The circuit operation does not change the normal functioning of SRAM cells.

4.1.2. PUF Circuit Design and Behavior

In the normal operation, the bit-cell's internal nodes, that is c and cn are either 01 or 10. On powerup, the cell begins in a metastable state, but shortly takes a preferred state as the power supply reaches it. The initial power-up state is influenced by the random variation and noise. With transistors that have large variation in a bit-cell, threshold substantially varied as compared to other transistors and hence the preferred state is strongly determined by such bit-cell. Both cn= 00 and

11 are unstable state for a latch configuration. In our design, we force the SRAM to meta-stable state by forcing both c and cn to logic “1” as shown in Fig. 4.1.

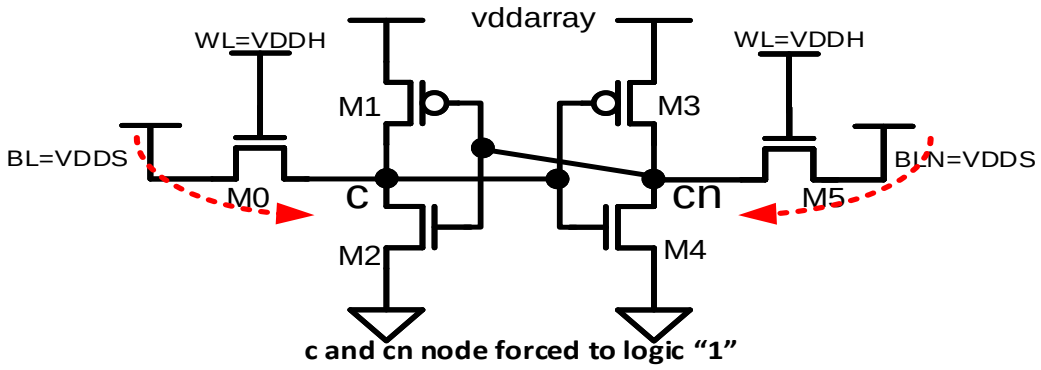

Fig. 4.1 6t-SRAM Bit-cell Condition in PUF Mode

To bring this cell to unstable state, the pre-chargers are turned ON simultaneously with the word line as shown in Fig. 4.2. The world-line enable signal wlena fires both the WL and prechn signals. It is to be noted that since the pre-charges are ON, the y-decoders are not required to be turned ON.

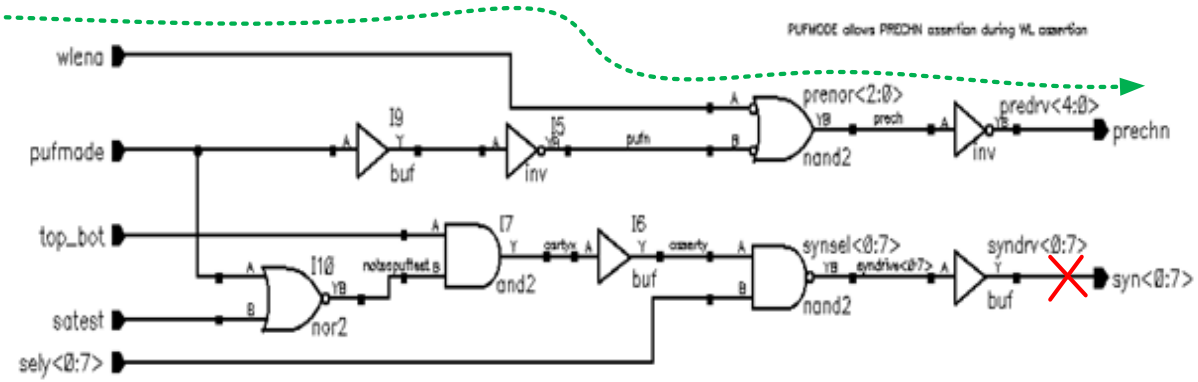

Fig. 4.2 Control Circuit Pre-Charge Enable Signal for PUF Mode.

Also, the read enable signal rdena should be high to generate the wlena signal, functional simulation results are shown in Fig. 4.3.

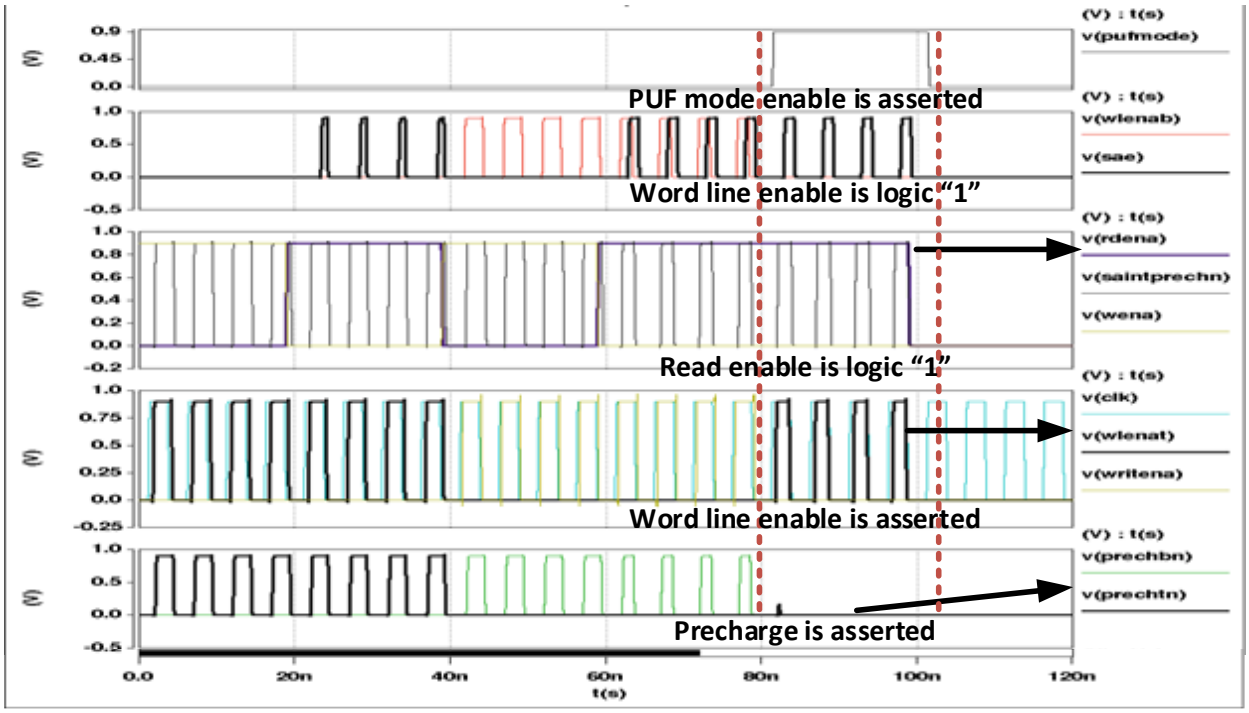

Fig. 4.3 Functional Simulation Check of PUF Mode Control Signals.

In the meta-stable cell, transistor variations cause the internal nodes (c and cn) to different voltages creating mismatch. After the cell is released from meta-stable state, the small mismatch between transistors is amplified by the feedback circuit and hence the SRAM reaches to a preferred state. It is also important to understand that certain time is required by the inverters to latch a value, this defines the wait time that should be set after the SRAM is put into PUF mode and before read operation.

4.2. Sense Amplifier Test (SA Test) Mode

We added direct measurement circuit in 6t-SRAM 16KB block to find and characterize the sense amplifier offset voltage. With this test structure, we can find the mismatches between the offset voltages of 64 sense amplifiers. In this scheme, the SRAM output through y-decoding multiplexers is blocked for sense amplifier input voltage. To find the offset voltage of each sense amplifier in 64 column groups, differential voltage is created through external direct access ports. Four analog direct access test ports are created on test chip and the port connections are further taken out to PCB.

4.2.1. Sense Amplifier Test Structure Configuration on TC25

At TC25 level, dedicated IO pads for test setup are defined, these IO ports are Spreg_clk, Spreg_addr, datx, daty, datdx and datdy; they are further directly connected to SRAM Memory Arrays ports. The Spreg_addr is a 4-bit wide address to three special registers inside SRAM Block, these registers are configured to enable control signals: satest, datmode and seldatgroup. These signals are further flopped to SRAM 1Mb and hence SRAM 16KB to enable the sense amplifier of banks. Data in to special registers is given through datain[31:0] pin.

Configuration of Special Registers in SRAM Array for SA Test mode		
	spreg_addr[3:0]	spreg_datain[31:0]
spreg_0	0000	32'h6000_FEFF
spreg_1	0001	32'h8000_0000
spreg_2	0010	32'h0000_0000

Table 4-1 Special Register Configuration in SA Test Mode

Spreg_0 register bits enable the satest and datmode. LSB 16 bits of this register are used to set sense amplifier delay. A higher value such as 16'hFEFF set the maximum delay for sense amplifier to fire. Spreg_1 and Spreg_2 register bits select the 64 column groups present in selected

bank of SRAM 1Mb block, this is shown in Table 4-1. The special registers sample the inputs for Spreg_addr at positive edge of Spreg_clk. First, these registers are configured to enable the DAT multiplexer that create differential voltage on SA and SAN. Next, the read enable signal is provided to turn on sense amplifiers to read dataout. The SRAM 1Mb samples all the signals at negative edge of clock and further pass them to SRAM 16KB banks.

The datx, daty, datdx and datdy are four additional pins on the test chip that are directly multiplexed to the 6t-SRAM banks sense amplifiers. Differential voltage signal for SA Test mode is directly supplied through these pins. The test mode operation is controlled by the circuits inside the SRAM 16KB bank. The test structure design for the offset measurement is adopted from [Clark13]. The functional operation of the direct access test circuit is further described in this chapter. Upon selection of a column group, the corresponding direct access test (DAT) multiplexer gets activated to provide inputs to sense amplifier nodes.

4.2.2. TC25 Functional Simulation for SA Test Mode

We performed functional simulation of TC25 RTL to check the intended functionality of special registers, this analysis is performed on ModelSim simulator. The collaterals required included the TC25 VHDL code, SRAM 1Mb Verilog Code, a top-level testbench and SRAM 1Mb level testbench module to send vectors to the design. In this analysis, we see that the signals configuration register input signals, shown in Fig. 4.4, are resolved to generate the control signals seldatgrp, satest and datmode which further get into the 6t-SRAM 16KB custom blocks. Separate circuit simulation analysis is performed on the custom block.

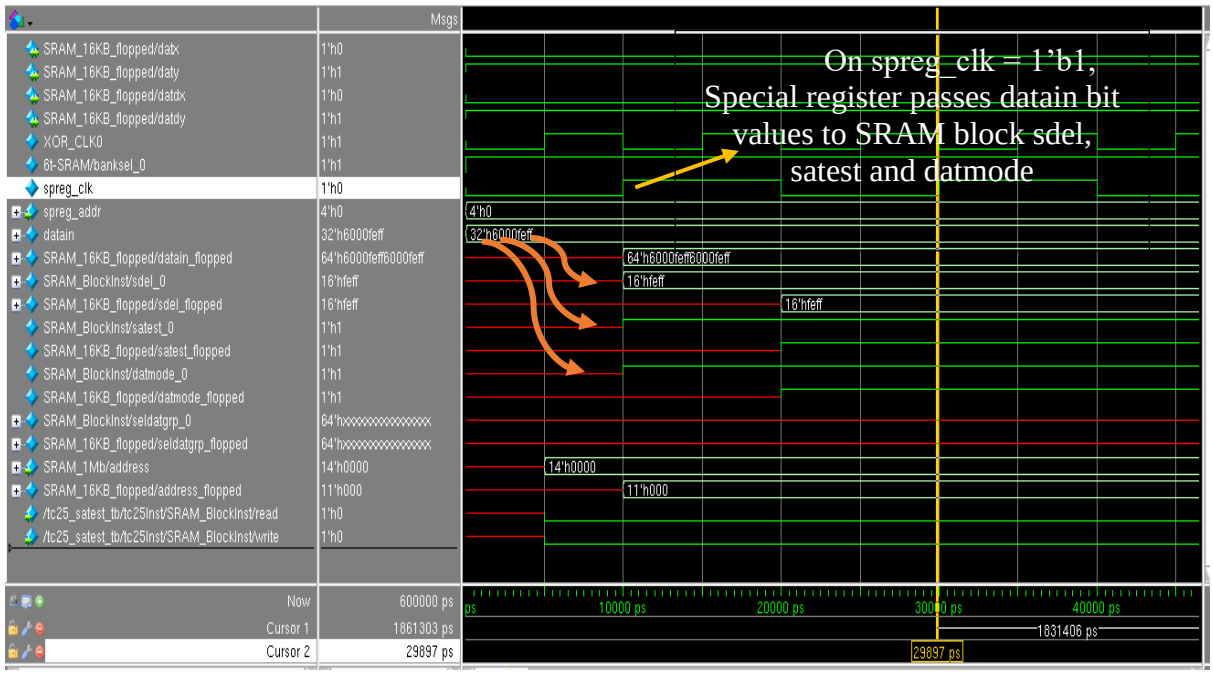

Fig. 4.4 Special Register spreg_0 and datain Decoded to sdel, satest and datmode Signals Inside SRAM Array in TC25

Similarly, we checked the decoding of Spreg_1 and Spreg_2 which generated seldatgrp signals. Later, in the post-silicon validation, this testbench is used to give signals to the SRAM.

4.2.3. Sense Amplifier Test Structure Configuration in SRAM 16KB

Inside 6t-SRAM 16KB, shown in Fig. 4.5, these signals are processed with other logic and generate enable signals SRAM column group that contain sense amplifiers and y-decoding logic. In the Sense Amplifier test mode, sense amplifier enable (sae) and pre-charge signals are controlled through satest and clock signal. The 7-to-128 x-decoders are also turned off in this test mode. This behavior is achieved by disabling the decoder word line enable circuit.

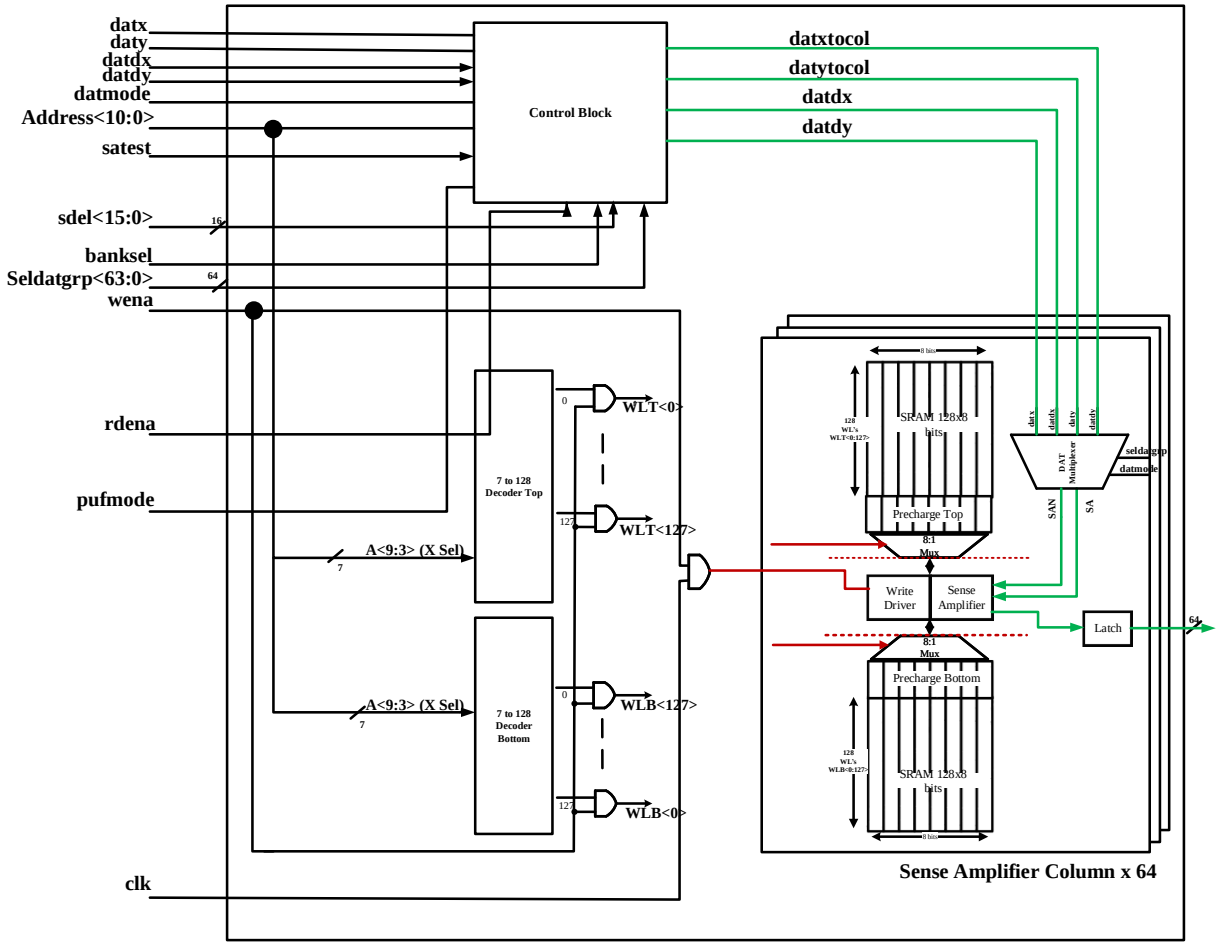

Fig. 4.5 SRAM 16KB Block SA Test Mode Data Flow Diagram

In the Fig. 4.5, the lines in red denote that the path is turned off and lines in green show active paths. This test by-passes the read and write control signals by directly enabling the sae as shown in Fig. 4.6. DAT mode data signals are propagated to only one selected bank out of 8 banks in SRAM 1Mb. Also, another mux in column groups further block/unblock the dat* signals based on the seldatgrp enable signal. To avoid leakage through column groups, only one seldatgrp is selected in a signal cycle.

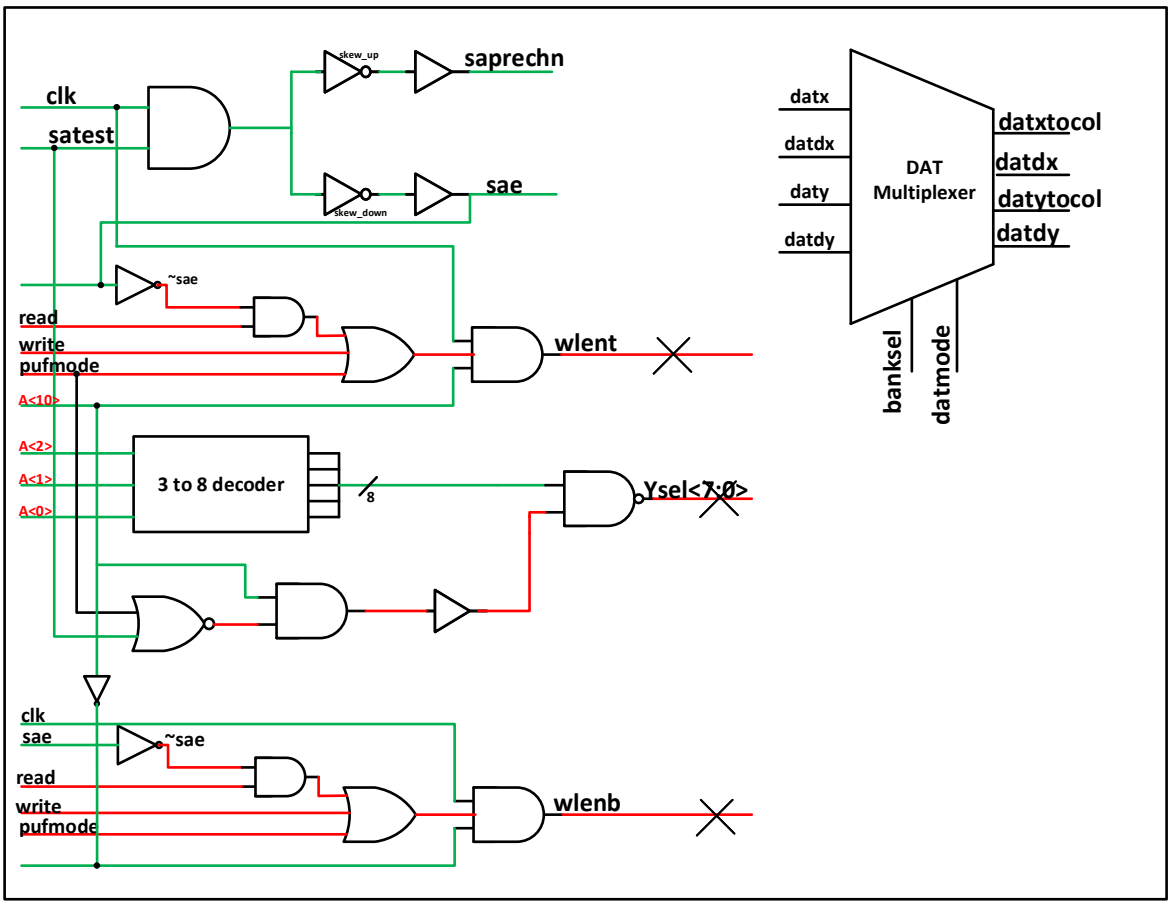

Fig. 4.6 Control Circuit and Signal Paths for SA Test Mode.

4.2.4. Circuit Behavior of Direct Access Test (DAT) Multiplexer

The DAT multiplexers, illustrate in Fig. 4.7, have two enable signals seldatgrp and datmode enable. When the enable signals are fired, the path from datx and daty to SA and SAN node open through the pass gate transistors. We have used pass gate logic to supply input voltages to the driving nodes. These SA and SAN nodes are connected to the sense amplifier input nodes, as shown in Fig. 4.7. To reduce impact of leakage generated by the previous operations, two additional pair of pass transistor gates are used.

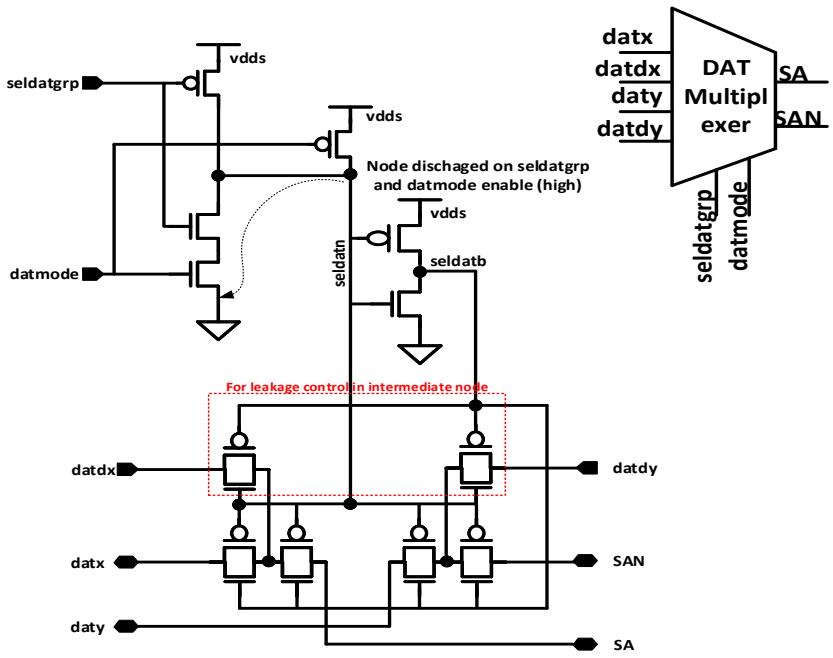

Fig. 4.7 DAT (Direct Access Test) Multiplexer [Clark13] to Set SA and SAN Nodes for SA Test Mode.

The port datdx and datdy are connected to the internal nodes of pass gates, when the circuit is non-functional, the datdx and datdy nodes are charged to known voltages equal to datx and daty, as in Fig. 4.8 . At offset of 100 mV, the signal is passed unperturbed to the sa and san nodes.

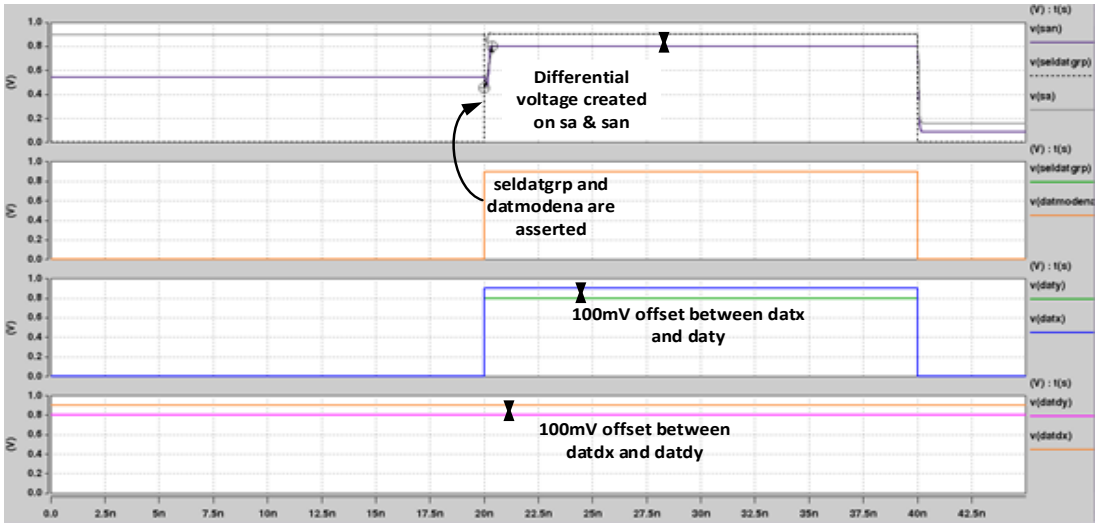

Fig. 4.8 Circuit simulation waveform of DAT multiplexer at TT corner.

4.2.5. Sense Amplifier Background and Circuit Behavior

Sense Amplifiers are primarily used in memory circuits because of their fast sensing capability to small voltage differential. By using the sense amplifier in the output reading, memory designers save read time. These amplifiers are analog circuits and hence are susceptible to mismatch. Many different approaches have been analyzed to replace sense amplifier (put some reference), but the fast sensibility to inputs is hard to achieve through alternate circuits such as latches, inverters and others.

Sense Amplifier is analog differential amplifiers i.e. it senses small differential input voltage and produces full rail. The voltage differential that it can sense depends on the gain of the input transistors. On these characteristics, amplifier needs some input different voltage that can be sensed as “high” or “low”. Once the required differential voltage is developed on inputs, sense amplifier is enabled. For this sense enabling, a tail transistor is connected at the tail end of sense amplifier as shown in Fig. 4.9**.** An enable signal called the sense amplifier enable (SAE) is input to the gate of tail transistor. The SAE signal should be fired only when the required differential is generated on the sensing nodes, otherwise it could sense wrong differential and give wrong results.

In our SRAM having dynamic read port, the bit lines are pre-charged to VDDS in every low clock phase. When the clock phase is high and read word-line gets asserted, one of the bit-line reading ‘0’ will start discharging while the other bit-line would stay at VDDS. The bit-line node is connected to the sense amplifier input terminal SA and SAN via y-multiplexers. Hence, during read a differential (offset) voltage is generated between BL/BLN and SA/SAN nodes depending upon the bit-cell being read.

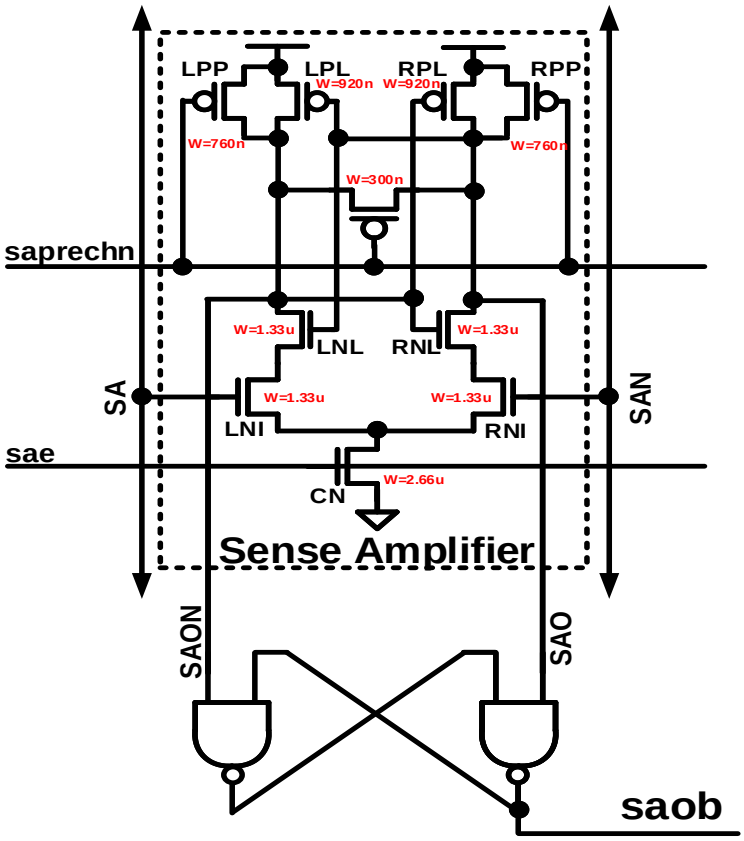

Fig. 4.9 Sense Amplifier Circuit in 6T-SRAM of TC25

The sense amplifier shown in Fig. 4.9 is a latch based circuit which has back-to-back inverters connected with the output node SAO and SAON. The functionality of nine transistors in our sense amplifier is described in Fig. 4.10.

CN: Common or the tail transistor whose gate is connected to the sae control signal LNI/RNI: Left and right nmos input pair which sense the differential voltage LPP/RPP: Left and right pmos prechargers for precharging the sense amplifier output nodes LNL/RNL: Left and right nmos pair at the output node, it is an input for the S-R latch LPL/RPL: Left and right pmos pair at the output node, it is an input to the S-R latch

Fig. 4.10 Functionality of Nine Transistors of TC25 Sense Amplifier Circuit.

The sensing transistors (LNI/RNI) and the back to back inverter circuitry (LNL/RNL and RPL/LPL) of the sense amp have higher gate length (100-nm) to enhance layout matching. The

tail transistor carries current from both the sides (LNI and RNI) and hence have higher width. In addition to the nine transistors, four more dummy transistors are used for diffusion matching. The SAO/SAON which forms the output nodes for the sense amplifier gets connected to the dynamic to static converter (S-R) latch which stores the static value for this dynamic circuit. As shown in section 2.2.3, separate signals generated by control logic are given to the precharge (saprechn) and sense amplifier enable (SAE), this is because we turn off precharge before firing sense amplifier enable (around 100 ps).

The delay between saprechn and sae is created by using up and down skewed inverters which are connected to the mux logic that generates the sadel signal as shown in Fig. 4.11, the skewed outputs have delay difference of 128.38 ps. This delay comprises of inverter delay arc difference and buffer delay.

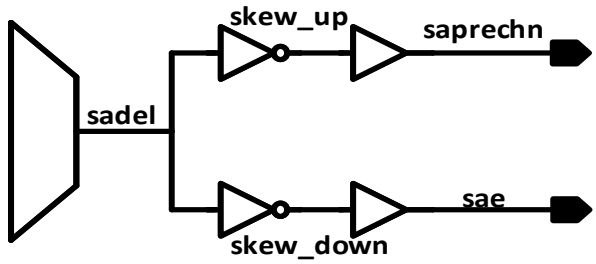

Fig. 4.11 Circuit Showing Signal Divergence for sae and saprechn with Skewed Gates

In skew_up inverter, the beta ratio (P/N) is large, in Table 4-2, to have faster P as compared to the skew_down inverter which has a slower P.

Circuit	PMOS	NMOS
skew_up inverter	1.26um	.24um
skew_down inverter	.46um	.84um

Table 4-2 Transistor Sizing for Skewed Gates.

4.2.6. Simulations of Sense Amplifier

We perform circuit simulation at TT (typical-typical) corner to check the functionality of sense amplifier with no variation element. This simulation, output in Fig. 4.12, helps capturing the delay value required to fire SAE after the saprechn node is deactivated.

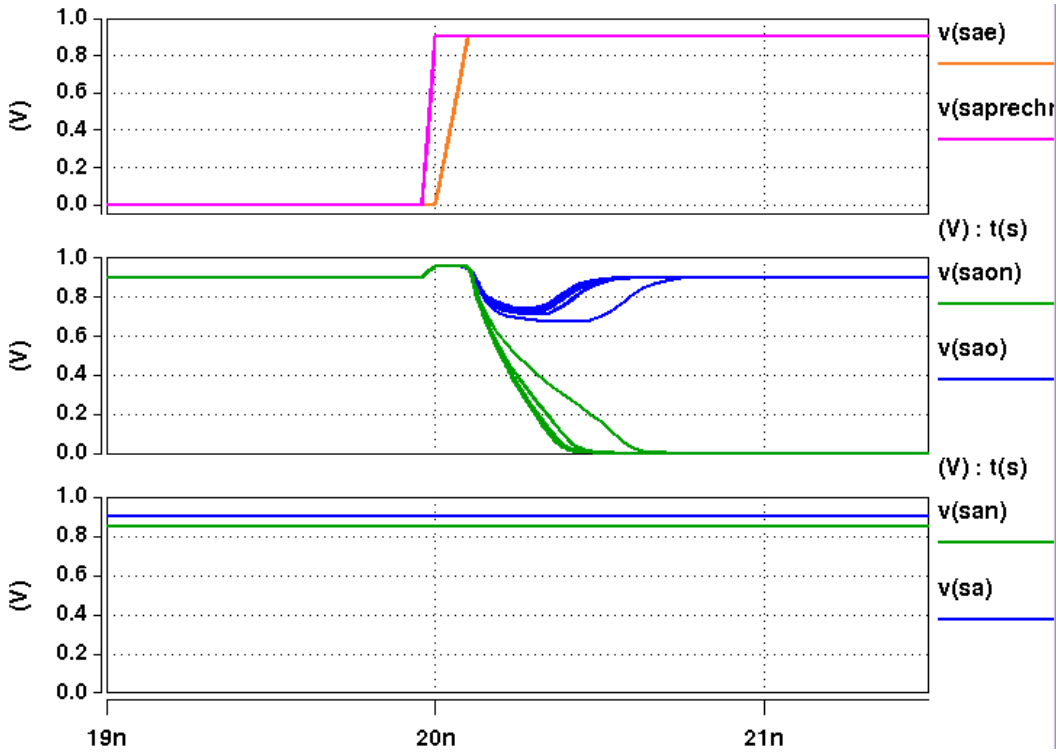

Fig. 4.12 Sense Amplifier Functional Check Waveform from Circuit Simulation. sa and san Node Offset Voltage is 50 mV, Simulation Run on TT Corner with Random Variation.

Since no variation is added to the devices, this does not show realistic behavior of the circuit rather a functional check. We performed detailed analysis with varied offset value under variation impact which is discussed in next section.

4.2.7. Monte Carlo Analysis Simulation Setup in Fujitsu PDK

Threshold variation for Monte Carlo was not inherently embedded in the previous versions of foundry PDK setup. Hence, we used the default aguass function with Monte Carlo enabled in the simulation testbench to generate the variation in threshold voltage through below method. First, the sigma delta V_{th} is calculated through the formula given in Fig. 4.13 and generate a value for threshold variation using aguass function in the HSPICE testbench to get the sense amp offset value. The calculated sigma delta Vth value is used to superimpose threshold increase on devices through the voltage dependent voltage sources.

$$\sigma(\Delta V_{th}) = A \times 1/SQRT(LxW)$$
$$\Delta V_{th} = V_{th1} - V_{th2}$$
V_{th} = Vgs when Vds=Vdd,Vbs=0 and Id/W = 0.1

Fig. 4.13 Formula for Sigma Delta Vth Calculation.

With the latest version, foundry has enabled random variation factors in the HSPICE simulation setup and has also updated the values of A_{vt} for PMOS and NMOS for all types of devices. The impact of systematic variation is not added since that at most depends on the layout of designs. We have used the embedded variation to characterize the sense amplifier offset. Initially, we performed some simulations with Monte Carlo enabled and observed that the first simulation run always has no variation added to the devices. Further, we found that HSPICE simulation deck given by foundry is created using "Monte Carlo Analysis Using the Variation Block Flow" [HSPICE14]. "Variation Block" consists of variation factor dependent equations that are introduced by manufacturing effects such as line edge roughness, random dopant fluctuation and other parameters. The different types of variations i.e. local, global and spatial can all be defined in the block. In this statistical model, only local variations are included; the simulation flow of the Monte Carlo analysis process is shown in Fig. 4.14.

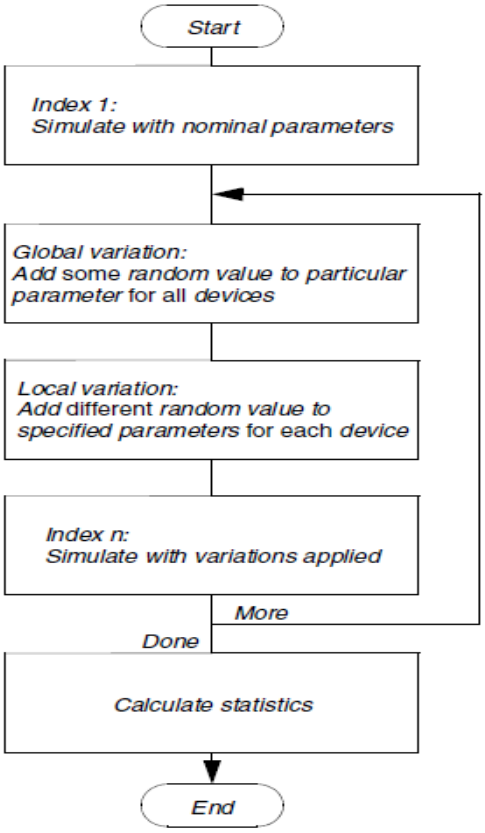

Fig. 4.14 Flow Diagram of Monte Carlo Analysis with Variation Block [HSPICE14].

Local Variations are defined as variations between devices in proximity, or with common centroid layout on the same chip; they are caused by the microscopic variations in materials and geometry, and affect different devices differently. Because of this, threshold voltage of devices varies. In differential amplifier circuit which are vulnerable to small noise, local variation impact is analyzed thoroughly for desired output measurement.

4.2.8. Circuit Simulation of Sense Amplifier for Offset Measurement

To check the Variation block behavior, we plotted the Id-Vgs curve; with different Monte Carlo runs, the Ids varies. Also, we performed a variation check with two Monte Carlo analysis results. In this check, we compared the local random variation in all devices (added by simulation

setup) for two combinations of SA and SAN used in two simulation runs. The results show that every time the simulation gets into *alter* condition, it sets same random variation values for a device. Variation in a device is same for two parallel Monte Carlo simulations for same circuit as the seed value is same. To qualify this, we have performed *gvim* file diff which confirms that for 38 different alters, the variation for devices is same, the local random variation is distributed uniformly across the Gaussian curve, in Fig. 4.15.

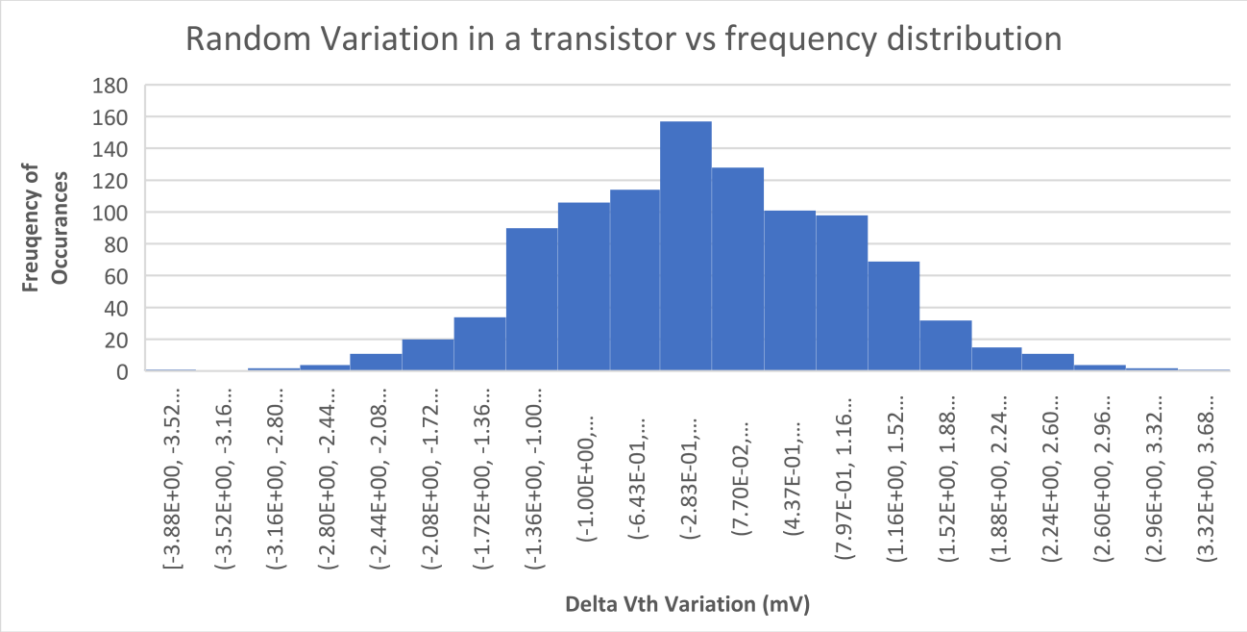

Fig. 4.15 Local Random Variation Distribution in a Transistor Across 1000 Monte Carlo Runs Performed on Circuit.

In practice, the sense amplifier offset voltage is non-zero because of random dopant fluctuations (RDF) and NBTI degradation that affect threshold voltage Vth of transistors. The differential input must substantially exceed the offset voltage to be sensed reliably; typically, the offset voltage is 50 mV [Weste05]. With technology scaling, the threshold variations and offset voltage are not changing very much whereas the supply voltage is scaled to as low as 900 mV in our design with reverse body biasing. Clearly, the offset voltage is a larger fraction of the supply

voltage, making sense amplifiers less effective [Weste05]. Also, sense amplifiers must be activated at just the right time such that the bit-lines may have developed enough voltage difference to operate reliably. If they fire too late, the SRAM is unnecessarily slow. The sense amplifier enable (SAE) is generated by control circuitry that must match the delay of address decoding and bit-line activation, as discussed in section 2.4.1. Also, bit-lines are susceptible to leakages from the other access transistors, we need to carefully consider the differential noise (capacitance) generated on the bit-lines.

Our Analysis in this section would be to characterize the sense amplifier offset voltage [Pileggi08] on Fujitsu 55 nm technology process. We would enable random variations in the transistors to include the effect of local random dopant fluctuation (RDF). These variations modify the Vth of transistors. We simulated the sense amplifier circuit with 1000 Monte Carlo samples for each of 200 SA and SAN voltage combinations.

In simulation testbench, we fix SA node to 0.9 V and provide a PWL waveform for SAN node, as in Fig. 4.16. This PWL (created from a Perl script) is swept from 0.85 V to 0.95 V across several clocked SAE cycles.

SAN PWL	
VSAN SAN 0 pwl	
+ 0	0.8
+ '3n+(40n*0)+(pw-tf)'	0.8
+ '3n+(40n*0)+(pw)'	0.801
+ '3n+(40n*1)+(pw-tf)'	0.801
+ '3n+(40n*1)+(pw)'	0.802
+ '3n+(40n*2)+(pw-tf)'	0.802
+ '3n+(40n*2)+(pw)'	0.803
+ '3n+(40n*3)+(pw-tf)'	0.803
+ '3n+(40n*3)+(pw)'	0.804
+ '3n+(40n*4)+(pw-tf)'	0.804
+ '3n+(40n*4)+(pw)'	0.805
+ '3n+(40n*5)+(pw-tf)'	0.805
+ '3n+(40n*5)+(pw)'	0.806
+ '3n+(40n*6)+(pw-tf)'	0.806
+ '3n+(40n*6)+(pw)'	0.807
+ '3n+(40n*7)+(pw-tf)'	0.807

Other Inputs
voffset = SA – SAN
voffset range (-100 mV, 100 mV, incremental step of 1 mV)
Temperature: 25C
Power Rail Voltage: 0.9 V
VBB (N well): 1.3 V
VBB (P Well): -0.4V
Period: 40ns
Rise/Fall time: 40ps
RC Corner: TT
Monte Carlo = 1000

Fig. 4.16 Offset Measurement Input SAN and Other Important Inputs.

The simulation run time is adjusted for all the sweep values, the reference Fig. 4.17 shows the input x (top) ramp up and down, and output y. The output, in Fig. 4.18, is measured at each cycle through measure statement. It can be ascertained that when the offset voltage is met, the SAO is constantly high. A Perl script generates measure statements as per no. of input voltages.

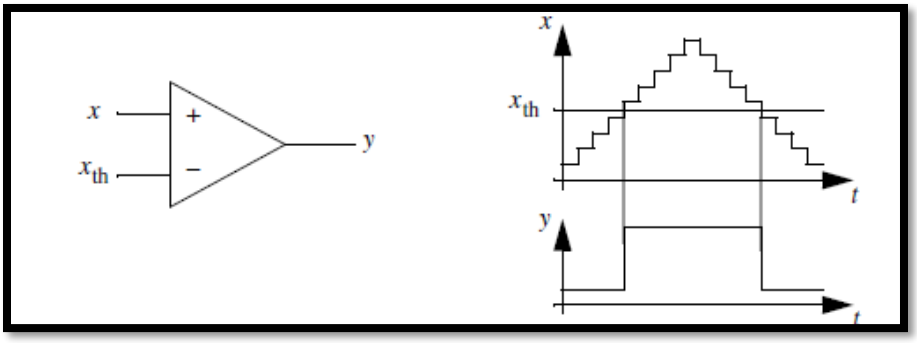

Fig. 4.17 A Methodology for the Offset-Simulation of Comparators [Graupner06]

The sense amplifier output is analyzed by post processing HSPICE results using Perl script. This Perl script generates a csv file that has sense amplifier offset voltage values for all 1k Monte Carlo variation samples.

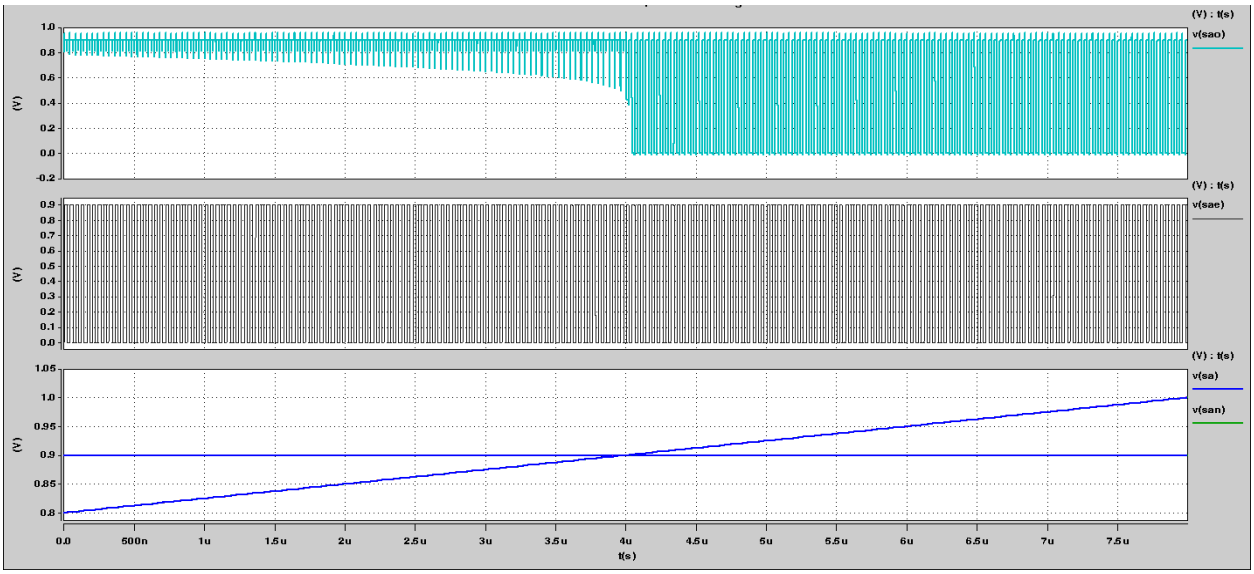

Fig. 4.18 Sense Amplifier Circuit Simulation Waveform for one Monte Carlo. SAN Swept from .8 V to 1 V and SA is Fixed.

We performed 1k Monte Carlo simulations and plotted the output on SAO node; the offset voltage distribution is further used to generate the Gaussian curve as shown in the Fig. 4.19. Also, statistics of variation and standard deviation is generated and shown in Table 4-3.

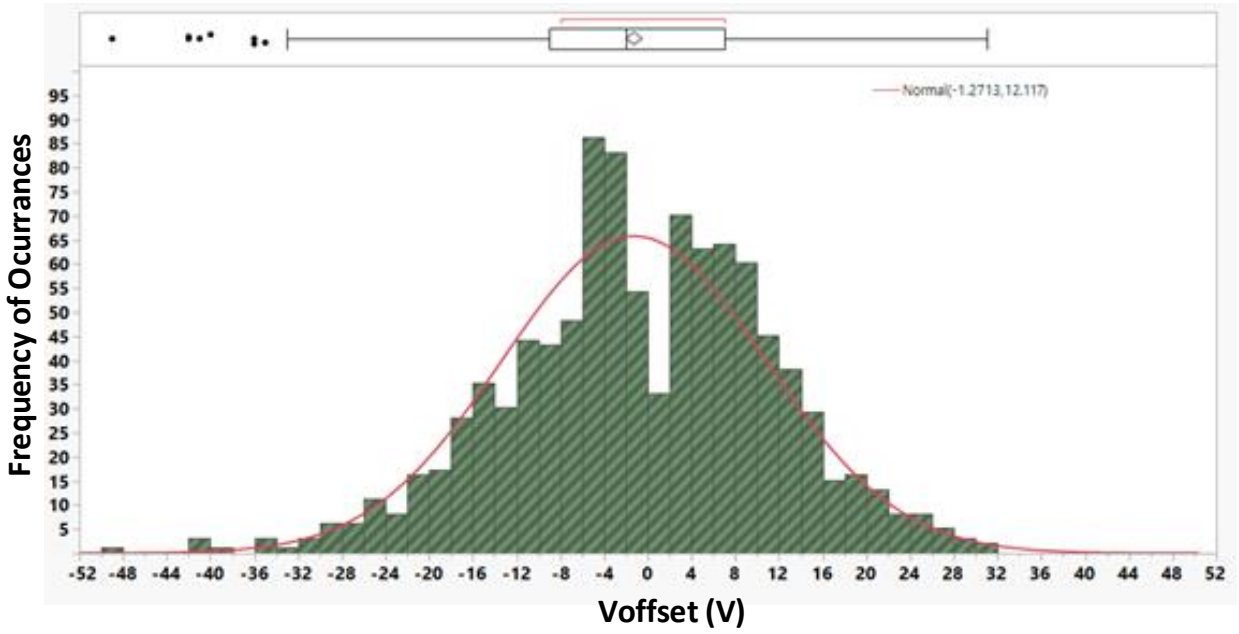

Fig. 4.19 Sense Amplifier Offset Voltage vs Frequency Distribution for 1k Monte Carlo Samples Performed on Circuit.

Statistical Parameters	**Value (mV)**
Mean	-1.27
Standard deviation	12.117
5σ voltage offset	60.585

Table 4-3 Statistical Data from 1k Monte Carlo Simulation for 200 Offset Voltages.

The output waveforms are monotonic, for two variations, we plotted the offset voltage vs sense amplifier output SAO and observe offsets at 15 mV and -1 mV, shown in Fig. 4.20.

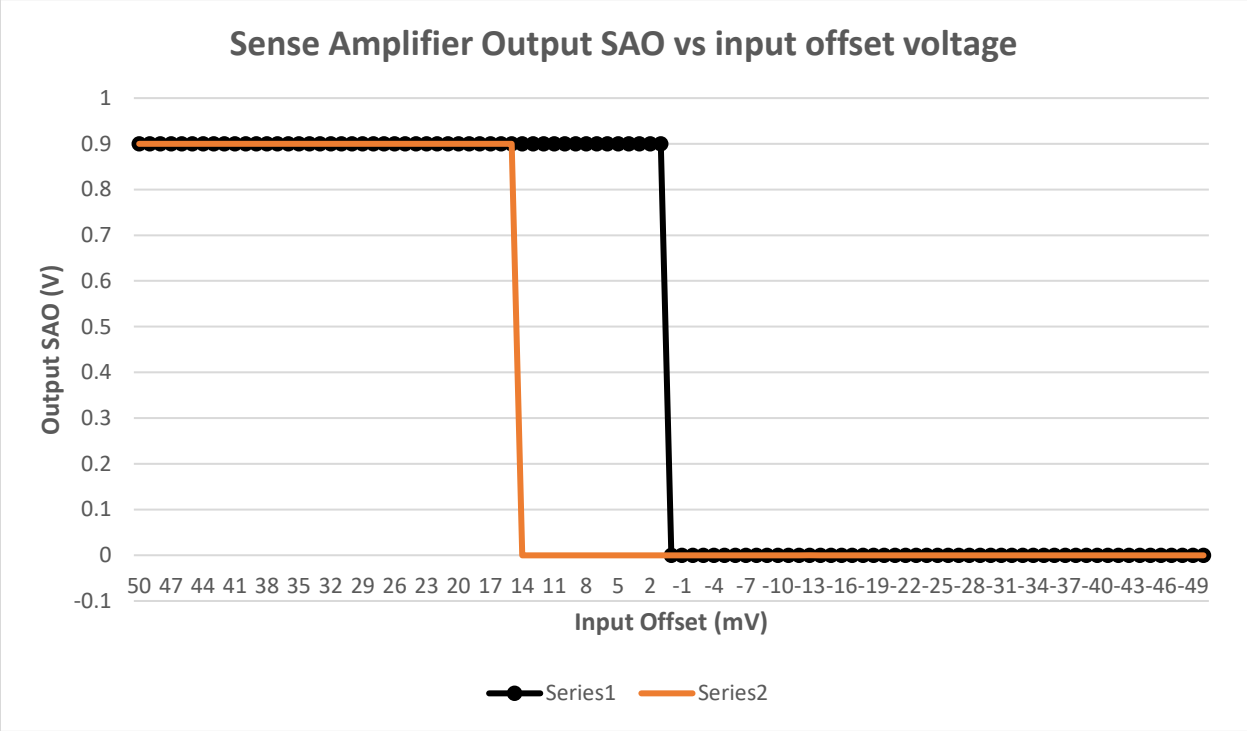

Fig. 4.20 Sense Amplifier Output SAO vs Offset Voltage with Variations in All Transistors.

CHAPTER 5. POST-SILICON VALIDATION OF SRAM NORMAL AND TEST MODE

5.1. Post-Silicon Validation Overview

Post-silicon validation of SRAM-1Mb normal and test modes was performed with the test setup shown in Fig. 5.1. The setup is created using TC25 test chip, printed circuit board (PCB), Verilog test bench, Xilinx Kintex-7 XEM7350-K160T FPGA and PC. The TC25 test-bench is implemented on FPGA which is attached to the TC25 chip through the FMC connector [reference Xilinx document]. The FMC (FPGA Mezzanine Connector) - VITA 57- is common connector design to interface large pin-counts to devices with configurable I/O. The TC25 PCB has 5 arrays of IO pin that connect to the FPGA through FMC pins as shown in Fig.5.2. The FPGA board is connected through USB 2.0 and the connections are controlled through Opal Kelly interface.

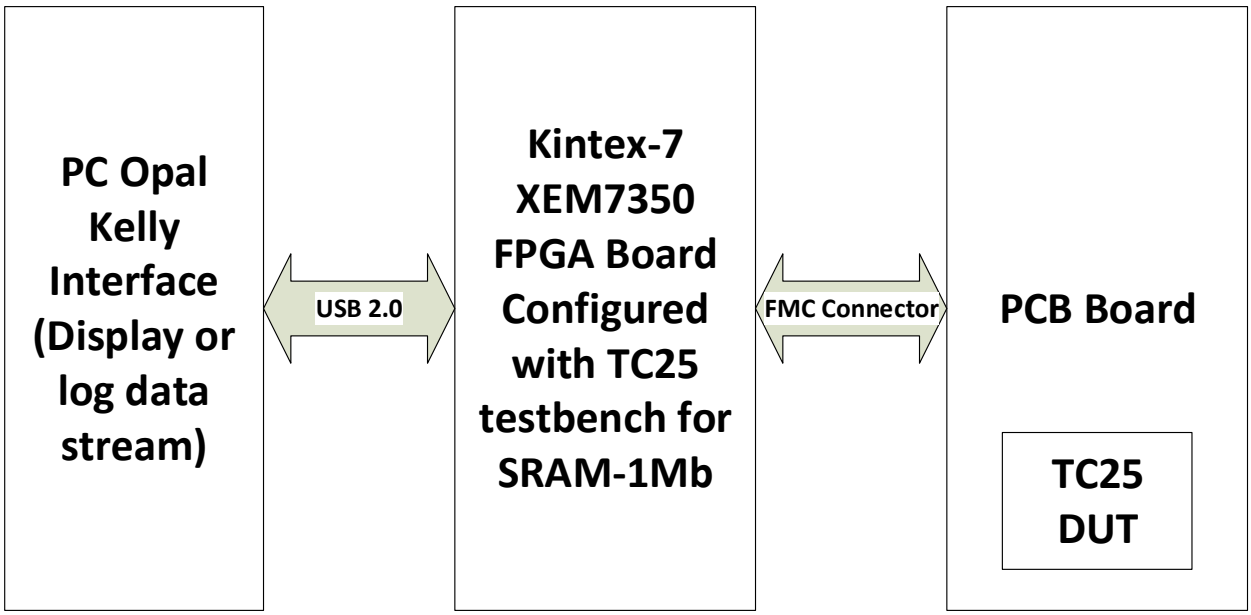

Fig. 5.1 TC25 Post-Silicon Validation Test Setup Block Diagram.

Opal Kelly interface provides Python, Java and C++ API to operate the connection from PC to FPGA through USB port. We wrote a C++ program to control and observe the binary data communication from PC to through the USB. The received data is printed and stored in log files

for further analysis. The data is controlled by a bitstream file that is called from within the C++ program.

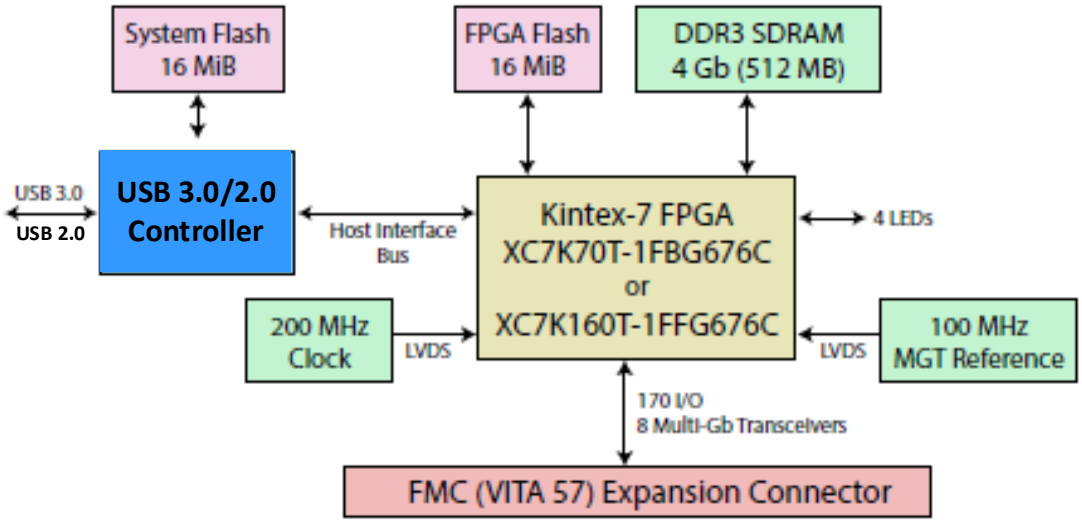

Fig. 5.2 XEM7350 Board with Kintex-7 Series FPGA Block Diagram [Xilinx14].

Fig. 5.2 shows the block diagram of XEM7350 board having Xilinx Kintex-7 FPGA. The PCB is 80mm x 70mm with four mounting holes on the corners. There are two connectors that have USB and DC power. As per the XEM7350 User's Manual, the XEM7350 has a single high pin count (HPC) FMC connector providing access to over 170 I/O, 8 multi-gigabit transceivers, and electrically-programmable adjustable voltage per the VITA-57 standard. The primary method for data communication between the FPGA and USB is through the host interface (okHost) buses. The host interface is the gateway for FrontPanel to control the design. FrontPanel connections are defined through endpoints. The USB uController data streaming is bi-directional. As shown in *Fig. 5.3*, an "In" endpoint moves data into the design while an "Out" endpoint moves data out of the design. The endpoints in a design are instantiated from Opal Kelly modules and share a common connection to the Host Interface.

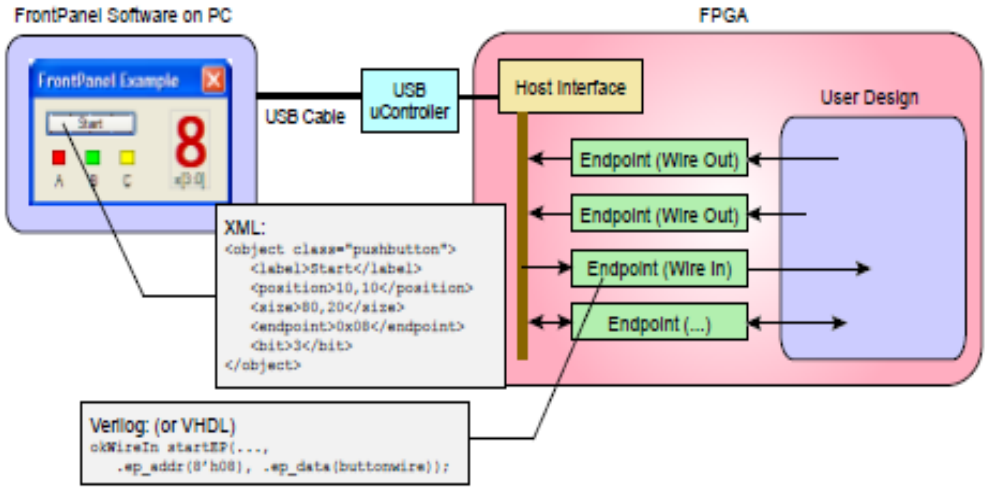

Fig. 5.3 FrontPanel GUI Interaction with FPGA [Xilinx14].

The HDL interface runs at a fixed clock rate, for USB 2.0 the operating frequency is 48 MHz (20.83 ns clock period). The Wire endpoint data bus are 16 bits wide giving a maximum burst data rate of 96 MBytes/sec.

5.2. SRAM Normal Mode Testing

The SRAM was tested for write and read operation and is found functional. We performed four tests to confirm the functionality of the SRAM. The tests included i) write and read full array with data==address, ii) write and read full array with data = ~address, iii) Write and read full array with 0s, and iv) write and read full array with 1s. In each of the tests performed, we observed expected results. Repeated tests on different corner parts resulted in expected outcomes which confirms the functionality of SRAM in silicon.

5.3. TC25 PUF Mode Testing

PUF (Physically unclonable function) of the SRAM is used to generate unique numbers/words that are used in encryption codes and identity (ID) recognition. As discussed in

chapter 4, fabrication mismatch that yield to random and systematic variation in SRAM bit-cell bring mismatch in Vth of SRAM transistors. This property makes one transistor faster as compared to other and the c and cn nodes tend to move towards a preferred state. On the TC25, PUF mode test structure is activated by enabling datain[31] for spreg_0 register. The other two special registers have all 0s value. Pseudo code in Fig. 5.4 shows the steps followed to bring the SRAM in PUF mode and read the results. We created separate test benches for each step of operation in PUF mode, these tests can each be run at different voltages; especially, we wanted to control the word line voltage VDDH in the PUF mode.

1. **SRAM_PUF_MODE_Write_Read_0s: Write and read all the locations with 0's to bring SRAM to a known state.**
2. **SRAM_PUF_MODE_LOOP_ARRAY: Enable PUF mode by configuring the special register Spreg_0 and loop through all address locations to upset them. Also, enable the read mode while the PUF mode is on. This should generate the word line enable signal.**
3. **SRAM_READ_ID: Read all the locations in 1Mb for each bit cell.**

Fig. 5.4 Pseudo-code for PUF Mode Test.

5.4. TC25 Sense Amplifier Test (SA Test) Offset Measurement

5.4.1. Test Overview

TC25 SRAM Block special registers need to be configured to enable SA Test mode. On the Spreg_clk, the special register flops are configured, bit values are previously shown in Table 4-1. Spreg_0 register bits enable the satest and datmode. LSB 16 bits of this register are used to set sense amplifier delay. A higher value such as 16'hFEFF set the maximum delay for sense

amplifier to fire. Spreg_1 and Spreg_2 register bits are used to select the 64 column groups present in each bank of SRAM 1Mb block. Upon selection of a column group, the corresponding DAT multiplexer gets activated to provide inputs to sense amplifier nodes. As per the generated differential voltage, when the sense amplifier enable signal is fired through internal circuit, the dataout is updated.

5.4.2. Test Setup

For the SA Test offset measurement, the direct access signals – mentioned in section 4.2 – are provided to TC25 chip through direct ports on board. The BNC connectors are used to connect the datx, daty, datdx and datdy ports to the power supply, the connections are checked through the multimeter.

Power supply to the "Agilent Dual Output DC Supply" is automated through ASRL6 "Measurement and Automation Explorer". It provides Perl voltage controller command libraries/modules to automate the power supply. We used those function and created sub-routines to turn on/off and change voltages on the supplies. In this test, dat* port connections and core voltage supplies are controlled. Further automation scripts are written to take multiple measurements from the test chip. Snippet of power control function to change the voltage is shown in Fig. 5.5.

```
# Turn off the power supply
write_power_supply("OUTPut OFF\n",$PortObj);
# Wait for some time
sleep (10);
# Turn on the power supply
write_power_supply("OUTPut ON\n",$PortObj);


# Set power supply 1 and 2
write_power_supply ( "INSTrument:NSELect 1\n",$PortObj);
write_power_supply("VOLTage $init_datx_voltage_power_supply \n",$PortObj);

write_power_supply ( "INSTrument:NSELect 2\n",$PortObj);
write_power_supply("VOLTage $init_daty_voltage_power_supply \n",$PortObj);
```

Fig. 5.5 Power Supply Control Measurement Commands.

5.4.3. Testbench and Results

We created automation that calls the test application executable and controls the power supply such that multiple tests are performed in one run. The SA Test mode testbench pseudo code is shown in below Fig. 5.6. The major signals for SA Test are shown as configured in the pseudo code, only MSB bits address<13:11> are important for this test as they select one bank out of the eight banks in SRAM 1Mb. The seldatgrp then selects one of the 64 sense amplifiers of measurement.

 # Set initial voltage differential -200mv

for run in $num_runs

1. **Set DAT* signals and other controlled power supply as specified**
2. **BLK_SEL = 00, SRAM_SEL=00, address<13:11>=3'b000**
3. **Send Clock to TC25 which will trigger sense amplifier. Drive the Spreg_clk**
4. **Configure Spreg_0, Spreg_1 and Spreg_2 in subsequent clock cycles to enable satest, datmode and seldatgrp control signals.**
5. **Drive Spreg_clk low.**
6. **Log the output in a file**
7. **Process the output through internal Perl subroutine call to generate dataout on each differential voltage.**
8. **Calculate the next datx and daty voltage values**

end

Fig. 5.6 SA Test Flow Pseudo-code.

The step7 in Fig. 5.6 mentioned Perl script to find the differential voltage output on dataout. This Perl sub-routine is called after every measurement such that at the end of test, dataout value is written out for each iteration corresponding to a differential input voltage.

In the initial test, we checked TT corner part with datx=0.9 V and daty=0 V for sense amplifier in column group 63 on one SRAM bank. In this case, the offset voltage i.e. "v(datx) - v(daty)" is very 0.9 V which gives good differential to sense amplifier inputs and generate desired output. The output of the test shows dataout flipping as desired on expected clock cycle. Next, we performed another 50 tests with datx= 900 mV and daty=700 mV on TT09 corner part, in this test daty is swept in a staircase manner incremented by step of 10 mV and each time the dataout is

captured. The result shows that at -40 mV the dataout starts coming out as expected, Fig. 5.7 shows the expected result.

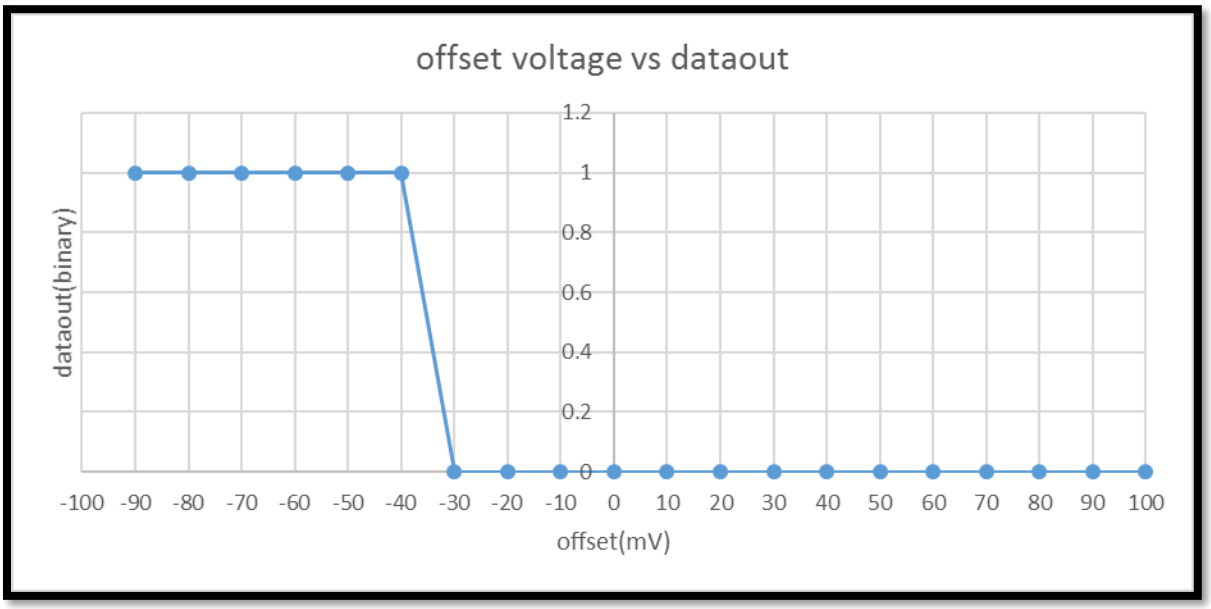

Fig. 5.7 Offset Voltage (on x-axis) vs Dataout (on y-axis) for TT10 (TT Corner) Chip.

Further, we are performing tests with other sense amplifiers in the eight banks to get the offset measurement.

CHAPTER 6. SUMMARY

The 6t-SRAM 16KB custom bank design is performed as shown in chapter 2. The control circuit is placed and routed through unique methodology which works seamlessly. In this flow, it is important to carefully generate APR tool compatible Verilog netlist. Also, it is advantageous to define the design floorplan through the top-down approach such that the relative positions of pins are fixed in the block with respect to the top level. As this flow includes two different design platforms, technology layers map files are required which should be correctly defined to avoid layer mismatches. The 16KB bank is assembled by using the decoders, control and array units, area of this block is 152x530 um^2. Section 2.4 provides details of address decode, write and read timing.

In section 3.2, the SRAM 16KB bank abstraction and characterization are described. This is performed to design the SRAM 1Mb block that uses eight 16KB banks. Also, the SRAM 1Mb RTL synthesis is discussed that generates gate level netlist and gives an estimate about the timing details and worst path based on gate delays and wire load models.

SRAM 1Mb also contains PUF and SA test structures, circuits for these modes are embedded in 16KB bank. The random variation in transistors of bit-cell are used to find a fingerprint known as “preferred state” [Chellappa16]. First, the SRAM is de-stabilize by writing logic “1” on both c and cn nodes, after waiting for some time that is required by SRAM to get to a preferred state, bit-cell is read. The circuit to configure SRAM in PUF mode is described in section 4.1.2. In the SA test mode, the sense amplifier offset mismatch analysis is performed through external differential voltage nodes; this scheme is known as Direct Access Test (DAT) [Clark13]. The internal connection of sense amplifier to the bit-lines are cut-off such that known

differential could be given to input nodes of amplifier. Offset mismatch analysis under random variation impact is performed on the sense amplifier, result shows 5-sigma variation of 60.58 mV.

Further, the SRAM-1Mb is added to the TC25 (test-chip), hence LEF file for top-level APR is generated. The TC25 is taped-out and silicon testing is performed. The silicon tests for SRAM check confirm that the normal mode of operation is functional. The tests include full array write and read with different patterns. A test-bench for PUF mode testing is written, post-silicon test-bench pseudo codes for both the tests are shown in section 5.4.3. Silicon results show both the test modes are working. For SA Test mode, preliminary tests on a column group is performed and post-silicon result is depicted.

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