High Speed Camera Chip

by

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ABSTRACT

The market for high speed camera chips, or image sensors, has experienced rapid growth over the past decades owing to its broad application space in security, biomedical equipment, and mobile devices. CMOS (complementary metal-oxide-semiconductor) technology has significantly improved the performance of the high speed camera chip by enabling the monolithic integration of pixel circuits and on-chip analog-to-digital conversion. However, for low light intensity applications, many CMOS image sensors have a sub-optimum dynamic range, particularly in high speed operation. Thus the requirements for a sensor to have a high frame rate and high fill factor is attracting more attention. Another drawback for the high speed camera chip is its high power demands due to its high operating frequency. Therefore, a CMOS image sensor with high frame rate, high fill factor, high voltage range and low power is difficult to realize.

This thesis presents the design of pixel circuit, the pixel array and column readout chain for a high speed camera chip. An integrated PN (positive-negative) junction photodiode and an accompanying ten transistor pixel circuit are implemented using a 0.18 μm CMOS technology. Multiple methods are applied to minimize the subthreshold currents, which is critical for low light detection. A layout sharing technique is used to increase the fill factor to 64.63%. Four programmable gain amplifiers (PGAs) and 10-bit pipeline analog-to-digital converters (ADCs) are added to complete on-chip analog to digital conversion. The simulation results of extracted circuit indicate ENOB (effective number of bits) is greater than 8 bits with FoM (figures of merit) =0.789. The minimum detectable voltage level is determined to be 470μV based on noise analysis. The total power

consumption of PGA and ADC is 8.2mW for each conversion. The whole camera chip reaches 10508 frames per second (fps) at full resolution with 3.1mm x 3.4mm area.

DEDICATION

To my parents

For their care and love

ACKNOWLEDGMENTS

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CHAPTER 1

INTRODUCTION

The image sensor market is experiencing rapid growth during the past decades owing to its broad applications in security, biomedical equipment, mobile phone and environmental monitoring. It is expected to reach 17.5 billion by 2020, at a compound annual growth rate of 10.30% between 2015 and 2020 [1]. Different imaging systems present different demands on the image sensor. The optical molecular imaging system, an emerging imaging application, require high speeds [2]. The image sensor which achieves over 250 frames per second or more than 1/1,000 image exposures is applied to observe the high speed phenomena or track fast-moving objects.

Most image sensors are either semiconductor charge-coupled devices (CCD) or a complementary metal-oxide-semiconductor (CMOS) type. Invented in 1969 by Boyle and Smith[3], in the last century the CCD used to be the most popular image sensor technology. However, with the development of lithography technologies, the CMOS image sensor has gradually began to dominate the market as shown in Figure 1.

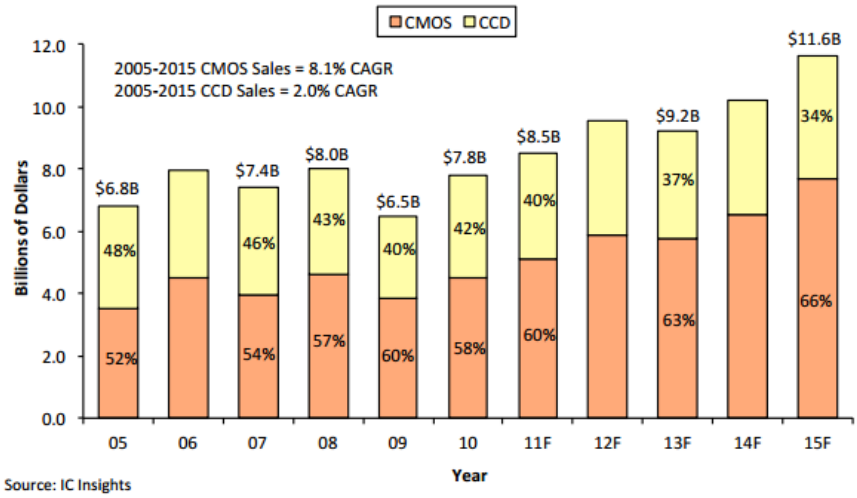


Figure 1 CMOS vs CCD Image Sensor Dollar Volumes [4].

Compared to the CCD sensor, the CMOS Image Sensor (CIS) has the advantages of lower cost, higher speed [5], higher power efficiency[6], monolithically integration[7] and ability to avoid blooming and smearing effects, which always appear in a CCD sensor. Fabricated in standard CMOS technology, the sensor is allowed to be integrated with readout and signal processing circuits at a low cost. Moreover, taking advantage of CMOS scaling, the CIS is able to achieve higher image quality, flexible functionality and better global shuttering performance because of the more transistors in each pixel. These make it possible for CIS to implement high speed image sensor with good performance.

1.1 Elements of Camera Chip

Even though applied to various imaging systems, image sensors have almost the same basic structure: (1) the pixel array, which completes the conversion from photons to electrons, (2) timing and control signals, including row and column selection circuits, and (3) the readout chain, built with analog-to-digital converters (ADC). Figure 2 illustrates the typical topology of the image sensor, which is implemented in this thesis.

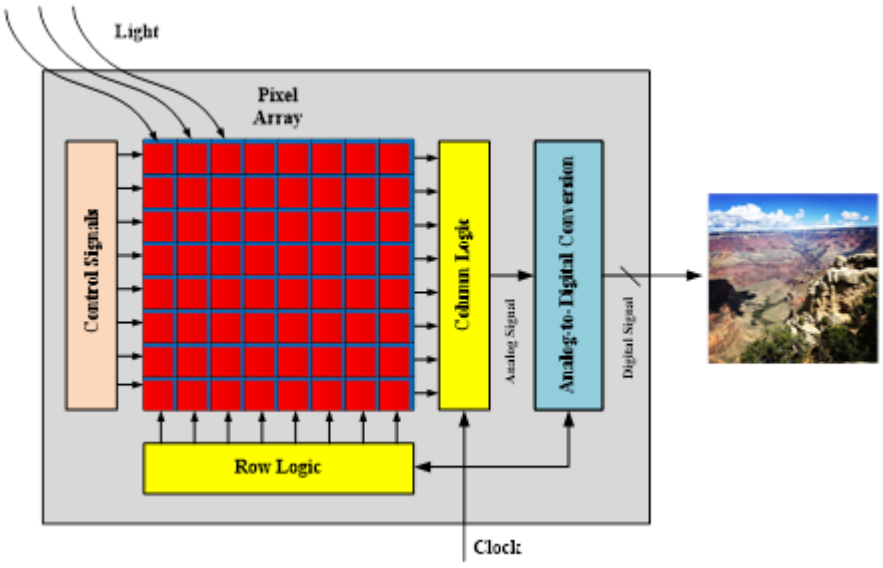


Figure 2 Typical Structure of Image Sensor

The photodiode, which located at each pixel location, is the light sensitive component. It absorbs the energy of photons or charged particles and then the transferred electrons result in the voltage drop across the photodiode with respect to the bias voltage. Other transistors in the pixel realize the function of resetting photodiode bias voltage and buffering the decreased photodiode voltage. Timing and control circuits pass the specific pixel voltage to the readout chain. The voltage is sampled and digitized through the ADC and then sent out for further processing.

1.1.1 Pixel

Pixels are divided into two types, active pixel sensors (APS) and passive pixel sensors (PPS). An APS has more transistors to buffer and amplify the signal, which solves the signal-to-noise ratio (SNR) problem of PPS. Therefore, the APS is currently the more common pixel type. There are several kinds of APS types including: photodiode, photogate, logarithmic APS, pinned diode, and capacitive trans-impedance amplifier APS (CTIA APS).

The high speed image sensor needs to provide fast image acquisition. In other words, pixels should have characteristics of no smear, no blooming and low lag [5]. As mentioned above, the CIS does not suffer from smear and blooming effects. Image lag is defined as the presence of information from previous frame [8]. Low lag is required to capture objects or phenomena when changing scenes rapidly.

The pinned photodiode APS does not produce image lag in principle. However, the large resistance of the fully depleted region will generate delay so that the charge will be left behind in diode rather than transferred [9]. The photogate APS also suffers from image lag. The capacitances of bridging diffusion have an effect on image lag, but the output is

limited to shot noise [9]. However, the image lag of photodiode APS is suppressed by both hard reset and soft reset [9]. Therefore, the photodiode type APS is the best choice for design presented in this thesis.

The photodiode APS should be reset between two frames to avoid image lag. There are two modes of reset. Rows of pixels are sequentially exposed to light and then reset from top to bottom with a rolling shutter. In global shutter mode, rows of pixels are exposed to the light and then reset simultaneously. Figure 3 depicts the operation of two reset modes.

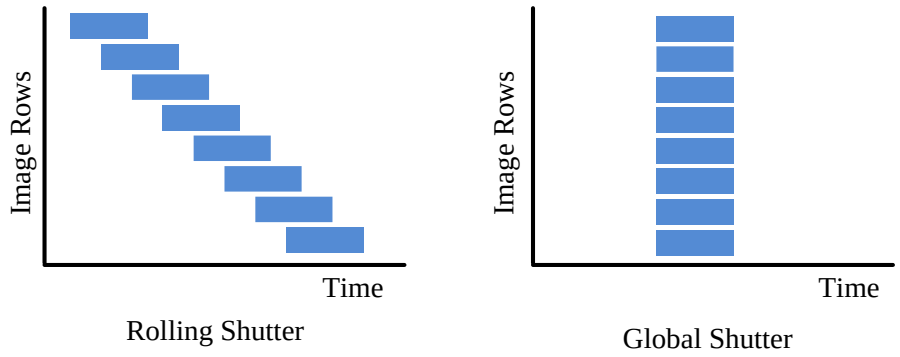


Figure 3 Rolling shutter vs Global Shutter

The rolling shutter is not appropriate for a high speed sensor since the image will change significantly during the different exposure time. The synchronized shutter helps capture images simultaneously across the array. High speed sensors require short integration time. Integration time is the time delay between resetting the row and reading the row. The integration time of global shutter is always short, but the rolling shutter can be varied [10].

1.1.2 Pixel Selection

The shift register is used to make a selection and usually only one pixel is selected each time. However, multiple pixels are often required to be selected. Summing neighboring pixels into large pixel is known as pixel binning, as shown in Figure 4. The

benefits of pixel binning are high signal to noise ratio (SNR), high frame rate and flexible resolution.

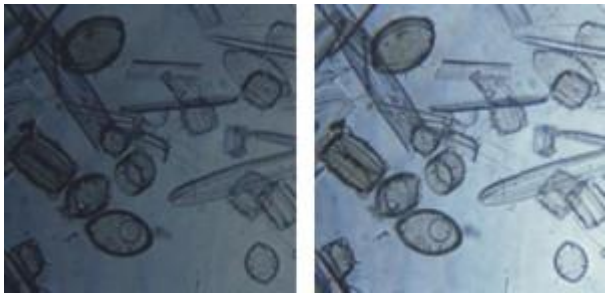


Figure 4 Full resolution vs 2x2 pixel binning[11]

Pixel binning always happens among neighbor pixels in a matrix. For a 2x2 matrix bin resolution is decrease by 2 both in x and y directions. If the image sensor has 2x3 pixel binning, the resolution is decreased by 2 in horizontal direction and by 3 in the vertical direction. Binning can be accomplished by software, especially at low-light levels [12]. For pixel binning, there is an inherent tradeoff between resolution for sensitivity. Moreover, binning support high frame rates owing to less pixel information required.

1.1.3 Readout Chain

The readout chain has different readout operation modes for exposure and reset. The frame rate is defined by how quick the readout process of whole pixels can be completed. In order to accelerate the frame rate with rolling shutter, each individual row of pixels is exposed to light after previous readout is complete. As a consequence, each row has the same exposure time and readout time, but starts at the different point, allowing for overlapping exposure. However, spatial distortion still occurs in a high speed applications even with short exposure times [10]. The rolling readout operation and global readout operation are illustrated in Figure 5.

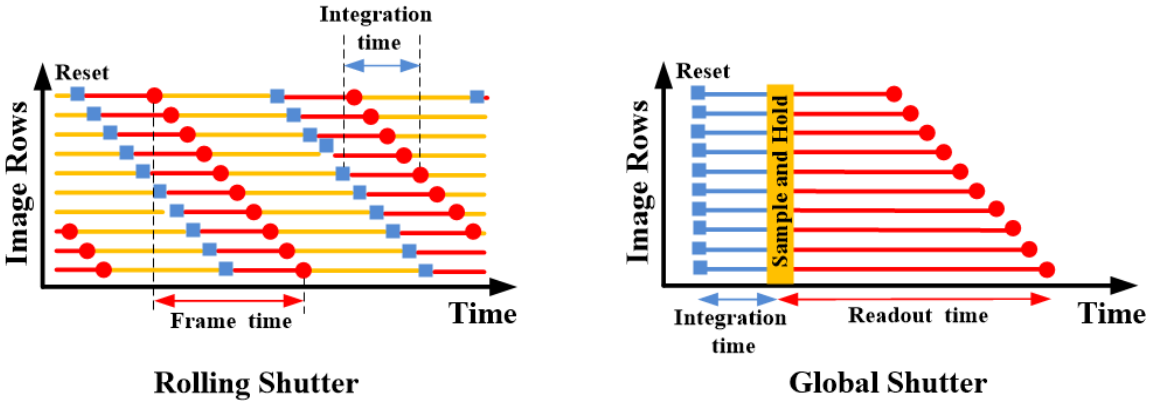


Figure 5 Rolling Readout vs global Readout

Rather than begin reading information at different time point, global shutter readout starts at the same time point and pixel information is read out row by row from top to bottom. This is beneficial for reducing the time delay across the frame, eliminating the spatial aberration and avoiding overlapping while switching channels[10]. The images of fast moving objects using two readout modes are illustrated in Figure 6. It is obvious that global readout image has better image quality while motion blur appears in rolling readout image.

Figure 6 Image of fast moving object with rolling and global readout[13]

1.2 Motivation

The high speed image sensor is very useful for our daily lives. For example, for automotive applications it is able to realize collision avoidance [14], crash observation [15], airbag control [16] and pre-crash sensing [17]. Human beings are much safer during the trip when their vehicle is being continuously monitored. Life science also needs high speed

image sensors [18-20]. Fast biological activities, such as muscle contraction, can be observed and analyzed through high speed imaging. As for industry, high speed sensors helps investigate the manufacturing process that cannot be seen by eyes, such as fluid or gas flow [21]. Moreover, the most common applications, TV and broadcasting system, use high speed image sensors to provide ultra-slow motion of some activities that cannot be tracked by eyes. People must be familiar with the Hawk-Eye in tennis and bullet time in the movie "the Matrix."

Several high speed image sensors have been reported since last century. A 128x128 photogate CMOS image sensor with 0.5μm process was reported in 1998 [22]. The frame rate reaches 400 per second and the exposure time is 75μm. N. Stevanovic and M. Hillebrand proposed a high speed CMOS camera in 2000 [23]. More than a 1K frame rate is achieved and a global shutter is implemented in each pixel. A 48K frame rate CMOS image sensor for real-time 3D sensing and motion detection was reported by Yoshimura, T. Sugiyama, K. Yonemoto and K. Ueda in 2001[24]. A 192x124 pixel array with 12bits digital output was realized. Since then, the pixel array density and readout speed has continued to improve.

A 128x128 pixel array with 1620 frame rate was developed in 2005 by Yukinobu Sugiyama, Munenori Takumi, Haruyoshi Toyoda, [25]. It was able to capture the image of a moving car at speed of 144km/h. In 2007, Masanori Furuta, Yukinari Nishikawa, and Toru Inoue reported an image sensor with 512x512 pixels [26]. The chip was fabricated in 0.25μm and reached 3500 frame rate. A high speed, 1300fps, 3.7M pixel CMOS image sensor(5 Gpixels/s) was proposed in 2015 [27]. The readout rate was improved by the novel

readout circuit with slew enhancement and a combination of interleaving and correlated double sampling (CDS) techniques.

Table 1 summarizes the performance of the different CIS designed mentioned above. It is seen that high speed image sensors often have a low fill factor. Fill factor represents the effective photosensitive area in each pixel. High fill factor has the ability to detect the low light signal. This thesis presents a high speed CMOS image sensor design with high fill factor and resolution. The chip is fabricated in a 0.18μm CMOS process.

Table 1 Summary of Image Sensors

REF	**TECH**	**Frame Rate fps**	**Array Size**	**Pixel Area**	**FF**	**Chip Area**	**ADC bits**	**Power**
[24]	0.35μm	48.8k	192x124	46.4μm x 54.0μm	25%	11.98mm x 9.24mm	12b	1.6W~2 W
[25]	0.6μm	2.4k	128x128	20.0μm x 20.0μm	44%	13.0mm x 14.3mm		450mW @125 fps
[26]	0.25μm	3.5k	512x512	20.0μm x 20.0μm	40%	17.0mm x 12.0mm	12b	1W @3.5k fps
[27]	0.15μm	1.3k	2560 x1440	6.0μm x 6.0μm		15.3mm x 8.6mm	8b	
This Work	0.18μm	10.5k	96 x 96	20.0μm x 20.0μm	64%	3.4mm x 3.1mm	8b	

1.3 Organization

Chapter two introduces the individual pixel circuit used in this thesis. Noise sources and techniques for eliminating noise are analyzed. The details of the10T architecture and performance are presented. The simulation results demonstrate that the pixel circuits have high filler factor, high speed and low leakage. Chapter three discusses the pixel array structure and shift register applied for this design. The basic components of the shift register are discussed. Chapter four focuses on the readout chain. Different levels of

readout chains are discussed first. The column level readout chain including a programmable gain amplifier (PGA) and an analog-to-digital converter (ADC) is demonstrated as the best choice. Each element of ADC and PGA is analyzed first and then comes to the system level consideration. The post-simulation results show that the readout chain is able to achieve high dynamic range, high speed, high resolution and low power. Finally, chapter five gives some suggestions and new method to improve the performance.

CHAPTER 2

The Pixel

The pixel plays an important role in the image sensor. It determines the image quality. Chapter two focuses on analyzing the pixel.

2.1 Photodetector

The photodetector is the component that detects the light. According to Einstein's photoelectric effect, electrons are generated through ionization when a photon hits the semiconductor material. The accumulated electrons represent the light density. Most CIS use a photodiode as a photodetector.

The PN junction is the core structure of the photodiode, shown in Figure 7. When the energy of a photon is greater than bandgap energy of silicon (1.1eV), the photon is absorbed by PN junction. Then it produces an electron-hole pair (EHP). The number of EHPs is controlled by the photon flux density. EHPs created far away from depletion region are likely to be recombined owing to the low field there. If they happen to be created close to or in the depletion region, the inner electric field forces electrons and holes to separate. Holes will transport towards the p-type regions and electrons toward the n-type regions. The transport of EHP is what constitutes photocurrent. The wider the depletion region is, the more photons are collected, hence the PN junction is always reversed biased for the image sensor.

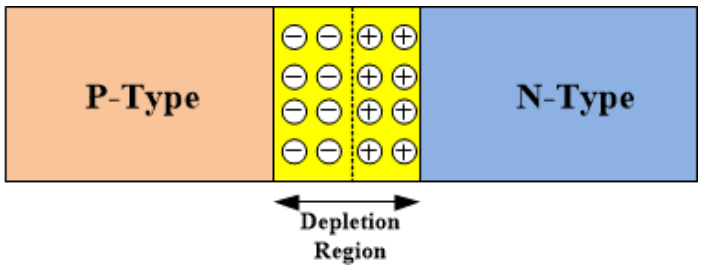


Figure 7 PN Junction

The most important parameters for the photodiode are quantum efficiency and dark current. When a photodiode is not exposed to light, there is still relatively small current flowing through it, which is defined as dark current. Quantum efficiency is as associated with the percentage of incident photons that contribute to the photocurrent. High quantum efficiency and low dark current are the essential conditions to obtain a high performance photodiode.

The light power absorbed in depletion region is described in terms of incident light power, P_0

$$P(w) = P_0\,(1 - e^{-\alpha_S(\lambda)w}) \tag{1}$$

where absorption coefficient $\alpha_S(\lambda)$ is the function of input wavelength and w is the width of the depletion region. The primary photocurrent is written as

$$I_P = P_0(1-e^{-\alpha_S(\lambda)w})(1-R_f)\ \frac{q}{hv}, \tag{2}$$

where h donates Plank's constant and R_f is entrance face reflectivity. The ratio of photocurrent to incident light power at a certain wavelength, R_λ, is defined as the responsivity of the photodiode, which quantifies its sensitivity to light. Quantum efficiency is expressed as

$$Q.E. = \frac{R_{\lambda\_observed}}{R_{\lambda\_ideal}} = \zeta(1-e^{-\alpha_S(\lambda)w})(1-R_f), \tag{3}$$

where ζ is the fraction of electron-hole pairs that contribute to the photocurrent.

A low reflection coefficient at the surface of the photodiode is required to attain high quantum efficiency. It can be realized by applying special dielectric coatings. The absorption coefficient is related to input wavelength and is an intrinsic quality of photodiode material. Due to the standard CMOS process, there is nothing much that can

be done to improve absorption coefficient.

Dark current of a photodiode under reverse bias is expressed as

$$I_d = I_{SAT}(e^{\frac{qV_A}{k_B T}} - 1), \quad (4)$$

where I_{SAT} is the reverse saturation current, V_A is the bias voltage, k_B is Boltzmann's constant and T is absolute temperature.

Dark current is mainly generated from two sources. The first source of dark current is the random generation of carriers which result from either thermal generation or random arrival of photons. The first source depends on the doping level, bandgap and temperature [28]. The second source of dark current is defects typically found near material interfaces. The second source is determined by the shape of the photodiode layout, cross section structure and the fill factor[29]. Therefore, operating at low temperature, smaller photodiode size and removing collection areas from interfaces are useful in reducing dark current.

2.2 Speed and Noise Analysis of Photodiode

The photocurrent discharges the photodiode capacitance that has been set to the reference voltage. The voltage drop depends on the junction capacitance and photocurrent, which is function of the light density. Swe and Yeo [30] presented the model of photodiode, which is shown Figure 8. R_s is the series resistance from the contacts and the undepleted silicon. R_j is the junction resistance that changes with photocurrent. C_{PD} is the junction capacitance. The diode is the PN junction and I_P indicates the photocurrent.

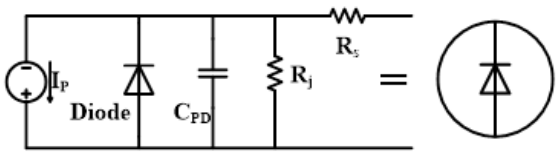


Figure 8 Model of Photodiode

The response speed of the photodiode is defined by how fast the generated EHPs are extracted as the output current. It is usually expressed as the rise time t_r for the output current from 10% to the 90% of peak value. The rise time is related to three time factors, RC delay time from the junction capacitor and load resistor, t_{RC}, diffusion time, t_D,and carrier transit time, t_C, in depletion layer. The rise time is expressed as

$$t_r = \sqrt{t_{RC}^2 + t_D^2 + t_C^2}, \tag{5}$$

where, t_{RC} equals to $0.7\pi C_j R_L$. The junction capacitor C_j is proportional to the photodiode area A and inversely proportional to the depletion layer W. It is calculated as

$$C_j = \frac{\varepsilon_{si}\varepsilon_o A}{W} = \frac{\varepsilon_{si}\varepsilon_o A}{[2\varepsilon_{si}\varepsilon_o \mu\rho(V_{bi}+V_A)]^{1/2}} = \frac{C_{j0}}{(1-\frac{V_A}{V_{bi}})^{1/2}}, \tag{6}$$

where ε_0 is the permittivity of free space, ε_{si} is the silicon dielectric constant, μ is the mobility of the electrons at 300 K, ρ is the resistivity of the silicon, V_{bi} is the built in voltage of silicon and V_A is the applied bias. It is seen that the capacitance varies with voltage, which is shown in Figure 9. C_{j0} is 297fF if the depletion layer is 100nm with an area of 18.2μm x15.5μm.

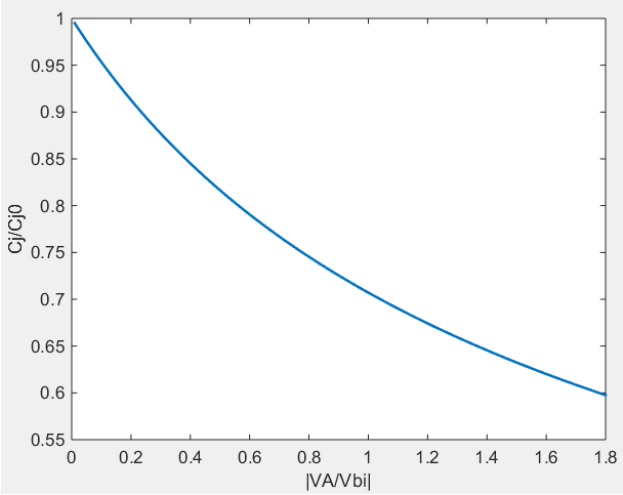


Figure 9 reverse bias vs junction Capacitance

The diffusion time and carrier transit time are expressed as

$$t_D=d^2/2D \qquad t_C=W/v_d\,, \tag{7}$$

where d is distance, D is the minority carrier diffusion coefficient, W is depletion layer width and v_d is mean drift velocity. The electron diffusion time through 10μm silicon is 8ns and the transit time across the 1μm depletion layer is around 10ps. A low rise time is required by the high speed application. Based on the discussion above, the diffusion time mechanism should be eliminated and the load resistance should be minimized.

The main noise sources for the photodiode are shot noise and Johnson noise. Shot noise is determined by fluctuations in the stream of electrons in the material [31]. Johnson noise is caused by the thermal fluctuation on conducting materials, such as shunt resistance and series resistance of the device and load resistance [32]. The equivalent circuit model of the photodiode is shown in Figure 10.

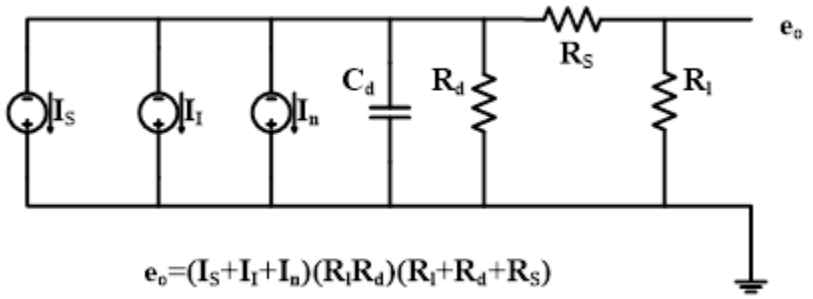


Figure 10 equivalent circuit model of photodiode

In Fig. 10, I_S is the signal current, I_I is the leakage current and I_n is the noise current. C_d represents diode junction capacitor, R_d stands for diode parallel shunt resistor, R_S is diode series resistor and R_l represents load resistor.

The shot noise and Johnson noise are given as

$$I_{Shot}=(2eI_dB)^{1/2}, \tag{8}$$

where I_{shot} is shot noise current, e is electron charge ($1.6*10^{-9}$ coulomb), I_d stands for the dark current(A) and B is the bandwidth(Hertz)

$$I_{Johnson}=\left(\frac{4k_BTB}{R}\right)^{1/2}. \quad (9)$$

Here $I_{Johnson}$ is Johnson noise current, k_B is Boltzmann constant ($3.8*10^{-23}$JK), T represents the absolute temperature(K), R is the resistance giving rise to noise(Ohms) and B is the bandwidth(Hertz).

If the photodiode operates at low frequency(~1Hz), the flicker noise dominates. Flicker noise is caused by fluctuations of the surface recombination velocity and bulk carrier mobility. It is related to the current as well as the mechanism that generates the current. The power spectrum of flicker noises is,

$$S_{I/f}(f)=a\frac{i_{dc}{}^{C}}{|f|} \text{ for } |f| \in [f_{min}, f_{max}], \quad (10)$$

where $0.5 \leq c \leq 2$, a is the constant value that is set by physical properties of the diode.

The total noise current is the root mean square sum of the individual currents, which determines the minimum detectable light power. It is expressed as

$$I_n^2=I_{Johnson}^2+I_{shot}^2=2eBI_d+4k_BTB/R_L=P_{min}^2R_\lambda^2. \quad (11)$$

Suppose silicon PN junction has 0.05 nA dark current, 25 MHz bandwidth, 0.55 A/W responsivity with 300K operation temperature and 1K Ohms load resistor. Then the minimum detectable light power is calculated as 6.139×10^{-8}W.

In a real CMOS Image Sensor noise is time variant. It is not accurate to apply the noise model directly to the circuit. Therefore, using the time domain noise analysis is more appropriate This is not discussed this thesis.

2.3 Pixel Architecture and Operation

The typical pixel circuit for a high speed image sensor is displayed in Figure 11[33]. It uses global shutter and achieves high sensitivity.

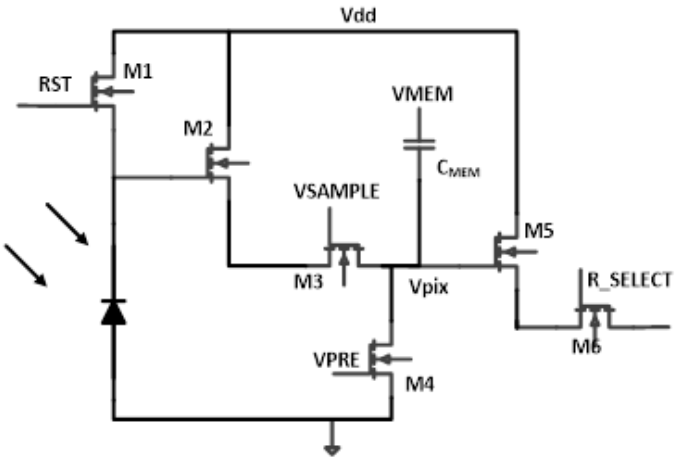


Figure 11 6T pixel circuit

When the reset transistor is turned on, the photodiode is pre-charged to a reference voltage. It always reaches VDD-V_{TH}. Then the reset transistor is turned off and the pixel is exposed to the light during the integration time. The photon generates the EHP and a photocurrent is generated. The photocurrent is proportional to the absorbed photon flux. The voltage at the cathode of photodiode decreases as the photocurrent goes through. At the end of integration time the readout signal is obtained and then sampled in the C_{MEM} capacitor. The C_{MEM} capacitor holds the value until the voltage signal is read out. The readout operation is controlled by the row select and column select signal. The timing of the control signals for pixel operation is shown as Figure 12.

The sampled voltage value should be stored on the C_{MEM} capacitor until it is read out. Therefore any current through the C_{MEM} capacitor before readout will have an effect on the image quality. The most important current paths are depicted in Figure 13.

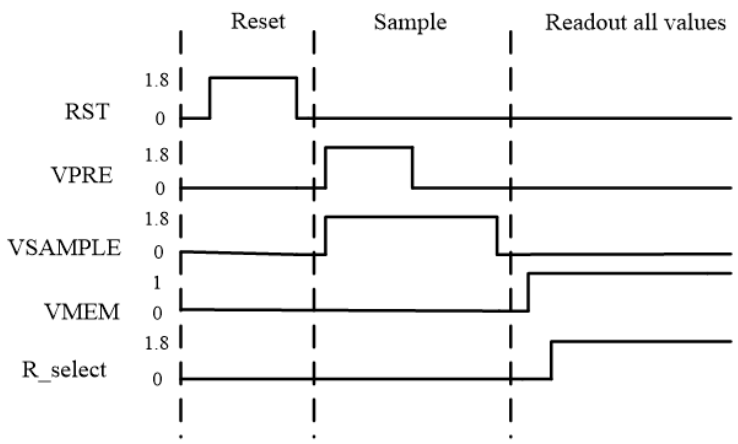


Figure 12 Timing of control signals for pixel

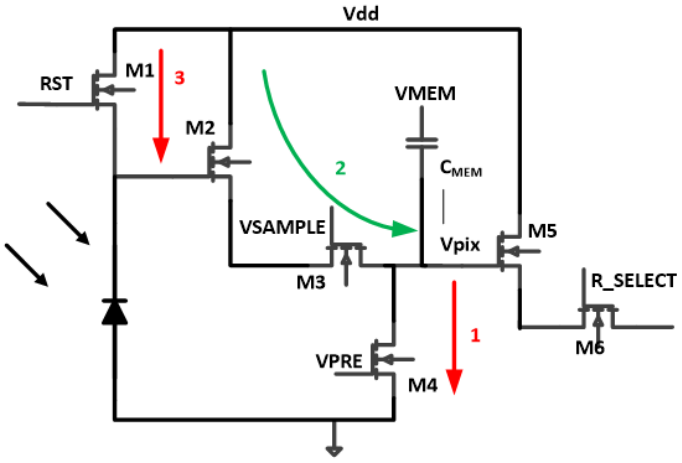


Figure 13 Leakage paths in 6T pixel circuit

Subthreshold current will occur through precharge switch, sample switch and reset switch. The first two switches are directly connected to the C_{MEM} capacitor and the third one is indirectly related to the voltage value. Moreover, the precharge switch decreases the voltage value and reset switch and sample switch increase the voltage value. The subthreshold current of transistor makes it difficult to detect accurate light signal and thus decreases the image accuracy. Therefore, reducing subthreshold current is one of the crucial tasks discussed in this thesis.

2.4 Pixel Design and Layout

Based on the discussion above , the four transistors are added to meet the requirements. These new devices are displayed in Figure *14*.

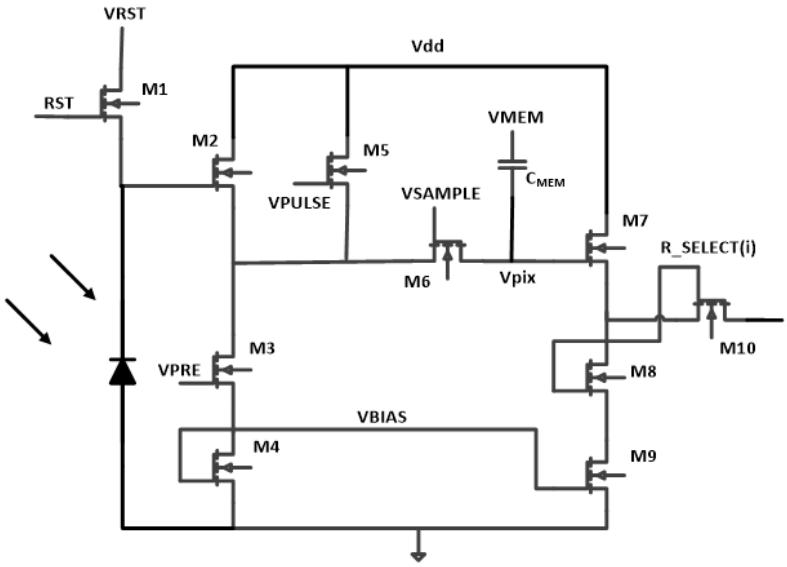


Figure 14 10T pixel circuit

The pixel is reset by turning on the transistor M1. In order to avoid image lag, the VRST is set to zero at first, forcing the voltage across the photodiode to be zero. Then, the VRST goes up to 1.8V, forcing the voltage across the photodiode to be 1.8V-V_{TH}. The V_{TH} is determined by the transistor M1. Once reset operation is completed, M1 is turned off by pulling down the RST signal. The photodiode is reverse biased now. Then the pixel is exposed to the light and the photocurrent starts to discharge the photodiode. At the end of the exposure time, the voltage across the photodiode is denoted as V_{PD}. The voltage difference (1.8V - V_{TH} - V_{PD}) represents the light signal. This means two operations are needed to obtain the light signal: the reset operation and the sample/readout operations.

The sample operation of the pixel is explained below. The VSAMPLE and VPRE signals go high first to deliver the voltage value of a photodiode to sampling capacitor, C_{MEM}. The source follower M2 drives the voltage of sampling capacitor V_{PIX} to V_{PD} - V_{TH}.

Owing to the threshold voltage loss in the second source follower M7, the V_{PIX} should be increased to improve the signal swing. Thus, after the VSAMPLE is pulled down, the VMEM is activated to enhance the dynamic range of readout circuit. What is more, the VPULSE signal is applied at the same time to minimize the effect of subthreshold currents.

The readout operation is controlled by the row select signal, R_select (i). Typically, only one of the row select signals is high at one time. It should be low before the VMEM ends. The period of the row select signal depends on the speed of readout chain, the number of pixel columns and number of readout chain.

The timing of eight control signals: RST, VRST, VMEM, VSAMPLE, VPULSE, VPRE and R_select (i) are shown in Figure 15.

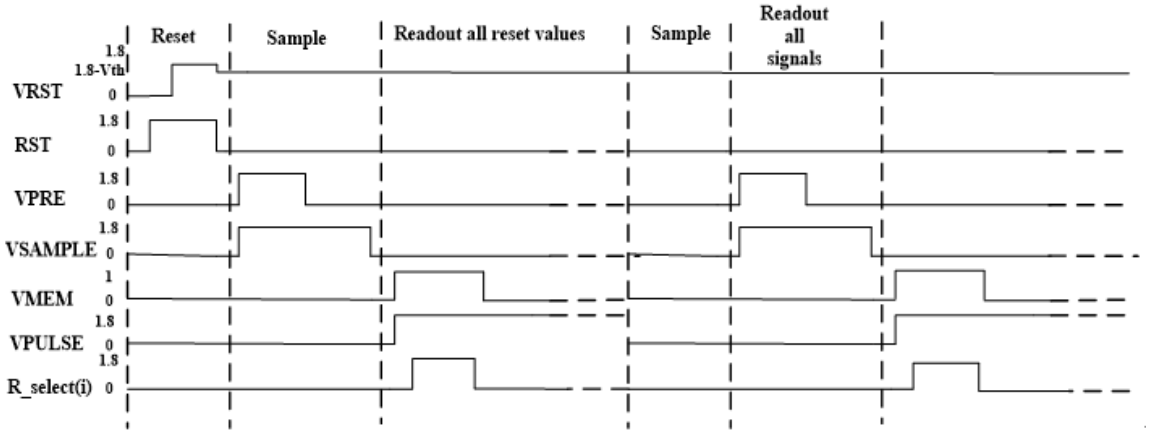


Figure 15 Timing diagram of eight control signals

Similar to the 6T pixel circuit, a 10T pixel circuit also has multiple current paths that that impact the charge on C_{MEM}, shown in Figure 16. As discussed above, the subthreshold current of the transistor is the main source of these current paths. The drain current of subthreshold region is expressed as

$$I_D = I_{D0}\frac{W}{L}e^{V_{gs}/nV_t}(1-e^{-V_{ds}/V_t}) \qquad (12)$$

where $V_t = kT/q$, $n = (C_{ox}+C_{depl})/C_{ox}$ and $I_{D0} = \mu_n C_{ox}(n-1)V_t^2 e^{-VTH/(nVt)}$. Based on this equation,

there are three methods to reduce the subthreshold current, decreasing gate-source voltage, drain-source voltage and transistor size. The subthreshold current of minimum size N type MOSFET is shown on the simulation results in Figure 17. The figure shows that the subthreshold current is reduced by more than 90% with a -0.2V gate-source voltage compared to zero gate-source voltage. Besides, when operating at the same gate-source voltage, the subthreshold current of lower drain-source voltage is much smaller than that of higher drain-source voltage.

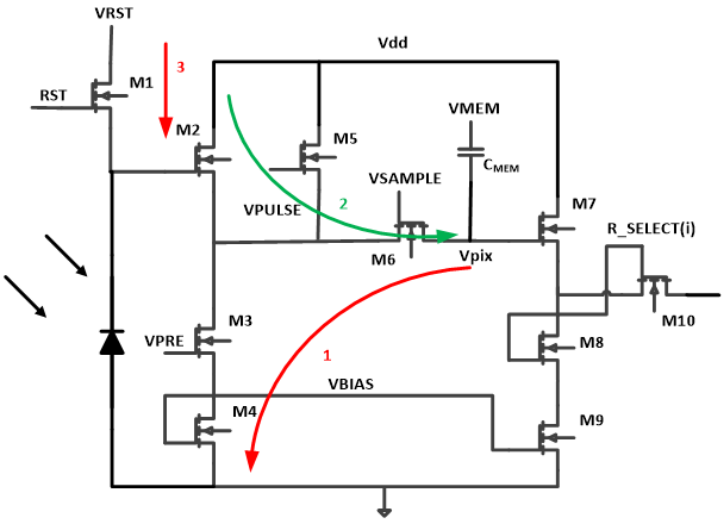


Figure 16 Leakage paths in 10T pixel circuit

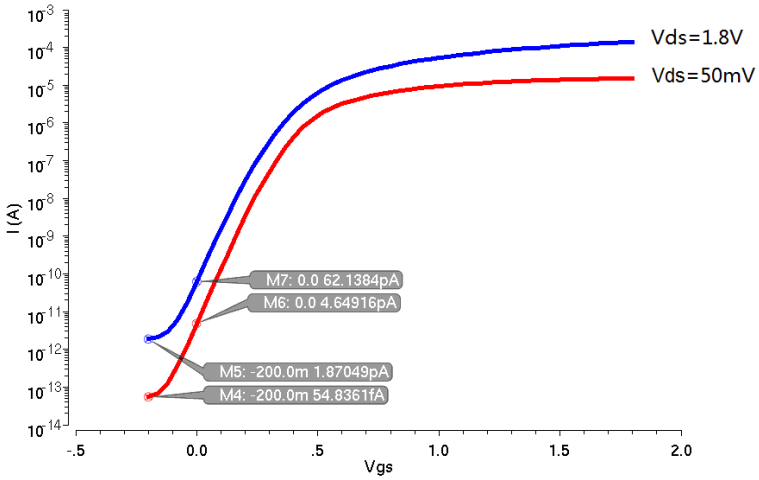


Figure 17 Subthreshold current simulation result of minimum size transistor

The current of path 3 (on Figure 16) is around 1 to 5pA because the transistor M1 is not turned off completely. To minimize this subthreshold current, the RST signal goes down to -0.2V after the reset operation. Moreover, the VRST is a tunable voltage that follows the voltage across the cathode of photodiode in order to minimize the drain-source voltage of M1. To overcome the current through paths 1 and 2, M4 and M5 are added. The M5 is controlled by VPULSE signal, which drives the source of M5 following V_{PIX} after VSAMPLE and VPRE are active low. This suppresses the current through path 2 by turning off the transistor M6. The M4 has a large length in order to increase the resistance, which consequently decreases the subthreshold current of path 1.

The area of each pixel is required to be 20μm x 20μm. The layout aims to maximizing the fill factor, therefore, the photodiode area should be maximized compared to the area of other pixel circuit blocks. There is one photodiode, one capacitor, 10 transistors, eight control signals, a power line and ground line for one pixel. The components will be discussed one by one.

A photodiode in a standard CMOS process can be realized using the n+/p-sub junction, which is shown in Figure 18. The highly doped n-type region is grown on p-substrate. Owing to its compact architecture, it is selected to increase the fill factor and detect low light signal.

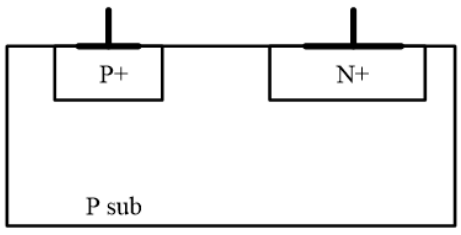


Figure 18 Photodiode structure

The capacitor value and type should be discussed. The KT/C noise at the input of

readout chain limits the value of the capacitor. The equation is described as

$$C \geq 12\, k_B T \left(\frac{2^B - 1}{V_{FS}}\right) \tag{13}$$

where, k_B is Boltzmann constant, T is absolute temperature, B is supposed to be 9 bit and V_{FS} represents 1V peak-to-peak signal swing. C is calculated more than 13fF.Considering the design margin, 30fF is chosen.

There are three types of capacitor that are always used in CMOS process, including MOS capacitor, poly capacitor and Metal-insulator-metal (MIM) capacitor. The voltage across the capacitor changes during reset operation and sample operation. Therefore, the basic requirement for a capacitor is the smallest variation of capacitance across a large range of voltage. The C-V characteristic of three kinds of capacitors are plotted in Figure 19. It is obvious that MIM capacitor has the best linearity compared to the other two kinds of capacitors.

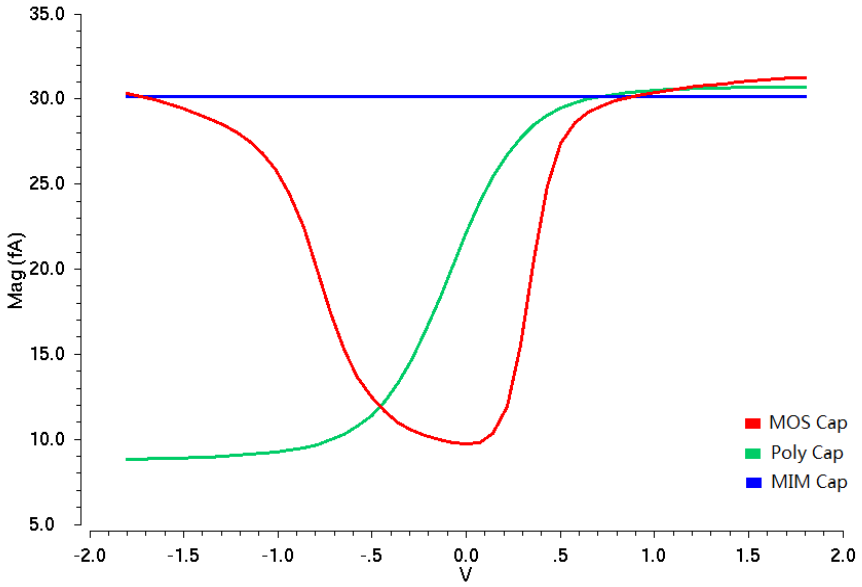


Figure 19 C-V characteristic of MOS cap, Poly Cap and MIM cap

Another requirement for sampling capacitor is the minimum layout area. Table 2 summarizes the estimation of layout area for three types of capacitor. The MIM cap

consumes the largest area compared to the other two types.

Table 2 Layout area of MOS cap, POLY cap and MIM cap

CAPACITOR	W	L	Layout Dimensions
MOS CAP	3.65μm	1μm	2.4μm x 5.26μm
POLY CAP	3.3μm	1μm	2.82μm x 5.32μm
MIM CAP	3.7μm	1.5μm	5.5μm x 8.5μm

Considering all aspects, the MIM capacitor is chosen to be applied in the pixel circuit owing to the high linearity.

The metal 1 is used to connect the transistors and the metal 2 is used for control signals. The MIM capacitor consists of metal 3, metal4 and metal5. Power line and ground line are accomplished via metal6 because of the low routing resistance. The metal layer arrangement guarantees the minimum area and high fill factor. To achieve a further increase on fill factor, layout sharing between adjacent pixels is applied. Figure 20 illustrates the novel layout technique. The readout circuit of each adjacent pixel is located in a common area. This technique allows for increasing the fill factor with the same photodiode area.

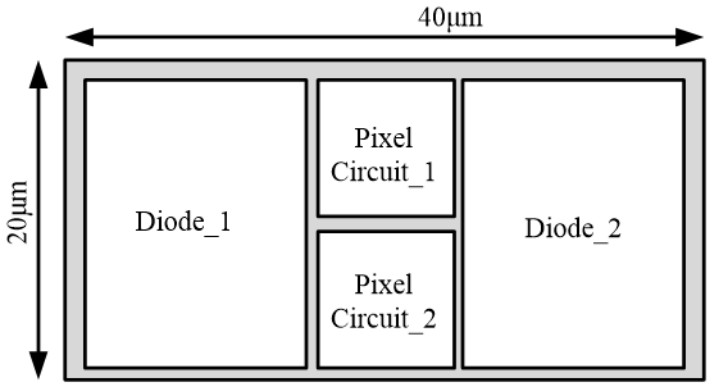


Figure 20 Layout sharing between adjacent pixels

2.5 Simulation Results

As discussed in section 2.3, the voltage value across photodiode is delivered through two source followers and two switches. Because of the variation in threshold voltage, the

non-linearity is introduced to the output signal. The relationship between V_{IN} and V_{OUT} is summarized as Table 3, where the V_{IN} is the input voltage difference and the V_{OUT} is the output voltage difference.

Table 3 Relationship between V_{IN} and V_{OUT}

V_{IN} (mV)	Ideal V_{OUT} (mV)	Observed V_{OUT} (mV)
1	1	0.643
10	10	6.16
100	100	76
200	200	152
300	300	228
400	400	303.79
500	500	377
600	600	449

As plotted in Figure 21, the offset is observed for the V_{OUT}. However, the V_{OUT} follows the V_{IN} in a linear way, which demonstrates that the gain of pixel circuit is almost constant.

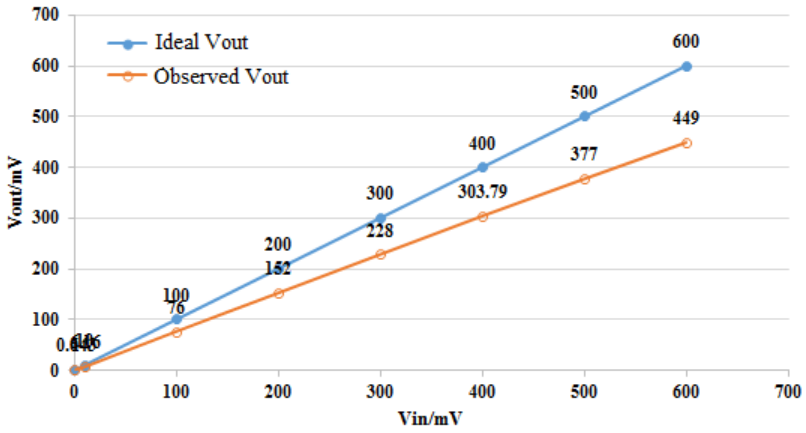


Figure 21 V_{IN} vs V_{OUT}

The junction capacitance of the photodiode is simulated in Figure 22. The capacitance keeps stable in 1pF from 50mV to 1.8V.

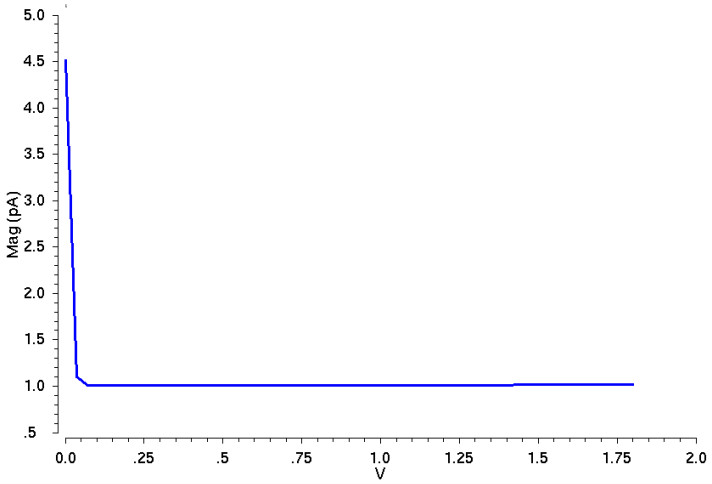


Figure 22 Junction capacitance of photodiode vs reverse bias voltage

The large dynamic range as well as the small signal detection requires low noise at the input of the readout chain, which is also the output node of pixel circuit. As mentioned in section 1.2, the readout chain has one PGA and one 10bit ADC. The PGA is applied to amplify the signal when it is too small to detect. Therefore, the noise at the input node of the PGA is of great importance. As the noise floor of 10bit ADC should be less than 1/2^10V and the minimum gain of the PGA is 1, the noise at the input of the PGA should be less than 976.5625μV. Figure 23 shows that the noise summary at the column select transistor is 116μV. Most of the noise comes from the column select transistor, which is 85μV. The noise is far less than 976.5625μV.

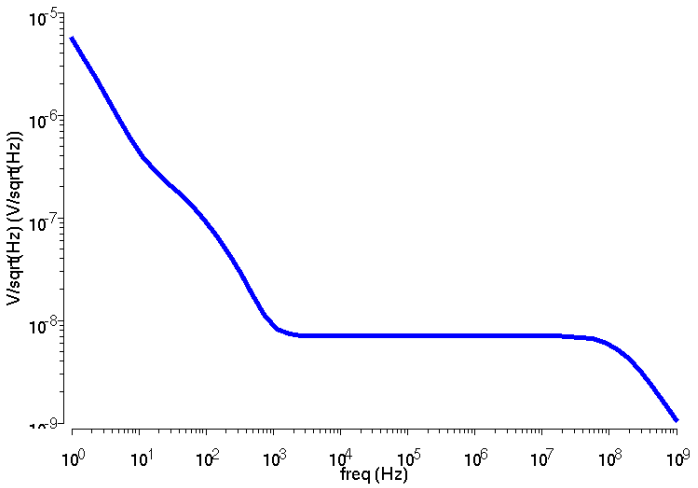


Figure 23 noise plot at the output node of column select transistor

Figure 24 shows the layout of 1x2 pixels. The PN junction is 14.705 x 17.63 μm^2 and the active area is 258.500μm^2. The fill factor is calculated as 64.625%. M1~M5 are routed above the photodiode to meet the density check.

After exposure time, the light signal is stored in the MIM capacitor. There are four readout chain on chip for 96x96 pixels. Thus, each readout chain needs to handle 96*96/4=2304 pixel signals. The operating frequency of readout chain is 25MHz so that the time required to complete reading out all pixels is 92μs. Figure 25 shows the voltage drift over 92μs due to the subthreshold current of sampling transistor. The voltage difference is 294μV, which is less than 976μV.

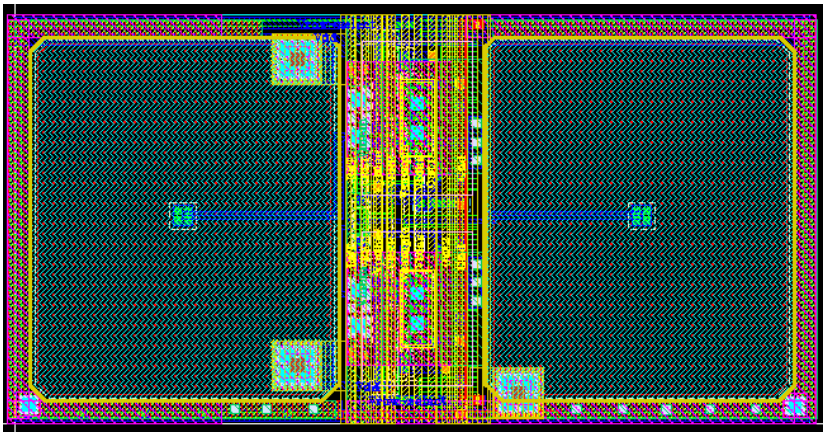


Figure 24 Layout of 1x2 pixels

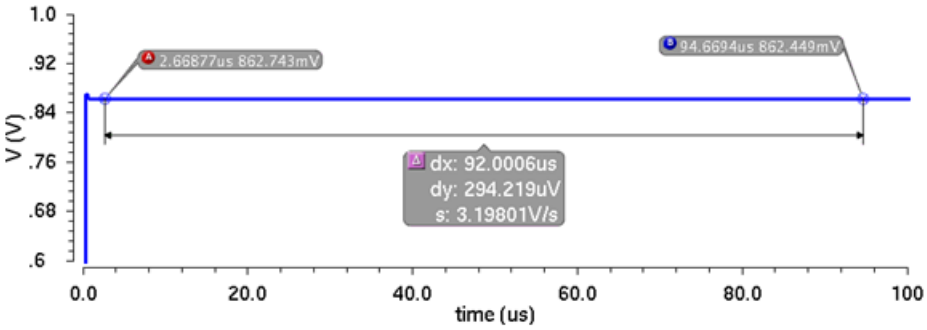


Figure 25 Voltage drifts over time

CHAPTER 3

Pixel Selection

In order to capture the image, multiple pixels should be carefully located together, which is called pixel array. This chapter will discuss the structure of the pixel array and explain how each pixel is selected to be read out.

3.1 Overview of Pixel Array and Pixel Selection circuit

The pixel array is the key component in the image sensor. According to the area limitation, 96x96 pixels are presented in this thesis. The pixel selection circuit aims at selecting pixels in certain ways. The pixel selection circuit consists of one column selection register, one row selection register and driving circuits.

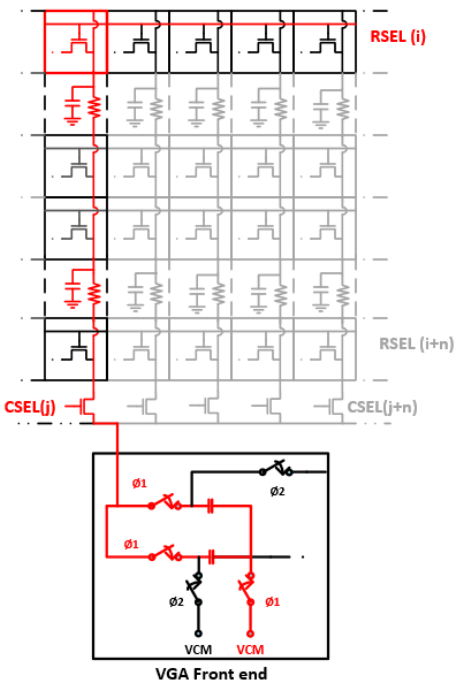


Figure 26 Model of pixel array

An output node of each pixel in one column is connected together. So do the row select signal of one row. The model of pixel array is shown as Figure 26. When one pixel

in one column is selected via row select signal, all the other row select signals are not active. As seen from Figure 26, there would be load capacitors from each pixel and resistors from column bus. This can be modeled as a lumped RC line[34]. The RC line will bring delay from the pixel output to the input of readout chain, which has effects on the speed. Since the speed of readout chain is 25MSPS, the settling time of pixel output should be less than 20ns. With the development of pixel number, the RC delay gradually becomes the main limitation of high speed image sensor[35]. This problem can be solved through implementing multiple readout chains, as shown in Figure 27. However, due to the area limitation, there are only four readout chains available on chip. Therefore, the maximum RC delay should satisfy the speed requirement. The maximum RC delay comes from the first row of the pixel array, which locates most far away from the readout chain. It must drive 95 load capacitors and whole column bus. Considering the design margin, the settling time across all corners should be less than 18ns. Thus, the column bus should be designed with low load impedance. What's more, a driver is designed to make sure it will meet the time constraint.

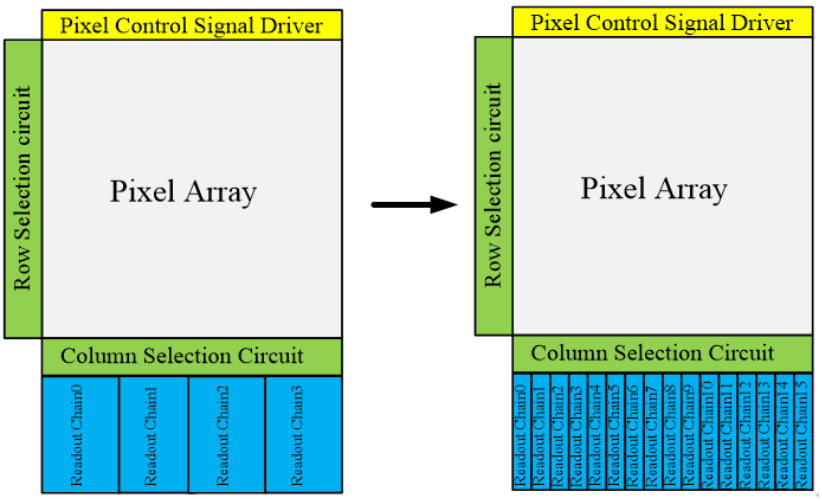


Figure 27 Multiple Readout Chain

The global shutter requires resetting all the pixels and capturing images at the same time. However, owing to the load capacitor of each pixel, it is difficult to operate without any delay. Therefore, increasing the driving ability of each control signal of the pixel is necessary for the global shutter.

Usually, the pixels are selected one by one; but, pixel binning requires a flexible function of pixel selection circuit. The shift register is one of the most popular structures for pixel selection circuit. It can generate one or multiple pulses according to the control signals. The simple architecture and small area are appealing to the image sensor design.

3.2 Pixel Selection Design and Layout

The row selection circuit is displayed in Figure 29. There are 96 shift registers and each shift register consists of one latch, one D flipflop and one driver. The four readout chains are designed for the pixel array, which means four pixel values are read out each time. Therefore, there are 96/4=24 shift registers in column selection circuit, which is shown in Figure 30. R_SET(24), R_SET(48) and R_SET(72) are added to implement flexible pixel selection.

The structure of the D flip flop and the D latch are shown in Figure 28 and the truth table of the D flip flop and the D latch are shown in Table 4 and Table 5.

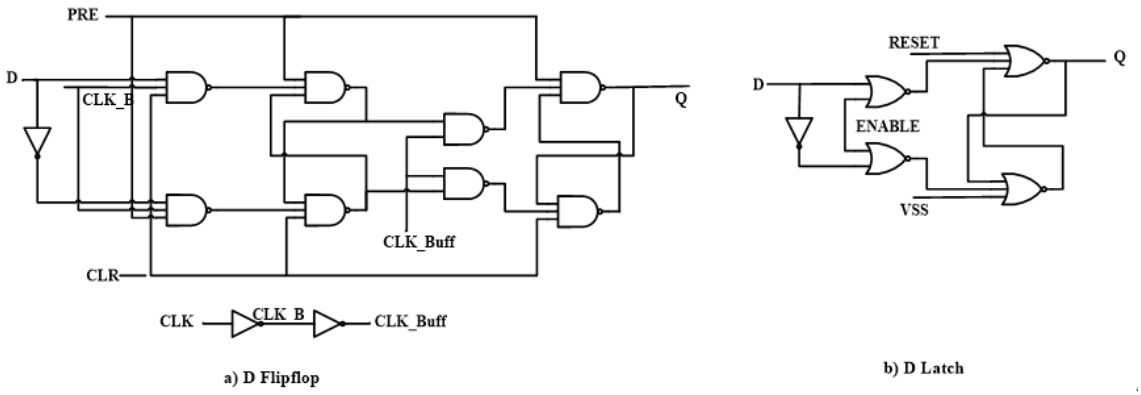


Figure 28 Structures of D flip flop and D latch

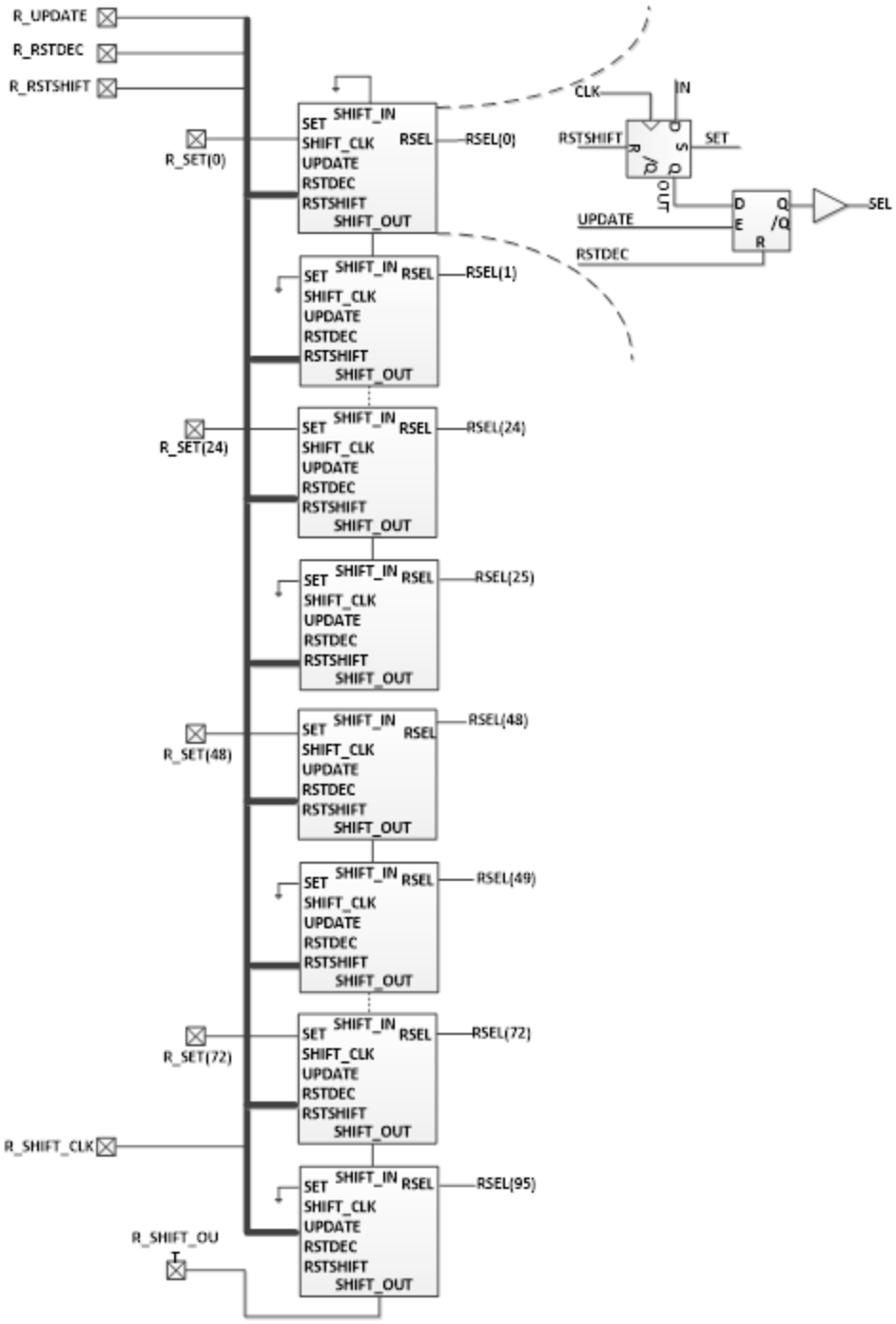


Figure 29 Row selection circuit

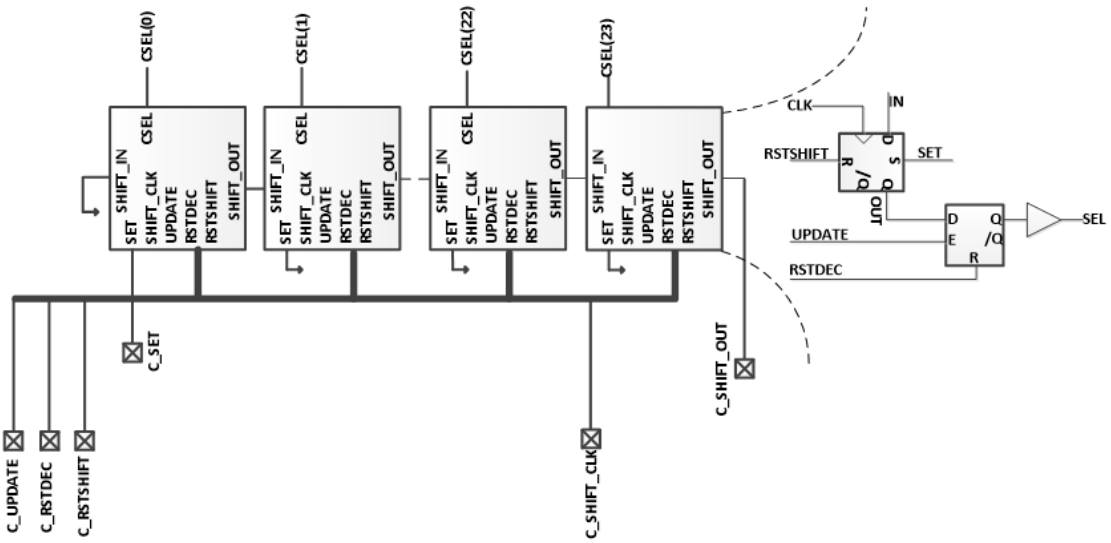


Figure 30 Column selection circuit

Table 4 D flip flop Truth Table

SET	RSTSHIFT	IN(D)	CLK	OUT
0	x	x	x	1
1	0	x	x	0
1	1	D	↑	D

Table 5 D Latch Truth Table

RSTDEC	UPDATE	OUT(D)	SEL
1	x	x	0
0	1	x	SEL
0	0	D	D

First, all row and column shift registers are reset with activating the signal RSTSHIFT_R, RESEC_R, RSTSHIFT_C and RESDEC_C. In order to read pixel values, the SET_R and the SET_C are activated. The period of activation should be less than one period to make sure one row or one column is selected each time. The clock signal for row and column selection are different. It depends on how the pixel values are read. As Figure 31 shown, one row is selected and all column values are read out. Therefore, the clock period of row selection is 24 times of the column selection clock period. After that, the following row is selected and all columns are consecutively read out. This operation will be repeated until all pixel values are read out.

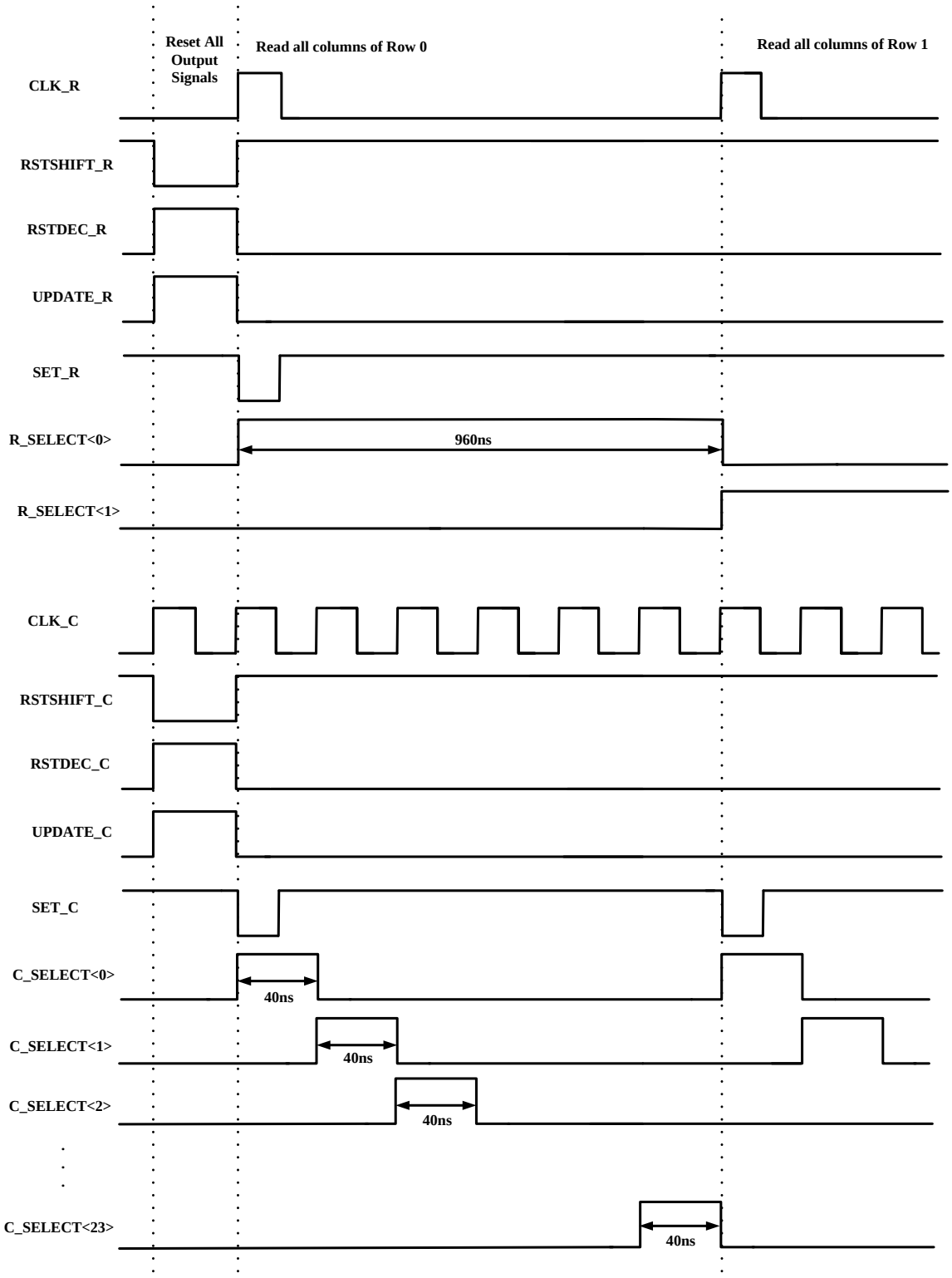


Figure 31 Timing diagram of Row&Column selection circuit

The driver of control signals for a pixel is shown in Figure 32. The signal V_{PULSE}

drives the C_{gs} and the C_{ds} of transistor, which needs strong driving capability. The signal SAM, PRE and RST are connected to the transistor gate, which should drive the C_{gs}. The signal V_{rst} and V_{mem} have multiple voltage values so that the selection circuit is designed as required. The MEM_SEL, RST_SEL(0) and RST_SEL(1) control the voltage value of two signals.

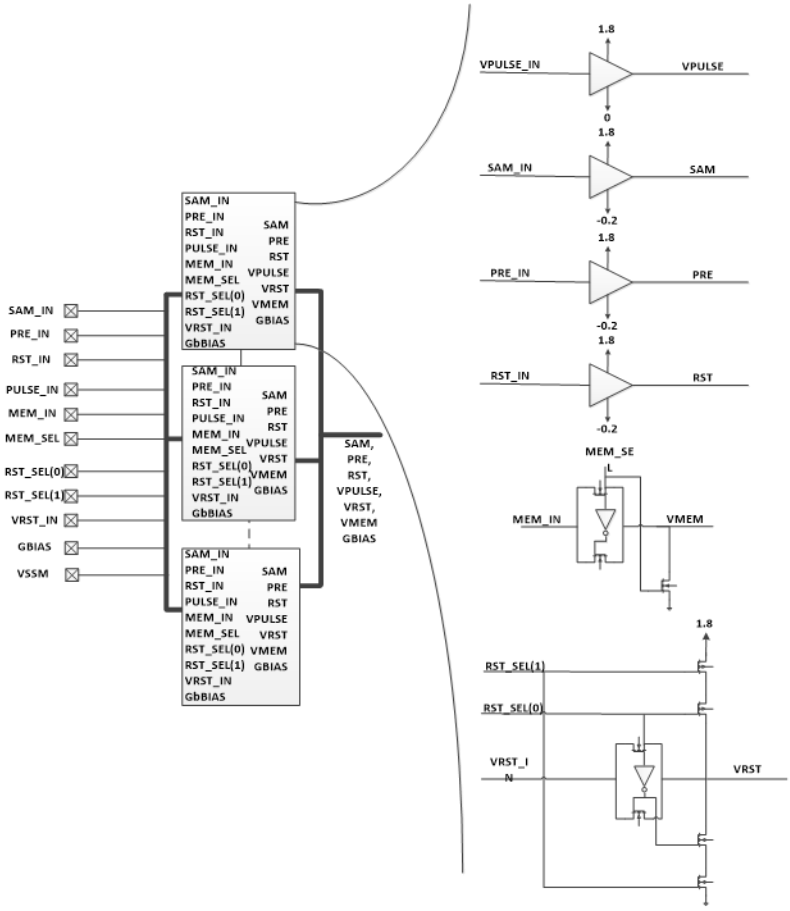


Figure 32 Driver of control signals for pixel

The layout of the row selection circuit, the column selection circuit and the driver for control signals are described in Figure 33, Figure 34 and Figure 35. Each row shift register is 20μm height to match one pixel and column shift register is 80μm wide to match four pixels.

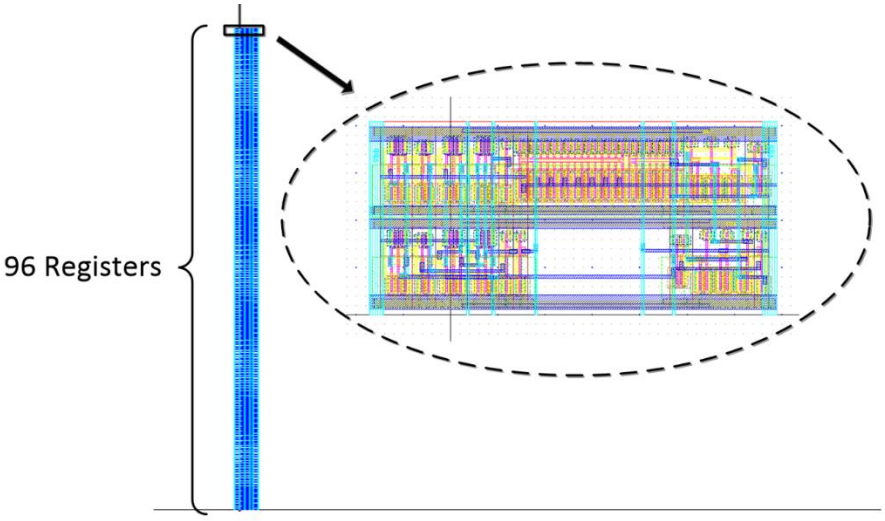


Figure 33 Layout of Row Selection Circuit

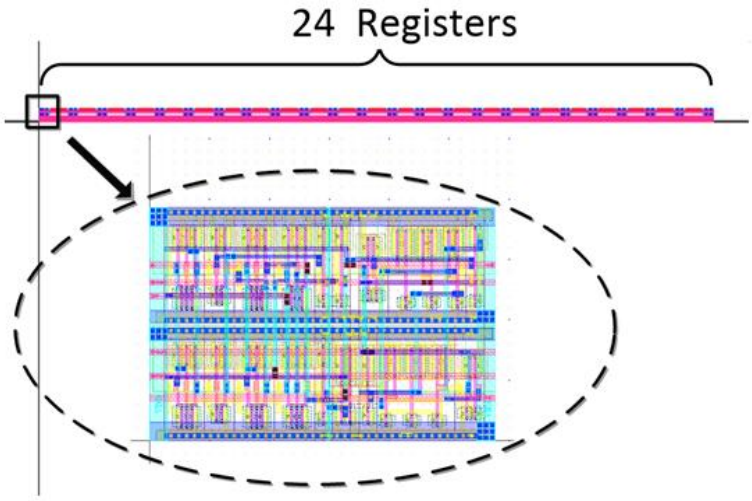


Figure 34 Layout of Column Selection Circuit

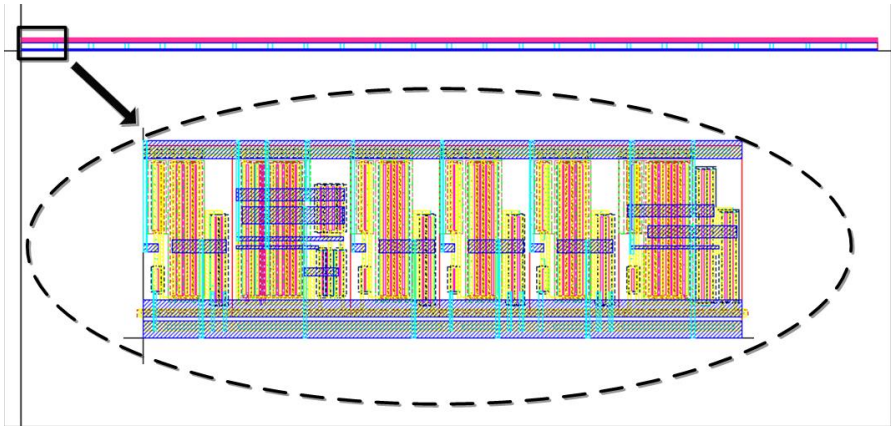


Figure 35 Layout of driver for control signals

The layout of the pixel array and the pixel selection circuit together is shown in Figure 36. The pixel array is 1.92mm x 1.92mm area. The power supply voltage variation crosses the pixel array should be less than 1mV. Usually, 0.4μm width metal 2 routing line causes 40mV variation. Therefore, the power and the ground lines have a mesh architecture in order to reduce the voltage drop and variation. The power and the ground line are designed as 2.74μm width in metal 6 so that the voltage variation is reduced to 0.75mV.

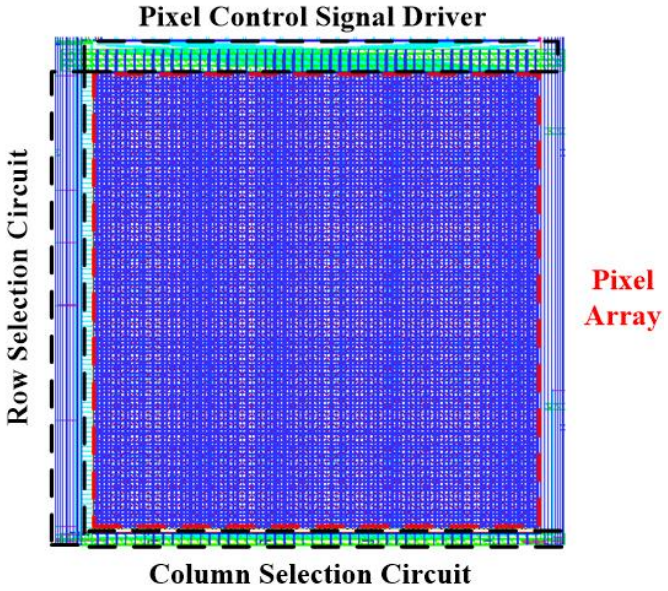


Figure 36 Layout of pixel array and pixel selection circuit

3.3 Simulation Results

The pixel settling time is one of the important parameters of the pixel array. The RC delay model is calculated as below. The metal wires and the row&column select transistor contribute to the resistance and the parasitic capacitors of the row&column select transistor from the load. The sheet resistance of routing metal is 82mΩ/square. Therefore, 96 pixel column bus has 393Ω resistance, the row select transistor has 2.2kΩ resistance and the column select transistor has 550Ω resistance. The total resistance is 3.093kΩ. The parasitic capacitor of row select transistor is 3.22fF and the parasitic capacitor of column select

transistor is 1.85fF. Thus, the RC delay is calculated as 16.83ns. Figure 37 is the simulation result of maximum settling time of schematic, which is 17.12544ns. The simulation result matches the calculation result.

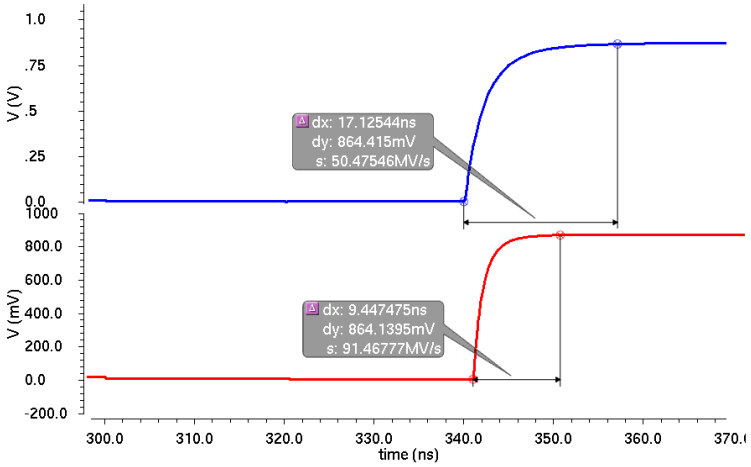


Figure 37 Delay time Simulation of Schematic

The post simulation results of the pixel control signal drivers, the row selection signals and the column selection signals are described in Figure 38, Figure 39 and Figure 40. The results match the design requirement. The pixel binning is also simulated in Figure 41.

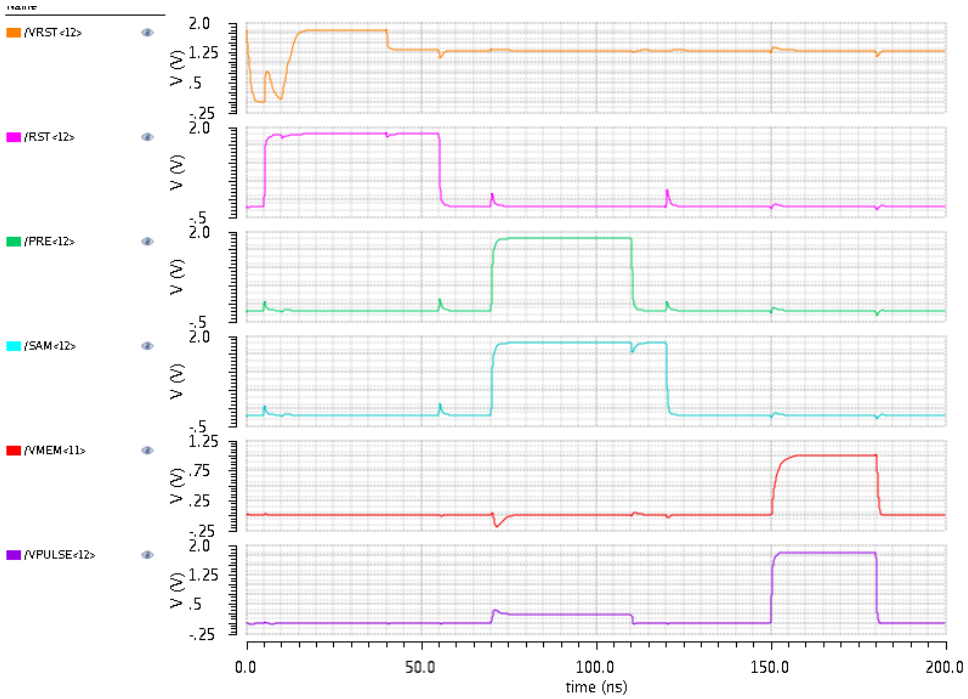


Figure 38 Post simulation results for Pixel Control Signals

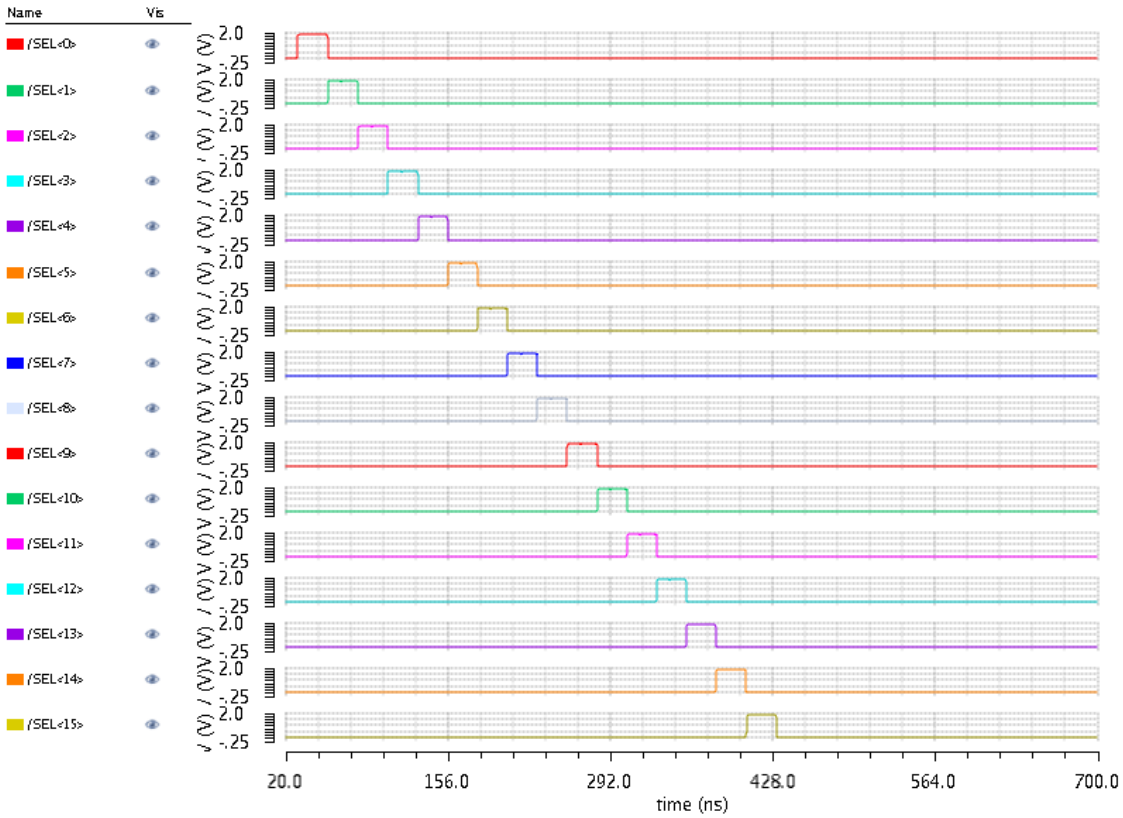


Figure 39 Post simulation results for column select signals

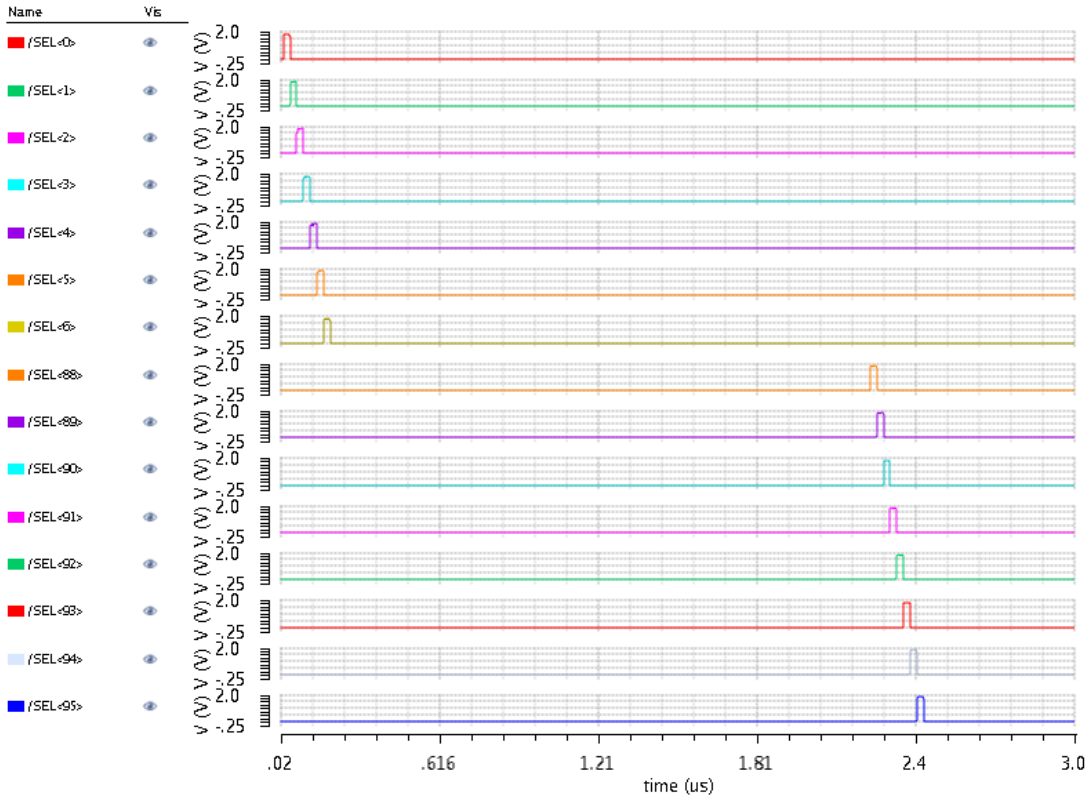


Figure 40 Post simulation results for row select signals

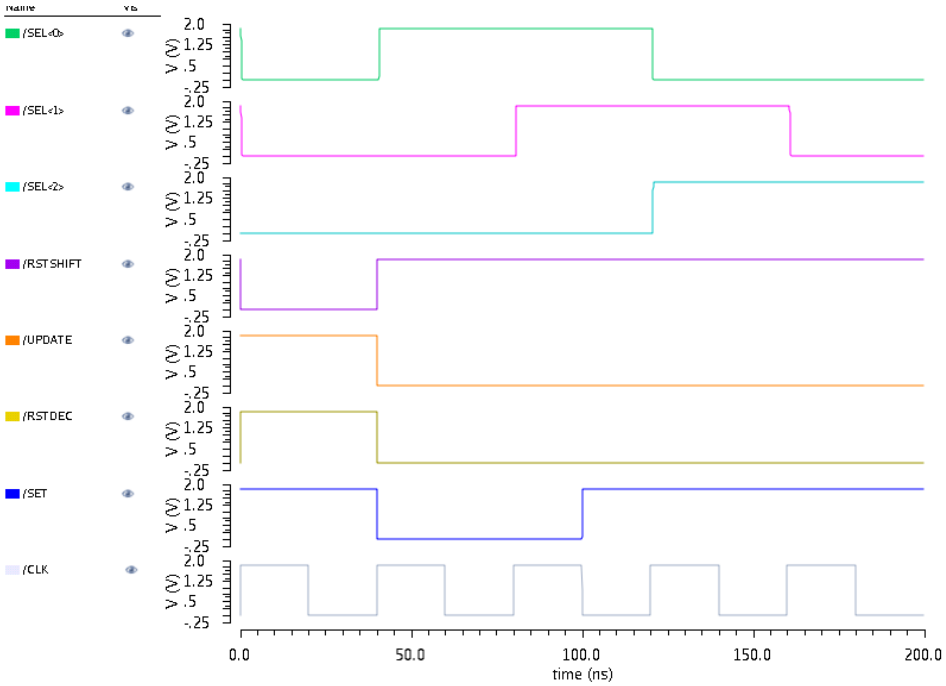


Figure 41 2x2 pixel row binning simulation result

3.4 Test Results

A uniform flash light is used as the light source for testing. The FPGA provides the control and timing signals and its logic flow is indicated as Figure 42. It is seen that the generated control signals are not related to the read out timing, providing flexible exposure time and readout time control. The analog output of the pixel is captured and stored in oscilloscope, given in Figure 43. The set signal of the row select shift register is used as the synchronized clock to capture data. The test board, chip and FPGA board is displayed in Figure 44.

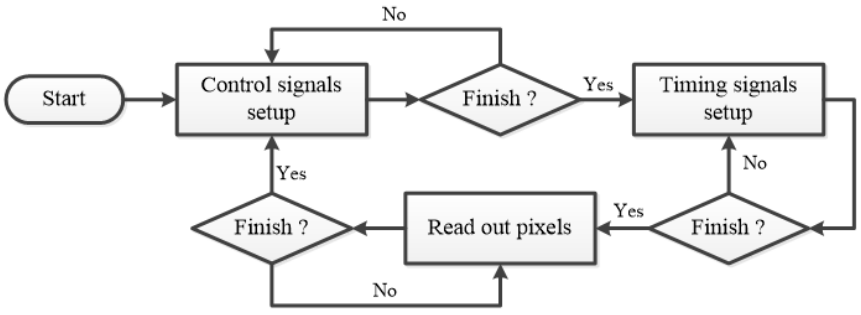


Figure 42 FPGA logic flow

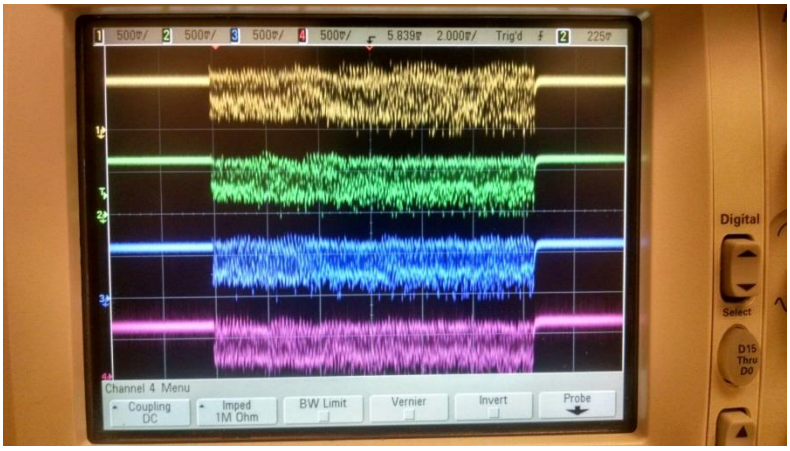


Figure 43 Data stored in oscilloscope

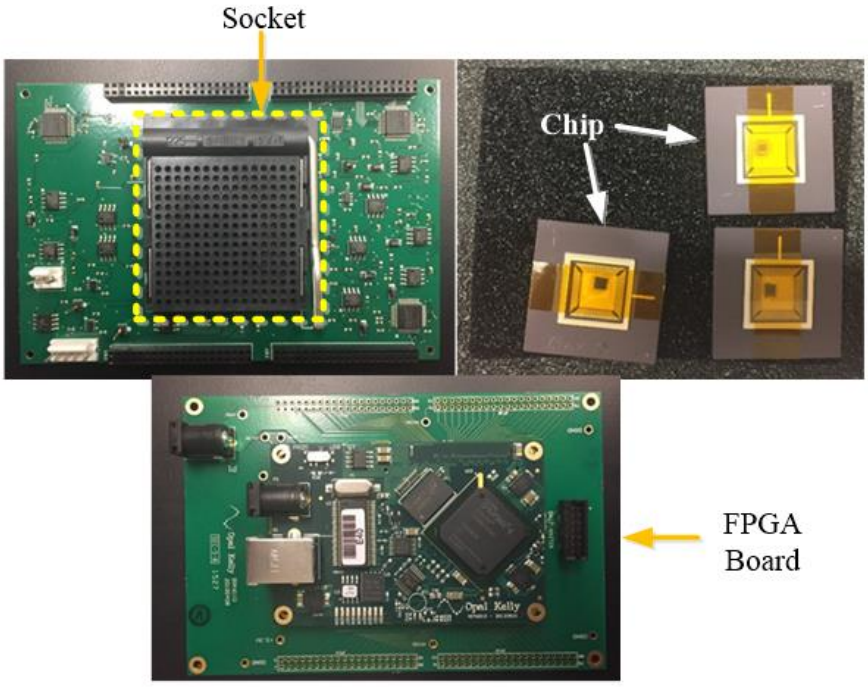


Figure 44 Test board

The experimental result of the light intensity versus the output voltage of single pixel is shown in Figure 45. The exposure time is set to 3μs and total readout time is set to 5μs. The linearity of pixel is measured as 93.56%.

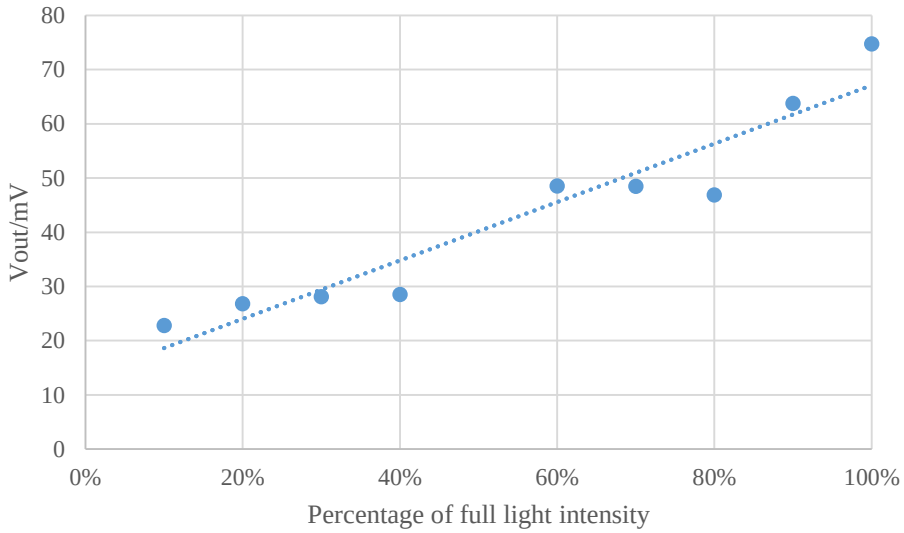


Figure 45 Light intensity vs output voltage

Apply the same readout time and longer exposure time to the whole pixel array. The data is first captured and stored on an oscilloscope and then fed into Matlab to be transferred to image. The generated images of different light are present in Figure 46. The grey edge of the full light image shows that the sensitivity of pixels on the top edge is less than that of other locations.

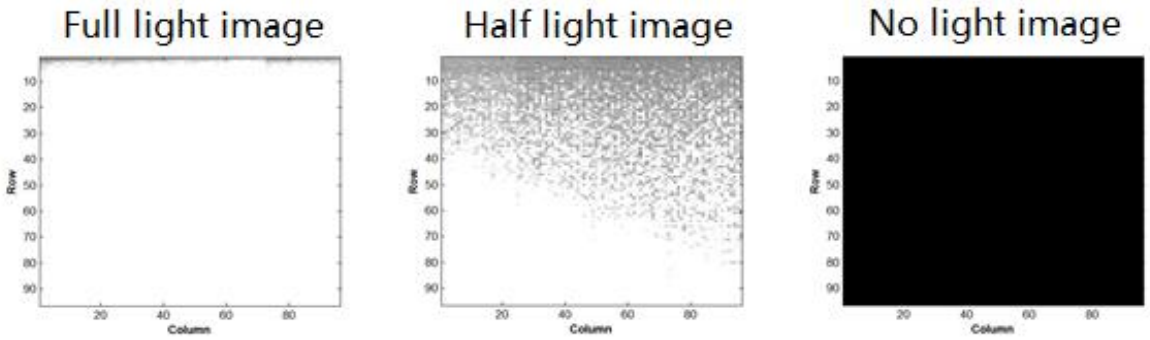


Figure 46 Images of different light

CHAPTER 4

Readout Chain

Previous chapter has discussed the details about the pixel circuit, the pixel array and the pixel selection. For CIS, the readout chain also needs to be carefully designed. This chapter will first present the different architecture of readout chain. Then comes to the circuit implementation and the simulation results. Finally, the test design will be discussed.

4.1 Readout Structure

The readout chain plays an important role in CMOS image sensor performance. So it is critical to select an appropriate architecture. The typical readout chain consists of an ADC. The ADC is classified into three categories according to location: chip level, column level and pixel level.

4.1.1 Chip Level Readout Circuit

Figure 47 indicates the chip level readout chain topology. Whole image sensor shares one readout chain[36].

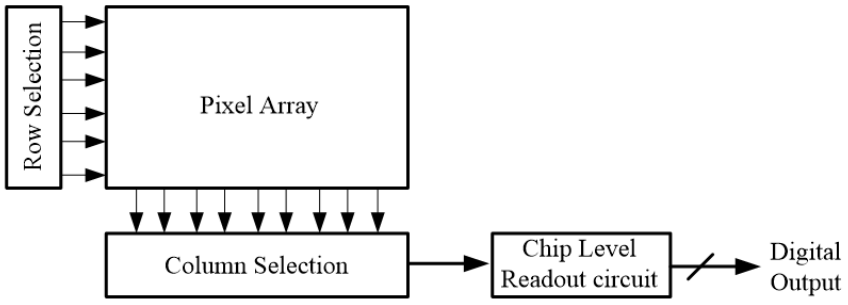


Figure 47 Chip level Readout Chain[37]

The pixel signals are delivered one by one to the readout chain. The advantages of this architecture are simplicity and uniformity. However, the frame rate is limited to the readout chain speed. Increasing the speed of the readout chain will bring more power to the chip. Thus, the image sensor with chip level readout chain is difficult to reach high

speed and high resolution. What's more, the noise floor of readout chain is increased due to more pixel circuit being connected to the input of readout chain. The chip level readout chain is popular in early time.

4.1.2 Column Level Readout Circuit

Figure 48 illustrates the topology of the column level readout chain. One column or multiple columns share one readout chain[38]. This improves the speed of image sensor and the noise performance. Also, the fill factor is increased. But the increasing number of readout chain brings large area and inconformity.

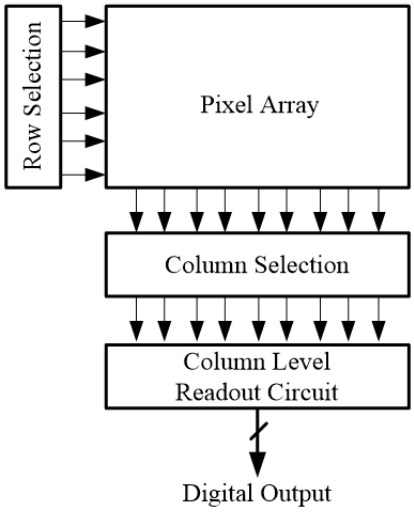


Figure 48 Column level Readout Chain[37]

4.1.3 Pixel Level Readout Circuit

Figure 49 indicates the topology of the pixel level readout chain. The pixel level readout chain means implementing the readout circuit inside each pixel[39].

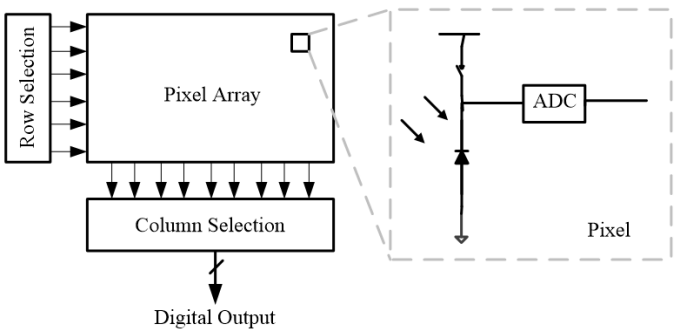


Figure 49 Pixel level Readout Chain[37]

The speed of the image sensor is further increased and noise performance is also enhanced with less transistors connected. However, it is obvious that the area will be increased and the fill factor will be reduced significantly.

4.2 Column Level Readout Circuit

As discussed in the previous part, the chip level readout chain and the pixel level readout chain are always applied for extreme requirements, such as ultrahigh speed or ultralow area. The column level readout chain provides good tradeoff among speed, area, fill factor, noise performance and power consumption. Therefore, the column level readout chain is the best choice for this thesis.

Typically, an ADC is the readout chain for CMOS image sensor. However, the input swing of ADC and the noise of front-end circuit limits the dynamic range of readout chain. Moreover, the accuracy of CMOS image sensor is determined by the resolution of the ADC. Thus, in order to improve the dynamic range and accuracy, a PGA is always placed in front of the ADC. The gain of the PGA is flexible so that it is able to detect the low light and small differences between two images.

4.2.1 Overview of ADC

The basic requirements for ADC are high resolution, high speed and low power. ADC always has 10~12 bits resolution in CIS[40].

Figure 50 depicts the trend of resolution vs frequency in popular ADC architectures. All possible ADC architectures regarding the basic requirements will be discussed in the following section.

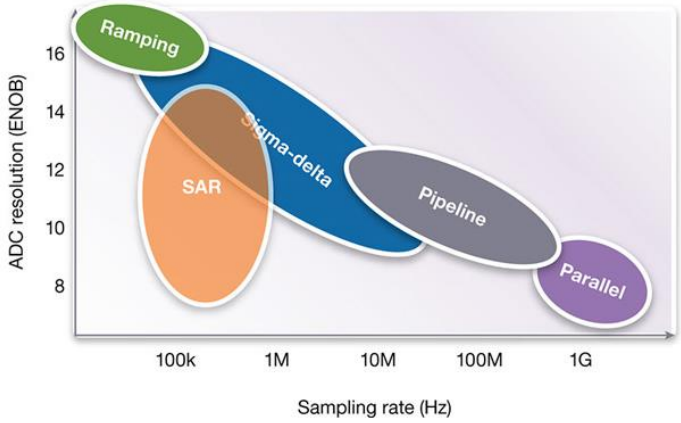


Figure 50 Sampling rate vs Resolution bits for various ADC structures[41]

4.2.1.1 Slope ADC

Slope ADC is widely used in the image sensor because of its simple structure[42]. A Single Slope ADC topology is shown in Figure 51. The operational amplifier, the resistor and the capacitor form an integrator. The integrator accumulates Vin and then produces the triangle waveform on the output node. The maximum integration value is set by the reference value, -Vref. From the moment that integrator starts accumulating, the counter starts counting from 0 to $2^{\wedge(n-1)}$. When the output of integrator reaches -Vref, the output buffer captures the last counter number, which represents the digital code for the analog input Vin. Meanwhile, the counter and integrator are reset at the same time for the next conversion.

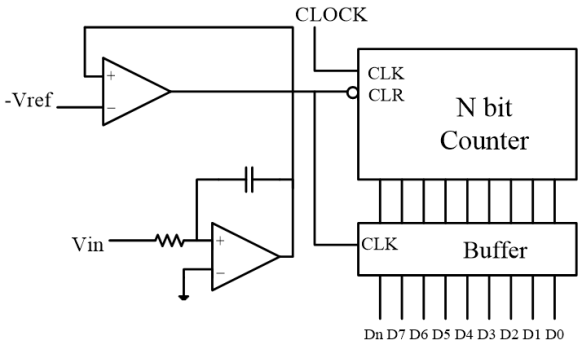


Figure 51 Single Slope ADC

Even though the single slope ADC is area efficient, the main drawback is readout speed. The large number of clock cycles for high resolution ADC makes it difficult to be applied in high speed application. For a 12-bits ADC, it takes up to 4096 clock cycles to complete one conversion of input.

In order to improve the speed, several new architectures of slope ADC are proposed, such as Dual Slope ADC[43] and DLL based Slope ADC[44].

A switch is added to Dual Slope ADC in Figure 52. Vin is first connected to integrator and integration time is constant. After completing integration, the switch connects -Vref to integrator. The sawtooth waveform generated on the output node decreases since -Vref is a negative value. When the output voltage reaches zero, the integrator and the counter are reset for next conversion. The output waveform of integrator is shown in Figure 53. Since T1 and Vref are fixed, the maximum voltage value is determined by input value and thus T2 is proportional to the input value. The Dual Slope ADC is faster than the Single Slope ADC and it solves the problem of calibration drift because the integrator is not related to a clock signal. What's more, multiple ramp single slope ADC is proposed[45]. It is much faster but less area and power efficient.

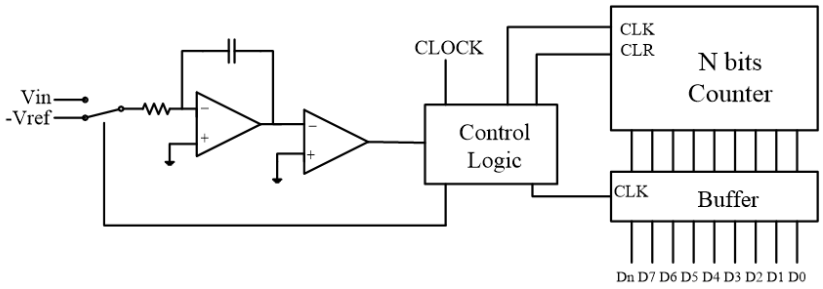


Figure 52 Dual Slope ADC

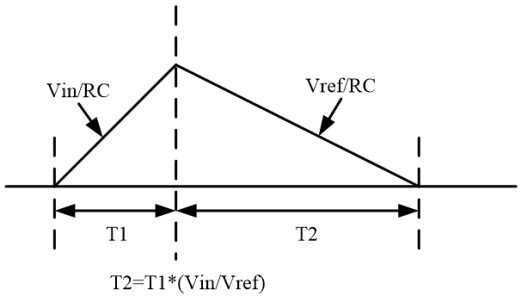


Figure 53 Output waveform of Dual Slope ADC

4.2.1.2 Sigma-Delta ADC

Sigma-Delta ADC is first proposed in 1978[46]. The architecture of the Sigma Delta ADC is shown in Figure 54. The sigma delta modulator regulates the noise to the high frequency domain and the following filter reduces the noise and generates the corresponding digital code. More stages the modulator has, fewer conversion cycles it needs. It has the advantages of high resolution and low area. However, high order of modulator brings complexity and more power. Besides, it operates at low speed.

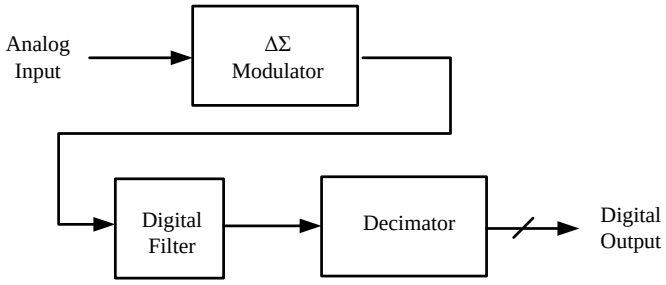


Figure 54 Sigma Delta ADC

4.2.1.3 SAR ADC

SAR ADC is displayed in Figure 55. The input signal is sampled first. The comparator

compares the input signal with the output of the DAC, which is controlled by register. The comparison result then is fed into SAR to generate the corresponding digital codes in order to regulate the DAC. The MSB in register is initialized to 1 and the other code are set to 0 at the beginning. Thus, the DAC output is initialized to Vref/2. If the input signal is less than Vref/2, the MSB will be reset to 0. Otherwise, it remains 1. Then the next bit is set 1 and repeats the same operation above until completing LSB. The binary search helps increasing the conversion speed significantly with the expense of area and power.

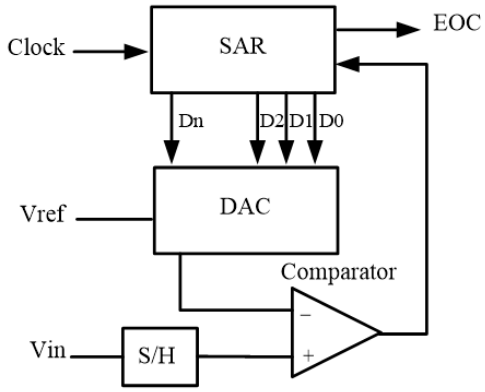


Figure 55 SAR ADC

The resistive DAC has poor accuracy and linearity. Thus, the capacitive DAC is widely used. The capacitive DAC architecture is shown in Figure 56. It consists of the capacitors with binary weighted and one dummy capacitor. It consumes large area and matching among capacitors is an issue. Thus, the improvement on SAR ADC aims at reducing the capacitor value in DAC. Several new architecture DACs are introduced[47-49].

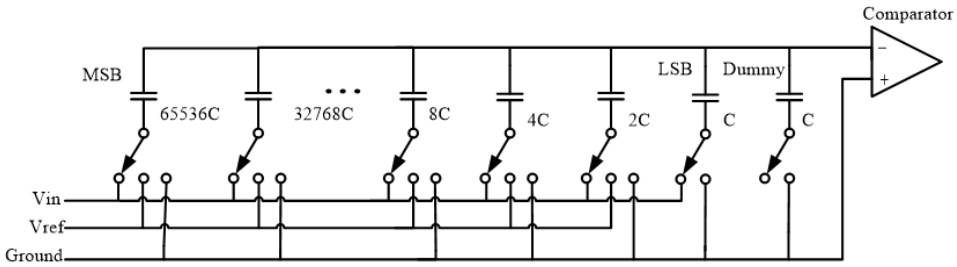


Figure 56 DAC Architecture

4.2.1.4 Cyclic ADC

Cyclic ADC, which is also called algorithmic ADC, is presented in Figure 57[50]. Because a high resolution DAC will occupy a large area and limit the ADC accuracy, Cyclic ADC is introduced to the image sensor. The conversion time is the same as SAR ADC. The input signal is sampled first. Then it is compared with a threshold voltage. The comparison result decides the digital code of the final sequence. Meanwhile, a 1bit DAC generates a reference voltage according to the digital code. The input signal is amplified by a factor of G at the same time. The amplified voltage substrates the reference voltage, producing a residue value. This operation is repeated until the desired digital codes are achieved. The first conversion generates the MSB and last conversion generates LSB.

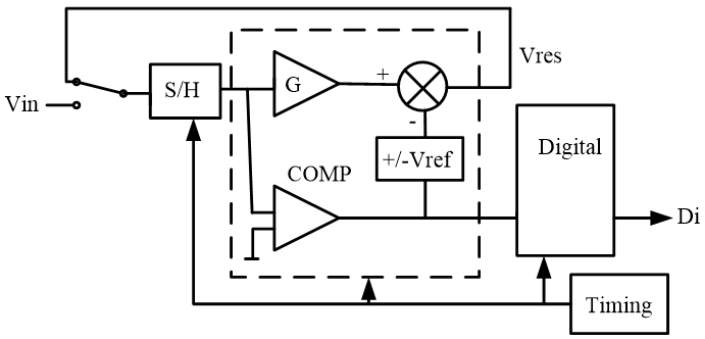


Figure 57 Cyclic ADC

The simplified DAC helps reducing area and power. However, the gain of amplifier needs to be accurate in order to achieve higher overall accuracy, which still increases the power consumption.

4.2.1.5 Pipeline ADC

The amplified residue is also applied to pipeline ADC, which is shown in Figure 58[51]. The input signal is sampled at first. Each stage quantizes the input and generates the residue voltage for the next stage. Once all stages are completed, a digital block corrects the digital codes and then the conversion is finished. The pipeline ADC is able to achieve high speed, but consume more power.

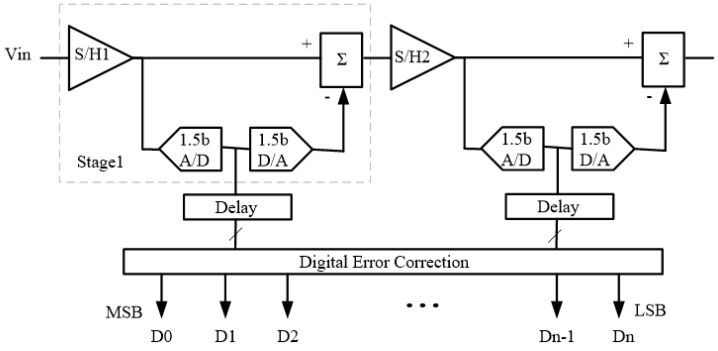


Figure 58 Pipeline ADC

The high speed Image sensor requires over 10bits resolution with more than 1MHz bandwidth, given in Figure 59. Ramping ADC, known as the Slope ADC, offers high resolution with low speed. Moreover, it is difficult for the SAR ADC to reach low power with high speed. So do the Sigma Delta ADC and the cyclic ADC. The parallel ADC, known as Flash ADC, is the fastest one. However, its low resolution stops itself from being applied to image sensor. That leaves pipeline ADC alone as the most reasonable choice.

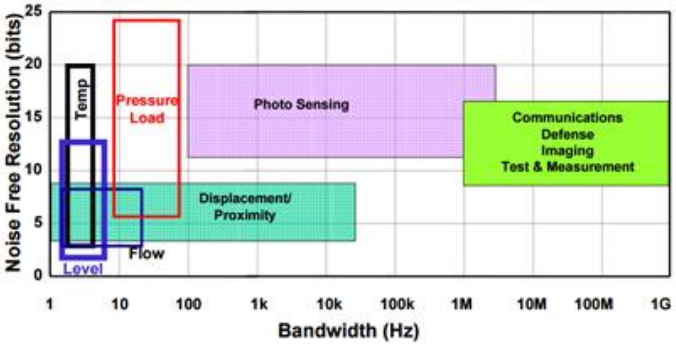


Figure 59 Real World vs Bandwidth[52]

4.2.2 Pipeline ADC Design Consideration

The topology of a pipeline ADC is shown in Figure 60. The operation principle is discussed in the previous section. The topology of 1.5b per stage is widely used as it offers the advantages in terms of design simplicity, power consumption, area and flexibility in layout orientation. It is the fastest as it requires the lowest interstage gain with the highest bandwidth, considering that their product is a constant for a given process technology and feature size.

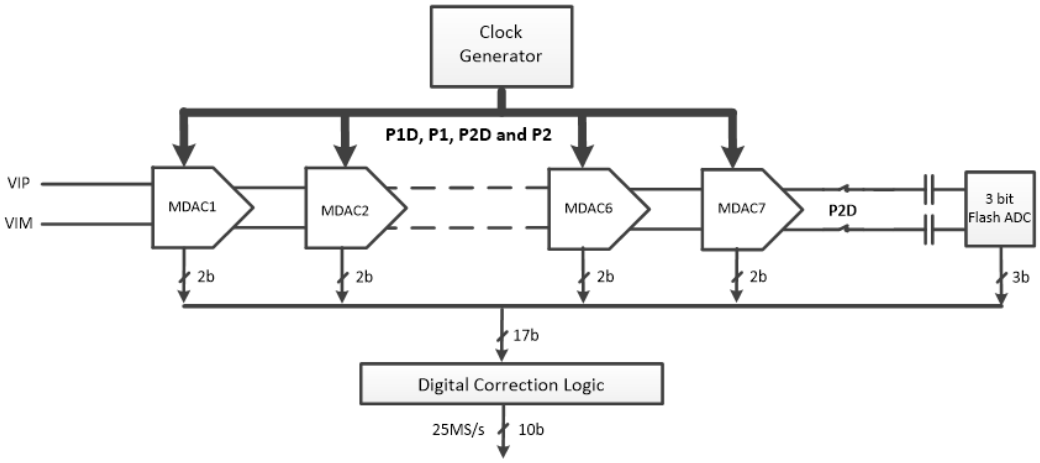


Figure 60 Block Diagram of Pipeline ADC

4.2.2.1 1.5b RSD

The topology of 1.5b RSD is shown in Figure 61.

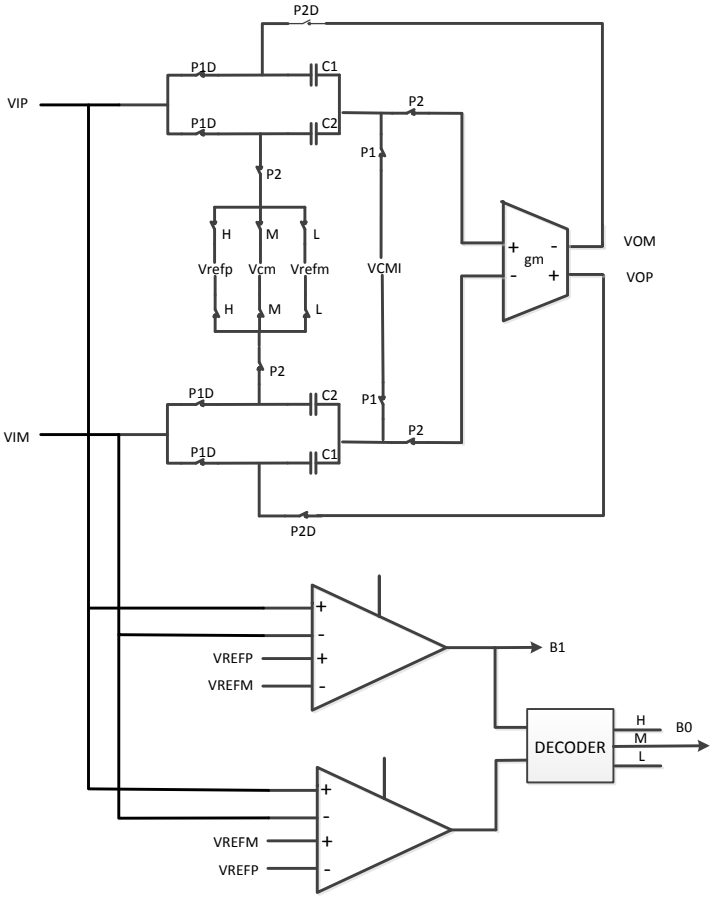


Figure 61 1.5b RSD Topology

The residue is calculated as

$$Vout\_ideal=Vin(1+{}^{C1}/_{C2})\mp Vr({}^{C1}/_{C2}) \qquad (14)$$

If C1=C2, Gvi=2 and Gvr=1.

An ideal Op-amp has the infinite gain so that there is no offset through the feedback network. However, due to the finite gain and the bandwidth, there appears gain error in 1.5bit RSD. The gain error is then calculated as

$$Vout\_error=Vout\_ideal\,\frac{1}{1+A\beta}, \text{ where } \beta=\frac{C1}{C1+C2} \qquad (15)$$

Suppose the maximum error is 0.5*LSB, the maximum gain of the op-amp should be greater than 72dB.

If an op-amp is modeled as single a pole system, the transfer function of its step response is expressed as

$$h(t)=h_0\left(1-e^{-\frac{t}{\tau}}\right), \text{ where } \tau=-1/\text{GBW} \quad (16)$$

Suppose the final voltage needs to be x% of h_0 with t, the unity gain frequency is calculated as

$$f_u=\frac{(x\%)}{-\beta t} \quad (17)$$

If sample rate is 25MHz, t equals to one quarter sample rate. X is always chosen to be 0.25LSB. Therefore, f_u is 2.58GHz.

Besides, the switched capacitor plays an important role owing to its thermal noise. The input referred thermal noise of a switch capacitor gain stage is shown as

$$V_{n,i}^2=\frac{KT}{C_{fb1\sim3}}\frac{1}{\beta}\frac{1}{G_{vi}^2}\left(1+\frac{1}{G_{vi}^2}+\frac{1}{G_{vi}^4}\right) \quad (18)$$

where k is Boltzman's constant, T is the temperature in Kelvin and C_{fb} is the feedback capacitor. Known from[53] that

$$V_{n,i}=\frac{A/\sqrt{2}}{10^{SNR/20}} \quad (19)$$

where SNR=0.63N+1.76+6=68dB. $V_{n.i}$ is calculated as 140μV and feedback capacitor C_{fb} is calculated as 137.6pF.

The input gain and the reference gain are highly dependent on the ratio of two capacitors. Hence, the ratio variation, which results from the capacitor mismatch, has a significant effect on the 1.5b RSD. For a 12-bit resolution ADC, the mismatch of first MDAC should be less than 0.025%. As discussed in the previous section, the MIM cap is the best choice due to the low mismatch across PVT.

As a switch has ON resistance, the size of the switch should be large enough to achieve

a small time constant when connecting to the sampling capacitor. The ON resistance is calculated as

$$R_{on}=-\frac{t}{C_{fb}ln\alpha/2^N}, \tag{20}$$

where α is maximum error, N is the bit of ADC and t equals to one quarter sample rate. The relationship between R_{ON} and the width of transistor is expressed as

$$R_{on}=\mu C_{ox}\frac{W}{L}V_{gt} \tag{21}$$

It is seen that the ON resistance is signal-dependent, which introduces the distortion to ADC.Hence, special techniques, such as bootstrapping[54] or clock-boosting[55], are required. However, area and power are increased.

Besides, the parasitic capacitor of the switch is also of great significance. The gate-source capacitor and the gate-drain capacitor cause clock feedthrough. The signal path is affected by the clock signal, which brings the spurious tone in output. Moreover, the switch activity causes charge injection owing to the charge stored on inversion layer. Even though it can be cancelled by bottom-plate sampling[56], the switch size should be minimized to reduce charge injection. Therefore, the tradeoff between charge injection and time constant should be carefully considered.

4.2.2.2 Offset

The transfer function of 1.5b RSD is plotted in Figure 61[57]. The non-ideal effect of the gain stage and the comparator brings offset. The effect of offset is shown in Figure 63[57]. It is seen that the offset may cause the residue output exceeding the full scale voltage, which resulting in error in digital code. The allowable offsets of the comparator are $\pm V_{ref}$, which can be compensated by the 1.5b RSD. Otherwise, the residue voltage will

exceed the full scale range. Therefore, the threshold voltage is important for comparator design.

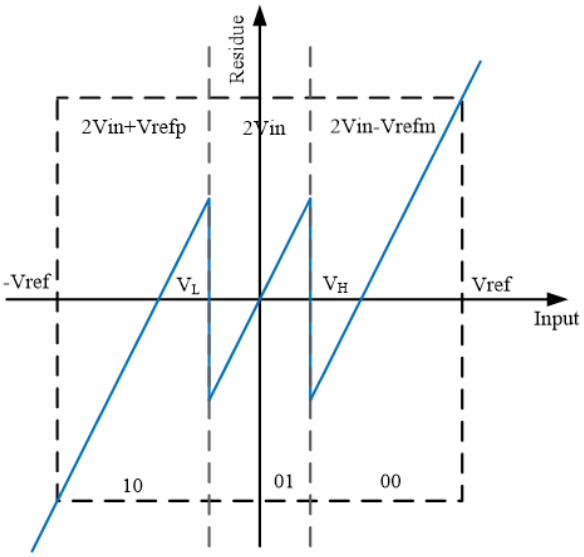


Figure 62 Transfer Function of 1.5b RSD

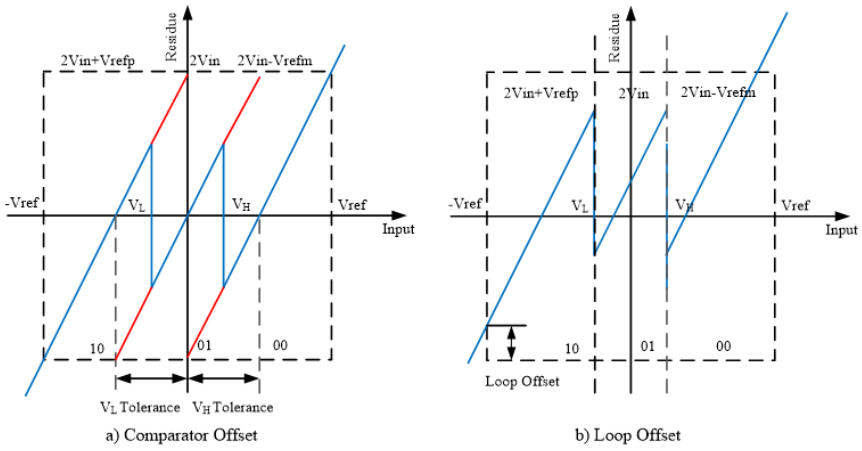


Figure 63 Effect of offset and error

4.2.3 Overview of PGA

A PGA is added to the front of the 10b ADC as it will help increasing dynamic range as well as detecting signals as small as few hundreds of microvolts. The complexity in identifying small signals is that the system should generate very low noise. As for 10b ADC, the noise floor is around 976μV. That means it is impossible to detect signal less than 976μV magnitude. Therefore, a PGA is necessary.

The gain of the PGA is programmable through the digital input. It is configured either for a decade gain like 1, 10, 100, etc. or binary gain such as 1,2,4, etc. The topology of the PGA is shown in Figure 64. The design issues such as how to implement the switch, gain accuracy, DC drift over PVT and distortion should be considered.

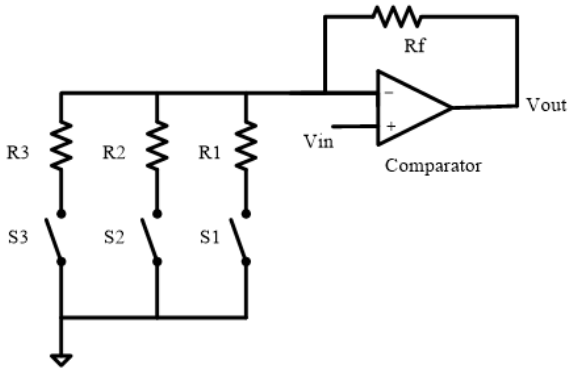


Figure 64 Topology of PGA

As seen in Figure 64, the gain is determined by the ratio of resistance. Thus, the switch resistance, R_{ON}, has influence on the gain accuracy. What's more, the R_{ON} varies with signal magnitude and temperature, which brings gain variation. Therefore, the R_{ON} independent gain expression is desirable.

The switch capacitor based PGA is introduced because of the following reasons. The structure of the switch capacitor based PGA is displayed in Figure 65. The gain is determined by the capacitor ratio, which has less variation across PVT and the R_{ON} only affects the settling time. With careful design, the high accuracy can be implemented and the settling time can easily satisfy the requirement.

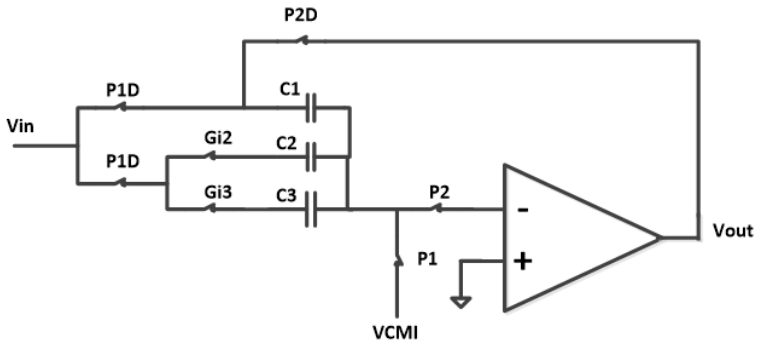


Figure 65 Switch Capacitor Based PGA

4.3 Pipeline ADC Design and Layout

4.3.1 Op-amp Design and Layout

ADC power specification is summarized in Table 6.

Table 6 Targeted for key specs of the ADC.

Specs	Resolution	Full scale swing	Power of 5opamps	Comparator Power (total)	RSD logic Power	Clock buffers power	Vdd	Total Power
Target	10 bits	$1V_{p-p}$	2.8 mW	0.5 mW	1 mW	1mW	1.8 V	5.6mW

In order to achieve the specs, a telescopic cascade is used, which is shown in Figure 66. The Thermal noise floor was taken to be ~65dB. The quiescent current, I_{M1}, is determined by the capacitor value and the settling time of SHA stages. As the first stage is the dominant one, both of its small signal and large signal settling analysis should be considered.

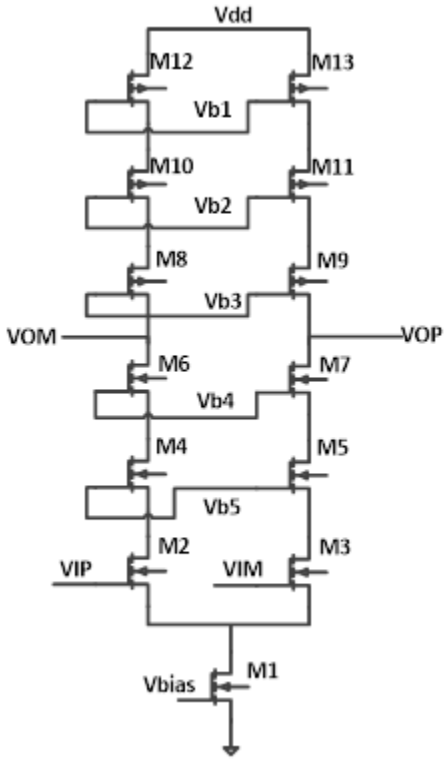


Figure 66 Topology of telescopic cascade op-amp

The unity gain frequency and slew rate of op-amp represent the small signal and large signal settling respectively. The unity gain frequency equation has been discussed in section 4.2.2.1. But the parameter β is different here.

$$\beta = C_1 / \left(2C_1 + C_{GS,M2}\right) = 0.45 \tag{22}$$

$f_{clk}=2.5\times10^7$ Hz is the clock frequency of the ADC. Plugging these numbers into the equation given above, the specification for the Bandwidth is calculated to be

$$BW > 212MHz \tag{23}$$

The slew rate of the opamp is equal to

$$SR = \frac{I_{tail}}{C_L} = \frac{V_{FS}}{t_{SL}} \tag{24}$$

where, V_{FS} is the full scale voltage and t_{SL} is the time of large signal slewing. The total settling time has to be less than 20ns which is half of the sampling period for a 25MSPS ADC. For a load capacitance of 0.31pF, the slew time t_{SL} is calculated to be 10ns.

The gain of the op-amp is calculated above as 72dB.Thus, the tail current is supposed to be 95μA and the saturation voltage $V_{DS,SAT}$ is assumed to be 1150mV for the transistors. The gain related to the small signal is given as

$$A \cong g_{m,M2}\left(\left(g_{m,M6}r_{o,M6}g_{m,M4}r_{o,M4}r_{o,M2}\right)^{-1} + \left(g_{m,M8}r_{o,M8}g_{m,M10}r_{o,M10}r_{o,M12}\right)^{-1}\right)^{-1} \quad (25)$$

where, g_ms are the transconductances and r_0s are the output resistances of the transistors. $g_m r_0$ is estimated around 100 so that the gain of telescopic cascade is assumed to be 60dB. In order to achieve the gain over 72dB, the input transistor sizes are increased to increase the g_m values.

The layout of the telescopic cascade is shown in Figure 67. The bode plot of extracted telescopic cascade op-amp is given in Figure 68. The gain is 72.5dB and the BW is 233MHz with a phase margin of 80dB. The simulated results, which are summarized in Table 7, satisfy the calculated requirement.

Table 7 Summary of post simulation result

	Gain	BW	Power	Cload
Target	72dB	212MHz	400μW	0.31pF
Achieved	72.5dB	233MHz	300μW	0.31pF

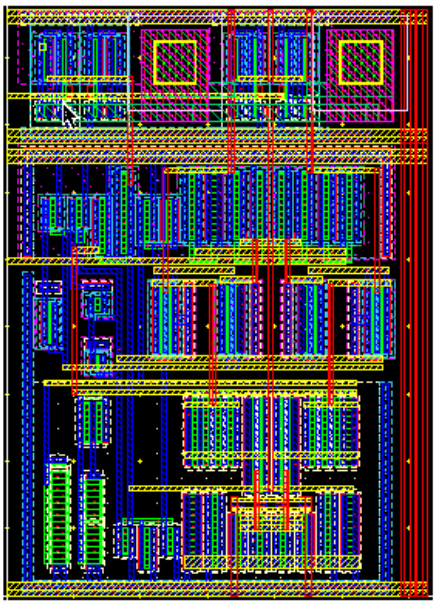


Figure 67 Layout of telescopic cascade op-amp

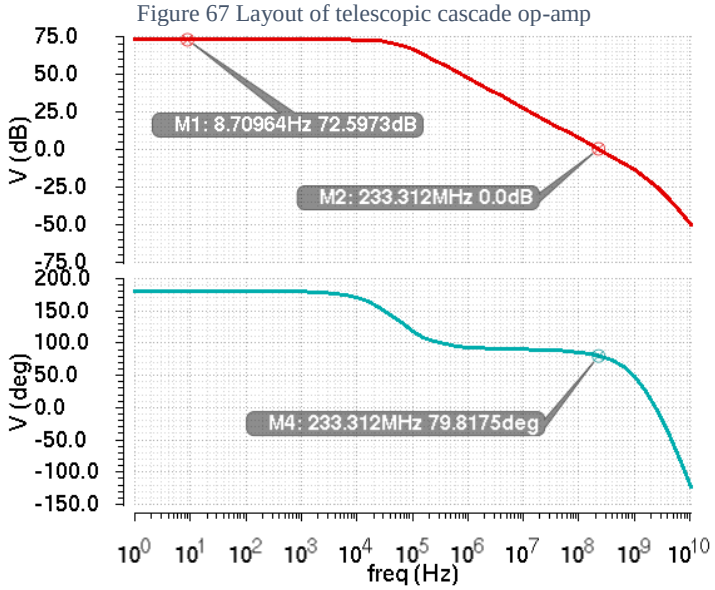


Figure 68 Bode plot of telescopic cascade op-amp

Corner simulations are applied to the gain, BW and phase margin. It is necessary to estimate the transistor behavior at the worst possible specs. The specs are provided from pdk (Process Design Kit) supplied by the vendor. LV represent low voltage(1.62V) and HV represents(1.98V). Meanwhile, S stands for slow and F stands for fast.

Table *8* shows the summary of gain stage performance under different PVT.

Table 8 Gain stage performance under process and temperature corner parameters.

Corner	Nominal	SS - 40 LV	SS - 40 HV	SS 85 LV	SS 85 HV	FF - 40 LV	FF - 40 HV	FF 85 LV	FF 85 HV	FS - 40 LV	FS - 40 HV	FS 85 LV	FS 85 HV	SF - 40 LV	SF - 40 HV	SF 85 LV	SF 85 HV	Ave
DC Gain (dB)	71	50	72	68	71	47	67	67	70	44	62	64	70	53	74	69	71	64
UGF (MHz)	269	112	336	220	263	106	333	230	280	82	269	211	266	149	358	231	277	235
Phase Margin (Deg)	76	84	76	76	77	85	77	77	77	86	79	77	77	83	76	76	77	79
SFDR (dB)	83	76	79	81	51	74	79	67	48	66	83	71	50	80	79	69	49	70
ENOB (Bits)	12	11.2	11.7	11.6	8.2	11.1	12.6	10.6	7.7	10.2	12.1	11.2	8.0	12.0	12.0	10.9	7.9	10.6

4.3.2 Comparator Design and Layout

Accuracy, which is defined as the magnitude of the offset voltage, and power consumption are the two most important aspects of the comparator to be designed and used in this design. Two of these will be used in each 1.5 bits RSD of the 10bit ADC. The last 3-bit flash stage will use 7 comparators.

Without calibration, the offset voltage is expected to surpass 10mV and consumes less power. İf calibration was applied, several cases for power consumption overhead are summarized in Table 9.

Table 9 Summary of power consumption in comparator with calibration

	Offset voltage	Power consumption	Area
[58]	1.3mV@250MHz	40µW@1V	544µm^2@90nm
[59]	3.8mV@500MHz	39µW@1.2V	152µm^2@90nm
[60]	1.89mV@1GHz	60µW@1V	1250µm^2@65nm

For a 10-bit design, the comparator without calibration is sufficient to satisfy the final

ADC accuracy requirements. The basic structure of the comparator is shown in Figure 69[61]. M14 & M15 are added to reduce the kickback noise (the bias network for these is not shown). When V_{latch} is set low, M8 and M13 are both ON, setting the drain of M14 and the M15 to the same voltage that is almost equal to V_{DD}. This same voltage is also seen on both of the output ports. In this phase, called the comparison phase, if (V_{in+}-V_{in-}) is greater than (V_{ref+}-V_{ref-}), then the source of M14 will be at a potential higher than the source of M15. In the opposite case, it will be lower. Once the V_{latch} is set high, M8, M9, M12 and M13 will all turn OFF and V_{out+} will be higher than V_{out-} by a few hundred mVs. As the source-gate overdrive voltage of M10 will be larger than that of M11, V_{out+} will continue to be pulled higher and higher until it reaches V_{DD} and shuts off M11, effectively pushing V_{out-} to V_{SS}. If (V_{ref+}-V_{ref-}) were greater than (V_{in+}-V_{in-}), then the exact opposite chain of events would occur with V_{out-} ending at V_{DD}.

The trip point for the comparator is set at 125mV in our simulations. The relationship between the input and the reference (trip point) at the onset of tripping is given by

$$V_{in^+} - V_{in^-} = \frac{\beta_3}{\beta_1}(V_{ref+} - V_{ref-}) \tag{26}$$

where β is the width to length ratio of a transistor. $(W/L)_{1,2}$ is set to be four times $(W/L)_{3,4}$ to reduce the area.

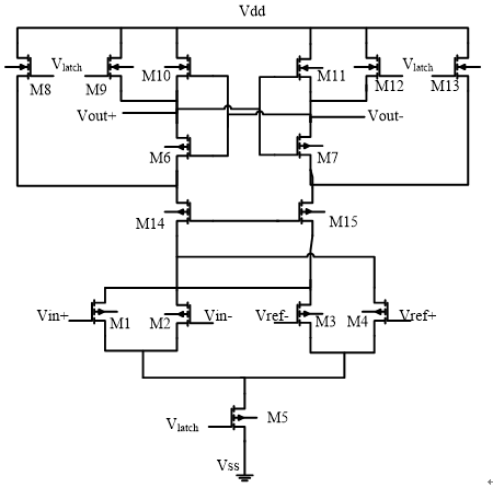


Figure 69 Topology of comparator

The main parameters for a comparator are the widths and lengths, the threshold voltages and the mobility of all transistors, and different parasitic capacitances on the output node[62]. Mismatch of the mobility and the threshold voltages are the dominant factors to cause the static offset. The overall static offset voltage σ_{Vos} is expressed as

$$\sigma_{Vos} = (\sigma_{Vos\_M1M4}{}^2 + \sigma_{Vos\_M2M3}{}^2 + \sigma_{Vos\_M6M7}{}^2 + \sigma_{Vos\_M8M9}{}^2 + \sigma_{Vos\_M10M11}{}^2)^{0.5} \quad (27)$$

where M8&M9 and M10&M11 contribute most of the offset. According to the calculation, the static offset voltage is 10.7mV. The dynamic offset comes from the variation among transistors and parasitic capacitors. The mismatch between input transistors has the dominant effect on the offset voltage. The simulation setup given in Figure 70[63] is based on a closed loop stage and is used to access the worst case performance of the comparator. A “typical model” response is shown in Figure 71. With TT corner, at room temperature and a supply voltage of 1.8V, the worst case offset is simulated to be -27.76mV.

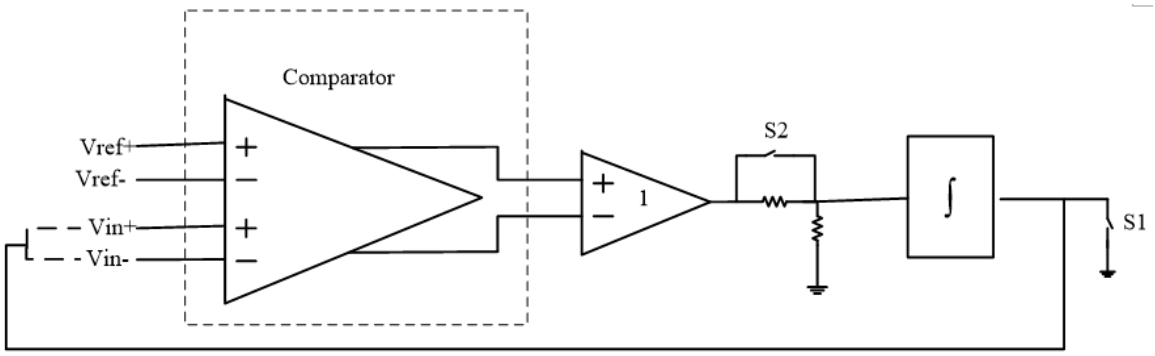


Figure 70 Simulation setup for worst case analysis of a fully differential comparator.

The offset performance under process and temperature corners are given in Table 10. These are acceptable levels as the RSD blocks can easily compensate for these as they are lower than 125mV which is half an LSB for the 2bits stage ADCs.

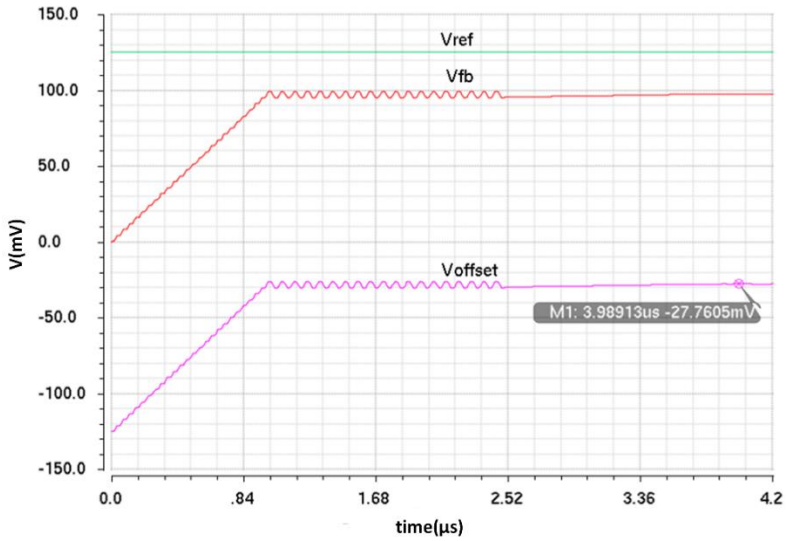


Figure 71 Typical output from the offset simulation circuit.

Minimum area and power are important parameters in the overall design, however, minimizing them will make the comparator slower, as well as increase the offset. Simulation results for five different layout sizes are shown Figure 72. It is found out that even for the smallest size (transistor width = 1um, length = 180nm) the operation takes 0.5ns to complete for this ultra-fast topology and a very small area can thus be used in the design. The offset calculated for the smallest tested transistor sizes also meets the

specifications of the 10-bit pipeline ADC in which redundant signed digit (RSD) error correction is used. RSD cancels out the effects of comparator offsets in 1.5-bit stages, but not in the 3-bit flash. This is fine as the errors at this last stage, when referred to the input by the total gain of the previous five stages turns out to be much less than 1LSB which is about 4mV for this ADC.

Table 10 Offset performance under temperature and process corners.

TT Corner			
Temperature / Supply	-40°C	27°C	160°C
1.62V	-28.80mV	-27.54mV	-27.10mV
1.8V	-29.09mV	-27.92mV	-27.46mV
1.98V	-29.36mV	-28.20mV	-27.76mV
SS Corner			
Temperature / Supply	-40°C	27°C	160°C
1.62V	-29.00mV	-27.48mV	-26.76mV
1.8V	-29.17mV	-27.75mV	-26.94mV
1.98V	-29.47mV	-27.94mV	-27.40mV
FF Corner			
Temperature / Supply	-40°C	27°C	160°C
1.62V	-28.60mV	-27.71mV	-27.32mV
1.8V	-29.04mV	-28.05mV	-27.77mV
1.98V	-29.27mV	-28.35mV	-28.22mV
SF Corner			
Temperature / Supply	-40°C	27°C	160°C
1.62V	-29.23mV	-27.77mV	-26.99mV
1.8V	-29.50mV	-28.11mV	-27.44mV
1.98V	-29.88mV	-28.40mV	-27.93mV
FS Corner			
Temperature / Supply	-40°C	27°C	160°C
1.62V	-28.48mV	-27.42mV	-27.18mV
1.8V	-28.63mV	-27.66mV	-27.38mV
1.98V	-28.85mV	-28.84mV	-27.76mV

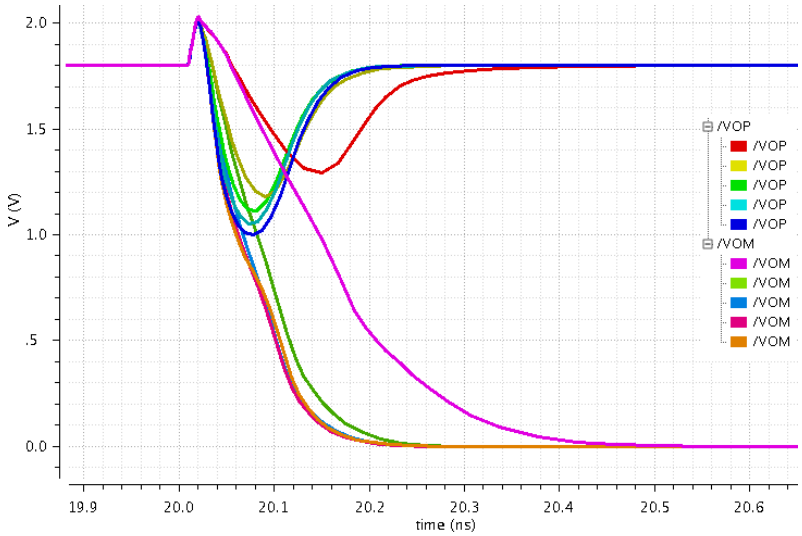


Figure 72 Comparator switching characteristics for different layout areas from parasitic extracted circuit

Monte Carlo simulation results as given in Figure 73 reveal a mean and standard deviation for the offset voltage of 328µV and 9.16mV respectively.

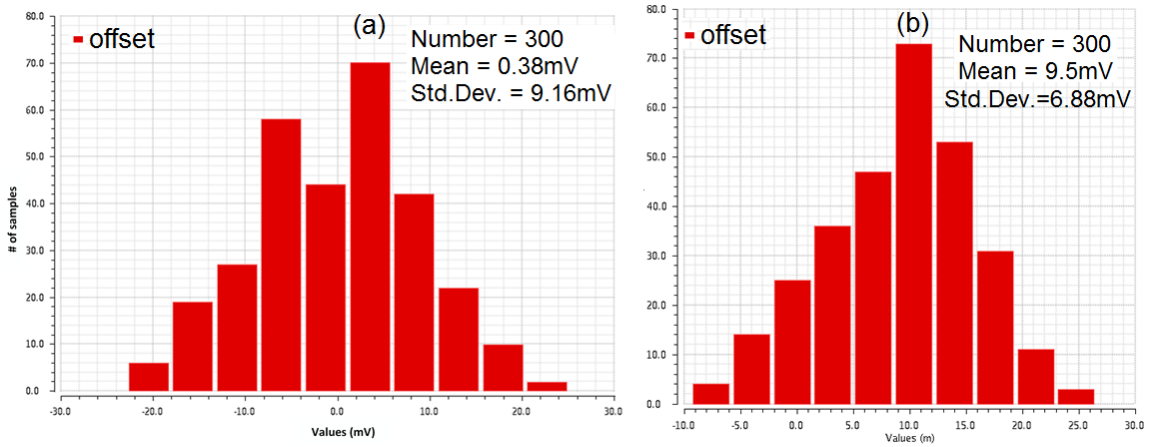


Figure 73 Offset voltage distribution given by a histogram resulting from a Monte-Carlo simulation for a) schematic simulation b) parasitic extracted circuit simulation.

4.3.3 Digital Block Design and Layout

The RSD LOGIC, shown as Figure 74, consists of a full adder, a half adder and a D flip flop.

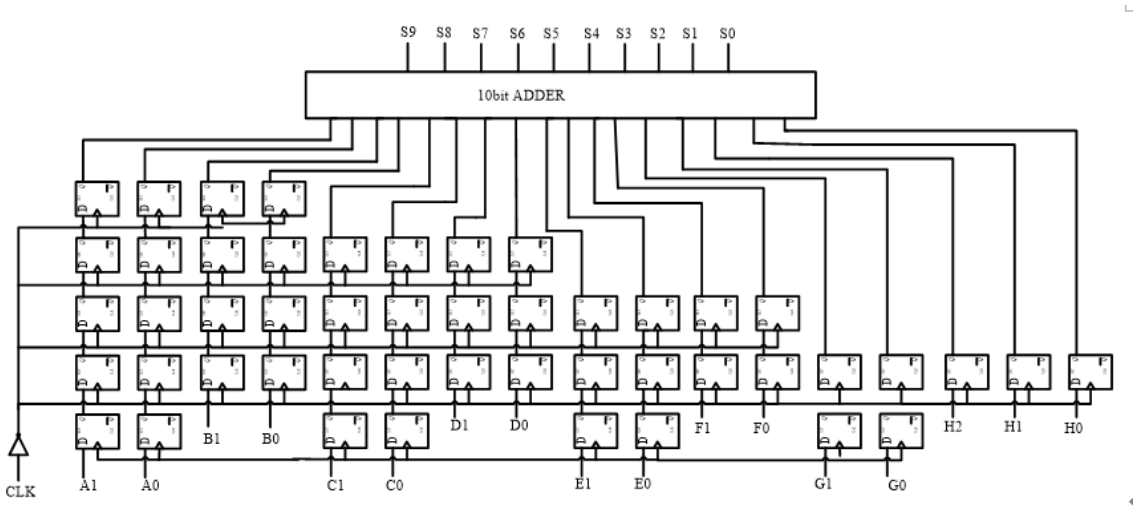


Figure 74 RSD_LOGIC

The structure of the D flip flop is shown in Figure 75. TSPC flip flop has the advantage of single clock distribution, small area for clock lines, high speed and no clock skew. The performance of D flip flop described in Table 11 demonstrate it can work at high frequency with low power consumption.

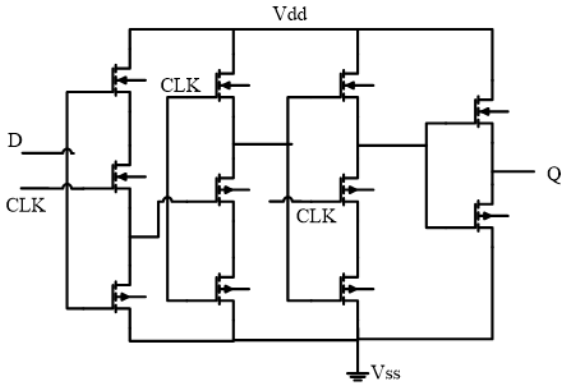


Figure 75 D flip flop

Table 11 D flip flop

Cload=10fF		
T_{cq_r}=75ps	T_r=61ps	Power consumption=3.5μW
T_{cq_f}=138ps	T_f=66ps	

The topology of the half adder and the full adder are shown in Figure 76 and the simulated performance of these circuits is described in Table 12 and Table 13.

Table 12 Half Adder

Cload=6Ff		
T_{S_r}=70ps	T_r=145ps(S)	Power consumption =33.9μW
T_{S_f}=130ps	T_f=155ps(S)	
T_{Cout_r}=80ps	T_r=67ps(Cout)	
T_{Cout_f}=99ps	T_f=75ps(Cout)	

Table 13 Full Adder

Cload=6Ff		
T_{S_r}=260ps	T_r=105ps(S)	Power consumption=47.5μW
T_{S_f}=250ps	T_f=103ps(S)	
T_{Cout_r}=161ps	T_r=94ps(Cout)	
T_{Cout_f}=160ps	T_f=94ps(Cout)	

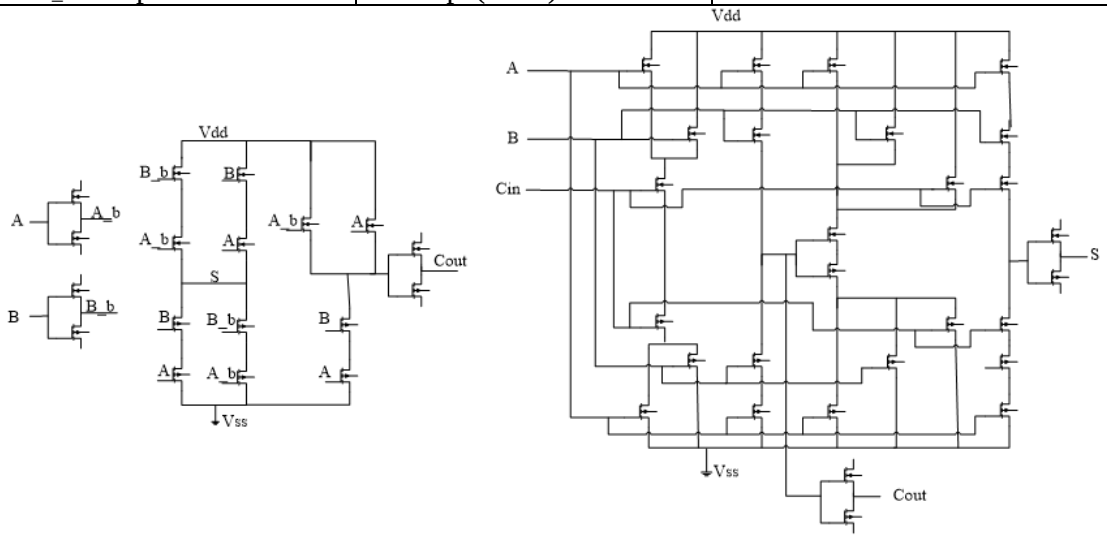


Figure 76 Half Adder and Full Adder

A RSD LOGIC is located according to the gain stages distribution since it is the last stage of the ADC. The layout of the RSD LOGIC is presented in Figure 77.

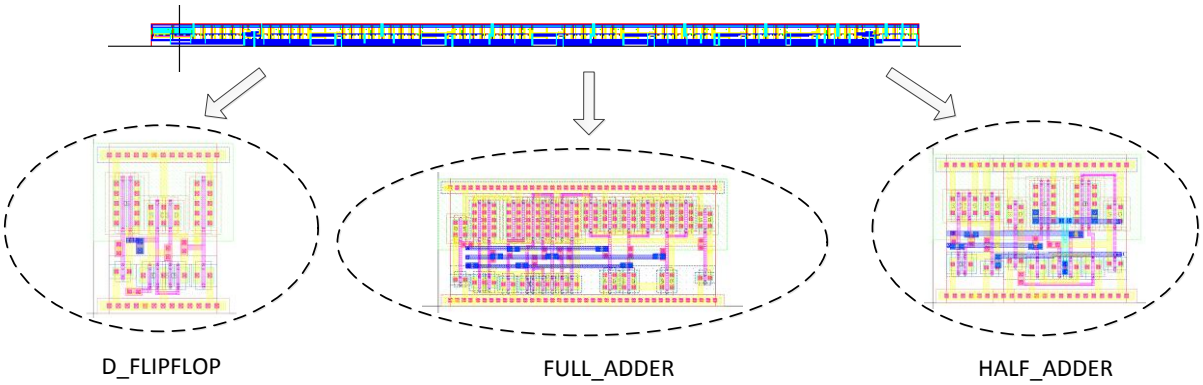


Figure 77 Layout of RSD LOGIC

Besides, the clock generator capable of generating non-overlapping and delayed clocks for the ADC out of a single-ended clock signal is given in Figure 78. The reference clock signal that is either generated on-chip or off-chip is fed in through the lone port on the left-hand side of the schematics. The two ports towards the center of the schematics at the very top and bottom give out the overlapping fully differential clock signals. The delays of the even number of inverters at the right-hand side (a couple is used in this case) define the duration of the non-overlapping portions of the clocks.

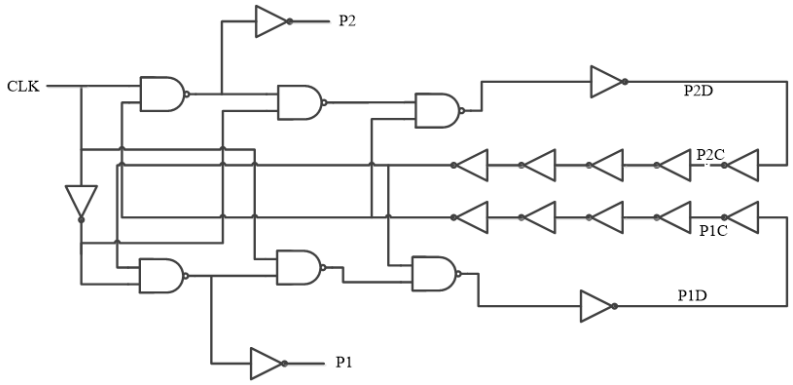


Figure 78 Non-overlapping clock generator schematic.

The clock signals obtained in simulations are plotted in Figure 79. The falling edge separation between P1 and P1D is easily discernable whereas P2 and P2D raise simultaneously, as required.

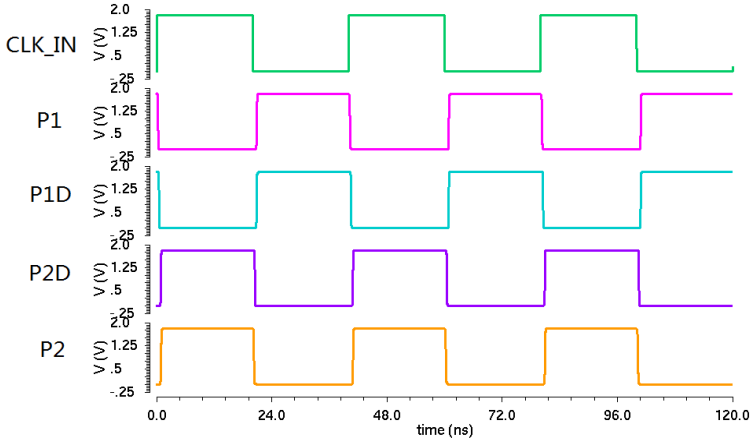


Figure 79 Non-overlapping clock signals simulated with transistor models in Cadence.

4.3.4 1.5b RSD Simulation Result

The layout of 1.5b RSD is shown in Figure 80. Care was taken to have the gain stage completely symmetric to avoid even harmonics.

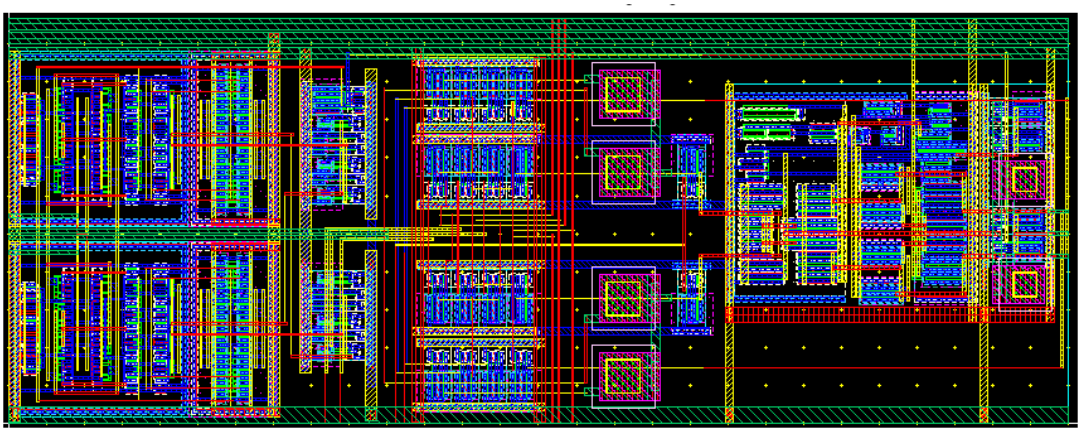


Figure 80 Layout of 1.5bit MDAC stage

The output waveform settles to within 300μV which is better than half an LSB as shown in Figure 81.

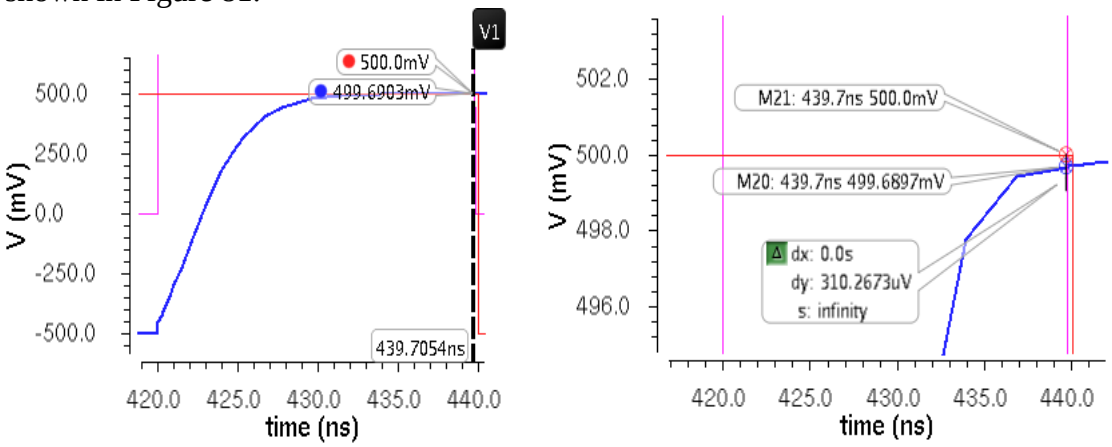


Figure 81 Step response of the parasitic extracted circuit of 1.5bit MDAC stage to a 1Vp-p input signal.

A full scale 12.5MHz sine wave is applied to the input for the THD characterization. A 512 points FFT is taken of the output in Figure 82. The THD is calculated to be -75dB for the extracted circuit.

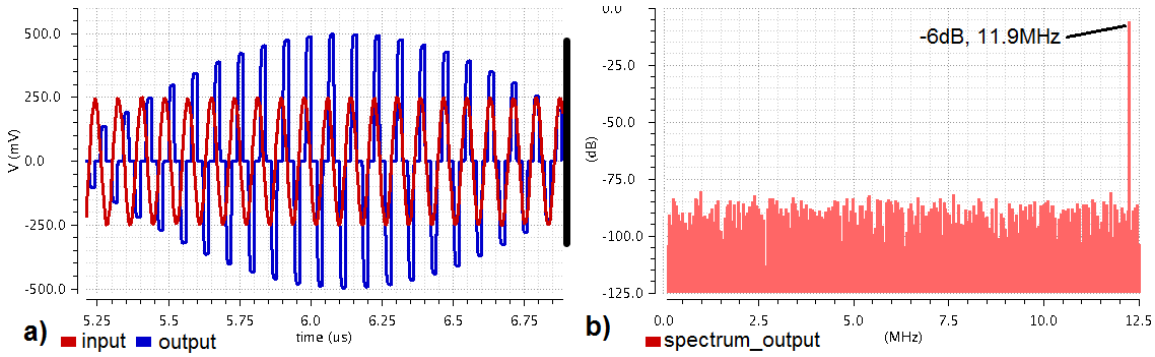


Figure 82 THD results ofr the extracted 1.5bit MDAC stage: (a) Time domain input and output of the Opamp to measure SFDR, (b) the FFT output.

4.3.5 ADC Simulation Result

The 8-bit ADC is simulated first, using 5 1.5 bit RSD and a 3-bit flash at the end. A full scale 11.923MHZ sine wave input is applied to obtain coherent sampling. A 128-point FFT is taken, shown in Figure 83. The transient input and output, and the FFT of the output show the ENOB is 7.87 Bits.

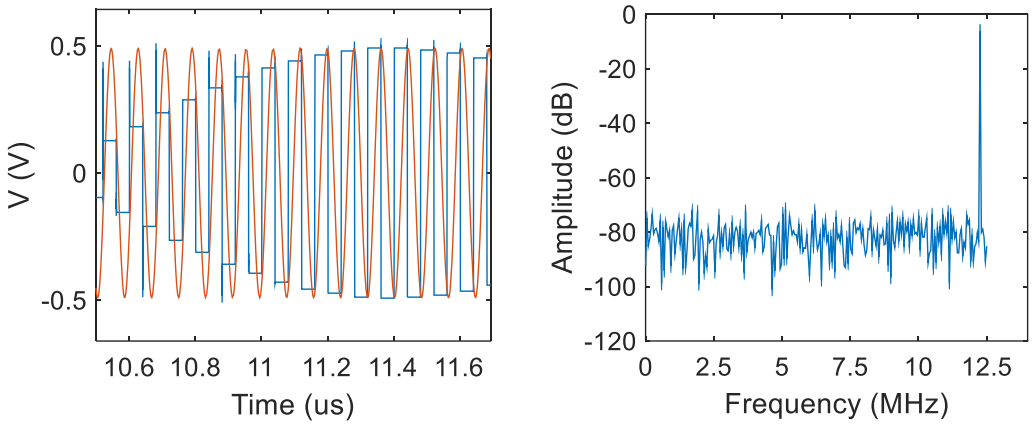


Figure 83 The temporal and spectral responses of the 8-bit ADC

Process and temperature simulations of 8-bit ADC indicates the worst ENOB is 6.2 bits and the average ENOB is 7.42 bits.

Adding two extra 1.5b RSD results in a 10b ADC, whose layout is shown in Figure 84. The sampling capacitor is creased to 200fF in order to reduce the thermal noise. Reference voltages are generated on the chip through buffers for MDAC in order to reduce

the voltage drop across the metal routing. 3b Flash ADC does not have a reference voltage buffer because the required accuracy of 3b Flash ADC is as low as 125mV. The voltage drop can be compensated via excessive voltage input.

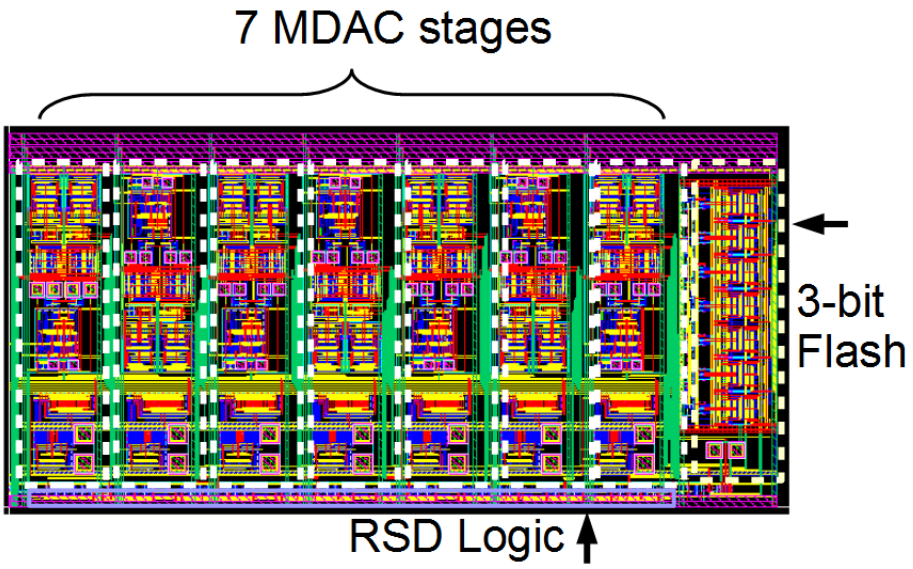


Figure 84 Layout of complete 10 bit ADC

Apply the same input signal to 10b ADC and a 128-point FFT is taken from the output of the ADC in Figure 85. The ENOB is 8.2 bits.

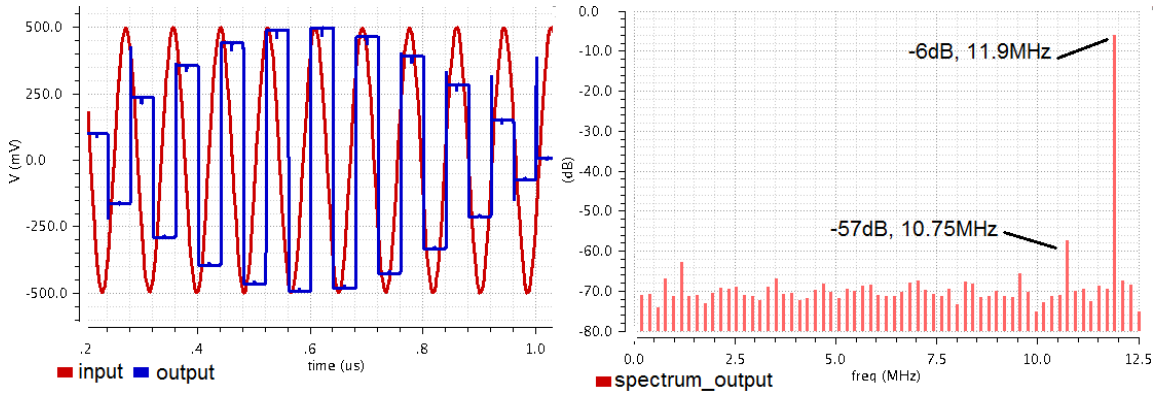


Figure 85 The temporal and spectral performance of the post-layout parasitics extracted 10 bit ADC.

Figure 86 and Figure 87 show the area distribution and power portions for different parts of the ADC. Total area of the ADC is estimated to be 0.1mm^2 and the total power is 5.8mW.

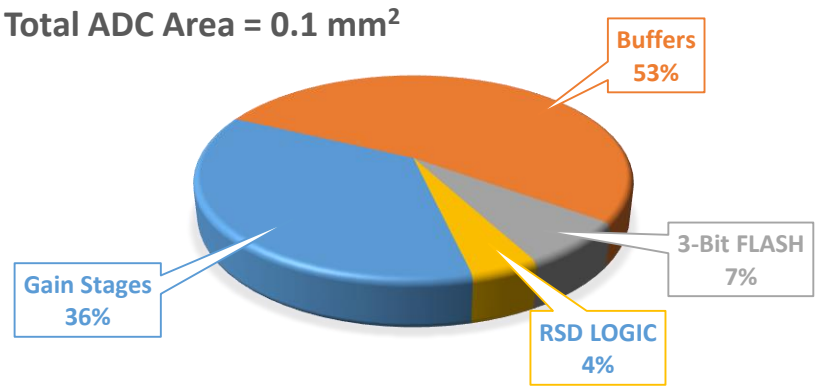


Figure 86 The area fractions of different ADC blocks.

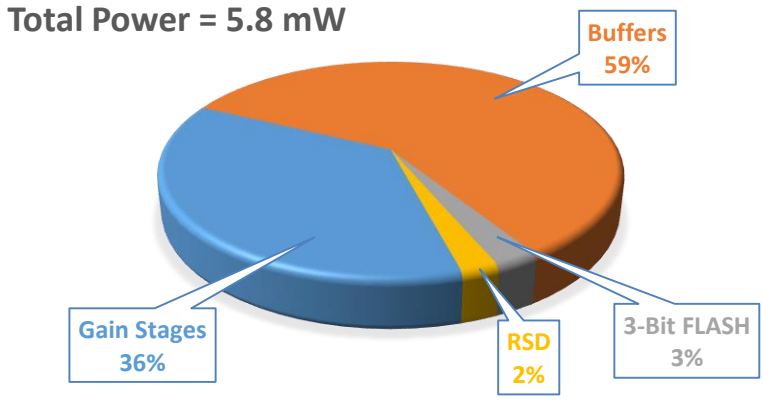


Figure 87 The power consumption ratios for the ADC blocks.

4.4 PGA Design and Layout

The gain stage of the ADC with larger input sampling capacitors is applied to implement PGA. The PGA is made up of 3 gain stages, given in Figure 88. The gain is controlled by the six digital inputs.

The layout of the PGA is shown in Figure 89. The post simulation results of the PGA with a gain factor of 1 and 32 are shown in Figure 90. The input signal for the gain of 1 is 1Vp-p and the input signal for a gain of 32 is 31.25mVp-p. The ENOB are 8.5bits and 5.12bits respectively. Figure 91 shows the noise at the input node of the PGA. The total

noise is 296μV, which is far from 976μV. Besides, the M28, the column select switch, is the dominant factor in noise distribution rather than the PGA itself.

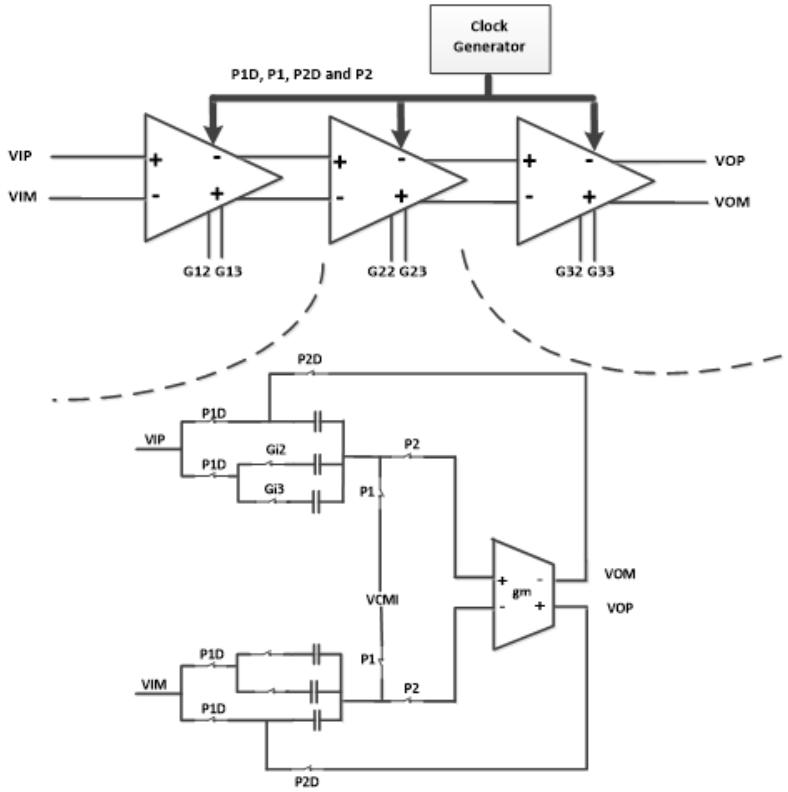


Figure 88 PGA structure

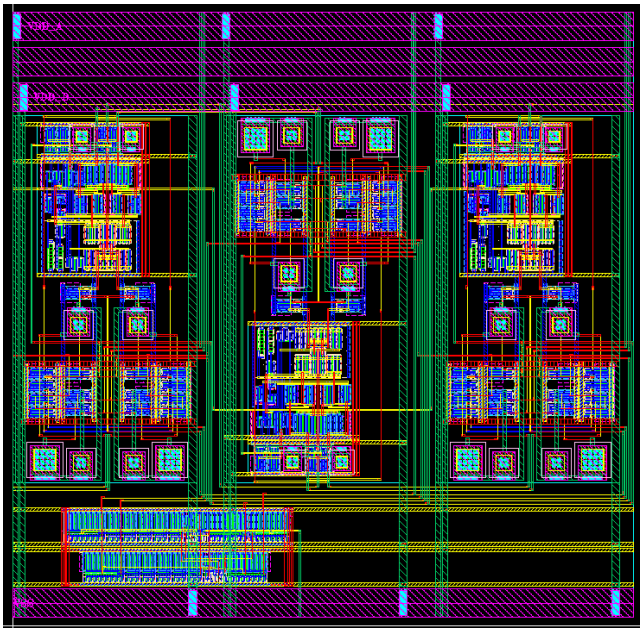


Figure 89. Layout of PGA

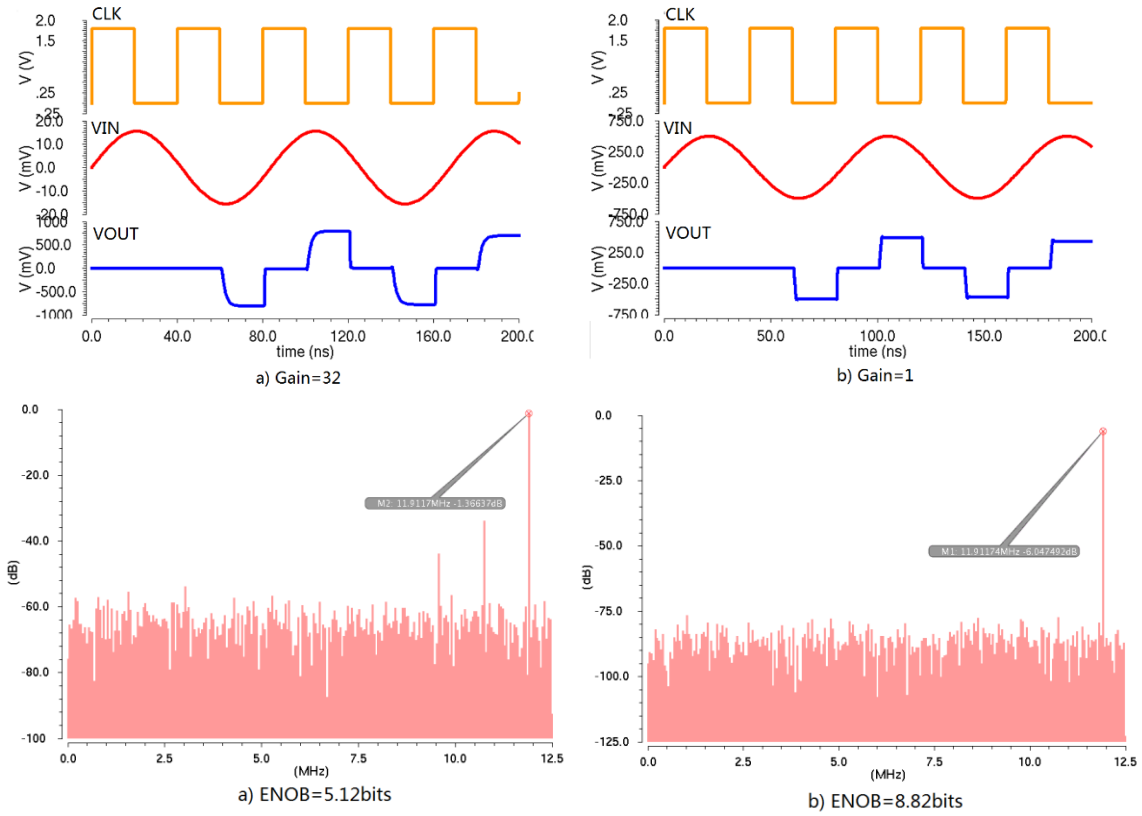


Figure 90 Post layout simulations of Extracted PGA in a) gain factor of '1' mode b) gain factor of '32' mode

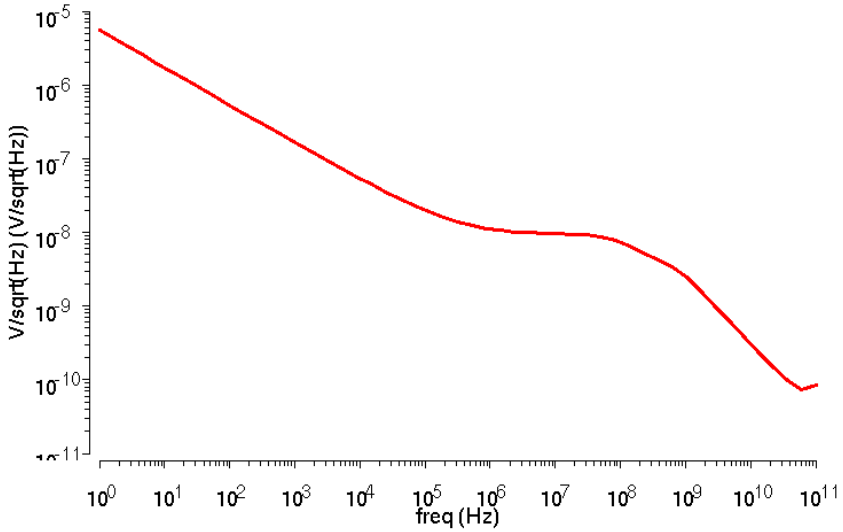


Figure 91 Input referred noise of first gain stage in the PGA

4.5 Chip Testbench

ADC block is placed in a test chip to measure the performance. The chip is packaged with CPG13229 and the bonding diagram is shown in Figure 92.

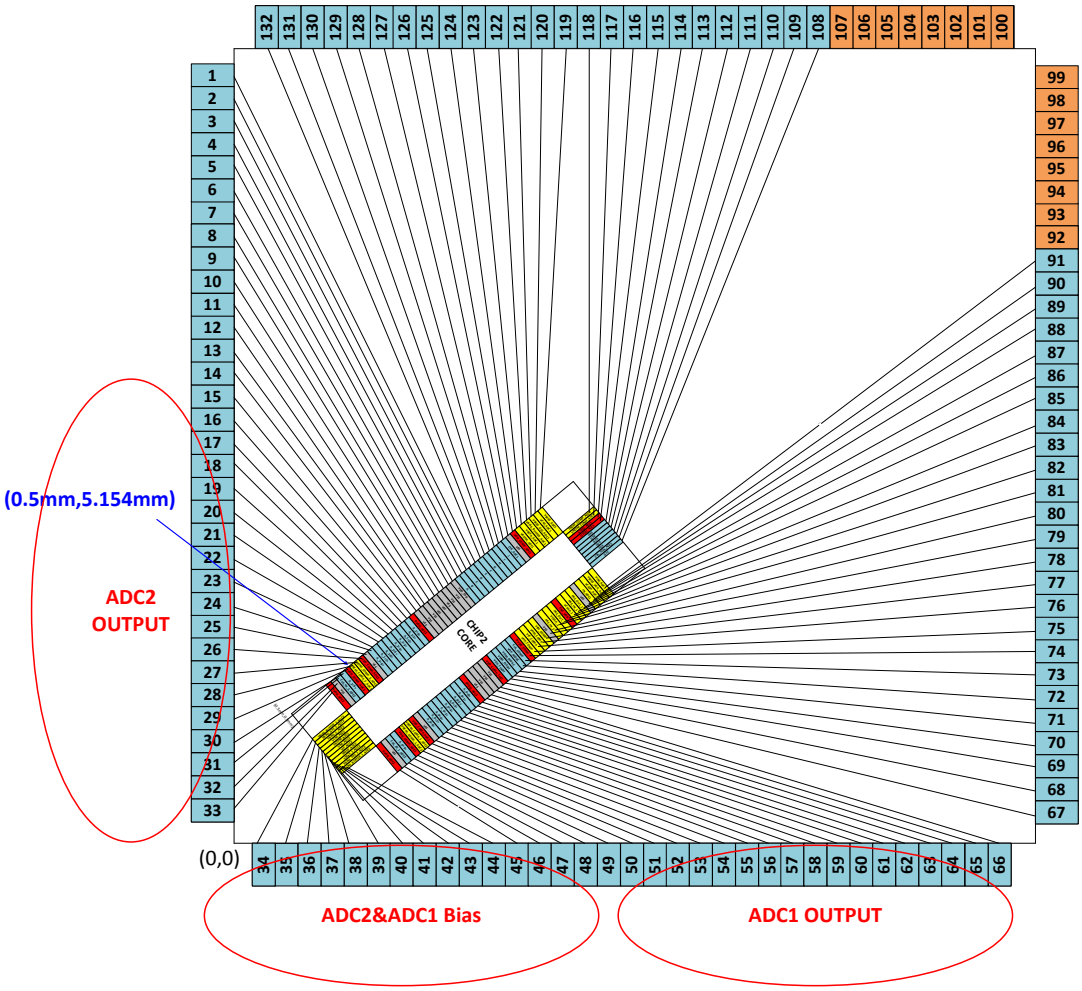


Figure 92 Bonding diagram of test chip

The input signals are summarized in Table 14. They are categorized into three types: DC voltage input, current bias and input signal with MHz frequency.

Table 14 Summary of input signals

Signal Name	Value
DVDD/AVDD/VDD_COMP	1.8V
VREFM/VREFM_COMP	0.65V
VREFP/VREFP_COMP	1.15V
CLK_IN	25MHz frequency
VCM	0.9V
VIP&VIM	DC Voltage: 0.9V Amplitude: 0.25V
VBIAS_GS1/VBIAS_BUFFER/ VBIAS_ADC	7.93uA/111.25uA/47.58uA

In order to have clean and stable DC voltage input, LDO, MAX 8516, is connected. The configuration is shown in Figure 93. Besides, several decoupling capacitors are added to the DC voltage input pins to reduce noise.

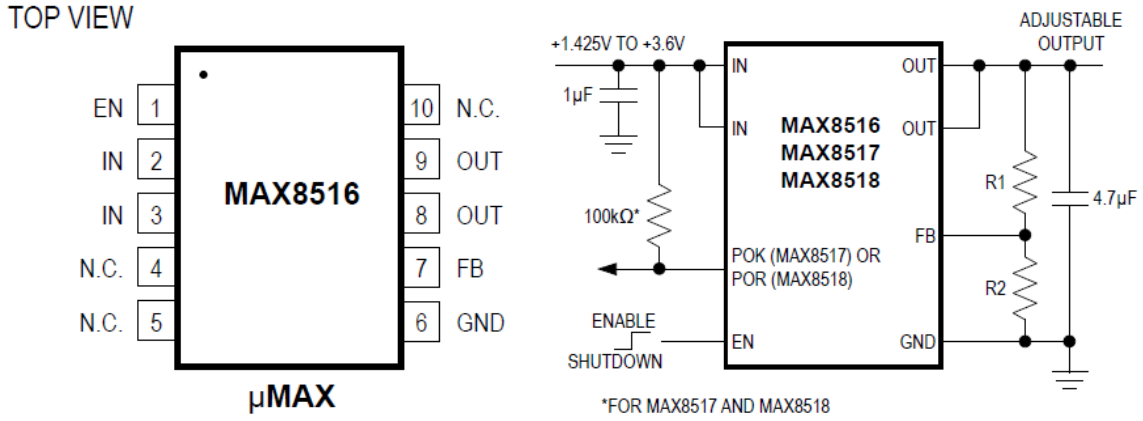


Figure 93 LDO configuration

According to the equation that Vout=Vfb(1+R1/R2), the R1 values are calculated in Table 15. Vfb is fixed to 0.5V.

Table 15 Summary of R1 values

Pins on Chip	Chips used on Board	Resistance (R2=500Ohm)
AVDD	MAX8516	R1=1.3KOhm
DVDD	MAX8516	
VDD_COMP	MAX8516	
VREFM/VREFM_COMP	MAX8516	R1=150Ohm
VREFP/VREFP_COMP	MAX8516	R1=650Ohm
VCM	MAX8516	R1=400Ohm

There are two methods to generate current bias. One is the current bias chip and another one is a potentiometer. The chip configuration of LM334 is shown in Figure 94.

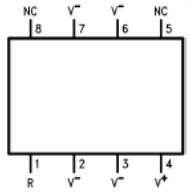


Figure 1. SOIC-8 Surface Mount Package
(LM334M; LM334M/NOPB; LM334MX; LM334MX/NOPB)
See Package Number D

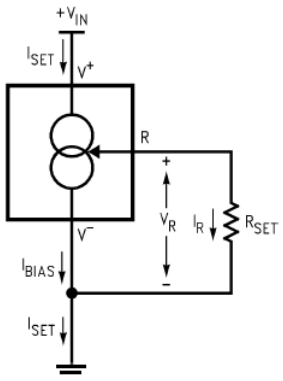


Figure 94 Chip configuration of current source

The target current is calculated as

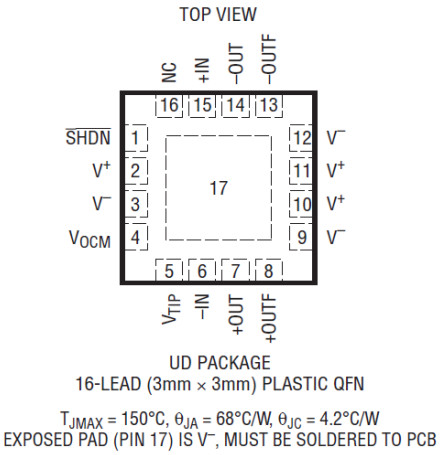
$$I_{SET} = I_R + I_{BIAS} = (\frac{V_R}{R_{SET}})(\frac{n}{n-1}) \quad (28)$$

Where n is typically 18 and V_R is 64mV/298K for $2\mu A \leq I_{SET} \leq 1mA$. The Rset is calculated in Table 16.

Table 16 Summary of Rset Value

Pins on Chip 2	Chips used on Board	Rset(Potentiometer)
VBIAS_GS1	LM334	8.55KOhm
VBIAS_BUFFER	LM334	609 Ohm
VBIAS_ADC	LM334	1.42KOhm

Differential input for ADC is generated through a single input to differential output chip LTC6406. The configuration is given in Figure 95.



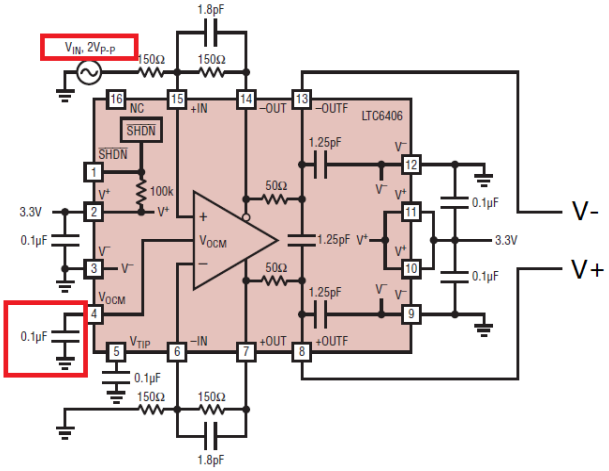


Figure 95 Chip Configuration of Single to Differential chip

V_{OCM} should be connected to 0.9V and Input signal should be replaced by 1Vp-p.

A logic analyzer is applied to capture the digital outputs. The whole test diagram is displayed in Figure 96. The synchronized clock is generated through signal generator equipment, Siglent SDG5122.

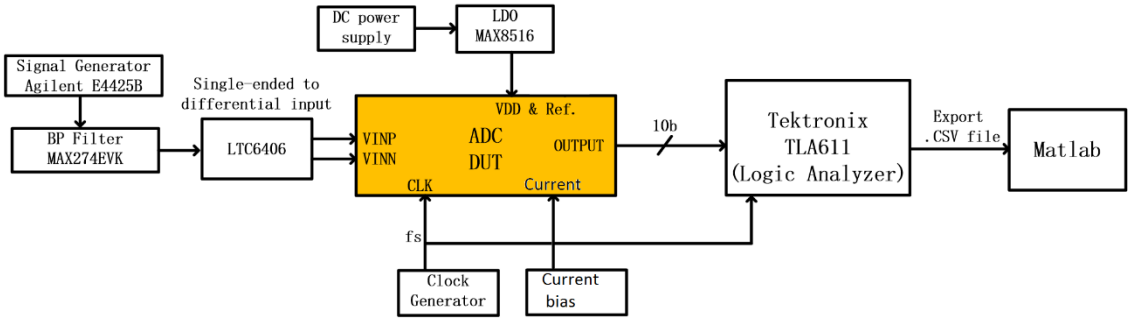


Figure 96 Logic analyzer test method system

The final PCB board is drawn in Figure 97. The impedance match of the clock signal is important. Therefore, the routing metal is set to 15mm width and a 50Ohm resistor is terminated.

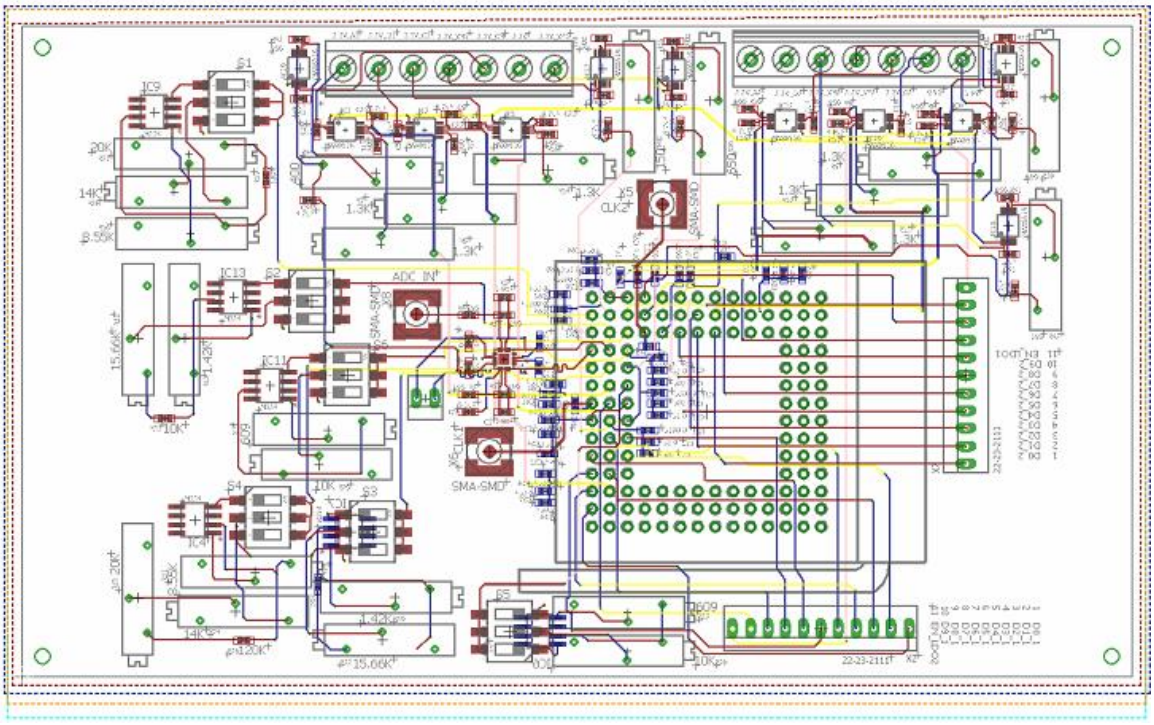


Figure 97 PCB Board

CHAPTER 5

CONCLUSION

A high speed sensor which is fabricated in the 180nm standard CMOS process is presented in this thesis. The die micrograph of whole chip is shown in Figure 98.

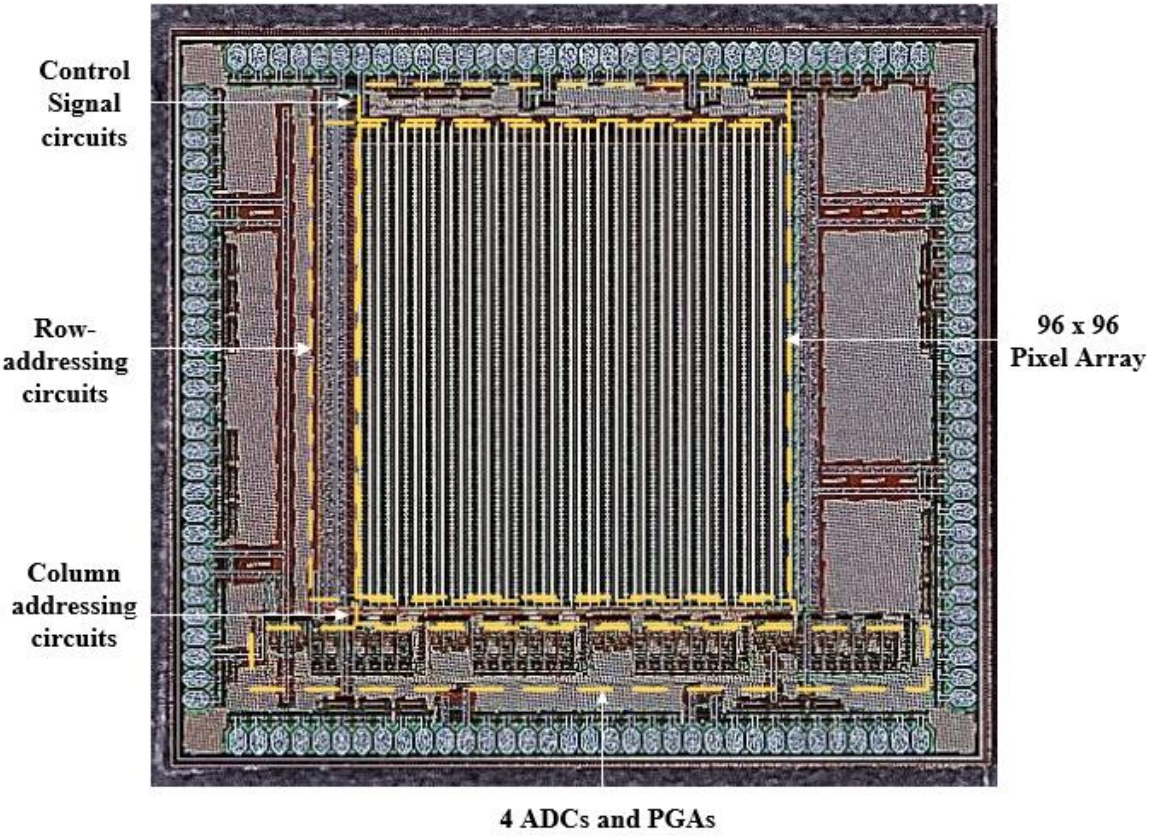


Figure 98 Die Micrograph of whole image sensor chip

The pixel circuit is designed to minimize the leakage current, which makes it possible to detect low light signals and increase image accuracy. The pixel sharing technique increases the fill factor to 64.625%. Besides, the readout chain circuit design makes it suitable to achieve high readout speed and capture low light image. The performance of the image sensor chip is summarized in Table 17. The frame rate is 10508 fps operating in continuous mode. The post simulation of each block proves that the circuit and layout deign satisfy the requirement of high speed, high fill factor and low leakage. The test results of

pixel array indicate that the photodiode, pixel and selection circuit work as designed.

Table 17 Summary of image sensor chip

Technology	0.18μm CMOS
Supply voltage	1.8V
Die size	3.1mm x 3.4mm
# of Pixels	96^{H} x 96^{V}
Pixel size	20μm x 20μm
Fill factor	64.625 %
Maximum frame rate (continuous mode)	10508 fps
Readout rate	96 M pixels/sec
Full well capacity	$121ke^{-}$
Linearity	93.56%
ADC resolution	8.2bits

Due to the time limit, the test results of ADC are not provided here. The test result will help improving the performance of image sensors. Apart from testing, several techniques should be applied to reduce noise and power with increased image accuracy. If possible, the pinned photodiode is preferable. It has low dark current, high conversion gain and high sensitivity. What's more, a 12b ADC is desirable to achieve high image accuracy. If the test result shows that the 10b ADC works well, the same structure will also be applied to the 12b ADC. Higher resolution will definitely come with more power. Therefore, the low power technique should be found out. CDS technique should also be implemented. It will effectively reduce the noise from pixel circuit. Finally, the on-chip calibration can be used in the image sensor, greatly reducing the fixed pattern noise[64, 65]. The method discussed above will further improve the performance of image sensor.

REFERENCES

[1] *Image Sensor Market by Type (CMOS, CCD, and Others), Specification, Application (Aerospace, Automotive, Consumer Electronics, Healthcare, Industrial, Entertainment, and Security & Surveillance), and Region - Global Forecast to 2020*. Available: http://www.marketsandmarkets.com/Market-Reports/Image-Sensor-Semiconductor-Market-601.html

[2] M. El-Desouki, M. J. Deen, Q. Fang, L. Liu, F. Tse, and D. Armstrong, "CMOS Image Sensors for High Speed Applications," *Sensors (Basel)*, vol. 9, no. 1, pp. 430-44, 2009.

[3] W. S. Boyle and G. E. Smith, "Charge coupled semiconductor devices," *Bell System Technical Journal*, vol. 49, no. 4, pp. 587-593, 1970.

[4] R. Lineback, "CMOS Image Sensors Regaining Growth Momentum," ed: Sr. Market Research Analyst IC Insights, Inc, 2011.

[5] M. Hillebrand, N. Stevanovic, B. Hosticka, J. S. Conde, A. Teuner, and M. Schwarz, "High speed camera system using a CMOS image sensor," in *Intelligent Vehicles Symposium, 2000. IV 2000. Proceedings of the IEEE*, 2000, pp. 656-661: IEEE.

[6] S. Kempainen, "CMOS image sensors: eclipsing CCDs in visual information?," *EDN*, vol. 42, no. 21, pp. 101-120, 1997.

[7] C.-H. Chen, H.-J. Tsai, K.-S. Huang, and H.-T. Liu, "Study for cross contamination between cmos image sensor and ic product," in *Advanced Semiconductor Manufacturing Conference, 2001 IEEE/SEMI*, 2001, pp. 121-123: IEEE.

[8] S. Ramaswami, S. Agwani, L. Loh, and N. Bossemeyer, "Characterization of pixel response time and image lag in CMOS sensors," *Image Capture Operation, Motorola Inc, Chandler, AZ*, vol. 24, 2001.

[9] E. R. Fossum, "Charge transfer noise and lag in CMOS active pixel sensors," in *IEEE Workshop on CCDs and Advanced Image Sensors*, 2003, vol. 1: Citeseer.

[10] *Rolling Shutter vs. Global Shutter*. Available: http://www.qimaging.com/ccdorscmos/triggering.php

[11] *Pixel Binning*. Available: http://www.quantumimaging.com/binning/

[12] *Binning to increase SNR and frame rate with CCD and CMOS industrial cameras*. Available: http://info.adimec.com/blogposts/bid/104547/Binning-to-increase-SNR-and-frame-rate-with-CCD-and-CMOS-industrial-cameras

[13] *Video of rolling shutter vs global shutter*. Available: https://www.youtube.com/watch?v=alXQWGyX3xk

[14] Y. Yagi, S. Kawato, and S. Tsuji, "Collision avoidance using omnidirectional image sensor (COPIS)," in *Robotics and Automation, 1991. Proceedings., 1991 IEEE International Conference on*, 1991, pp. 910-915: IEEE.

[15] J. Wenger, "Future Trends in Automotive Radar/Imaging Radar," in *Microwave Conference, 1998. 28th European*, 1998, vol. 1, pp. 636-641: IEEE.

[16] J. S. Conde, M. Hillebrand, A. Teuner, N. Stevanovic, U. Iurgel, and B. J. Hosticka, "A smart airbag solution based on a high speed CMOS camera system," in *Image Processing, 1999. ICIP 99. Proceedings. 1999 International Conference on*, 1999, vol. 3, pp. 930-934: IEEE.

[17] C.-C. Ku, C.-P. Young, and C.-H. Lin, "Vision Assisted Active Safety System for Vehicles on the Highway," in *Intelligent Information Hiding and Multimedia Signal Processing, 2013 Ninth International Conference on*, 2013, pp. 489-492: IEEE.

[18] B. A. Wandell, A. El Gamal, and B. Girod, "Common principles of image acquisition systems and biological vision," *Proceedings of the IEEE*, vol. 90, no. 1, pp. 5-17, 2002.

[19] H. K. Kim, G. Cho, S. W. Lee, Y. H. Shin, and H. S. Cho, "Development and evaluation of a digital radiographic system based on CMOS image sensor," *IEEE Transactions on Nuclear Science*, vol. 48, no. 3, pp. 662-666, 2001.

[20] S. W. Lee, H. K. Kim, G. Cho, Y. H. Shin, and Y. Y. Won, "A 3-D X-ray microtomographic system with a CMOS image sensor," *IEEE Transactions on Nuclear Science*, vol. 48, no. 4, pp. 1503-1505, 2001.

[21] M. Tabet and R. Hornsey, "Cmos image sensor camera with focal plane edge detection," in *Electrical and Computer Engineering, 2001. Canadian Conference on*, 2001, vol. 2, pp. 1129-1133: IEEE.

[22] G. Yang, O. Yadid-Pecht, C. Wrigley, and B. Pain, "A snap-shot CMOS active pixel imager for low-noise, high-speed imaging," in *Electron Devices Meeting, 1998. IEDM'98. Technical Digest., International*, 1998, pp. 45-48: IEEE.

[23] N. Stevanovic, M. Hillebrand, B. J. Hosticka, and A. Teuner, "A CMOS image sensor for high-speed imaging," in *Solid-state circuits conference, 2000. Digest of technical papers. ISSCC. 2000 IEEE international*, 2000, pp. 104-105: IEEE.

[24] S. Yoshimura, T. Sugiyama, K. Yonemoto, and K. Ueda, "A 48 kframe/s CMOS image sensor for real-time 3-D sensing and motion detection," in *Solid-State Circuits Conference, 2001. Digest of Technical Papers. ISSCC. 2001 IEEE International*, 2001, pp. 94-95: IEEE.

[25] Y. Sugiyama *et al.*, "A high-speed CMOS image sensor with profile data acquiring function," *IEEE journal of solid-state circuits*, vol. 40, no. 12, pp. 2816-2823, 2005.

[26] M. Furuta, Y. Nishikawa, T. Inoue, and S. Kawahito, "A high-speed, high-sensitivity digital CMOS image sensor with a global shutter and 12-bit column-parallel cyclic A/D converters," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 4, pp. 766-774, 2007.

[27] S. Okura *et al.*, "A 3.7 M-pixel 1300-fps CMOS image sensor with 5.0 G-pixel/s high-speed readout circuit," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 4, pp. 1016-1024, 2015.

[28] I. Shcherback, A. Belenky, and O. Yadid-Pecht, "Empirical dark current modeling for complementary metal oxide semiconductor active pixel sensor," *Optical Engineering*, vol. 41, no. 6, pp. 1216-1219, 2002.

[29] C.-Y. Wu, Y.-C. Shih, J.-F. Lan, C.-C. Hsieh, C.-C. Huang, and J.-H. Lu, "Design, optimization, and performance analysis of new photodiode structures for CMOS active-pixel-sensor (APS) imager applications," *IEEE Sensors Journal*, vol. 4, no. 1, pp. 135-144, 2004.

[30] T. Swe and K. Yeo, "An accurate photodiode model for DC and high frequency SPICE circuit simulation," in *Tech Proc. of the 2001 International Conference on Modelling and Simulation of Microsystems*, 2001, pp. 362-365.

[31] H. Tian, B. Fowler, and A. E. Gamal, "Analysis of temporal noise in CMOS photodiode active pixel sensor," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 1, pp. 92-101, 2001.

[32] *Johnson Noise*. Available: http://web.mit.edu/dvp/Public/noise-paper.pdf

[33] *LUPA3000*. Available: http://www.onsemi.cn/pub_link/Collateral/NOIL1SN3000A-D.PDF

[34] K. Tang and E. G. Friedman, "Lumped versus distributed RC and RLC interconnect impedances," in *Circuits and Systems, 2000. Proceedings of the 43rd IEEE Midwest Symposium on*, 2000, vol. 1, pp. 136-139: IEEE.

[35] Y. Tochigi *et al.*, "A global-shutter CMOS image sensor with readout speed of 1-Tpixel/s burst and 780-Mpixel/s continuous," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 1, pp. 329-338, 2013.

[36] T. G. Etoh *et al.*, "2.7 A CCD Image Sensor of 1Mframes/s for Continuous Image Capturing of 103 Frames," 2002.

[37] C. Ma, "Pixel ADC Design for Hybrid CMOS Image Sensors," Master, Microelectronics & Computer Engineering, Delft University of Technology, 2010-08-31.

[38] C. Niclass, C. Favi, T. Kluter, M. Gersbach, and E. Charbon, "A 128 128 single-photon image sensor with column-level 10-bit time-to-digital converter array," *IEEE Journal of Solid-State Circuits,* vol. 43, no. 12, pp. 2977-2989, 2008.

[39] B. Fowler, A. El Gamal, and D. X. Yang, "A CMOS area image sensor with pixel-level A/D conversion," in *Solid-State Circuits Conference, 1994. Digest of Technical Papers. 41st ISSCC., 1994 IEEE International*, 1994, pp. 226-227: IEEE.

[40] J. A. Leñero-Bardallo, J. Fernández-Berni, and Á. Rodríguez-Vázquez, "Review of ADCs for imaging," in *IS&T/SPIE Electronic Imaging*, 2014, pp. 90220I-90220I-6: International Society for Optics and Photonics.

[41] *ADC fs vs resolution*. Available: https://www.synopsys.com/Company/Publications/SynopsysInsight/Pages/Art5-data-converters-IssQ3-13.aspx?cmp=Insight-I3-2013-Art5

[42] D. Lee, K. Cho, D. Kim, and G. Han, "Low-noise in-pixel comparing active pixel sensor using column-level single-slope ADC," *IEEE Transactions on Electron Devices,* vol. 55, no. 12, pp. 3383-3388, 2008.

[43] *Dual Slope ADC*. Available: http://www.asdlib.org/onlineArticles/elabware/Scheeline_ADC/ADC_ADC_Dual_Slope.html

[44] S. Yoshihara *et al.*, "A 1/1.8-inch 6.4 Mpixel 60 frames/s CMOS image sensor with seamless mode change," *IEEE Journal of Solid-State Circuits,* vol. 41, no. 12, pp. 2998-3006, 2006.

[45] M. F. Snoeij, P. Donegan, A. J. Theuwissen, K. A. Makinwa, and J. H. Huijsing, "A CMOS image sensor with a column-level multiple-ramp single-slope ADC," in *2007 IEEE International Solid-State Circuits Conference. Digest of Technical Papers*, 2007, pp. 506-618: IEEE.

[46] B. E. Boser and B. A. Wooley, "The design of sigma-delta modulation analog-to-digital converters," *IEEE Journal of solid-state circuits,* vol. 23, no. 6, pp. 1298-1308, 1988.

[47] C.-Y. Liou and C.-C. Hsieh, "A 2.4-to-5.2 fJ/conversion-step 10b 0.5-to-4MS/s SAR ADC with Charge-Average Switching DAC in 90nm CMOS," in *2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers*, 2013, pp. 280-281: IEEE.

[48] H. Wei *et al.*, "A 0.024 mm 2 8b 400MS/s SAR ADC with 2b/cycle and resistive DAC in 65nm CMOS," in *2011 IEEE International Solid-State Circuits Conference*, 2011, pp. 188-190: IEEE.

[49] B. P. Ginsburg and A. P. Chandrakasan, "An energy-efficient charge recycling approach for a SAR converter with capacitive DAC," in *2005 IEEE International Symposium on Circuits and Systems*, 2005, pp. 184-187: IEEE.

[50] S. Kawahito, J.-H. Park, K. Isobe, S. Shafie, T. Lida, and T. Mizota, "A CMOS Image Sensor Integrating Column-Parallel Cyclic ADCs with On-Chip Digital Error Correction Circuits," in *ISSCC*, 2008, pp. 56-57.

[51] T. Watabe *et al.*, "A 33Mpixel 120fps CMOS image sensor using 12b column-parallel pipelined cyclic ADCs," in *2012 IEEE International Solid-State Circuits Conference*, 2012, pp. 388-390: IEEE.

[52] *real world vs bandwidth*. Available: http://analogictips.com/considerations-choosing-sigma-delta-adc-vs-sar-vs-pipeline/

[53] *ADC input noise*. Available: http://www.analog.com/en/analog-dialogue/articles/adc-input-noise.html

[54] C. R. Grace, P. J. Hurst, and S. H. Lewis, "A 12-bit 80-MSample/s pipelined ADC with bootstrapped digital calibration," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 5, pp. 1038-1046, 2005.

[55] Z. Zhao and M. Wang, "A gain boosting switch for S/H circuit using clock boosting and symmetrical techniques to decrease the effect of channel charge injection," in *Computational Problem-solving (ICCP), 2013 International Conference on*, 2013, pp. 308-311: IEEE.

[56] A. N. Karanicolas, H.-S. Lee, and K. Barcrania, "A 15-b 1-Msample/s digitally self-calibrated pipeline ADC," *IEEE Journal of Solid-State Circuits*, vol. 28, no. 12, pp. 1207-1215, 1993.

[57] *1.5b RSD*. Available: https://www.maximintegrated.com/en/app-notes/index.mvp/id/1023

[58] M. Miyahara, Y. Asada, D. Paik, and A. Matsuzawa, "A low-noise self-calibrating dynamic comparator for high-speed ADCs," in *Solid-State Circuits Conference, 2008. A-SSCC'08. IEEE Asian*, 2008, pp. 269-272: IEEE.

[59] M. Miyahara and A. Matsuzawa, "A low-offset latched comparator using zero-static power dynamic offset cancellation technique," in *Solid-State Circuits Conference, 2009. A-SSCC 2009. IEEE Asian*, 2009, pp. 233-236: IEEE.

[60] C. Chen *et al.*, "A low-offset calibration-free comparator with a mismatch-suppressed dynamic preamplifier," in *2014 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2014, pp. 2361-2364: IEEE.

[61] Y. Jinda, W. Xianbiao, L. Li, C. Xu, G. Yawei, and Z. Xiaoyang, "A novel low-offset dynamic comparator for sub-1-V pipeline ADCs," *Journal of Semiconductors,* vol. 32, no. 8, p. 085005, 2011.

[62] J. He, S. Zhan, D. Chen, and R. L. Geiger, "Analyses of static and dynamic random offset voltages in dynamic comparators," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 56, no. 5, pp. 911-919, 2009.

[63] T. W. Matthews and P. L. Heedley, "A simulation method for accurately determining DC and dynamic offsets in comparators," in *48th Midwest Symposium on Circuits and Systems, 2005.*, 2005, pp. 1815-1818: IEEE.

[64] M. Loose, K. Meier, and J. Schemmel, "A self-calibrating single-chip CMOS camera with logarithmic response," *IEEE Journal of Solid-State Circuits,* vol. 36, no. 4, pp. 586-596, 2001.

[65] S. Kavadias, B. Dierickx, D. Scheffer, A. Alaerts, D. Uwaerts, and J. Bogaerts, "A logarithmic response CMOS image sensor with on-chip calibration," *IEEE Journal of Solid-State Circuits,* vol. 35, no. 8, pp. 1146-1152, 2000.