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NANOPATTERNING OF SILICON NITRIDE MEMBRANES

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Abstract

Membranes are typically created by a thin silicon nitride (SIN) layer deposited on a silicon wafer. Both, top and bottom side of the wafer is covered by a thin layer of the silicon nitride. The principle of silicon nitride membranes preparation is based on the wet anisotropic etching of the bottom side of the silicon wafer with crystallographic orientation (100). While the basic procedure for the preparation of such membranes is well known, the nano patterning of thin membranes presents quite important challenges. This is partially due to the mechanical stress which is typically presented within such membranes. The resolution requirements of the membrane patterning have gradually increased. Advanced lithographic techniques and etching procedures had to be developed. This paper summarizes theoretical aspects, technological issues and achieved results. The application potential of silicon nitride membranes as a base for multifunctional micro system (MMS) is also discussed.

Keywords: E-beam writer, silicon nitride membranes, nano patterning, anisotropic etching

1. INTRODUCTION

The extensive overview of various microfabrication techniques is comprehensibly elaborated in [1]. This study of the grid production using micro and nano structured membranes is based on the current trend and application potential of these elements, such as beam splitters for X-ray spectroscopy, calibration standards for electron microscopy (EM), both transmission EM (TEM) and scanning EM (SEM), application processing of ultra-violet (UV) and extreme UV light [2], micro electro-mechanical systems (MEMS) for micro-sensors and micro-fluidic applications, grid for processing of electron beam in the electron optics [3] and many others.

The technology of silicon nitride membranes was studied and developed since a couple of years, e.g. a pressure sensor with Si_3N_4 diaphragm [4]. In the actual work, the membranes are not used as a support for functional structures but the structure is created directly in the SIN layer. Different etching techniques had to be adopted for the technology steps: plasmatic etching [5], reactive ion etching, and anisotropic wet silicon etching [6]. High resolution e-beam nano patterning ([7], [8], [9]) was necessary due to the grid resolution requirements.

The aim of this contribution is to prepare chips with nano-structured silicon nitride (SIN) membrane, which application belongs to the field of electron optics, namely the study of the properties of coherence of the electron beams in SEM [10], [11]. This application requires a structure on the surface of a thin membrane with open slits in the range of 50 to 100 nm. The system of these slits forms the basis for the diffraction grating. Parametric inputs for two selected motifs of such structure are depicted in **Figure 1**.

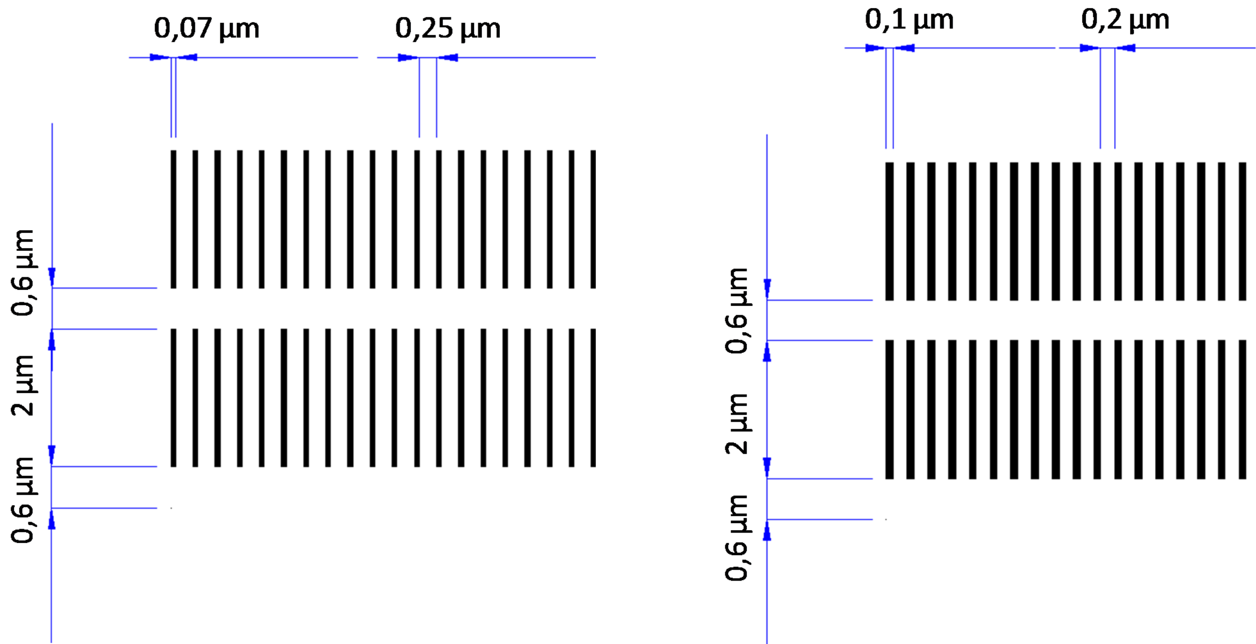

Figure 1 Two selected diffraction gratings motifs for structuring of the nitride membrane

2. METHOD

The first step before the actual implementation is the feasibility study, in terms of which there is also a record-defined grid structures on the electron beam pattern generator. This is followed by identification of appropriate techniques, equipment selection and determination of critical technology steps, which are supposed to require the optimization of process parameters. The result of the study is a schematic illustration of the main steps of the production process, see **Figure 2**.

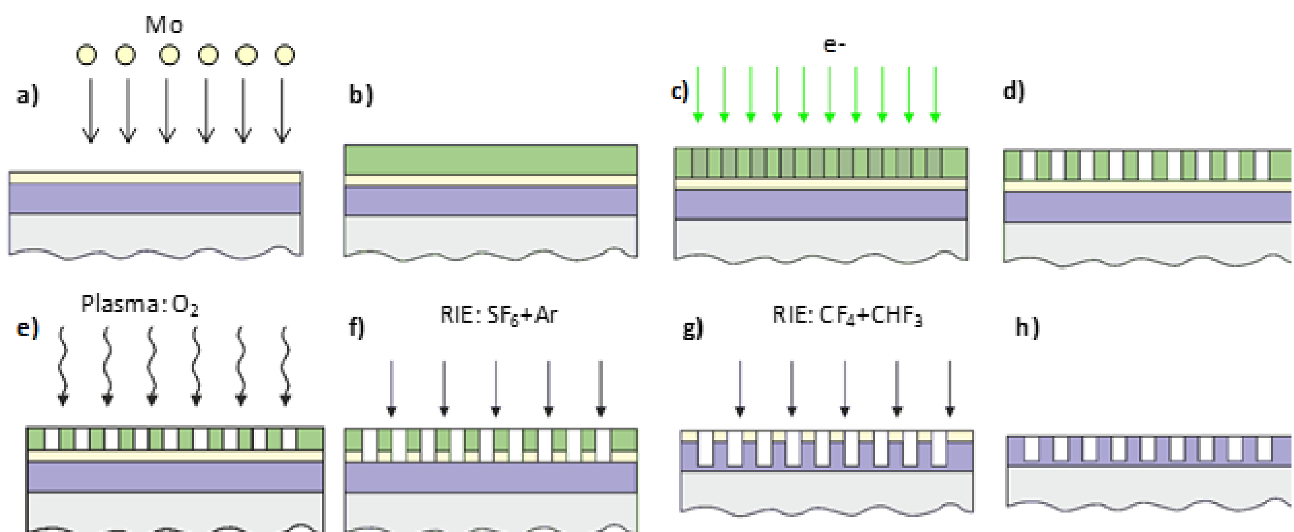

Figure 2 The result of the study: a schematic illustration of the main steps of the production process - lithography on the top (polished) side of the silicon wafer

Technological procedure for the realization of a nano-structured nitride membrane comprises the following steps (probably critical process requiring optimization is marked by*, critical process with the necessary optimization is marked by **):

- deposition of molybdenum (Mo);
- deposition of the PMMA resist;
- * exposure of the motif grid using EBL (Vistec EBPG5000+ES);
- * process of resist development in the mixture IPA : H_2O;
- plasma etching of the PMMA in O_2;
- * transferring of the grid motif from PMMA to Mo layer by the RIE method (see details in **Table 1**);
- ** transferring of the grid motif from Mo to Si_3N_4 layer by RIE (see details in **Table 2**);
- wet etching of the Mo layer (H_3PO_4 : HNO_3 : H_2O).

These lithography process steps of the top side of the wafer are followed by the bottom side lithography steps and by the finalization steps.

3. EXPERIMENT

On the polished side of the wafer with a silicon nitride (SIN) layer, a thin layer of molybdenum (thickness w = 20 - 25 nm) was deposited by magnetron sputtering. Next, on this molybdenum (Mo) layer, a thin layer of electron resist poly(methyl methacrylate) - PMMA (molar weight, MW = 950k, a thickness of 110 nm) was deposited by spin coating. A record of the grating motif to the resist layer was exposed by an electron beam pattern generator EBPG5000plusES (Vistec, actually Raith). The exposed motif was developed by immersion in a centrifuge using a high contrast developer based on isopropyl alcohol IPA (IPA : H_2O in ratio 1 : 10). The developing process was checked by both optical microscope and profilometer.

The next step was to remove resist residues (polymer and solvent residues in holes of the grating motif). For this purpose we used a plasma etching process in oxygen at Diener Nano plasma apparatus (see e.g. [5]), a plasma apparatus with a cylindrical chamber and capacitively excited plasma at a frequency of 40 kHz. Etching parameters were as follows: gas flow of 40 sccm (standard cubic centimeters), chamber pressure of 0.4 mbar, high frequency power of 500 W (at 40 kHz), cycle time 90 seconds. During this step, the thickness of the PMMA layer was reduced across the silicon wafer by approximately 25 nm (i.e. about 22 % of the initial thickness). At the same time, there has been a thorough check of the nitride layer in the holes of the PMMA mask.

The transferring of the grating motif into the layer of molybdenum was performed using the RIE apparatus with inductively coupled plasma (ICP) brand Oxford Instruments. We selected a recipe with the gaseous mixture of sulfur hexafluoride (SF_6) and argon (Ar) for the etching of molybdenum. It was necessary to verify parameters of Mo layer etching experimentally, on a number of samples. Optimization of the process parameters in this case was necessary, in order to avoid etching of the nitride film. The depth of etching was verified with a contact probe at the profilometer Alpha 120 brand KLA Tencor. The Mo etching rate at selected recipe was set to the range of 2 to 2.5 nm/sec. Final optimized parameters of etching used during transmission of the grating motif into the Mo layer are shown in **Table 1**.

Table 1 Process parameters: the molybdenum mask etching

Step	Gas	Time	Power ICP	Power RIE	T_{wafer}
Tempering	SF_6 (50 ccm) + Ar (40 ccm)	120 s	0	0	60 °C
Etching	SF_6 (50 ccm) + Ar (40 ccm)	12 s	3000 W	10 W	60 °C

The Mo layer etching was followed by a step during which the PMMA layer was removed. This process took place through the plasma combustion in oxygen. The reason for this choice of dry way resist removal is to avoid possible contamination of the Mo mask in case of application of solvents.

The next step was the transferring the motif grid into the SIN layer through the Mo mask by the RIE method. It was chosen a gas mixture of tetrafluormethan (CF_4) and fluoroform (CHF_3) for the etching of the nitride. The selectivity of the SIN etching through the Mo mask is in this process approximately 1 : 20 (Mo : SIN). The use of the Mo layer for the transfer of the grid motif to the SIN layer is preferable, compared to the direct transmission of motif over PMMA, because there is not such significant expansion of the etched holes in the lateral direction caused by the loss of the etching mask during etching process. The transfer of the grid image is in this case almost perfect. The actual process of etching of the nitride layer was one of the most critical points of the process. This was due to the technological requirement to etch only 80-90 % of the total thicknesses of the SIN layer with very high uniformity of etch rates over large area. The reason for this requirement was to avoid the opening of the silicon surface in the holes etched in the SIN, i.e. the etching must be carried so that the silicon surface remains masked by at least a thin residue of the SIN layer. That means that the portion of nitride layer covers the underlying silicon substrate to ensure that on this side there will be no etching of the silicon surface in a subsequent process of the anisotropic etching of the hole from the back side of the wafer. To achieve this technological requirement, it was necessary a tedious process of tuning parameters of the etching in the RIE apparatus, including test reproducibility of the etching. In order to achieve a better control the etching process, i.e. that etching did not proceed too rapidly, it was necessary to optimize the rate of excitation of plasma by reducing the ICP power. In terms of the repeatability of the etching process, it appears necessary to adjust the basic length of the tempering step. The tempering step has two roles: first, the heating of the sample to the working temperature and, secondly, the homogenization of the working gas concentration in the chamber before the onset of the etching. It was proven that the length of the tempering cycle of 180-240 seconds is appropriate for the temperature of 60 °C.

Final etching parameters, which led to the etching of holes in the SIN layer to the depth of 64 to 69 nm, are shown in **Table 2**.

Table 2 Process parameters: the etching of silicon nitride through the molybdenum mask

Step	Gas	Time	Power ICP	Power RIE	T_{wafer}
Tempering	CF_4 (10 ccm) + CHF_3 (40 ccm)	180 s	0	0	60 °C
Etching	CF_4 (10 ccm) + CHF_3 (40 ccm)	26 s	1000 W	50 W	60 °C

4. RESULTS

The grid motif after etching was inspected by the AFM (atomic force microscope) Nano-R brand Pacific Nanotechnology **(Figure 3** and **Figure 4**). Besides this surface relief scan, an inspection using a SEM Magellan 400 brand FEI was also carried on (**Figure 5** and **Figure 6**).

The etching of grid motif holes into the nitride layer completed the lithographic process on the top polished side of the silicon wafer - **Figure 2**, steps from ***a)*** to ***h)*** - and it was followed by the lithographic process of machining the unpolished (bottom) side of the wafer by the wet anisotropic etching of silicon.

The whole process was accomplished by the finalizing etching step that finished the opening of the remaining residual SIN layer on the top side of the silicon wafer.

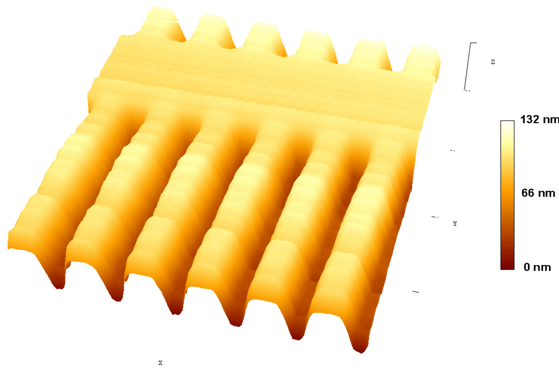

Figure 3 The image of the etched motif in the SIN layer (AFM scan); the line width of 200 nm and the gap of 200 nm (scale on the z axis is 132 nm)

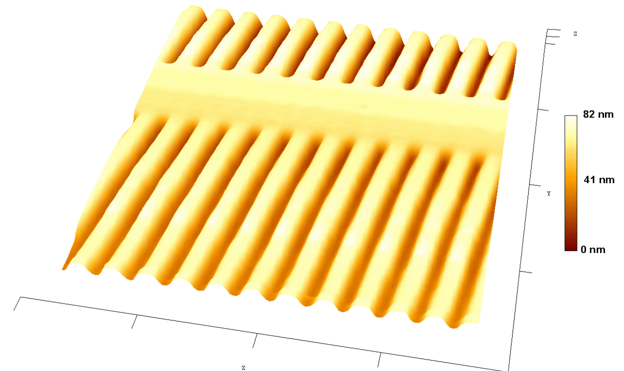

Figure 4 The image of the etched motif in the SIN layer (AFM scan); the line width of 100 nm and the gap of 200 nm (scale on the z axis is 82 nm)

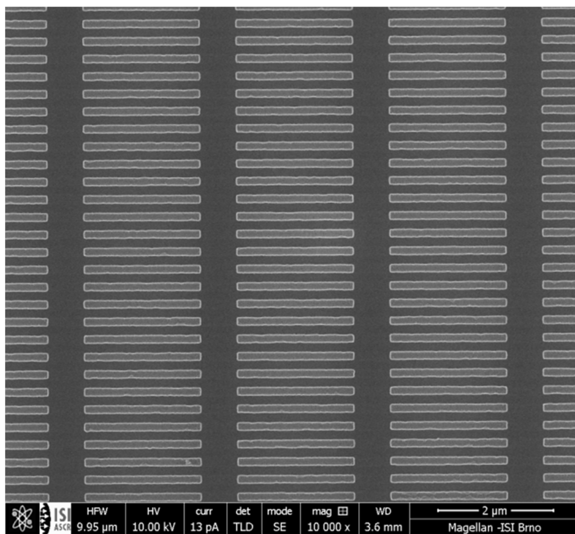

Figure 5 The SEM image of the etched surface of the nitride layer with the grid motif after the RIE process; the line width of 200 nm and the gap of 200 nm

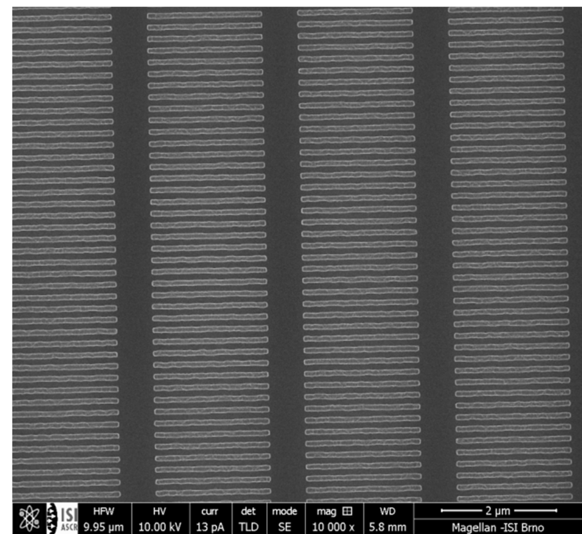

Figure 6 The SEM image of the etched surface of the nitride layer with the grid motif after the RIE process; the line width of 100 nm and the gap of 100 nm

5. CONCLUSIONS

We have described processes used during fabrication of grid motifs with sub-100-nm openings for free-standing structure in Si_3N_4. Samples with the free-standing gratings were recently used at the Institute of Scientific Instruments of the CAS in Brno for the study of coherence of the primary electron beam in the low energy scanning electron microscope and electron diffraction in scanning electron microscope. Recently, the first results of the study were presented [10], [11].

We expect further use of this fabrication technology for the preparation of more complex free-standing patterned structures for study of electron diffraction and for other applications such as preparation of free-standing patterns for processing of EUV light, soft-X-ray radiation and metrology.

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