



The  
University  
Of  
Sheffield.

# **Design and Evaluation of a Single Phase 5 Level Full Bridge Neutral Point Clamped Multi Level Converter**

**By:**

Jonathan David Gomez Palomino

A thesis submitted in partial fulfilment of the requirements for the degree of  
Doctor of Philosophy

The University of Sheffield  
Faculty of Engineering  
Electronic and Electrical Engineering Department

September 2017

## Summary

This thesis describes multilevel converters (MLC) designed for use with a repurposed electronic vehicle battery (battery 2<sup>nd</sup> life). MLC is of particular interest due to the low harmonic distortion content and reduced voltage stress in the switching devices. A detailed study of the MLC topologies and modulation techniques is presented. Space vector modulation is analysed and implemented to evaluate the converter. A comprehensive assessment of the MLC is presented using wide bandgap (WBG) devices highlighting the devices' thermal and high switching frequency features.

The converter is designed to be used in construction sites where a reduced output voltage is required. For battery management a DC-DC converter is also added to the system. The modulation of the converters has been evaluated in simulation and a space vector modulation adaptation for single phase converters has been selected to generate the switching sequence and capacitor voltage balancing.

The topology studied in this research is a full bridge 5-Level Neutral Point Clamped (NPC). This thesis presents the evaluation of the MLC including the design and system validation through simulation and physical implementation, showing the feasibility of the use of the converter for the intended application. The control of the converters was developed using NI LabVIEW FPGA and validated using Co-simulation. In this thesis, the use of the Co-simulation with NI Multisim to evaluate the system provided a design environment for a smooth transition into the hardware implementation and it enabled a robust and reliable control system.

This thesis also presents an evaluation of performance using WBG semiconductor devices in the MLC based on the temperature rise over a range of frequencies. Therefore, a comparison between WBG and silicon devices is assessed and an investigation on the power quality of the converter has been examined in terms of the harmonic content and overall efficiency. The experimental results using WBG devices show a considerable advantage in terms of a reduced temperature rise and an increase in the overall efficiency when the MLC was operated using WBG devices.

## Publications

- [P1] **J.D. Gomez-Palomino**, M.P. Foster and D.A. Stone, 'Performance evaluation of SiC MOSFET in 5-level single phase converter' IET Power Electronics Machines and Drives (PEMD) 2016.
- [P2] **J.D. Gomez-Palomino**, M.P. Foster and D.A. Stone, 'Bidirectional cascaded DC-DC converter and multilevel converter (MLC) integrated for vehicle-to-grid (V2G) interface using hybrid/electric vehicle's (HEV/EV) battery' UK Energy Storage (UKES) 2014.

## Acknowledgements

I would like to thank firstly to my supervisors Prof. Martin Forster and Prof. David Stone for their guidance and support during my studies.

A special acknowledgement to my parents for their support and encouragement to complete my degree.

I would also like to thank all the staff in the University of Sheffield EEE department for their support and dedication to maintain the department and EMD group running smoothly. Special thanks to my colleagues Jonathan Davidson, David Hewitt, Shahab Nejad, Sami Abuzed and my friends Chi Wa Tsang and Rui Zhao for their help and support.

This study was done with financial support of the Mexican Council of Science and Technology (CONACyT) under the scholarship number 215289

## Table of contents

Summary .....	i
Publications .....	ii
Acknowledgements .....	iii
Table of contents .....	iv
Symbol list .....	viii
Acronyms list .....	x
List of Figures .....	xii
List of Tables.....	xvii
Chapter 1 Introduction .....	1
1.1 Application and Motivation .....	2
1.2 Thesis outline .....	4
1.3 References .....	5
Chapter 2 – Background.....	6
2.1 – Introduction .....	6
2.2 – Multi-Level Converters .....	7
2.2.1 Neutral-Point Clamped Converter.....	8
2.2.2 Flying capacitor converter.....	15
2.2.3 Cascaded H-Bridge. ....	22
2.2.4 Comparison .....	25
2.3 – Modulation in MLC .....	26
2.3.1 Selective harmonic elimination.....	26
2.3.2 Space Vector Modulation.....	26
2.3.3 Sinusoidal PWM .....	27
2.4 – Applications .....	27
2.4.1 – Battery connected MLCs .....	29
2.5– Conclusion .....	31
2.6 – References .....	32

Chapter 3 – Modulation Techniques .....	36
3.1 – Introduction .....	36
3.2 – Sinusoidal PWM .....	38
3.2.1 Sinusoidal PWM simulation .....	43
3.3 – 1-D Space vector modulation.....	58
3.3.1 Nearest 2 vectors modulation for 5-L-FB-NPC .....	59
3.3.2 Capacitor Voltage Balancing N2V.....	61
3.3.3 – Simulation space vector modulation .....	63
3.4 Chapter conclusion.....	66
3.5 References .....	66
Chapter 4 – Converter design.....	68
4.1 Introduction .....	68
4.2 Platform system description and specification.....	69
4.3 Converter Design .....	71
4.3.1 DC-DC converter design.....	71
4.3.2 Multilevel converter design.....	76
4.4 System Simulation Results.....	82
4.4.1 Discharging mode with nominal battery voltage .....	83
4.4.2 Discharging mode with minimum battery voltage.....	84
4.4.3 Charging mode with maximum grid voltage .....	87
4.4.4 Charging mode with minimum grid voltage .....	87
4.4.5 Closed loop evaluation.....	88
4.5 Chapter conclusion.....	91
4.6 References .....	91
Chapter 5 – System experimental evaluation.....	93
5.1 – Introduction .....	93
5.2 – FPGA control platform .....	94
5.2.1 FPGA implementation. ....	95

5.3 Gate driver circuit design .....	99
5.4 Isolated voltage and current input and output .....	100
5.4.1 Isolated voltage transducer.....	101
5.4.2 Isolated current transducer.....	102
5.5 DC-DC converter evaluation.....	103
5.5.1 Inductor .....	104
5.5.2 DC-DC converter testing .....	105
5.6 Multilevel converter testing .....	109
5.6.1 Multilevel converter full bridge operation and capacitor voltage balancing	110
5.6.2 Full-bridge 5-level converter operation .....	111
5.6.3 Transformer.....	113
5.7 Phase locked loop with grid .....	113
5.7.1 PLL to generate reference signal for MLC .....	114
5.8 Safety and protection circuit.....	115
5.8.1 Fuse selection.....	115
5.8.2 Battery protection circuit.....	115
5.8.3 Safety enclosure .....	116
5.9 Chapter conclusion.....	117
5.10 References .....	117
Chapter 6 – Evaluation of 5L-FB-NPC MLC featuring wide bandgap semiconductor devices.....	119
6.1 – Introduction .....	119
6.2 – 5-level NPC Converter.....	121
6.3 – Wide bandgap semiconductors devices .....	121
6.3.1 – Si and SiC evaluation devices .....	122
6.4 – Experimental evaluation.....	123
6.4.1 – Hardware setup.....	124
6.4.2 – Temperature rise and efficiency results .....	126

6.4.3 – Voltage and current waveforms comparison.....	130
6.5 – Conclusion .....	135
6.6 – References .....	136
Chapter 7 – Power quality evaluation in 5L-FB-NPC MLC .....	137
7.1 – Introduction .....	137
7.2 – Multilevel converter (MLC) filter .....	138
7.2.1 – L filter.....	138
7.2.2 – LC filter .....	139
7.2.3 – LCL filter .....	139
7.2.4 – Damping circuit.....	140
7.3 – Power Quality .....	143
7.3.1 Norms and standards .....	144
7.3.2 MLC harmonic evaluation .....	145
7.3.1 THD comparison Si and SiC.....	147
7.4 – Conclusion .....	153
7.5 – References .....	154
Chapter 8 – Conclusion and further work .....	156
8.1 Conclusion .....	156
8.2 Further work.....	158



## Symbol list

<b><i>Symbol</i></b>	<b>Definition</b>
$\Delta I_L$	Current ripple
$\Delta V_C$	Capacitor voltage ripple
$a$	Reference signal
$A, B$	Output terminals
$A_{CU}$	Conductor area
$A_e$	Effective area
$A_W$	Winding area
$B_s$	Saturation flux density
$C, C0, C1, \dots, C15$	Capacitors
$C_{DC}$	DC link capacitor
$C_f$	Damping capacitor
$C_{ISS}$	Input capacitance
$D$	Duty cycle
$D, D0, D01, D1, \dots, D6$	Diodes
$D_{boost}$	Duty cycle in discharging mode
$D_{buck}$	Duty cycle in charging mode
$f$	Frequency
$f_{sw}$	Switching frequency
$I_{DS}$	Drain to source current
$I_G$	Gate current
$I_L$	Inductor current
$I_{out}$	Output current
$I_{sw}$	Switch drain source current
$k_{CU}$	Packing factor
$L$	Inductor
$L_f$	Inductor filter
$l_g$	Airgap length
$L_g$	Grid side inductor
$m$	Number of levels
$N_{min}$	Minimum number of turns
$P_{out}$	Output power

$Q1, \dots, Q4$	MOSFETs
$Q1', \dots, Q4'$	MOSFETs operating in complementary form
$Q_G$	Gate charge
$R_b$	Base resistor
$R_{DS}$	Drain to source resistance
$R_f$	Damping resistor
$R_G$	Gate resistor
$R_{load}$	Load resistor
$R_{th}$	Thermal resistance
$S, S1, \dots, S8$	MOSFETs
$S', S1', \dots, S8'$	MOSFETs operating in complementary form
$S11, S21, S31, S41$	MOSFETs operating in complementary form
$t_{transition}$	Transition time
$V, V/2, V/4$	Voltages
$V_1$	Fundamental component
$V_{batt}$	Battery voltage
$V_C, V_{C1}, V_{C2}$	Capacitor voltage
$V_{DC}$	DC-link voltage
$V_{DS}$	Drain to source voltage
$V_{grid}$	Grid voltage
$V_n$	Harmonics of fundamental
$V_{out}$	Output voltage

## Acronyms list

<b>Acronym</b>	<b><i>Definition</i></b>
AC	Alternating Current
APOD	Alternately in Opposition Disposition
ASIC	Application Specific Integrated Circuits
BSI	British Standards Institution
CENELEC	Comite Europeen de Normalisation Electrotechnique
CHB	Cascaded H-Bridge
DC	Direct Current
DSP	Digital Signal Processor
EMC	Electromagnetic Compatibility
EV	Electric Vehicle
FACTS	Flexible AC Transmission System
FB	Full Bridge
FCC	Flying Capacitor Converter
FFT	Fast Fourier Transform
FPGA	Field Programmable Array
GaN	Gallium Nitride
GTO	Gate Turn-Off
HB	Half Bridge
HBC	H-Bridge Converter
HEV	Hybrid Electric Vehicle
IC	Integrated Circuit
IEEE	Institute of Electrical and Electronic Engineers
IGBT	Insulated Gate Bipolar Transistor
LB	Logic Blocks
LUT	Look-Up Tables
MEA	More Electric Aircraft
MLC	Multi-level Converter
MMC	Modular Multilevel Converter
MOSFET	Metal-Oxide Semiconductor Field Effect Transistor
N2V	Nearest 2 vectors
NI	National Instruments

NPC	Neutral-Point Clamped
PD	Phase Disposition
PHEV	Plug-in Hybrid Electric Vehicle
PI	Proportional and Integral controller
PLL	Phase-Locked Loop
POD	Phase Opposition Disposition
PWM	Pulse Width Modulation
SiC	Silicon Carbide
STATCOM	Static-Synchronous Compensation
SVM	Space Vector Modulation
THD	Total Harmonic Distortion
V2G	Vehicle to Grid
VHDL	VHSIC Hardware Description Language
WBG	Wide bandgap

## List of Figures

Figure 1.1: Circuit diagram for the 5-level single-phase converter .....	4
Figure 2.1 Functional diagram of a DC to AC converter.....	6
Figure 2.2 Neutral-Point Clamped 3-levels single phase.....	8
Figure 2.3 NPC 3-levels output waveform .....	9
Figure 2.4 Neutral-Point Clamped 5-levels full bridge single phase.....	10
Figure 2.5 NPC 5-levels full bridge output voltage waveform.....	11
Figure 2.6 Neutral-Point Clamped 5-level Half Bridge Single phase.....	12
Figure 2.7 NPC 5-levels output voltage waveform.....	13
Figure 2.8 Neutral-Point Clamped 9-level Full Bridge Single phase .....	14
Figure 2.9 NPC 9-levels full bridge output voltage waveform.....	14
Figure 2.10 Flying capacitor 3-level single phase .....	16
Figure 2.11 Flying capacitor 3-levels output voltage waveform .....	17
Figure 2.12 Flying Capacitor 5-level Full Bridge Single phase .....	18
Figure 2.13 Flying capacitor 5-levels output voltage waveform .....	19
Figure 2.14 Flying capacitor 5-level half bridge single phase .....	19
Figure 2.15 Flying capacitor 5-levels half bridge output voltage waveform.....	20
Figure 2.16 Flying capacitor 9-level full bridge single phase.....	21
Figure 2.17 Flying capacitor 9-levels output voltage waveform .....	22
Figure 2.18 Cascaded H-bridge 3-levels topology.....	22
Figure 2.19 H-bridge 3-levels output voltage waveform .....	23
Figure 2.20 Cascaded H-bridge 5-levels topology.....	24
Figure 2.21 5-levels cascaded H-bridge output voltage waveform.....	24
Figure 2.22 Bidirectional buck boost cascade converter .....	30
Figure 2.23 Simplified bidirectional buck boost cascade conveter.....	31
Figure 3.1 MLC modulation classification .....	37
Figure 3.2 5-level Neutral Point Clamped Converter .....	39
Figure 3.3. PWM generator for 5-level converter.....	40
Figure 3.4 Sinusoidal reference and carrier signals for Phase Disposition PWM .....	41
Figure 3.5 Switching pulses Phase Disposition .....	41
Figure 3.6 Sinusoidal reference and carrier signals for Phase Opposition PWM.....	42
Figure 3.7 Switching pulses Phase Opposition Disposition .....	42
Figure 3.8 . PWM sinusoidal reference and carrier signals for Alternately in Opposition PWM.....	43

Figure 3.9 Switching pulses Alternately in Opposition Disposition.....	43
Figure 3.10. 5-level Diode Clamped Single Phase Half Bridge MLC.....	45
Figure 3.11. Diode Clamped 1 leg 5-level converter - Phase Disposition.....	46
Figure 3.12. Diode Clamped 1 leg 5-level converter - Phase Opposition Disposition. .	47
Figure 3.13. Diode Clamped 1 leg 5-level converter - Alternatively Opposition Disposition. ....	48
Figure 3.14. Flying Capacitor 5-level Single Phase Half Bridge.....	49
Figure 3.15. Flying Capacitor 1 leg 5-level converter - Phase Disposition. ....	50
Figure 3.16. Flying Capacitor 1 leg 5-level converter - Phase Opposition Disposition.	51
Figure 3.17. Flying Capacitor 1 leg 5-level converter - Phase Alternatively Opposition. ....	52
Figure 3.18. Diode Clamped 9-level Single Phase, Full Bridge. ....	53
Figure 3.19. Diode Clamped Full Bridge 9-level converter.....	54
Figure 3.20. Flying Capacitor Full Bridge 5-level converter.....	55
Figure 3.21. Flying Capacitor Full Bridge 9-level converter.....	56
Figure 3.22 Diode Clamped Full Bridge 5-level converter.....	57
Figure 3.23 NPC Full Bridge 5-level converter waveform and FFT .....	58
Figure 3.24. Control region for 5-level inverter.....	60
Figure 3.25 1-D Nearest 2 vectors control regions .....	61
Figure 3.26. Simulink model of the 5-level converter. ....	63
Figure 3.27 Output voltage with no balance algorithm implemented.....	64
Figure 3.28 Voltage in the DC-link capacitors with no balance algorithm implemented. ....	64
Figure 3.29 Output voltage with balance algorithm implemented.....	65
Figure 3.30 Voltage in the DC-link capacitors with balance algorithm implemented....	65
Figure 4.1 Block Diagram of the system. ....	69
Figure 4.2 DC-DC bidirectional converter .....	71
Figure 4.3 DC-DC bidirectional converter .....	74
Figure 4.4 Simulink Model Boost Buck Converter .....	74
Figure 4.5 Boost Mode test circuit.....	75
Figure 4.6 Boost (Discharge)Mode Output voltage.....	75
Figure 4.7 Buck Mode test circuit.....	75
Figure 4.8 Buck (Charge) Mode Output .....	76
Figure 4.9 5-level NPC converter in full bridge topology. ....	77

Figure 4.10 Output voltage per phase and total .....	77
Figure 4.11 DC-DC and MLC converter integrated. ....	79
Figure 4.12 5-level NPC single phase full bridge converter Multisim model. ....	80
Figure 4.13 Co-Simulation Front Panel Output Voltage and phase voltages. ....	80
Figure 4.14 CoSimulation block diagram. ....	81
Figure 4.15 DC-DC and MLC integrated .....	82
Figure 4.16 DC-DC converter input and output waveforms. On the right graph the DC link capacitor voltages.....	83
Figure 4.17 Output Voltage and Current waveforms with $V_{batt}=144V$ .....	83
Figure 4.18 Current and Voltage FFT in discharging mode with $V_{batt}=144V$ $V_{batt}=140V$ . .....	84
Figure 4.19 Generator Mode DC-DC converter input and output waveforms. On the right graph the DC link capacitor. ....	85
Figure 4.20 Output Voltage and Current waveforms with $V_{batt}=108V$ .....	85
Figure 4.21 Current and voltage FFT.....	86
Figure 4.22 Charging Mode DC-DC converter input and output waveforms. On the right graph the DC link capacitor voltage.....	87
Figure 4.23 Charging Mode DC-DC converter input and output waveforms. On the right graph the DC link capacitor voltage.....	87
Figure 4.24 Control loop block diagram.....	88
Figure 4.25 DC-link voltage in closed loop with $V_{batt}=108V$ .....	89
Figure 4.26 MLC output voltage in closed loop with input voltage $V_{batt}=108V$ .....	89
Figure 4.27 DC-link voltage in closed loop with $V_{batt}=144V$ .....	90
Figure 4.28 MLC output voltage in closed loop with input voltage $V_{batt}=108V$ .....	90
Figure 5.1 5-level NPC converter in full bridge topology. ....	96
Figure 5.2 S1 and S3 pulses Co-Simulation output. ....	96
Figure 5.3. S1 and S3 Digital Output FPGA.....	97
Figure 5.4 S11 and S31 pulses Co-Simulation output. ....	97
Figure 5.5. S11 and S31 Digital Output FPGA.....	97
Figure 5.6 S2 and S4 pulses Co-Simulation output. ....	98
Figure 5.7 S2(CH1) and S4(CH2) Digital Output FPGA. ....	98
Figure 5.8 S21 and S41 pulses Co-Simulation output. ....	98
Figure 5.9 S21(CH1) and S41(CH2) Digital Output FPGA. ....	99
Figure 5.10 Gate Driver Circuit interface with MOSFET. ....	100

Figure 5.11 Voltage transducer circuit.....	101
Figure 5.12 Voltage transducer characterisatic curve.....	102
Figure 5.13 Current transducer circuit.....	102
Figure 5.14 Current transducer characteristic curve.....	103
Figure 5.15 Bidirectional DC-DC converter.....	104
Figure 5.16. DC-DC converter PCB and FPGA.....	104
Figure 5.17 Boost mode test circuit.....	106
Figure 5.18 Input and output voltages in boost mode with minimum battery voltage.....	107
Figure 5.19 Input and output voltages in boost mode with maximum battery voltage.....	107
Figure 5.20 Buck mode test circuit.....	108
Figure 5.21 Input and output voltages in buck mode.....	109
Figure 5.22. 5-level diode clamped full bridge converter.....	109
Figure 5.23 Phase A (3-level) converter circuit.....	110
Figure 5.24 Output voltage of phase A, Co-simulation.....	110
Figure 5.25 Phase A output voltage tested.....	110
Figure 5.26 Co-simulation front panel output voltage and output voltages per phase.....	111
Figure 5.27. 5-level converter output test at 50V input.....	111
Figure 5.28 DC-link capacitor voltage balanced.....	111
Figure 5.29 DC-DC and MLC integrated.....	112
Figure 5.30 5-level output voltage before filtering.....	112
Figure 5.31 5-level output voltage filtered.....	113
Figure 5.32 Block diagram of the grid interface.....	113
Figure 5.33 PLL with sinusoidal generated in FPGA Vgen(blue) and Vref(green).....	114
Figure 5.34 PLL with grid voltage Vgrid(blue) and Vref(green).....	115
Figure 5.35 Battery protection circuit.....	116
Figure 5.36 Enclosure safety box.....	116
Figure 6.1: Circuit diagram for the 5-level single-phase converter.....	119
Figure 6.2: Block diagram of MLC system.....	121
Figure 6.3: MOSFET with external SiC antiparallel diode and blocking diode.....	124
Figure 6.4 Converter enclosure component distribution.....	125
Figure 6.5 Hardware of converter evaluated.....	126
Figure 6.6: Temperature rise of Si N95 MOSFETs in MLC.....	127
Figure 6.7: Temperature rise of Si FDP MOSFETs in MLC.....	127
Figure 6.8: Temperature rise of SiC 280 MOSFETs in MLC.....	128



Figure 6.9: Temperature rise of SiC 040 MOSFETs in MLC.....	128
Figure 6.10: Average temperature as a function of frequency for the Si and SiC devices .....	129
Figure 6.11: Efficiency comparison as a function of frequency .....	130
Figure 6.12 Si N95 voltage and current waveforms .....	131
Figure 6.13 Si N95 voltage FFT .....	131
Figure 6.14 Si FDP voltage and current waveforms .....	132
Figure 6.15 Si FDP voltage FFT .....	132
Figure 6.16 SiC 280 voltage and current waveforms.....	133
Figure 6.17 SiC 280 voltage FFT.....	133
Figure 6.18 SiC 040 voltage and current waveforms.....	134
Figure 6.19 SiC 040 voltage FFT.....	134
Figure 7.1 L-filter.....	138
Figure 7.2 LC-filter .....	139
Figure 7.3 LCL filter .....	139
Figure 7.4 MLC with LC filter.....	140
Figure 7.5 R damping circuit .....	141
Figure 7.6 RC damping circuit.....	141
Figure 7.7 Output voltage FFT without filter .....	141
Figure 7.8 Output voltage FFT for the R damped LCL filter with $R_{fa}=R_{fb}=0\Omega, 0.5\Omega,$ $1\Omega, 1.5\Omega, 2\Omega$ and $2.5\Omega$ .....	142
Figure 7.9 Output voltage FFT for the RC damped LCL filter with $R=1.5\Omega C=1.5\mu F,$ $R=1.5\Omega C=2.5\mu F, R=2\Omega C=1.5\mu F, R=2\Omega C=2.5\mu F,$ .....	142
Figure 7.10 Output voltage FFT with $R=2\Omega C=2.5\mu F$ and $R=2.5\Omega$ .....	143
Figure 7.11 MLC with LC filter.....	146
Figure 7.12 Output voltage waveform .....	146
Figure 7.13 Filtered output voltage waveform.....	147
Figure 7.14 THD comparison with different dead time. ....	149
Figure 7.15 THD comparison with 5 ticks.....	150
Figure 7.16 THD comparison with 9 ticks.....	150
Figure 7.17 SiC 280 THD comparison .....	151
Figure 7.18 SiC 040 THD comparison .....	152
Figure 7.19 Si FDP THD comparison.....	152

Figure 7.20 Si N95 THD comparison .....	153
---	-----

## List of Tables

Table 2.1 Switch states 3-level Neutral-Point Clamped .....	9
Table 2.2 Switch states 5-level Neutral-Point Clamped Full Bridge .....	10
Table 2.3 Switch states 5-level Neutral-Point Clamped .....	13
Table 2.4. Switching states and output voltage 3L-HB-FC .....	16
Table 2.5 Switch states 5-level Flying Capacitor Full Bridge .....	18
Table 2.6. Switch states 5-level Flying Capacitor .....	20
Table 2.7 CHB switching states and output voltage .....	23
Table 2.8. Comparison of components and levels of the NPC and FC topologies. ....	25
Table 3.1. THD comparison for Different PWM techniques and topologies. ....	52
Table 3.2. Switching states for the 5-level full bridge NPC (5L-FB-NPC) converter in Figure 3.22. ....	60
Table 3.3. States Sequence based on reference signal “a” .....	61
Table 3.4. Voltage effect in the DC link capacitors for the 5-level converter. ....	62
Table 4.1 System specification .....	69
Table 5.1 Test conditions .....	106
Table 5.2 Specifications buck mode .....	108
Table 6.1 Switching devices for performance evaluation in 5-level single phase converter .....	123
Table 6.2 Experimental evaluation test conditions .....	123
Table 6.3: Characteristics of blocking diode and antiparallel diode .....	124
Table 6.4 Harmonics voltage FFT magnitude.....	135
Table 7.1 Switching times of the devices evaluated .....	147
Table 7.2 Dead time in ns and ticks .....	148

## Chapter 1 Introduction

The impact created by the advancement of electronic systems has had, and is still having, an unprecedented impact on society. Electronics has not only created an industry in its own right, but has had a major impact on our quality of life. This impact can be felt everywhere and in a variety of market sectors including: i) electric transportation (trains, trams and now electric vehicles (EV)); ii) medical and health (MRI scanners to automated dosing); iii) information and communications technologies (computing and the internet); iv) automation of industry (improved industrial process and manufacturing) and v) consumer electronics and entertainment (television, game consoles). All of these are supported by networks of manufacturers and taken together this has led to enormous wealth creation.

Energy management is still a major concern with many actors including governments, energy suppliers, equipment manufacturers and users wanting to reduce wastage. Most electronic systems require some form electricity conditioning circuit to generate the correct voltage levels for operation. Power electronic conversion is now widely accepted as the best way of achieving this translation at high-efficiency and now is one of the most active research areas encompassing circuit topologies, devices and control.

The increasing concern surrounding the use of fossil fuels has motivated the use of electrical alternatives demanding efficiency and reliability. An example of this is the growing demand of EVs, in 2015 the UK government reiterated the promise to make sure that nearly all cars and vans are zero emission vehicles by 2050 [1-1]. One recent publication [1-2] shows that the number of electric vehicles registered during the second quarter (Q2) 2016 increased in 49% compared to 2015 and 253% compared to 2014 and it also details a plan introduced by the UK government to help to buy an EV with grant plans for up to £8,000.

EVs require a rechargeable battery and it is predicted that these batteries will reach their end of life within 5 to 10 years of standard driving as capacity reduction through ageing and wear out will make them no longer viable for vehicle applications. However, the EV battery will retain some useful capability and so it is predicted that 2<sup>nd</sup> life applications will emerge for them before their ultimate end-of-life and recycling. With the predicted

increased in the numbers of EVs on the road, the battery second life can help to reduce the cost of applications such as residential storage for a solar panel system.

There is presently a transition occurring in the energy generation industry where countries such as the UK are phasing out older fossil fuel power stations and replacing them with greener renewable energy supplies including both wind and solar. This transition presents many challenges and opportunities for power electronic energy conversion and energy storage systems, which are required to interface the renewable energy generators to the grid and provide grid support to maintain correct voltage levels and frequency. These power converters not only have to be efficient but they also have to produce a good power quality low distortion waveforms.

The previously described new and emerging applications are supported by significant advances in electronic technologies including semiconductor devices, power electronic converter topologies and digital control. High power converters require the use of electronic devices capable of withstanding high voltage and current stresses and this has led to the development of multilevel converters (MLC) that conveniently divide a high voltage into lower voltage levels suitable for power devices. By their virtue, these multiple levels introduce further quantisation steps in the output waveform, which significantly lower harmonic distortion and improve power quality when compared to conventional 2-level converters. Numerous MLC topologies have been studied with different characteristics that make them more appropriate for certain applications. Some MLC use separate DC voltage sources while others split a single DC voltage into several levels using capacitor dividers and diodes and require elaborated control algorithms to ensure waveform cleanliness by maintaining the capacitor voltage balanced.

## 1.1 Application and Motivation

This thesis describes the development of a 2<sup>nd</sup> life battery powered single-phase multilevel converter based power supply for operating hand tools and lighting on construction sites. A Neutral Point Clamped (NPC) multilevel converter was chosen as it represented the best option for this application since, not only it is the most studied topology in recent years, but it provides good performance in terms of harmonic reduction. A two stage conversion process was used where the multilevel converter provided a high power factor AC-DC interface and a buck-boost stage was used for

battery voltage conversion. Considering the application, the main focus of the research was:

- Control – In the MLC the voltage balancing of the DC-link capacitors and the output voltage. The DC-DC control to balance the DC-link and operation in both modes, charging and discharging.
- Efficiency – The efficiency improvement as a result of control methods, thermal management or new trends in devices.
- Emerging power device technology – The use of emerging wide band gap semiconductor devices in power electronics in MLC and DC-DC.
- Filtering – With an incremented number of levels on the MLC the reduction of harmonics and better voltage waveforms can be achieved which results in a reduction of filter size.
- Co-simulation – The use of modern design tools for system simulation and controller design within a single development environment.

A Five Level, Neutral Point Clamped Multilevel converter (5L-NPC-MLC) shown in Figure 1.1 was designed, constructed and experimentally validated. The National Instruments Multisim and LabVIEW environment was selected as the co-simulation platform and the control was implemented using an FPGA to provide fast and reliable control. The use of wide bandgap devices in the MLC proving the effects on thermal and efficiency improvements compared to those of the Si counterparts. Moreover the effect of WBG on harmonic distortion is also addressed.

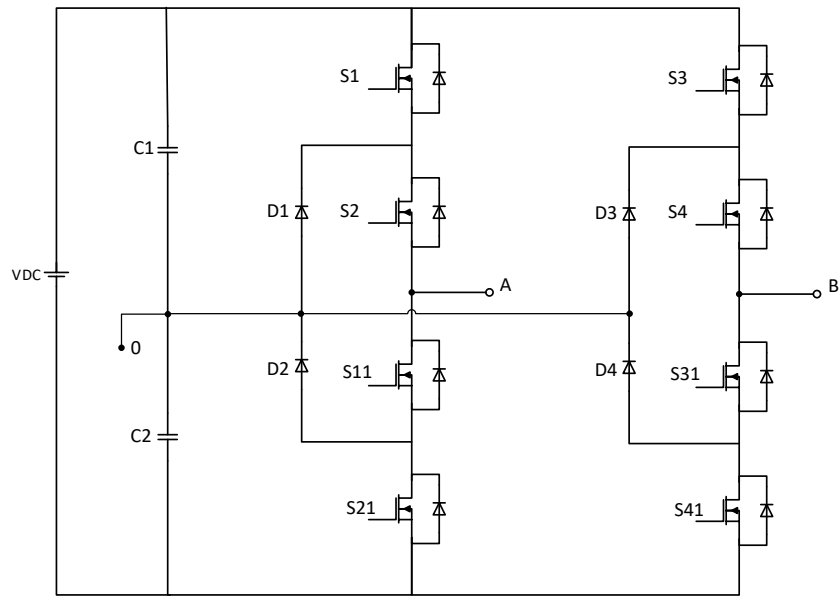


Figure 1.1: Circuit diagram for the 5-level single-phase converter

## 1.2 Thesis outline

This section briefly outlines the contents of the thesis chapter by chapter.

A review of prior research is presented in Chapter 2, which incorporates a literature review. This chapter describes formative work by introducing the main multilevel converter topologies, circuit operation, typical waveforms and control requirements including modulation techniques.

Modulation techniques are covered in further detail in Chapter 3. A typical multilevel converter consists of multiple switching devices (i.e. MOSFETs or IGBTs) connected to multiple voltage sources. The conduction states of the switching devices are controlled by a modulator whose role is to ensure: i) the required output is generated, ii) prevent damage occurring via cross-conduction (i.e. shoot-through) and for some specific topologies iii) to manage voltage levels on batteries or capacitors. This chapter reviews sinusoidal and space-vector modulation techniques and presents the Nearest 2 Vectors (N2V) method implemented in the hardware platform.

Chapter 4 describes the detailed design of the 5-level NPC multilevel converter (MLC) hardware platform used for experimental validation in this study. Detailed simulation

results of the subsystem in Simulink and then the integration of both sub-systems (DC-DC and MLC) in LabVIEW Co-simulation with Multisim.

Chapter 5 describes the design, implementation and experimental validation of the prototype hardware. The basic operating concepts of bidirectional converter are discussed alongside experimental results. The FPGA controller is described and the design power electronic converter stages are given. Throughout this chapter, LabVIEW was used as a co-simulation development system to expedite the design by allowing the FPGA based control system to be developed within a simulation environment and then downloaded onto the hardware platform. Experimental results demonstrating the performance of the system are also given.

Chapter 6 presents an experimental study on the performance of SiC MOSFETs and SiC anti-parallel diodes operating within a 5-level NPC MLC. The thermal performance of the MLC operating with SiC devices is compared with that of Si devices by measuring the temperature rise of the devices and the total efficiency of the converter. A description of the complete system and converter is presented and the semiconductor devices used in the evaluation are described.

Expanding on the previous section, Chapter 7 investigates the impact of SiC devices on the output waveform total harmonic distortion. This chapter initially review filter design and damping circuit through simulation and discusses norms and standards for power quality. A comparison with the THD performance against frequency and dead-time is given for the same SiC devices used in the previous chapter.

Conclusions and Future work are discussed in Chapter 8.

### 1.3 References

- [1-1] A. Jones “UK government pledges bold ambition for electric cars” DfT press notice, Dec. 2015 [Online]. Available: <https://www.gov.uk/government/news/uk-government-pledges-bold-ambition-for-electric-cars>
- [1-2] L. Butcher. “Electric Vehicles and infrastructure” Briefing Paper number CBP07480. House of Commons library. Dec. 2016 [Online]. Available: <http://researchbriefings.files.parliament.uk/documents/CBP-7480/CBP-7480.pdf>

## Chapter 2 – Background

### 2.1 – Introduction

The principal function of a converter is to transform energy in a form of direct current (DC) or alternating current (AC) to either the same form or to the other i.e. DC to DC, AC to AC or DC to AC. Converters can also be operated in bidirectional mode, permitting the reduction of system components when used in certain applications such as starter-generator drive systems.

The use of power electronic semiconductors in such converters, alongside filtering components (inductors and capacitors), allows efficient conversion of electrical energy. For DC-DC conversion, the input voltage may be stepped up or down both with or without the use of a transformer. For the case of the DC to AC, a suitable sequence and ON time of the switching components is required to form the required output voltage.

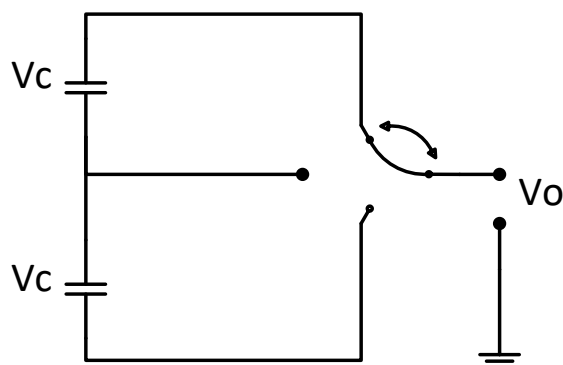


Figure 2.1 Functional diagram of a DC to AC converter

As shown in Figure 2.1 the conversion from DC to AC requires the voltage taken from the DC-link capacitors ( $V_c$ ) being switched to the output ( $V_o$ ) and periodically reversed at the output to provide AC and a very rough approximation to a sinusoidal voltage output. By using more switching elements, an appropriate switching sequencing, and clamping or balancing elements, the approximation to the sinusoidal output signal can be much improved and further enhanced by adding more steps (or levels) to the output to form a staircase waveform. The multilevel converter (MLC) was first introduced in [2-1] and the different topologies are investigated and explained in the following sections.

Although the increased number of levels significantly improves the quality of the waveform, it has a negative outcome in terms of the control of the voltage on the DC-link and the sequencing of the switches. Nowadays the use of Field Programmable Gate Array



(FPGA) to control the converters allows a profusion of levels due to: the availability of pulse width modulation (PWM) configurable cells; the reduction in cost; and ease of programming. An implementation of an algorithm proposed in [2-2], [2-3] is programmed and tested for the selected topology of MLC, as will be discussed later.

## 2.2 – Multi-Level Converters

Having an increased number of switching elements compared to the 2-level converter and clamping or balancing elements to generate the n-level staircase different topologies of multi-level converter are reviewed in [2-4] [2-5] and [2-6].

In recent years, there has been an increasing amount of literature on MLC. The most known and studied are concerned with:

- Neutral-Point-Clamped Converter (NPC)
- Flying Capacitor Converter (FCC)
- H bridge Converter (HBC)

The first topology of a 3-level converter was introduced in 1980 [2-1], the Neutral-Point-Clamped (NPC) converter, this converter uses diodes to clamp the voltage to form the 3-level output. The second topology FCC was introduced in 1992 by Maynard Foch, this uses capacitors to divide the voltage to form the n-level output. These two converters use a single DC source so the introduction of new topologies using separate DC sources are described in [2-7] mostly derived from the H-bridge topology and a combination with the previous basic topologies.

The conversion from DC to AC using MLCs allows generating a low distortion output and the advantages of reduced device ratings (voltage and current) for the components. The single-phase converter can be implemented in half-bridge (HB) or full-bridge (FB) for both topologies, [2-8] provides an example giving the analysis and design of the single phase system as it is implemented. Interfacing with the grid for applications on renewable energy sources feeding the network and vehicle to grid (V2G) is studied in [2-9] [2-10].

In the following subsections the 3 main topologies are introduced, with a description of each topology and the typical output waveforms. The waveforms were obtained from an open-loop simulation under no-load conditions for illustration. The switching frequency used is 5 kHz so the switching events are visible and the input DC voltage is 200V. At

the end of this section, a comparison of the topologies introduced will be available in terms of number of levels, output voltage and number of clamping elements.

### 2.2.1 Neutral-Point Clamped Converter

The neutral point clamped converter takes its name from the operation principle of clamping the voltage of each level using a diode. Taking only one phase from the topology proposed in [2-8] the 3-Level Half-Bridge Neutral-Point Clamped (3L-HB-NPC) topology is formed, the topology and waveform are shown in Figure 2.2 and Figure 2.3. The DC-link is composed of the capacitors  $C_1$  and  $C_2$  where the voltage is divided in 2 to create the level  $V/2$  and  $-V/2$  and the diodes  $D1$  and  $D2$  to clamp the voltage. The antiparallel diodes shown in each switch ( $S1 - S2$ ) and ( $S1' - S2'$ ). The MOSFETs in this case allow the converter to work in regeneration mode, enabling the converter to work as an AC to DC converter.

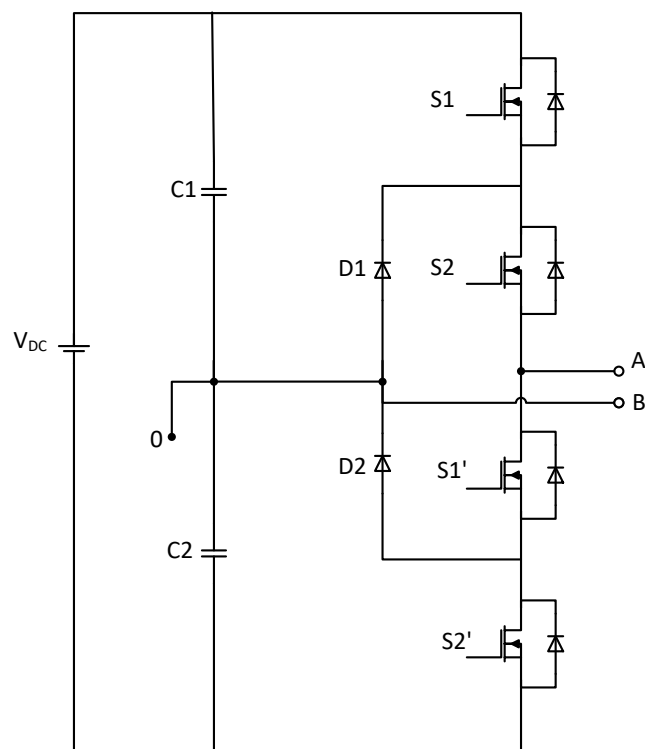


Figure 2.2 Neutral-Point Clamped 3-levels single phase

The output of the converter is taken from nodes A and B, where node B is the neutral point between the 2 capacitors, and the switches are controlled in such a way to ensure each capacitor is charged at  $V/2$  so the Voltage in AB can be  $-V/2$ , 0, and  $V/2$ , these makes the 3 levels. The states of the switches ( $S_1, S_2$ ) and the complementary switches

( $S_1'$ ,  $S_2'$ ) are shown in Table 2.1 where '1' means the switch is ON and '0' indicating the switch state is OFF.

<b>Vout</b>	<b>S<sub>1</sub></b>	<b>S<sub>2</sub></b>	<b>S<sub>1</sub>'</b>	<b>S<sub>2</sub>'</b>
<b>V<sub>dc</sub>/2</b>	1	1	0	0
<b>0</b>	0	1	1	0
<b>-V<sub>dc</sub>/2</b>	0	0	1	1

Table 2.1 Switch states 3-level Neutral-Point Clamped

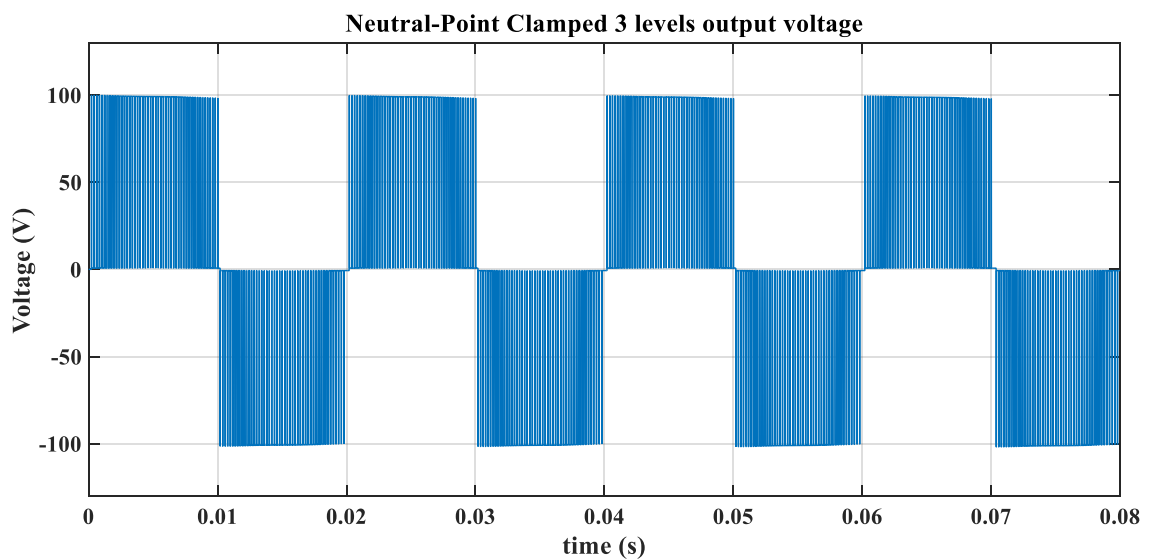


Figure 2.3 NPC 3-levels output waveform

The main advantages of this topology are the lower harmonic content of the output as the number of levels increase, reducing the size of the filter components, and also the control is easy to implement. The main disadvantage of this topology is the number of clamping diodes when the number of levels is high.

There are different implementations of the NPC topology reviewed in [2-11], for a single phase system, an additional leg or phase can be added to the topology as shown in Figure 2.4 making a 5-Levels Full-Bridge NPC (5L-FB-NPC) topology.

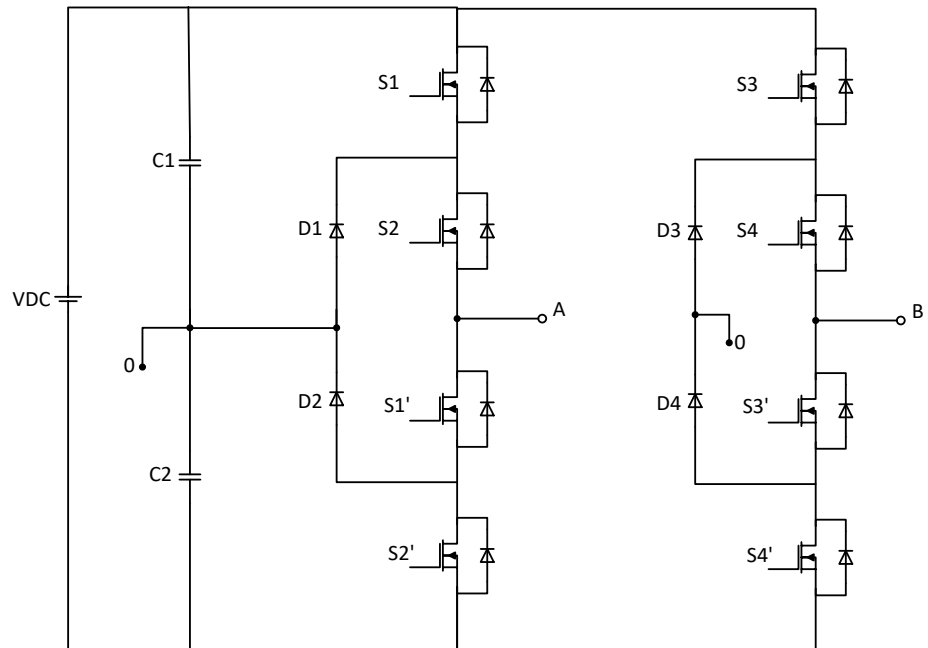


Figure 2.4 Neutral-Point Clamped 5-levels full bridge single phase

The advantage of this topology is the increased number of output levels, and these being  $V$ ,  $V/2$ ,  $0$ ,  $-V/2$  and  $-V$  with a single DC source. The switching states are shown in Table 2.2

<b>Vout</b>	<b>S<sub>1</sub></b>	<b>S<sub>2</sub></b>	<b>S<sub>1</sub>'</b>	<b>S<sub>2</sub>'</b>	<b>S<sub>3</sub></b>	<b>S<sub>4</sub></b>	<b>S<sub>3</sub>'</b>	<b>S<sub>4</sub>'</b>
<b>Vdc</b>	1	1	0	0	0	0	1	1
<b>Vdc/2</b>	0	1	1	0	0	0	1	1
<b>0</b>	0	0	1	1	0	0	1	1
<b>-Vdc/2</b>	0	0	1	1	0	1	1	0
<b>-Vdc</b>	0	0	1	1	1	1	0	0

Table 2.2 Switch states 5-level Neutral-Point Clamped Full Bridge

The waveform can be seen in Figure 2.5. The redundant states to generate the output voltage levels are detailed in the next section. The drawback of this topology is the common mode voltage.

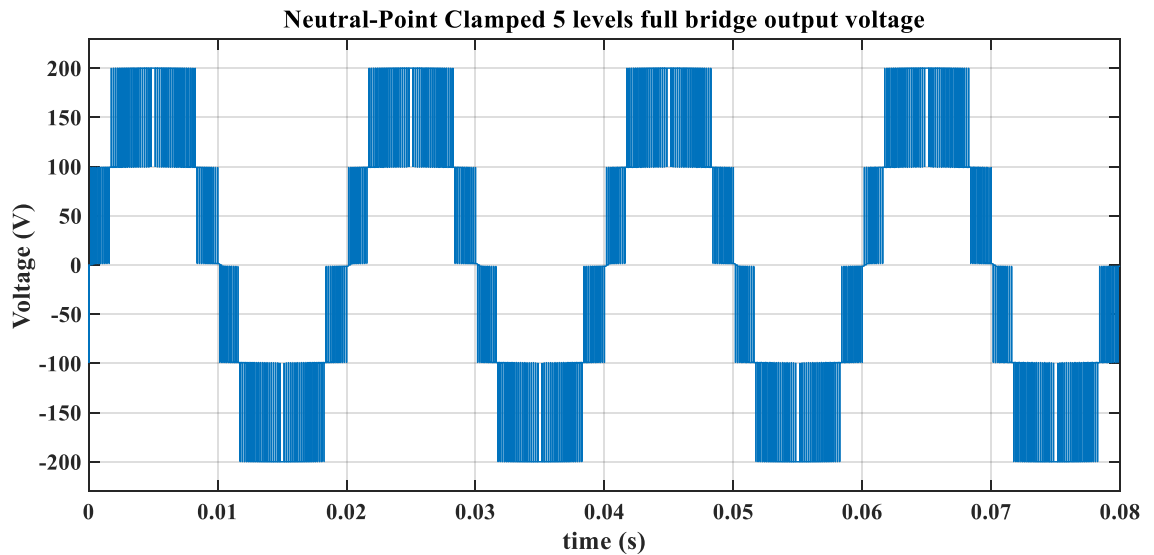


Figure 2.5 NPC 5-levels full bridge output voltage waveform

The 5-Level Half Bridge (5L-HB-NPC) topology and the output voltage waveform is shown in Figure 2.6 and Figure 2.7 respectively, this topology has the same number of levels as the 5L-FB-NPC topology explained previously, but the levels are  $V/2$ ,  $V/4$ ,  $0$ ,  $-V/4$ ,  $-V/2$ . The number of switching elements in each topology is the same but the number of DC-link capacitors is now 4, with 6 clamping diodes.

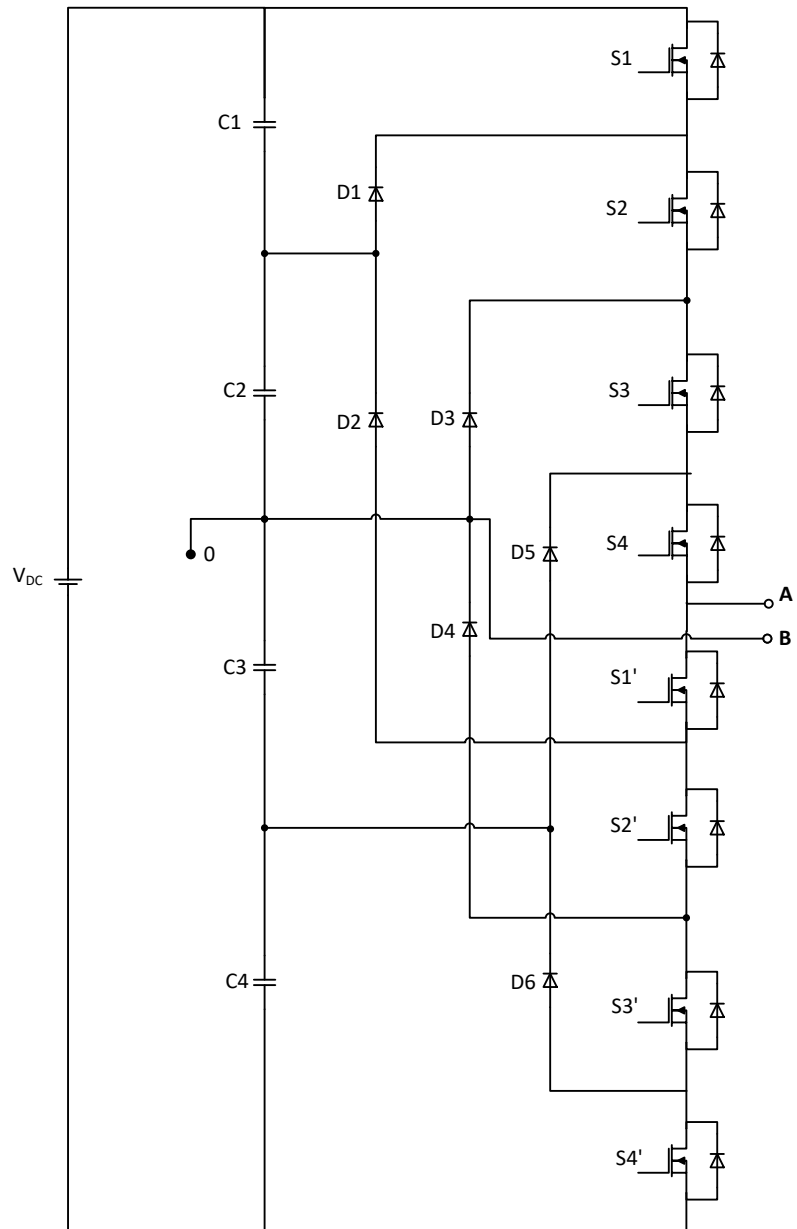


Figure 2.6 Neutral-Point Clamped 5-level Half Bridge Single phase

The switching states for  $S_1$  to  $S_4$  and their correspondent complementary states to generate each of the levels are shown in Table 2.3.

The control of the switching sequences can be achieved using PWM or Space Vector Modulation (SVM) techniques explained in following sections.

<b>Vout</b>	<b>S<sub>1</sub></b>	<b>S<sub>2</sub></b>	<b>S<sub>3</sub></b>	<b>S<sub>4</sub></b>	<b>S<sub>1</sub>'</b>	<b>S<sub>2</sub>'</b>	<b>S<sub>3</sub>'</b>	<b>S<sub>4</sub>'</b>
<b>V<sub>dc</sub>/2</b>	1	1	1	1	0	0	0	0
<b>V<sub>dc</sub>/4</b>	0	1	1	1	1	0	0	0
<b>0</b>	0	0	1	1	1	1	0	0
<b>-V<sub>dc</sub>/4</b>	0	0	0	1	1	1	1	0
<b>V<sub>dc</sub>/2</b>	0	0	0	0	1	1	1	1

Table 2.3 Switch states 5-level Neutral-Point Clamped

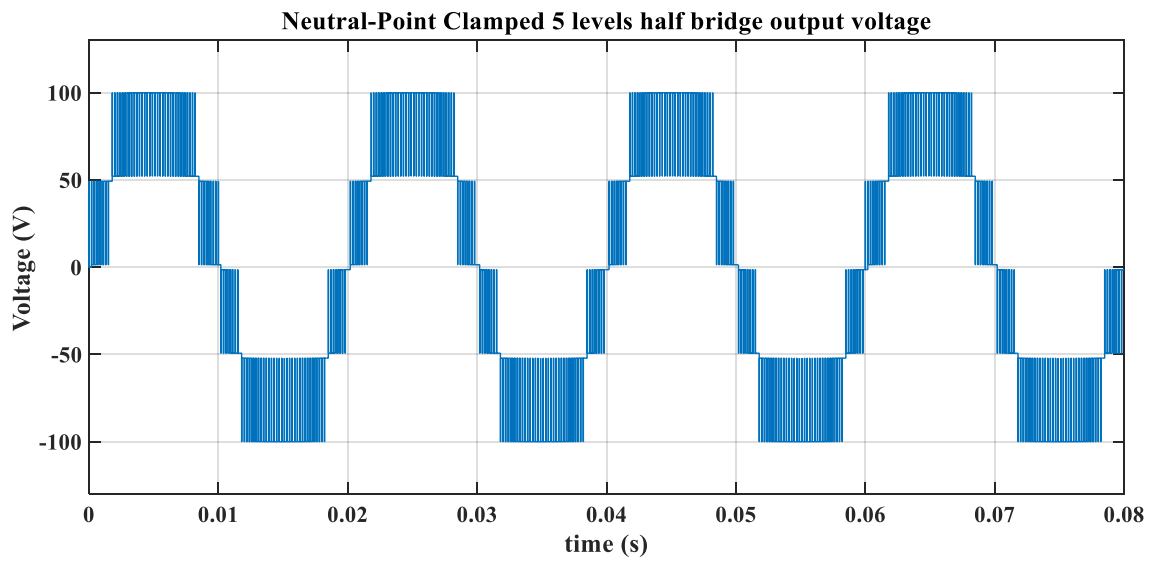


Figure 2.7 NPC 5-levels output voltage waveform

Similar to the adaptation made to form the 5L-FB-NPC, another leg or phase is added to the 5L-HB-NPC to form a 9-Levels Full-Bridge Neutral-Point Clamped (9L-FB-NPC) as shown in Figure 2.8 the 9-levels can be appreciated in Figure 2.9.

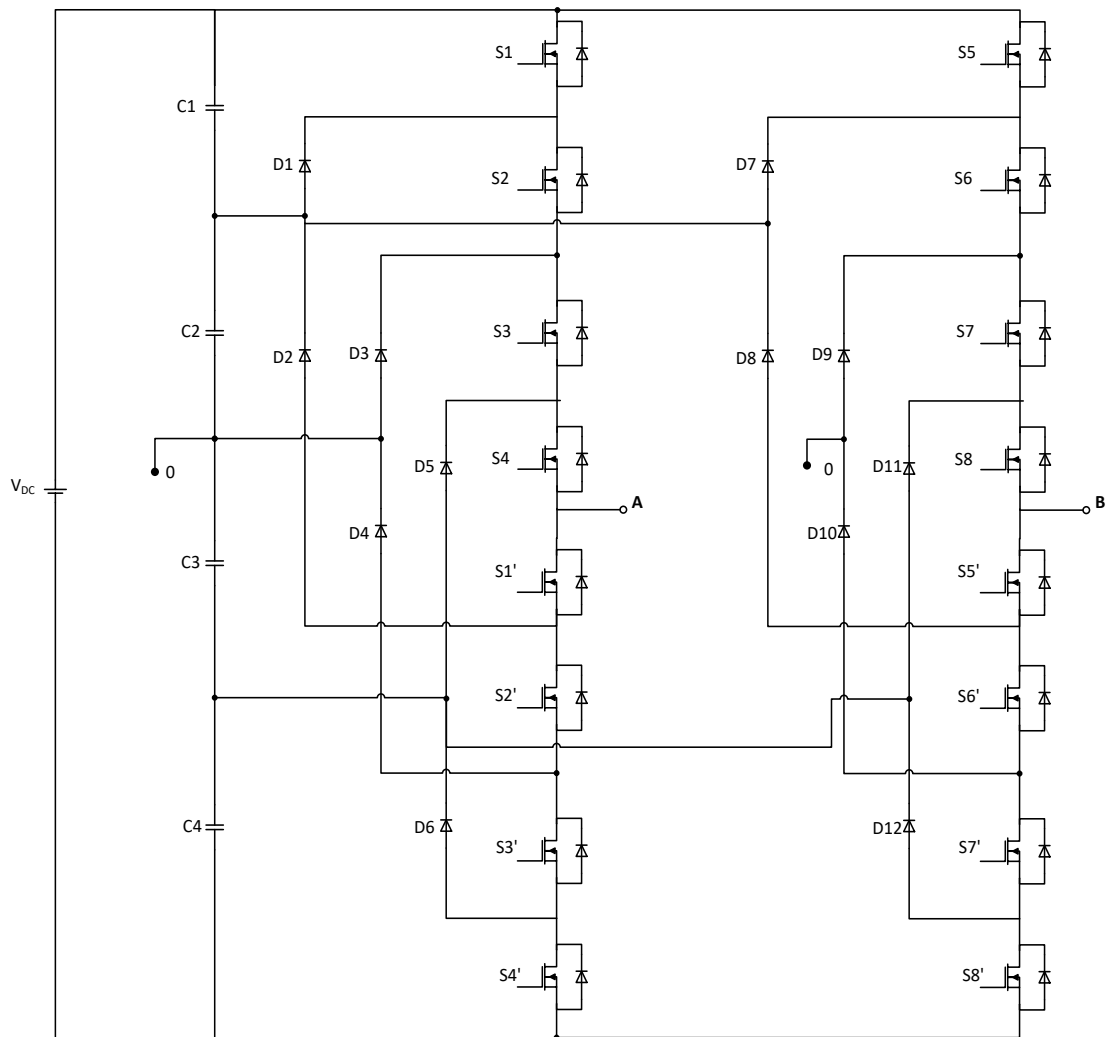


Figure 2.8 Neutral-Point Clamped 9-level Full Bridge Single phase

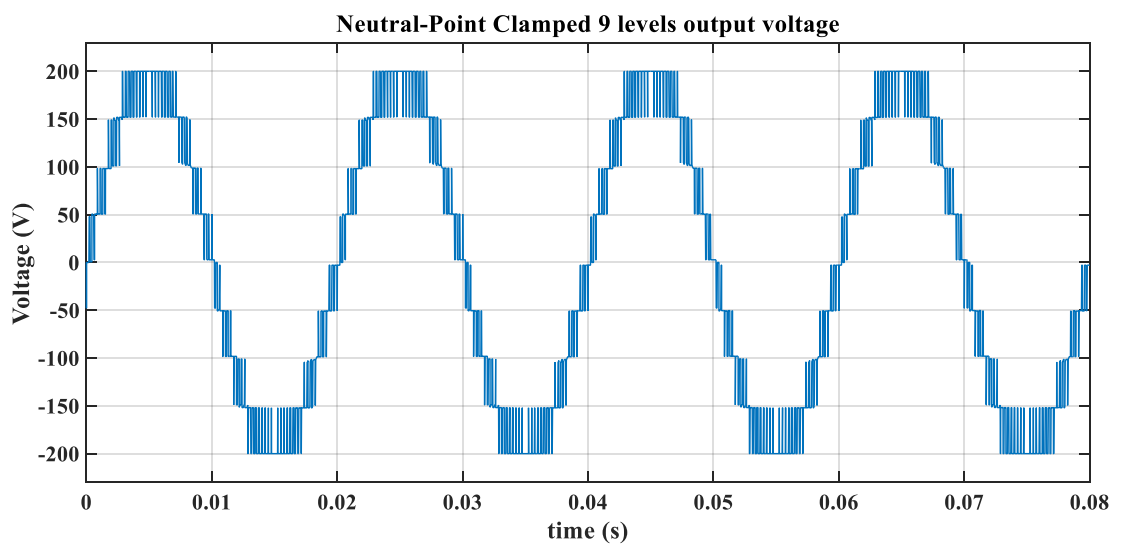


Figure 2.9 NPC 9-levels full bridge output voltage waveform



The complexity of the control of this topology is greater as there are 16 switches to control, along with 4 capacitors to balance in the DC-link.

The levels can be increased to n-number following the concept presented in this section. The literature presented in [2-12] investigates a 5 and 7 levels converter and a comparison is made between NPC, FCC and HB converters. A 7-level converter in [2-13] studies back-to-back converters focusing on the control and harmonic content of the system. A work presented in [2-14] introduces a simulation system for a 13-level converter analyzing the Total Harmonic Distortion (THD) and simulation performance.

### 2.2.2 Flying capacitor converter

In Figure 2.10 the 3 levels FCC is presented, this topology uses four switches (S1, S2, S1' and S2'). Two of those switches control the current flow while the other two generate the switching to form the output waveform. The converter also has two input capacitors (C1 and C2) to split the input voltage in two parts in a similar way to the NPC discussed previously. Additionally, a third capacitor (C) is included, denominated as a flying capacitor for its position in this topology, this capacitor generates the level zero in the output waveform Figure 2.11. The output is taken as well from nodes A and B and the operating principle is similar to that in the NPC but instead of using diodes to block the levels, capacitors are used to do it. The switches are controlled in such a way to ensure each capacitor is charged at  $V/2$  and  $-V/2$  so the Voltage in AB can be  $-V/2$ , 0, and  $V/2$ , these makes the 3 levels.

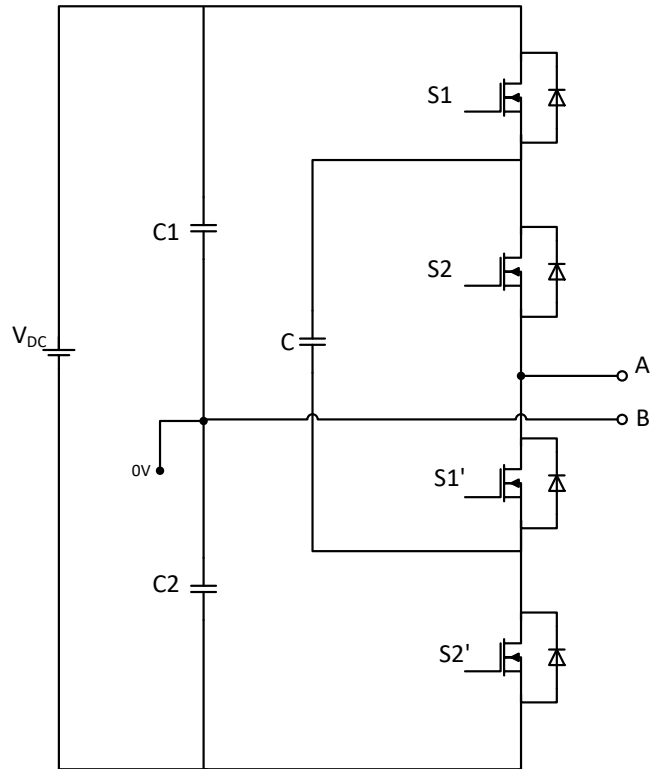


Figure 2.10 Flying capacitor 3-level single phase

The switching states of the 3L-HB-FC are shown in Table 2.4. It can be seen that for the level 0 there are 2 different states that can be used, known as redundant states. As the number of levels increase, the redundant states increase, giving degrees of freedom to control different characteristics in the converter, such as the balance in the DC-link capacitors.

<b>Vout</b>	<b>S<sub>1</sub></b>	<b>S<sub>2</sub></b>	<b>S<sub>1</sub>'</b>	<b>S<sub>2</sub>'</b>
<b>V<sub>dc</sub>/2</b>	1	1	0	0
<b>0</b>	1	0	0	1
<b>0</b>	0	1	1	0
<b>-V<sub>dc</sub>/2</b>	0	0	1	1

Table 2.4. Switching states and output voltage 3L-HB-FC

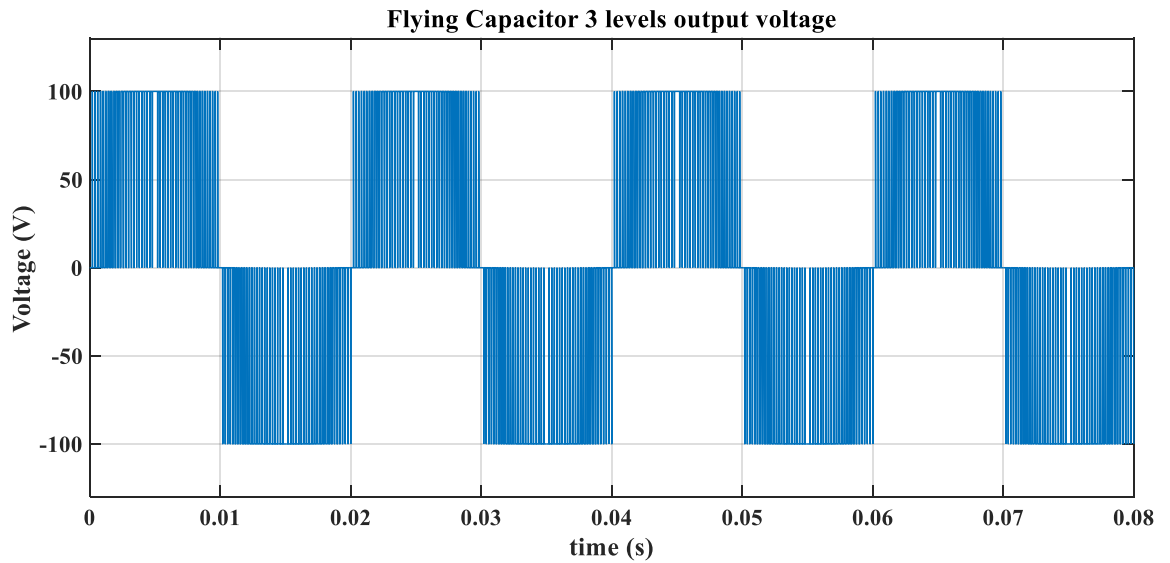


Figure 2.11 Flying capacitor 3-levels output voltage waveform

The main advantages of this topology are the redundant combinations required to generate a level that allows the capacitor voltage balancing, the reduction in filtering size when the number of levels is high. The main disadvantage is that it requires an excessive amount of capacitors as the number of levels increases. The capacitors tend to suffer from large volumes, high costs, and lower reliability when compared to semiconductors.

The 5-Levels Full-Bridge Flying-Capacitor is shown in Figure 2.12 formed by adding an additional leg to the 3L-HB-FC. The switching states are shown in Table 2.5. The topology employs 2 capacitors (C3 and C4) to balance the voltage in order to form the staircase waveform of 5-levels see Figure 2.13

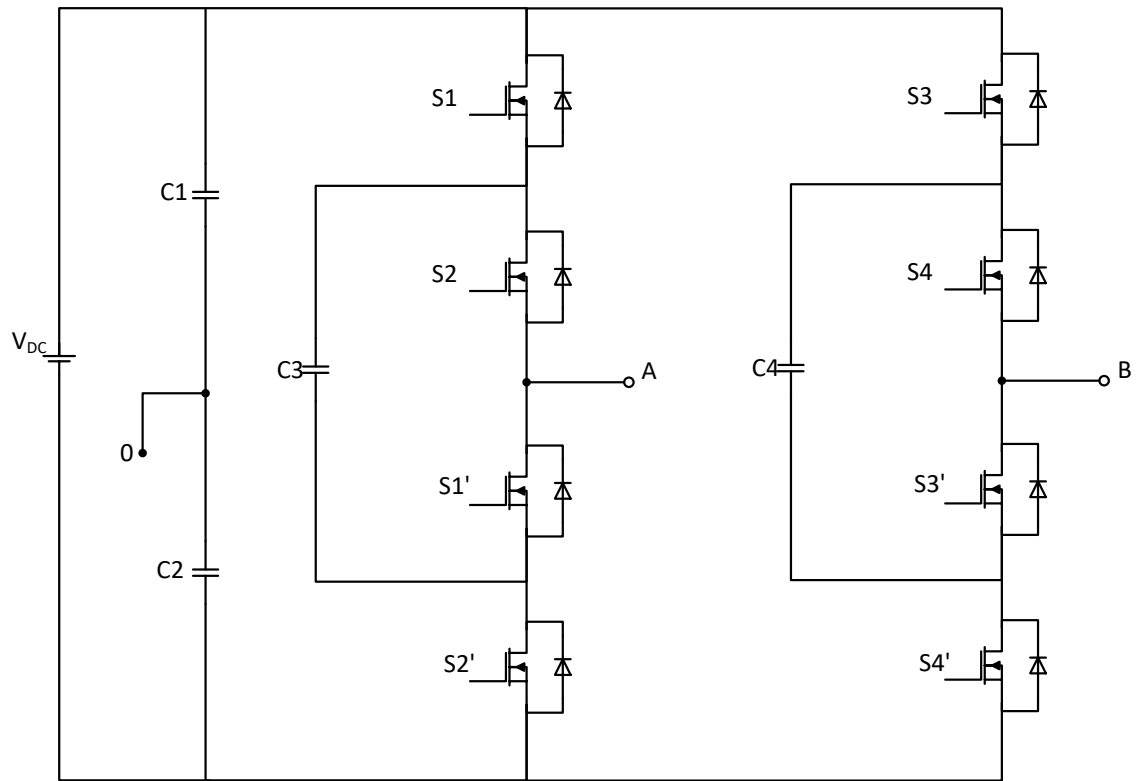


Figure 2.12 Flying Capacitor 5-level Full Bridge Single phase

<b>Vout</b>	<b>S<sub>1</sub></b>	<b>S<sub>2</sub></b>	<b>S<sub>1</sub>'</b>	<b>S<sub>2</sub>'</b>	<b>S<sub>3</sub></b>	<b>S<sub>4</sub></b>	<b>S<sub>3</sub>'</b>	<b>S<sub>4</sub>'</b>
<b>Vdc</b>	1	1	0	0	0	0	1	1
<b>Vdc/2</b>	1	0	0	1	0	0	1	1
<b>0</b>	0	0	1	1	0	0	1	1
<b>-Vdc/2</b>	0	0	1	1	1	0	0	1
<b>-Vdc</b>	0	0	1	1	1	1	0	0

Table 2.5 Switch states 5-level Flying Capacitor Full Bridge

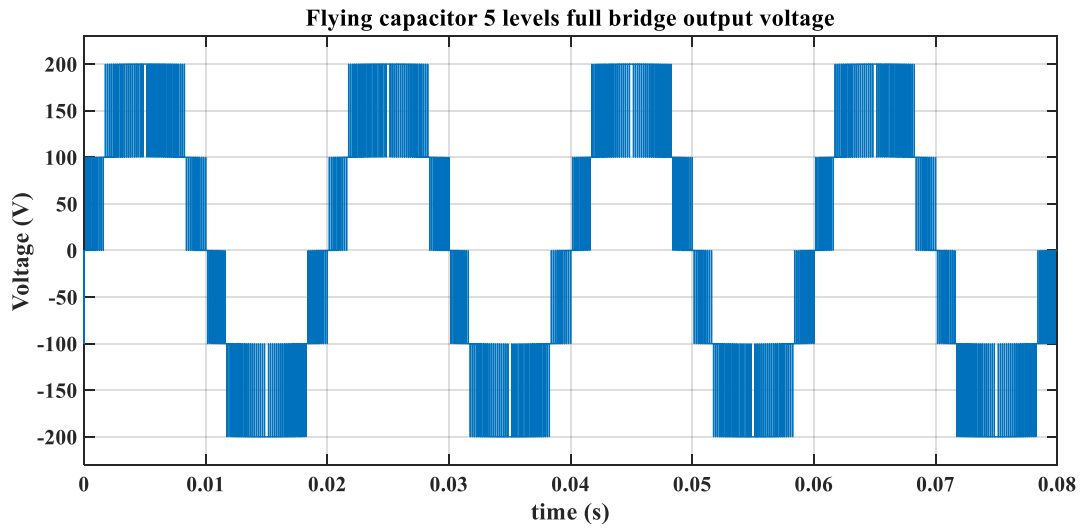


Figure 2.13 Flying capacitor 5-levels output voltage waveform

The number of levels can be incremented in a similar fashion as with the NPC, to increase the levels to 5, the topology used in a Half bridge FCC (5L-HB-FCC) is shown in Figure 2.14.

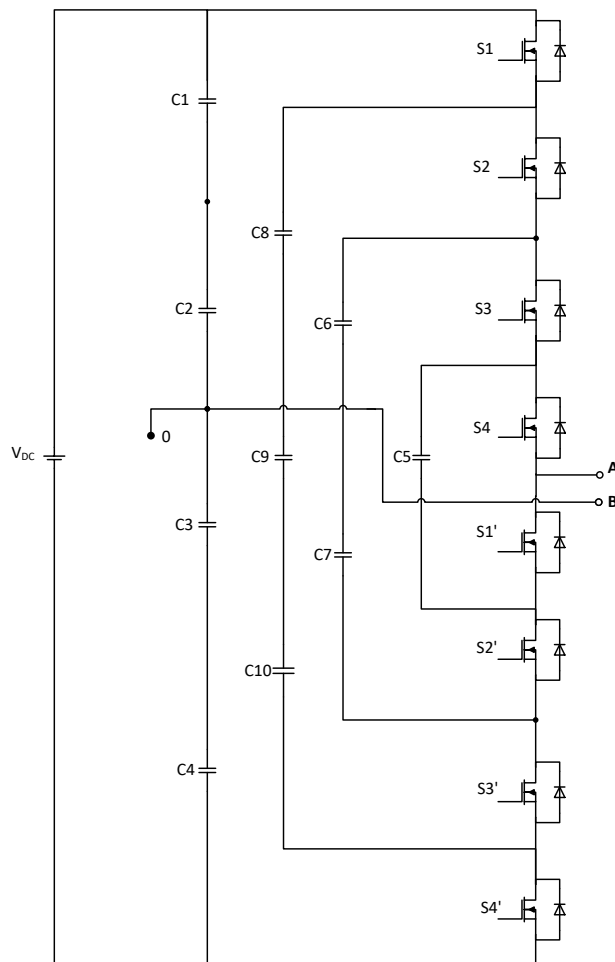


Figure 2.14 Flying capacitor 5-level half bridge single phase

The states applied to the switches to form the output AC voltage is shown in Table 2.6 and the output waveform is shown in Figure 2.15

<b>Vout</b>	<b>S<sub>1</sub></b>	<b>S<sub>2</sub></b>	<b>S<sub>3</sub></b>	<b>S<sub>4</sub></b>	<b>S<sub>1</sub>'</b>	<b>S<sub>2</sub>'</b>	<b>S<sub>3</sub>'</b>	<b>S<sub>4</sub>'</b>
<b>Vdc/2</b>	1	1	1	1	0	0	0	0
<b>Vdc/4</b>	1	1	1	0	1	0	0	0
<b>0</b>	1	0	1	1	0	0	1	0
<b>-Vdc/4</b>	1	0	0	0	1	1	1	0
<b>Vdc/2</b>	0	0	0	0	1	1	1	1

Table 2.6. Switch states 5-level Flying Capacitor

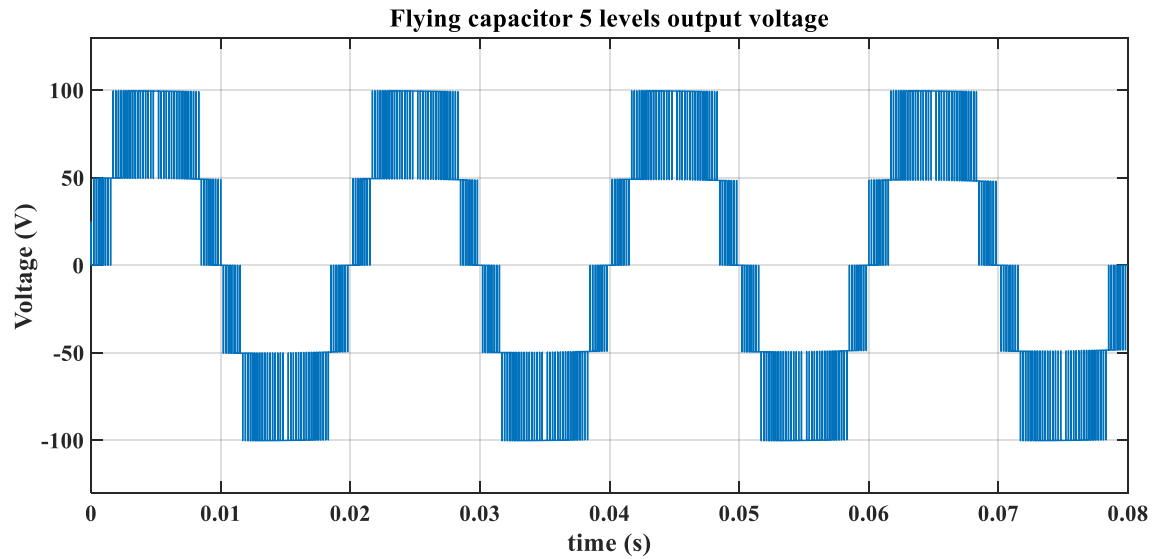


Figure 2.15 Flying capacitor 5-levels half bridge output voltage waveform

The 9-level FCC is formed with 2 legs, each being a 5-level FCC. Figure 2.16 shows the topology, and the waveform generated is shown in Figure 2.17. It can be seen that the number of capacitors in this topology is large, with each capacitor voltage rating being equal to that of the switching devices, in which case the number of capacitors as a function of number of levels ( $n$ ) would be  $(n-1)*(n-2)/2$ . As each capacitor voltage requires balancing, this introduces a large difficulty in the control and balance of the levels, even in open loop. It may be seen that in no-load conditions, Figure 2.17, the some of the levels are unbalanced during the switching states to form  $V_{dc}/4$ ,  $0$  and  $-V_{dc}/4$  where there is a voltage step of  $\pm 30V$  instead of the  $\pm 50V$  to form  $\pm V_{dc}/4$ . The level unbalance is due to

the open loop conditions where no balance algorithm has been used Therefore, in order to generate the MOSFET gate signals, a modulation technique must be used to achieve the desired output voltage while balancing the voltage levels across the various capacitors in a similar way to that presented for the NPC topology.

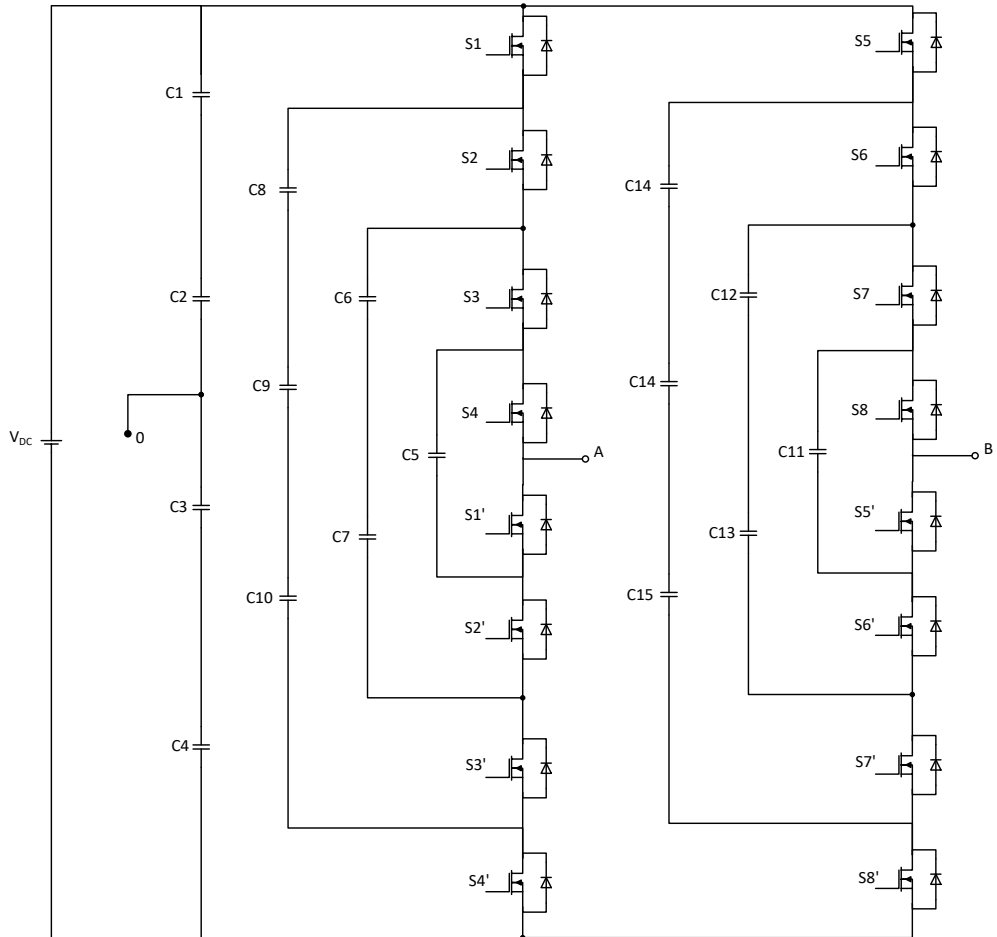


Figure 2.16 Flying capacitor 9-level full bridge single phase

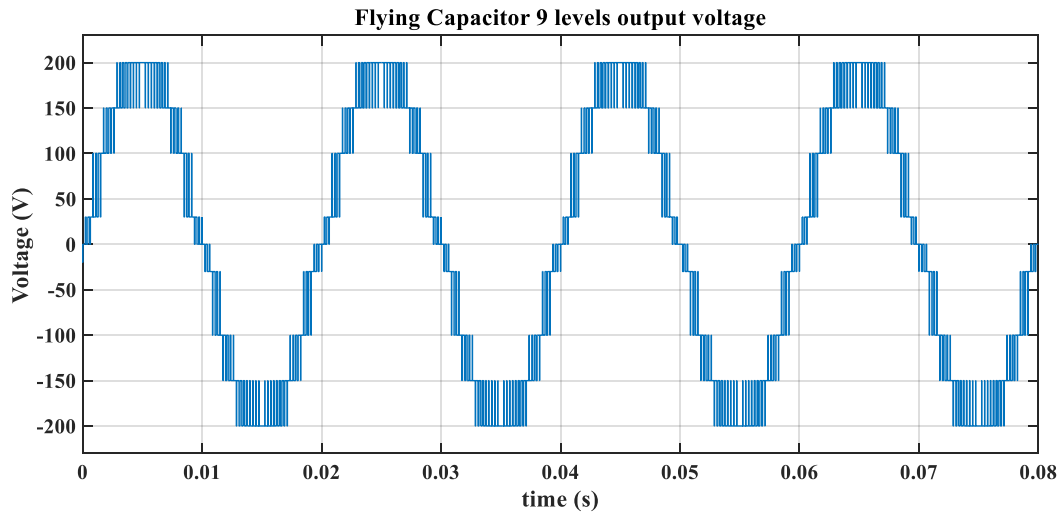


Figure 2.17 Flying capacitor 9-levels output voltage waveform

For both the NPC converter and FCC inverters, the states for each level are detailed in, Table 2.1, Table 2.3, Table 2.4 and Table 2.6 respectively. For the FCC, output levels of  $\pm V_{dc}/2$ , 0 and  $\pm V_{dc}/4$  provide redundant switching states that can be utilised for capacitor balancing.

### 2.2.3 Cascaded H-Bridge.

This topology is formed by cascading single phase H-bridges, the characteristic of this converter is that it requires an independent DC source, for each level. The topology is shown in Figure 2.18, where it can be seen that it doesn't have clamping diodes or 'flying' capacitors. To increase the levels with this topology, an addition of voltages generated from other cells or bridges, is implemented.

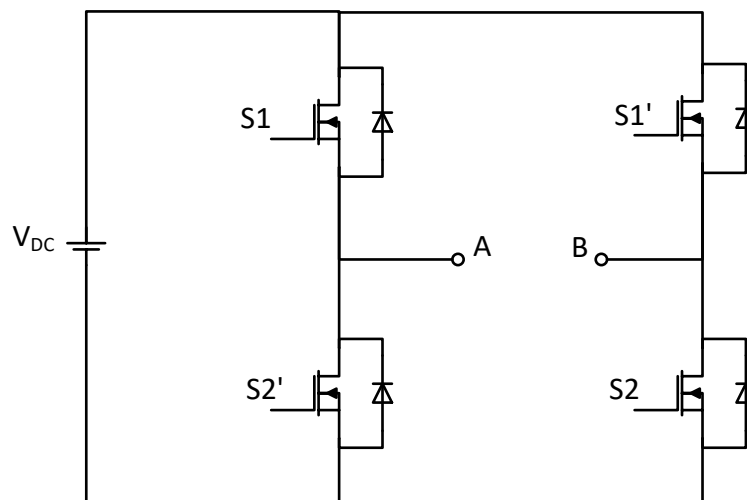


Figure 2.18 Cascaded H-bridge 3-levels topology.



The converter shown in Figure 2.18, has four switching devices, two of the switches are located in one leg of the H-bridge and the other two to the other side. The switching states of the Cascaded H-Bridge (CHB) are presented in Table 2.7, the switches operate in a complementary form. This topology doesn't divide the input voltage in two as the previous topologies presented. Due to this, the switching devices have to block all the input voltage. However, the voltage of each level is lower than the DC input in the NPC and FCC.

<b>Vout</b>	<b>S<sub>1</sub></b>	<b>S<sub>2</sub></b>	<b>S<sub>1</sub>'</b>	<b>S<sub>2</sub>'</b>
<b>V<sub>dc</sub></b>	1	1	0	0
<b>0</b>	0	1	1	0
<b>-V<sub>dc</sub></b>	0	0	1	1

Table 2.7 CHB switching states and output voltage

The output voltage from terminals A and B is of three levels as shown in Figure 2.19.

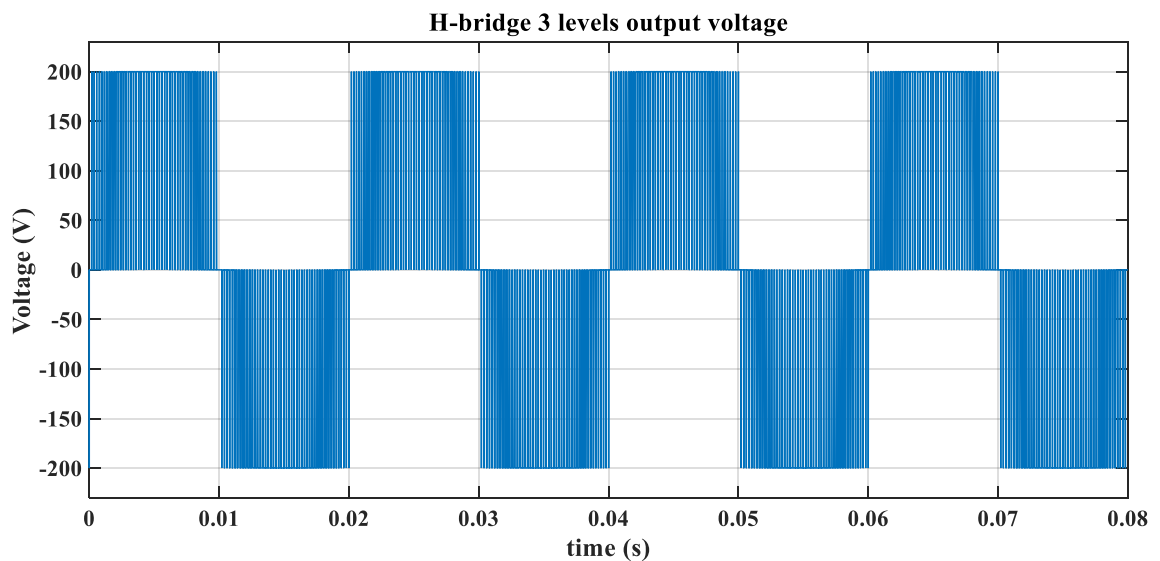


Figure 2.19 H-bridge 3-levels output voltage waveform

The topology in Figure 2.20 corresponds to the 5-level H-bridge converter, this topology requires separate DC sources and the output is taken from nodes A and B. This topology shows how the cascading of the converters to increase the levels. The output voltage is shown in Figure 2.21, the levels are 5 with the maximum voltage as  $2 \cdot V_{DC}$ .

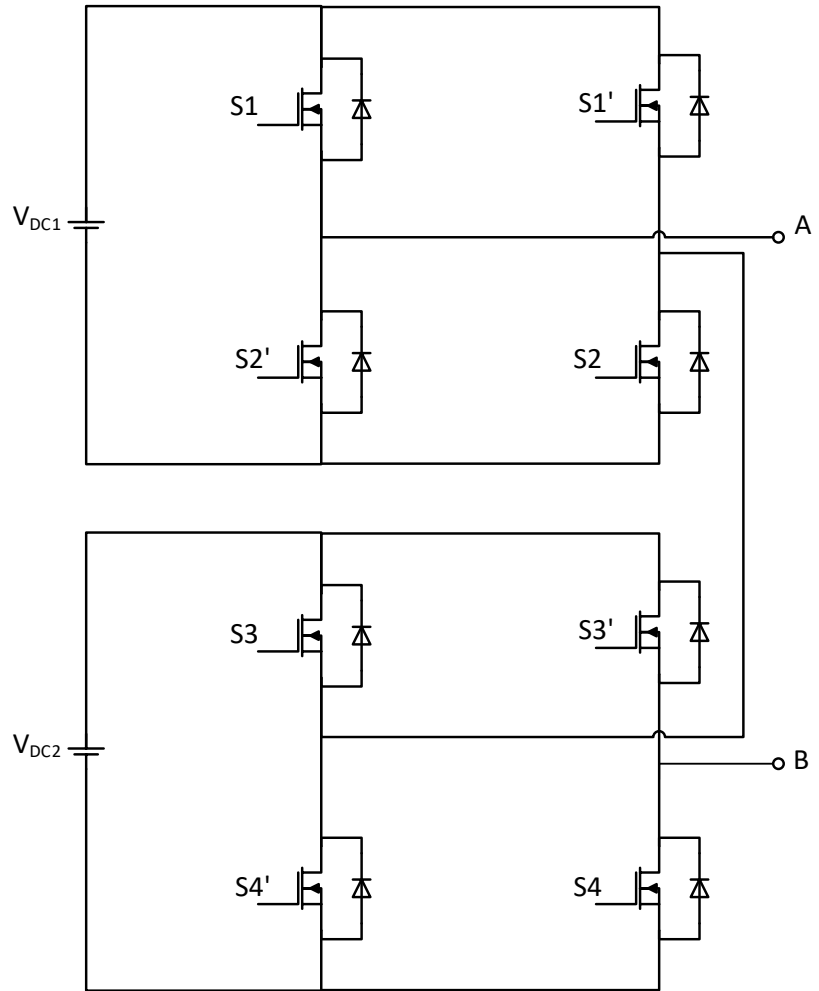


Figure 2.20 Cascaded H-bridge 5-levels topology

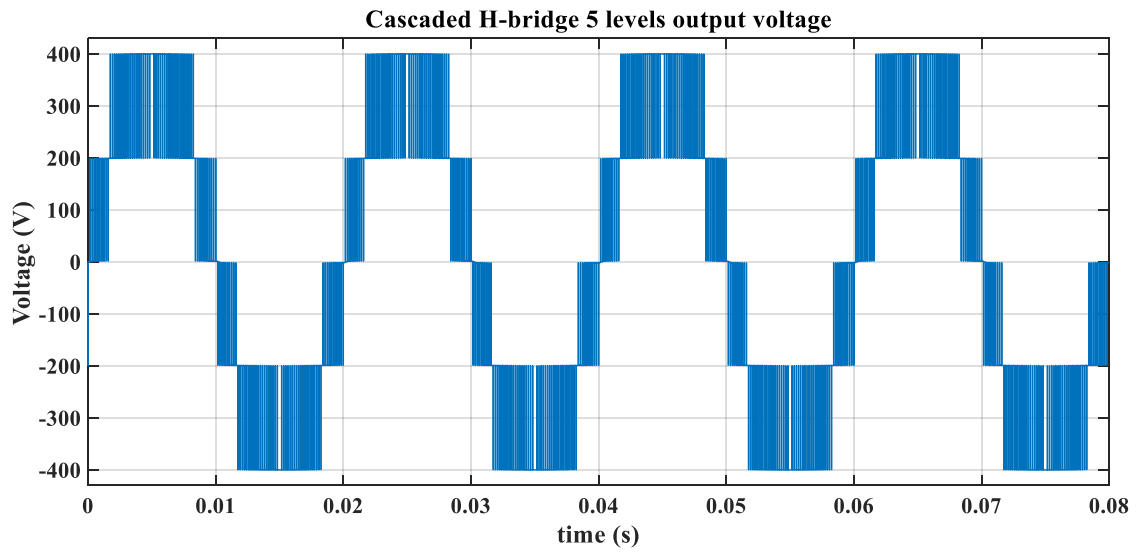


Figure 2.21 5-levels cascaded H-bridge output voltage waveform

The main advantages in comparison with NPC and FCC is that it doesn't need external clamping diodes or capacitors to generate the level zero. The main disadvantage is the need of individual voltage sources for real power applications. A modification of this topology is the modular multilevel converter (MMC) where a capacitor is used as the DC source and this topology is beginning to find favour in power systems applications by virtue of its ability to handle high voltages. A study in [2-15] presents a MMC as a motor drive focusing on the balance of the losses controlled with an algorithm proposed for the 1MW drive. An MMC for a renewable energy application presented in [2-16] analyses the efficiency and thermal loading on the converter used in a wind power generator at 2MW and 10MW.

#### 2.2.4 Comparison

For an m-leg converter formed with n-level converters, the characteristics in terms of number of components are detailed in Table 2.8, m=1 for a HB and m=2 for FB converter topologies.

Topology	Max. $V_{out}$	Legs	Output Voltage Levels	DC-link Capacitors	Switching Devices	Clamping Diodes or Capacitors
<b>Neutral-Point Clamped</b>	$\frac{V_{DC}}{2}$	1	3	2	4	2
	$V_{DC}$	2	5	2	8	4
	$\frac{V_{DC}}{2}$	1	5	4	8	6
	$V_{DC}$	2	9	4	16	12
<b>Flying Capacitor</b>	$\frac{V_{DC}}{2}$	1	3	2	4	1
	$V_{DC}$	2	5	2	8	2
	$\frac{V_{DC}}{2}$	1	5	4	8	6
	$V_{DC}$	2	9	4	16	12
<b>Cascaded H-Bridge</b>	$V_{DC}$	2	3	0	4	0
			5		8	
			9		16	

Table 2.8. Comparison of components and levels of the NPC and FC topologies.

A converter with an output voltage of  $V_{DC}$  will be used to maximize the use of the power source and to reduce the size of a DC-DC converter. Having reviewed the characteristics

for each MLC with output voltage level of  $V_{DC}$ , it can be seen from Table 2.8 that the Cascaded H-Bridge can generate the required voltage level with no clamping elements and no DC-link capacitors with the same number of switching devices compared to NPC and FCC. However, the main characteristic of CHB topology is the requirement of individual DC sources per level, making this topology not viable for use with a single battery pack.

FCC with 2 legs and 5 levels only uses 2 flying capacitors and 2 DC-link capacitors but the size and reliability was felt to be too restrictive and so that topology was not chosen. The NPC with 2-legs and 5-levels (5L-FB-NPC) was chosen due to the reduced number of clamping elements (diodes) and DC-link capacitors.

### 2.3 – Modulation in MLC

The complexity of the PWM modulation in MLC increases with the number of levels. The greater the number of levels, the greater the number of integrated circuits (IC) that have to be used when implementing the modulator. This means an increased modulator size and a reduced reliability of the system.

There are extensive literature reviews analyzing and studying PWM in [2-4], [2-5], [2-17], [2-18] and [2-19]. From these papers it may be found that the modulation techniques for MLC most frequently utilized are: selective harmonic elimination, space vector and sinusoidal.

#### 2.3.1 Selective harmonic elimination

This is a modulation at a fundamental frequency or staircase [2-20]. The main characteristic of this technique is the elimination of the output voltage with low frequency content. The modulation index in this technique doesn't allow a wide voltage control.

The complexity of the calculations makes this technique very difficult to implement in levels greater than three. In [2-21] a method to implement the modulation in unbalanced DC inputs is proposed as well as an evaluation at a wider range of index modulation.

#### 2.3.2 Space Vector Modulation

The advantage of this modulation technique is the maximum use of the DC link allowing the modulator to operate in an over modulation region. Moreover, SVM enables the

switching devices to operate more effectively as the control algorithm is fast and simple to compute.

The main characteristic of this technique is the reduction of switching losses by selecting the vectors appropriately. In three phase systems the modulation can be solved using Park transformation by using rotating frame references of an AC signal. However, the vector selection becomes more difficult as the redundant or number of levels increase.

There has been an increasingly interest on this modulation technique making it an active research topic in power electronics, however the implementation can become very complex in 3-phase converters and with higher number of levels. There is a variation of this method introduced in Chapter 3 for a single phase MLC that has produced very good results in this investigation.

### 2.3.3 Sinusoidal PWM

This technique has been widely studied and applied to MLCs. Its simplicity and ease of implementation even in the over modulation region makes it a very popular object of study.

The implementation consists of a comparison of sinusoidal signal and a triangular carrier signal within the hardware modulator. Depending on the number of levels an  $(n-1)$  number of carrier signals are required, where  $n$  is the number of levels.

PWM can be divided in two major categories: disposition and shifting of the carrier signals. In Chapter 3, the modulation involving the disposition of the carrier signals is presented.

## 2.4 – Applications

The first implementations of MLCs used Gate Turn-Off devices (GTOs) as the switching device [2-1] [2-22]. Recent applications have employed IGBTs at higher power and frequencies. Lately, the tendency is to use Silicon Carbide (SiC) and Gallium Nitride (GaN) devices in MLC. Chapter 6 presents an evaluation of SiC devices as switches in MLC NPC.

Some of the MLC applications are presented in this section. There is a large range of applications but most of them are in the middle to high power.

### I. AC motor drives.

There are several advantages to use a multilevel converter as a motor drive over the conventional drives [2-23] [2-24]. The converter topology being used is dependent on the characteristics of the DC voltage source, and whether or not the regenerative braking energy will be stored. For systems connected to the mains (AC) a rectifier is necessary (passive or active), and if the power returns to the source then a back-to-back bidirectional converter will be required.

## II. Static-Synchronous Compensation (STATCOM)

In order to compensate the reactive power in the grid, capacitor banks are connected through a MLC topology. A compensator presented in [2-25] is an example of a reactive power compensation using an 11-level, full bridge cascaded topology. There are also some other examples of this particular application in [2-26] and [2-27].

## III. Flexible AC Transmission Systems (FACTS)

In this application the aim is to regulate the active and reactive power in the grid to improve the performance and use of the power network [2-28]. FACTS is based on the principle of distributed feeds, where a series of systems are connected to the network and depending on what is required the systems will store or feed power in a flexible manner.

## IV. Renewable energy sources interfaced with the grid

Nowadays, an increase in studies on renewable energy (wind and solar) interfacing with the grid using MLC have been reported [2-29] [2-30]. There are many advantages to using MLC for this application, for example, reduced size, improved efficiency, higher power operation and signal quality. A particular application on this category is the V2G interface [2-31] this represents an application of a future power system as an aid to fuel from fossil resources, where a vehicle's battery can be used to generate and feed the grid at peak times.

To investigate the benefits of using the topology and control described above, the first approach to the use of MLC is an application system on construction sites power supplies. The characteristic of such power supplies is the use of low voltage (110 VAC) and single-

phase to operate hand tools and lighting in construction sites in the UK. Working with low voltage is required to reduce the accidents caused by electric faults. Moreover, a repurposed EV battery can supply the MLC. In the following subsection, a review of MLC connected to batteries is presented and the stage to interconnect the battery and the MLC is also introduced.

#### 2.4.1 – Battery connected MLCs

The efficiency improvement in power converters is a common subject of study throughout the power electronics industry, more specific in electric vehicle (EV) applications. There are many different approaches to achieving efficiency improvements by utilizing novel techniques and topologies. In Chapter 4, the description of the system studied in this work is presented in detail. In general, the main parts of the system are, the DC source, converters (DC-DC and MLC) and controller, in this case an FPGA. The DC source considered for this system is a ‘second-life’ battery from a HEV, to be re-purposed as a battery for construction site stand-alone power supplies. In this section a review of previous work done where a MLC is sourced with a battery is presented.

References [2-32] and [2-33] highlighted the importance of energy storage dynamics by combining different forms of storing and supplying the energy, it is possible to enhance the performance. Combining the use of fast and slow dynamics but with different capacities results in a better power system. Batteries, with the aid of ultra-capacitors provide a great improvement of the systems performance and battery life can be achieved.

Batteries connected in parallel with ultra-capacitors are presented in reference [2-33]. In this setup the voltage is constant across both devices and a buck-boost converter provides the energy stored in the ultra-capacitors. The disadvantage of this setup is that the demand of energy from the capacitors is directly from the batteries.

To minimise the problem mentioned previously, an additional buck-boost converter can be placed between the batteries and the capacitors to control the power supplied by the battery when the capacitors require extra power.

A study presented in [2-34] of a conversion of an internal combustion engine vehicle to an electric vehicle (EV). A battery bank and an inverter was used to power the vehicle. An auxiliary power source consisting of ultra-capacitors and a DC-DC converter was

introduced to adjust the voltage levels from the battery required for acceleration. The control of the system used a PI controller.

A continuation of the study mentioned in the previous paragraph [2-34] presenting an optimized algorithm, improvements in the efficiency using neural networks. An auxiliary storage system such as battery banks, capacitors and fuel cells were implemented to aid the setting off the vehicle.

An alternative study uses DC-DC converters in cascade [2-35] along with main and auxiliary power sources. This configuration enables the use of reduced size devices and an increase in efficiency with the use of a hybrid topology presented and evaluated in simulation.

A battery can vary from a maximum to a minimum voltage level as it discharges, for this reason it cannot be connected directly to the MLC. In order to keep the voltage constant a bi-directional buck-boost converter is employed.

The control strategy for this converter is based on a reference voltage and an output voltage sensor. Using PWM to control the switching device, a PI controller is added in the feedback loop that will be varying the PWM signal according to the battery and output voltages.

In EV applications, a bidirectional converter is key to allow both motoring and regenerative power flow. A comparison of two bi-directional converters in [2-36] present the design and test of a bidirectional buck-boost converter and a bidirectional buck-boost cascade converter shown in Figure 2.22.

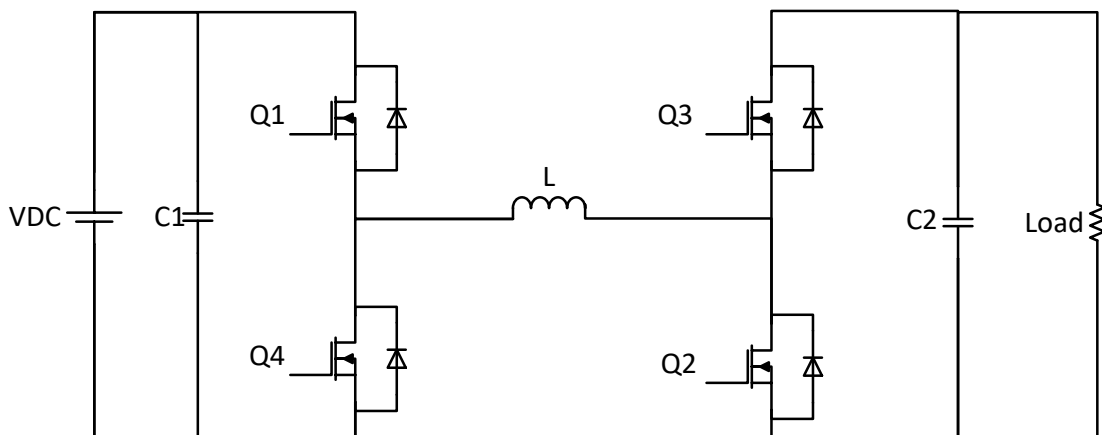


Figure 2.22 Bidirectional buck boost cascade converter



The converter in Figure 2.23 is a simplified version of the topology studied in [2-36], this topology will be used throughout this study and is presented in detail in Chapter 4.

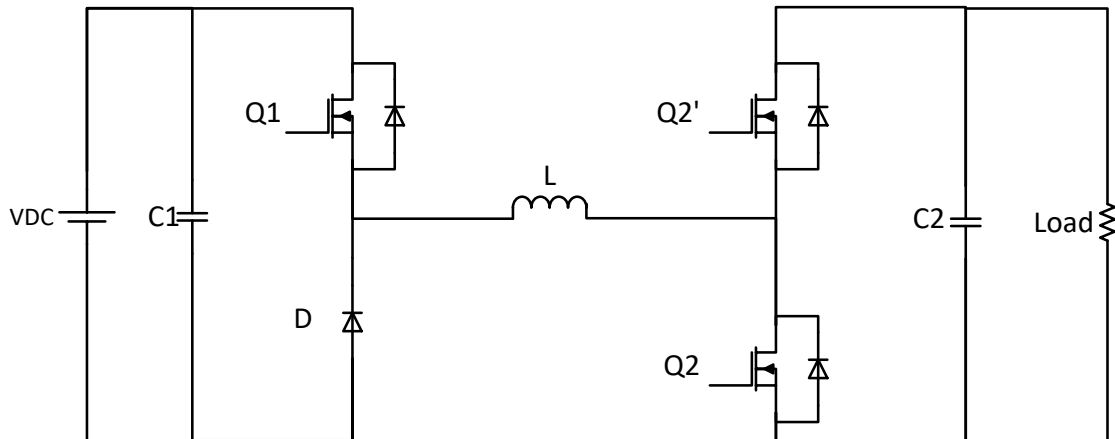


Figure 2.23 Simplified bidirectional buck boost cascade converter

The simplified topology of the converter can work in boost mode by activating switch Q1. For a buck mode the switch Q1 should be turned off. Q2 and Q2' operate in a complementary form. In this way, when Q1 is conducting, the power flow is in the direction to the load, and when Q1 is not conducting, the power flows in the direction to the VDC side. The design of this converter and the integration with the MLC is presented in Chapter 4 and the experimental evaluation in Chapter 5.

## 2.5– Conclusion

This chapter presents the background on the converters used in this project. Presenting the different configuration of the existing ML and after evaluating the number of components and the main advantages and disadvantages, the 5L-FB-NPC was selected as the MLC topology to study and evaluate. The background on DC-DC converters used in EV has been presented and the converter for the application construction site power supplies was selected.

A discussion of the MLC and DC-DC converters is presented as a motivation of research, highlighting the areas of interest and introducing the approach of addressing them in this study.

All the studies reviewed on multilevel converters topologies aim at the reduction of harmonics and improvement of efficiency. The Cascaded H-bridge topology has a main drawback considering that the power source in this application is a two terminal battery pack from an EV. The flying capacitor has the advantage of redundant states that makes

the system more flexible and easy to control. However, the capacitor required to generate the level zero can be a problem when it comes to the size, cost and reliability of the converter.

The following chapter introduces the MLC modulation techniques for the topologies presented in this chapter. Simulations of the techniques and evaluation of the selected method to control the converter are also covered.

## 2.6 – References

- [2-1] A. Nabae, I. Takahashi, and H. Akagi, “A New Neutral-Point-Clamped PWM Inverter,” *IEEE Trans. Ind. Appl.*, vol. IA-17, no. 5, pp. 518–523, 1981.
- [2-2] J. I. Leon, R. Portillo, L. G. Franquelo, S. Vazquez, J. M. Carrasco, and E. Dominguez, “New Space Vector Modulation Technique for Single-Phase Multilevel Converters,” *2007 IEEE Int. Symp. Ind. Electron.*, pp. 617–622, Jun. 2007.
- [2-3] J. I. Leon, R. Portillo, S. Vazquez, J. J. Padilla, L. G. Franquelo, and J. M. Carrasco, “Simple Unified Approach to Develop a Time-Domain Modulation Strategy for Single-Phase Multilevel Converters,” vol. 55, no. 9, pp. 3239–3248, 2008.
- [2-4] J. Rodríguez, J. Lai, and F. Z. Peng, “Multilevel Inverters : A Survey of Topologies , Controls , and Applications,” *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, 2002
- [2-5] L. G. Franquelo, J. Rodríguez, J. I. Leon, S. Kouro, R. Portillo, and M. A. M. Prats, “The Age of Multilevel Converters Arrives,” *IEEE Ind. Electron. Mag.*, no. June, pp. 28–39, 2008.
- [2-6] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. Wu, J. Rodriguez, M. A. Pérez, and J. I. Leon, “Recent Advances and Industrial Applications of Multilevel Converters,” *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553–2580, 2010.
- [2-7] L. M. Tolbert, F. Z. Peng, T. G. Habetler. Multilevel inverters for electric vehicle applications. *Power Electronics in Transportation, 1998*. IEEE, 1998. pp. 79-84.
- [2-8] J. Lai and F. Z. Peng, “Multilevel Converters-A New Breed of Power Converters,” *IEEE Trans. Ind. Appl.*, vol. 32, no. 3, pp. 509–517, 1996.
- [2-9] I. Patrao, E. Figueres, F. González-Espín, and G. Garcerá, “Transformerless topologies for grid-connected single-phase photovoltaic inverters,” *Renew. Sustain. Energy Rev.*, vol. 15, no. 7, pp. 3423–3431, Sep. 2011.
- [2-10] O. C. Onar, J. Kobayashi, D. C. Erb, and A. Khaligh, “A Bidirectional High-Power-Quality Grid Interface With a Novel Bidirectional Noninverted Buck –

- Boost Converter for PHEVs,” *IEEE Trans. Veh. Technol.*, vol. 61, no. 5, pp. 2018–2032, 2012
- [2-11] J. Rodriguez, S. Bernet, P. K. Steimer, and I. E. Lizama, “A Survey on Neutral-Point-Clamped Inverters,” vol. 57, no. 7, pp. 2219–2230, 2010.
- [2-12] Hui, Z., Khambadkone, A. M., & Kazuya, O. Investigation and loss comparison of 6.6 kV 5-level converters. In *Applied Power Electronics Conference and Exposition (APEC)*, 2015 IEEE pp. 297-303
- [2-13] Bifaretti, S., Zanchetta, P., Iov, F., & Clare, J. C. Predictive current control of a 7-level AC-DC back-to-back converter for Universal and Flexible Power Management system. In *Power Electronics and Motion Control Conference, 2008. EPE-PEMC 2008. 13th* pp. 561-568
- [2-14] Rabinovici, R., Tokar, D., & Baimel, D. Medium voltage multi-level inverters: Hardware-in-the-loop (HIL) simulations. In *Electrical & Electronics Engineers in Israel (IEEEI)*, 2012 IEEE 27th Convention of pp. 1-5
- [2-15] Du, S., Wu, B., Tian, K., Zargari, N. R., & Cheng, Z. An Active Cross-Connected Modular Multilevel Converter (AC-MMC) for a Medium-Voltage Motor Drive. *IEEE Transactions on Industrial Electronics*, 63(8), pp. 4707-4717.
- [2-16] Popova, L., Pyrhonen, J., Ma, K., & Blaabjerg, F. Device loading of modular multilevel converter MMC in wind power application. In *Power Electronics Conference (IPEC-Hiroshima 2014-ECCE-ASIA), 2014 International* pp. 548-554
- [2-17] B.P McGrath and D. G. Holmes, “Multicarrier PWM Strategies for Multilevel inverters” *IEEE Transactions on Industrial Electronics*, Vol. 49, No. 4, August 2002, pp 858–867.
- [2-18] A. Radan, A. Shahirinia and M.Falahi, “Evaluation of Carrier Based PWM Methods for Multilevel Inverter” *IEEE International Symposium on Industrial Electronics*, Vol. 4, No. 7, June 2007, pp 389 – 394
- [2-19] Chinnaiyan V.K., Jerome, J., Karpagam and J. Suresh, “Control Techniques for Multilevel Voltage Source Inverters”, *IEEE International Power Engineering Conference IPEC*, December 3-6 2007, pp 1023 – 1028
- [2-20] Perez, M. Kouro, S. Rodriguez, J. Bin Wu, Modified Staircase Modulation with Low Input Current Distortion for Multicell Converters”, *IEEE on Power Electronics Specialists Conference PESC*, 15-19 June 2008, pp 1989-1994
- [2-21] Dahidah, M.S.A. Agelidis, V.G., “Generalized Formulation of Multilevel Selective Harmonic Elimination PWM: Case I -Non-Equal DC Sources”, *IEEE on Power Electronics Specialists Conference PESC*, June 18-22 2006, pp 1- 6.
- [2-22] N. S. Choi, J. G. Cho, G. H. Cho, 'A General Circuit Topology of Multilevel Inverter'. *IEEE Power Electronics Specialists Conference (PESC'91)*, Vol. 1, pp. 96-103, 1991.

- [2-23] J. Courault, O. Lapierre, J. L. Pouliquen, 'Industrial Interest of Multilevel Converters'. *Proceedings of the 8<sup>th</sup> European Conference on Power Electronics and Applications*. (EPE'99). 1999
- [2-24] E. Persson, 'Transient effects in application of PWM inverters to induction motors'. *IEEE Trans. On Industry Applications*, Vol. 28, no. 5, pp. 1095-1101, Sept/Oct. 1992
- [2-25] F. Z. Peng, J. S. Lai, J. McKeever, J. VanCoevering, 'A Multilevel Voltage-Source Inverter with Separate DC Sources for Static VAR Generation'. *IEEE Trans. On Industry Applications*, Vol. 32, No. 5, Sept/Oct. 1996.
- [2-26] G. C. Cho, N. S. Choi, C. T. Rim, G. H. Cho, 'Modeling, Analysis and Control of Static Var Compensator Using Three-Level Inverter'. *IEEE Industry Appl. Soc. Annual Meeting Conference (IAS'92)*, Vol. 1, pp. 837-843, 1992.
- [2-27] M. Benghanem, A. Draou, A. Tahri, 'Reactive Power Control in Distribution System using an NPC Inverter Topology'. *IEEE Industrial Electronics Society Annual Meeting (IECON'01)*, Vol. 2, pp. 927-930, 2001
- [2-28] V. Karasik, K. Dixon, C. Weber, B. Batchelder, G. Campbell, P. Ribeiro, 'SMES for Power Utility Applications: A Review of Technical and Cost Considerations'. *IEEE Trans. On Applied Superconductivity*, Vol. 9, no. 2, pp. 541-546, June 1999
- [2-29] A. Arancibia, K. Strunz and F. Mancilla-David, "A Unified Single- and Three-Phase Control for Grid Connected Electric Vehicles," in *IEEE Transactions on Smart Grid*, vol. 4, no. 4, pp. 1780-1790, Dec. 2013.
- [2-30] S. Alepuz, A. Gilabert, E. Argüelles, J. Bordonau, J. Peracaula, 'A New Approach for the Connection of a Three-Level Inverter to the Power Grid for Applications in Solar Energy Conversion'. *IEEE Conf. On Industr. Electr. and Instrum. (IECON'02)*, Vol. 4, pp. 3285-3290, 2002.
- [2-31] S. S. Hosseini, A. Badri and M. Parvania, "The plug-in electric vehicles for power system applications: The vehicle to grid (V2G) concept," *2012 IEEE International Energy Conference and Exhibition (ENERGYCON)*, Florence, 2012, pp. 1101-1106.
- [2-32] S. M. Lukic, J. Cao, R. C. Bansal, F. Rodriguez, and A. Emadi. "Energy Storage Systems for Automotive Applications". *IEEE Transactions On Industrial Electronics*, Vol. 55, NO.6, June 2008, pp 2258-2265.
- [2-33] S. M. Lukic, S. G. Wirasingha, F. Rodriguez, C. Jian, and A. Emadi, "Power management of an ultracapacitor/battery hybrid energy storage system in an HEV," in Proc. VPPC, 2006, pp. 1-6
- [2-34] M. Ortúzar, J. Moreno, and J. Dixon. "Ultracapacitor-Based Auxiliary Energy System for an Electric Vehicle: Implementation and Evaluation". *IEEE Transactions On Industrial Electronics*, Vol. 54, NO. 4, August 2007. pp 2147-2155

- [2-35] H. Qiao, Y. Zhang, Y. Yao and L. Wei. "Analysis of Buck-Boost Converters for Fuel Cell Electric Vehicle". *Vehicular Electronics and Safety, 2006. ICVES 2006. IEEE International conference*. December 2006. pp 109-113
- [2-36] F. Caricchi, F. Crescimbin, F. Giulii Capponi, L. Solero. "Study of Bi-Directional Buck-Boost Converter Topologies for Application in Electrical Vehicle Motor Drives". *Applied Power Electronics Conference and Exposition, 1998. APEC '98. Conference Proceedings 1998., Thirteenth Annual. IEEE February 1998*

## Chapter 3 – Modulation Techniques

### 3.1 – Introduction

In the previous chapter (2), the literature review on modulation in MLC was presented. In this chapter, the modulation strategy is examined in more detail, as in order to turn on and off the switching devices in the converter to obtain the desired output voltage waveform, the gate signals for the MOSFETs are generated and controlled with a microprocessor [3-1] or FPGA. The method by which the switching signals are generated is discussed here.

One of the simplest and most common modulation techniques used for a two level inverter is PWM with a sinusoidal reference. For a two level inverter, only a single carrier signal is required as there are 2 switching devices per phase. Considering a PWM signal applied to one switching device as HIGH or ‘1’ for the switch to conduct and LOW or ‘0’ for a non-conducting state, the signal applied to the second switch is simply the complement of the original PWM generated as the switches always operate in a complementary form.

A typical multilevel converter consists of multiple switching devices (i.e. MOSFETs or IGBTs) connected to multiple voltage sources. The conduction states of the switching devices are controlled by a modulator whose role is to ensure: i) the required output is generated, ii) prevent damage occurring via cross-conduction (i.e. shoot-through) and for some specific topologies iii) to manage voltage levels on batteries or capacitors. Typically this type of control is achieved using PWM techniques and the many ways generate to generate PWM signals has been studied in the literature, with Sinusoidal PWM (SPWM) being the most commonly studied [3-2] . An overview of some of these techniques is provided here.

Modulation techniques to control the voltage in the DC-link have been studied in [3-3] [3-4], [3-5], [3-6], and [3-7]. A comprehensive classification of MLC modulation is shown in Figure 3.1 was presented in [3-5]. The classification is divided in space vector and voltage reference. The first major classification on the left covers all the vector based algorithms from the control to the modulation in 2-D and 3-D for inverters with 3 and 4 legs. The second group on the right includes the reference level algorithms from sinusoidal based to the hybrid modulations.

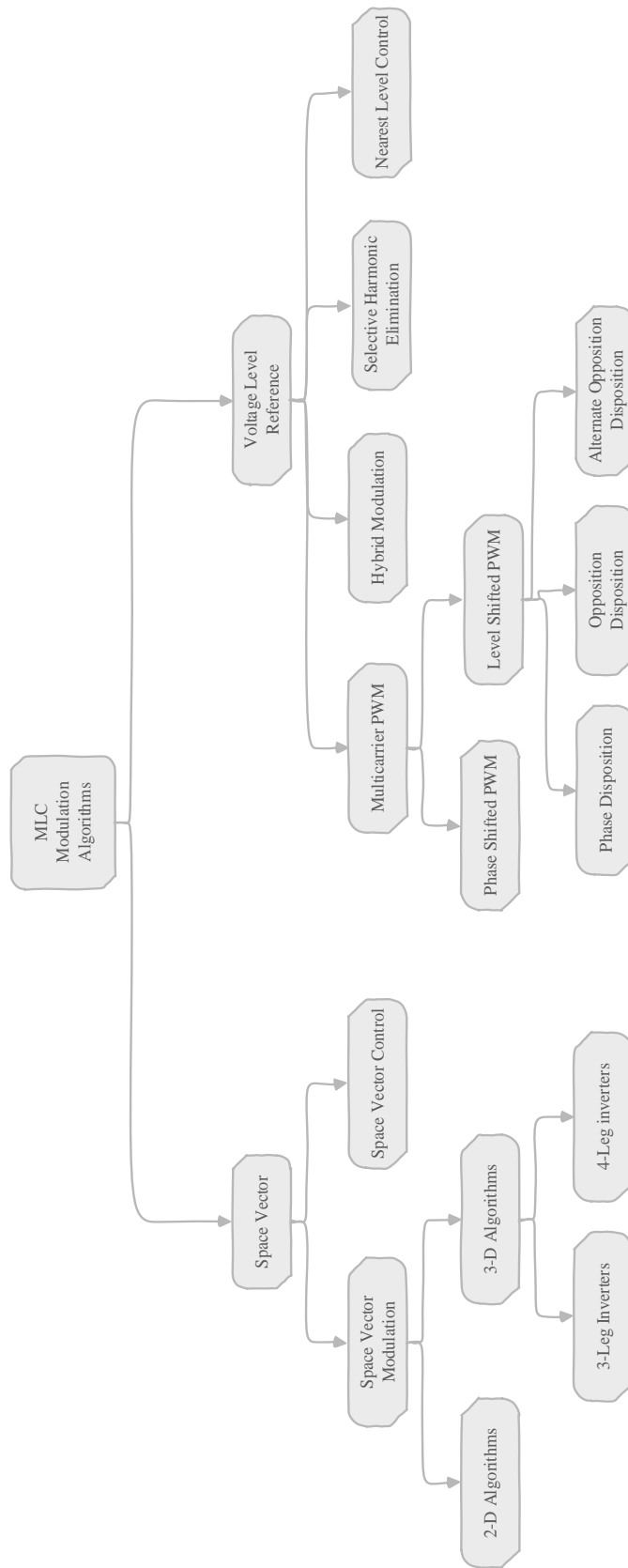


Figure 3.1 MLC modulation classification

The three most frequently studied techniques are space vector, selective harmonic elimination and multicarrier PWM. The most versatile technique is Space Vector Modulation, a technique based on the selection of the states to control the converter. The modulation techniques described in most of the published work are described for 3-phase systems, however, as we are considering single phase, the nearest two vectors (N2V), which is described in [3-8] represents a good approach for the control of a single phase system. A further comparison of the introduced techniques is presented in [3-9].

In general, the output of a MLC should generate a low-distortion sinusoidal voltage in order to reduce the filter size and stress caused in the switching devices, the aim of the modulation technique is to reduce the output distortion by selecting the best algorithm according to the application. The algorithm is then used to apply the pulses generated to control the switching devices. For this work, the algorithm to control the switching sequence and capacitor balancing is presented in the rest of the chapter. N2V represents a simple algorithm in terms of the calculations used and as a result the FPGA implementation is convenient.

### 3.2 – Sinusoidal PWM

The formation of the pulses is made by making a comparison between a carrier signal (triangle waveform) and the reference signal (sinusoidal) are made to generate the switching states by comparing if the reference is greater than the carrier, it will have an output of 1 or 0 for the opposite condition. The frequency of the carrier signals should be greater than the reference signal and the reference signal is the same as the output signal to be generated.

In Sinusoidal PWM, the sinusoidal reference signal is compared to a high-frequency carrier signal (usually a triangle waveform). For an n-level multilevel converter (n-1) carrier signals are compared to the reference to generate the MOSFET gate drive signals. Each carrier signal has a normalise peak-to-peak amplitude of  $1/(n-1)$  and is subject to a DC offset such that the entire modulation space is divided into discrete regions. This way only a single level is being subjected to PWM at a given time. For the 5 level converter considered here, 4 carrier signals are required and all 4 are compared to one reference signal to obtain the control pulses for the switches.



The four triangular signals to generate the pulses can be supplied in 3 basic different forms:

- Phase Disposition (PD disposition). All the signals with the same phase. Figure 3.4
- Phase Opposition (POD disposition). Both of the carriers in the positive plane (0 to 1) in phase with each other and the carriers in the negative plane (0 to -1) in opposite phase ( $180^\circ$ ) respect to the positive signals. Figure 3.6
- Alternately in Opposition (APOD disposition). Carriers in the positive plane are shifted in phase by  $180^\circ$  with respect to each other and the same for the signals in the negative plane Figure 3.8

The following section presents the results of simulations in Simulink for the 3 forms presented above. The MLC, an NPC in Figure 3.2 generates 5-levels, therefore 4 carrier signals are needed to generate the appropriate PWM signals. In the inverter leg, the switches are labelled from S1 to S4 and their complements from S1' to S4'.

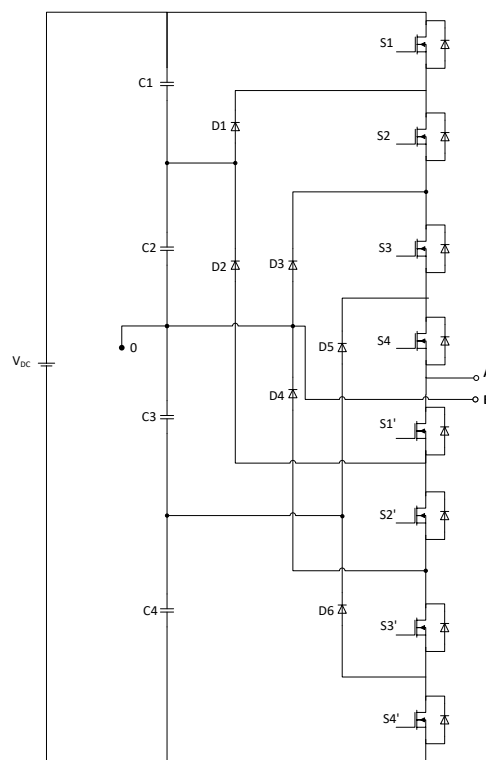


Figure 3.2 5-level Neutral Point Clamped Converter

To generate the PWM signal for this 5-level converter, the model shown in Figure 3.3 was used in Simulink and by changing the phase in the triangular signals the waveforms for each of the phase dispositions explained above, the modulation could be achieved,

where the output 1 corresponds to S1 and the complement output 5 to S1' and so on for S2, S3 and S4.

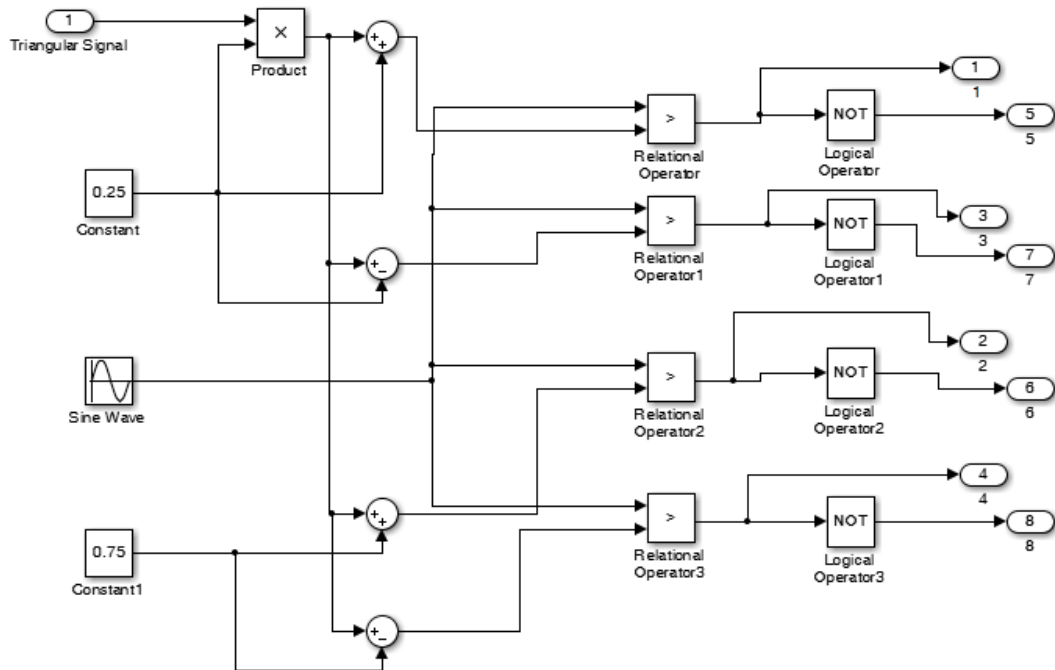


Figure 3.3. PWM generator for 5-level converter.

For each PWM technique implemented in Simulink, the output of the comparison between the carrier and the reference signal is shown. Four pulses are shown and that will control the upper switches in the converter (S1 to S4) shown in Figure 3.2, the lower switches are controlled by the complement of the signal used in the upper switch because the switches work in a complementary function as (S1 and S1') is S1 is on, S1' has to be off and vice versa. Pulses applied to the converter switches (S1 to S4) are shown in Figure 3.5, Figure 3.7, and Figure 3.9

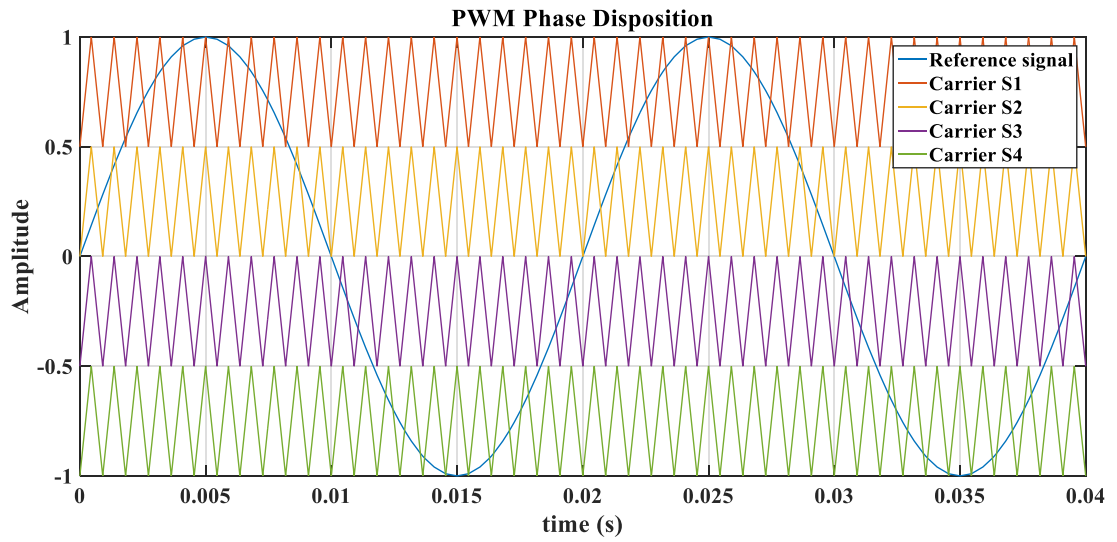


Figure 3.4 Sinusoidal reference and carrier signals for Phase Disposition PWM

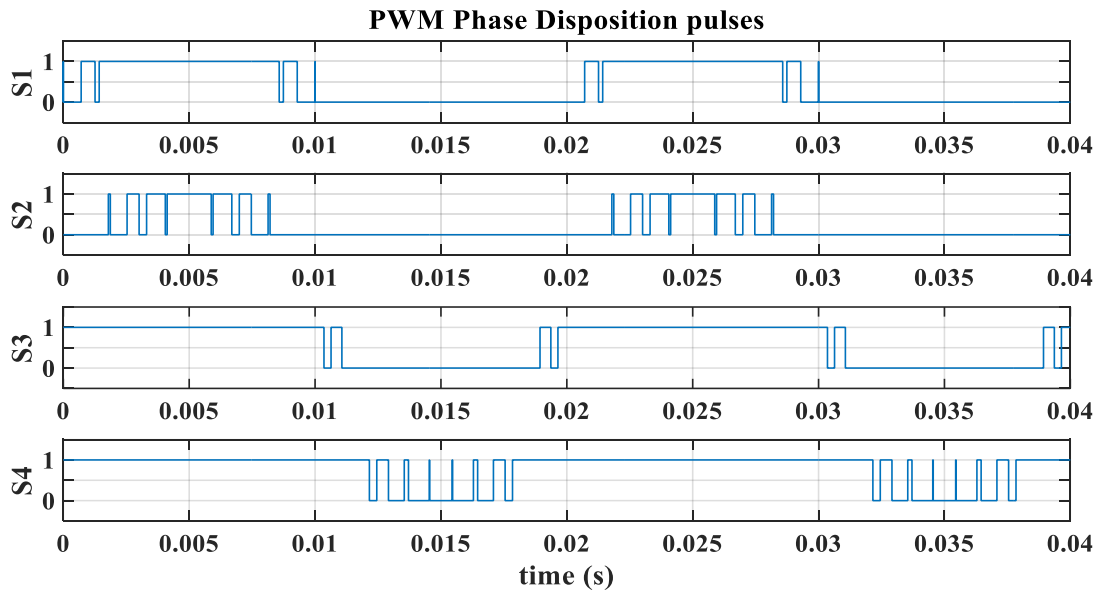


Figure 3.5 Switching pulses Phase Disposition

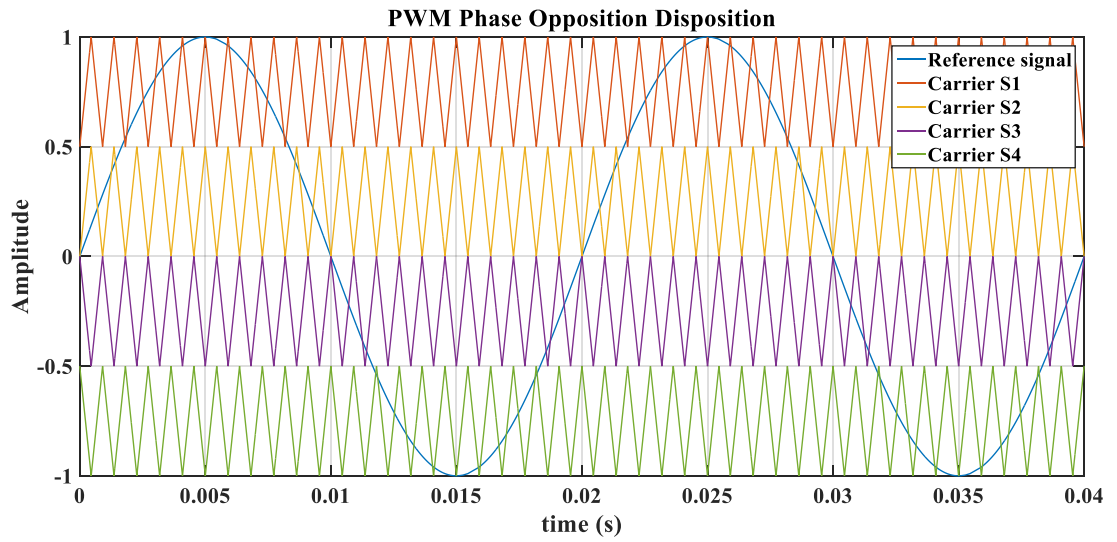


Figure 3.6 Sinusoidal reference and carrier signals for Phase Opposition PWM.

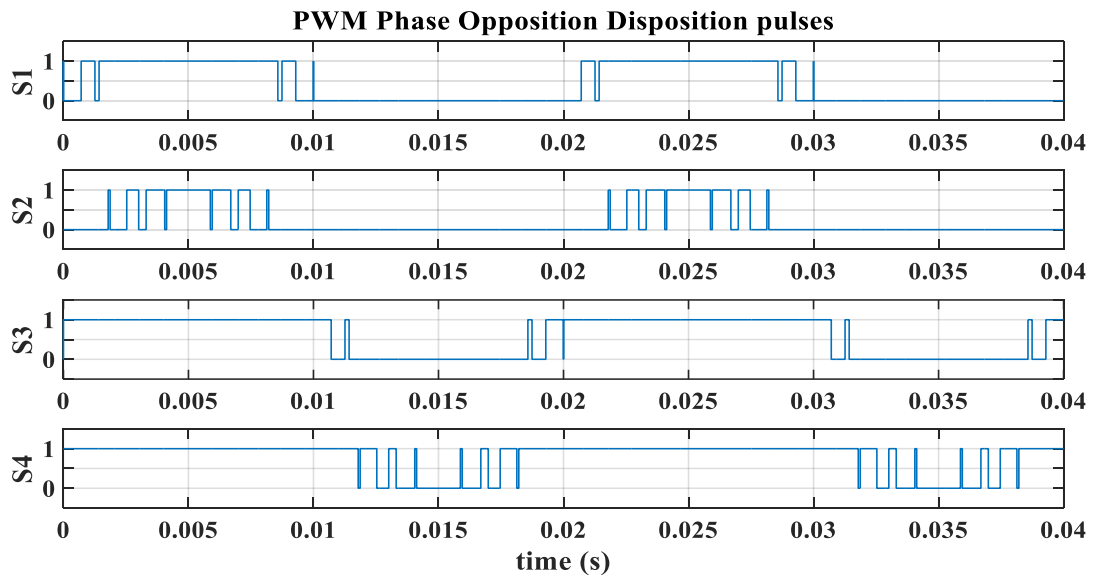


Figure 3.7 Switching pulses Phase Opposition Disposition

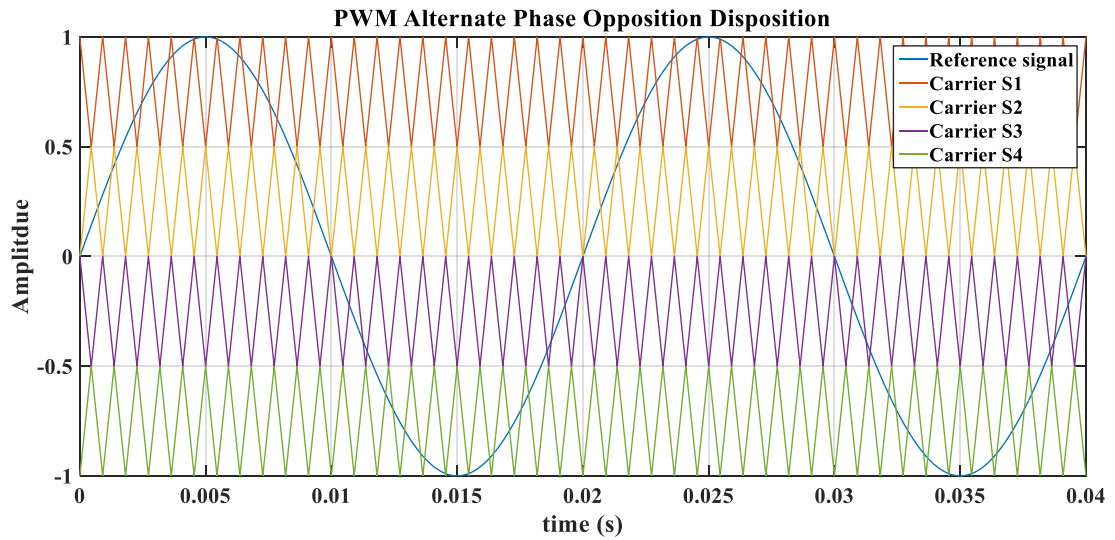


Figure 3.8 . PWM sinusoidal reference and carrier signals for Alternately in Opposition PWM.

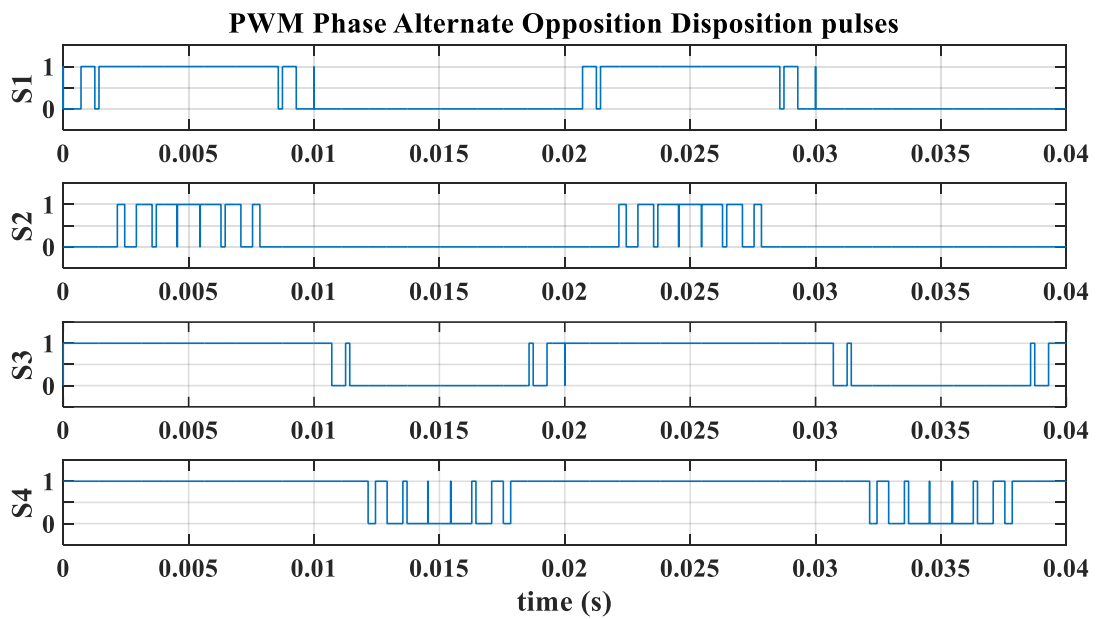


Figure 3.9 Switching pulses Alternately in Opposition Disposition

The techniques presented in this section are most commonly used in NPC MLC. In the next section, a simulation of the techniques presented is performed for a 5-levels NPC and FCC.

### 3.2.1 Sinusoidal PWM simulation

According to the different forms of triangular PWM techniques described in this chapter, the simulation for the 5L-HB-NPC and the 5L-HB-FCC with the 3 forms of carrier based PWM modulations (PD, POD, and APOD) are implemented.

The output voltage and the FFT for each case are presented. The THD in percentage is also calculated using (3.1)

$$THD = \frac{\sqrt{V_{rms}^2 - V_1^2}}{V_1} * 100 \quad (3.1)$$

Where  $V_{rms}$  is the RMS voltage at the output and  $V_1$  is the fundamental.

A comparison based on the THD is then presented at the end of this section and the modulation with the lowest THD is selected and used to simulate the 9L-HB-NPC and 9L-HB-FCC to evaluate the performance of the different topologies and confirm the topology to use based on the THD of the output voltage. The frequencies of the carrier signals in the PWM modulator are 20 kHz and the reference signal is 50 Hz, which is the output frequency for the power supply. The simulation was carried out in open loop with a large load resistor of 10 k $\Omega$  with a  $V_{DC}$  of 200V.

#### 3.2.1.1 Diode Clamped Half Bridge Simulation

The simulation of the 5L-HB-NPC using each of the PWM techniques explained previously and a comparison of the THD will be discussed at the end of this section. Figure 3.10 shows the circuit used in Simulink for the 5L converter. The output signal for each of the aforementioned PWM techniques is shown in Figure 3.11, Figure 3.12 and Figure 3.13 - the figures also show the FFT of the output voltage waveform and THD.

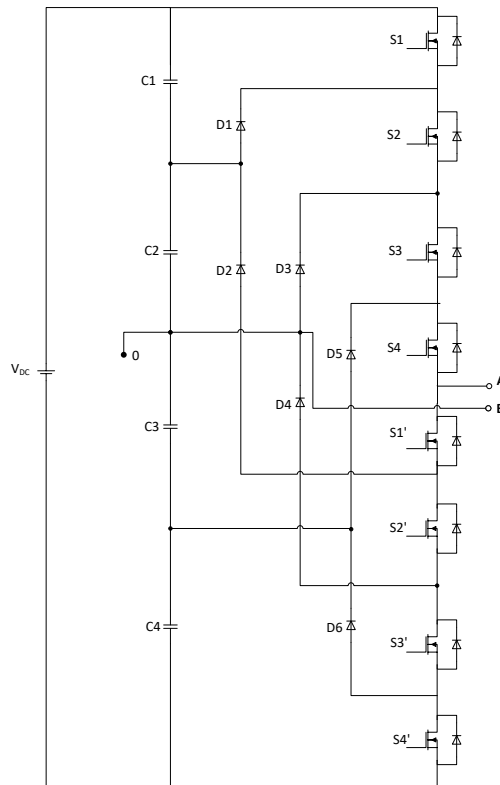


Figure 3.10. 5-level Diode Clamped Single Phase Half Bridge MLC

#### Phase Disposition (PD) PWM

The 5 level MLC depicted in Figure 3.10 is simulated with PD PWM. Figure 3.11 shows the output voltage and the frequency content of the signal at 50Hz and switching frequency of 20 kHz and its respective harmonics. THD was found to be 27.97%.

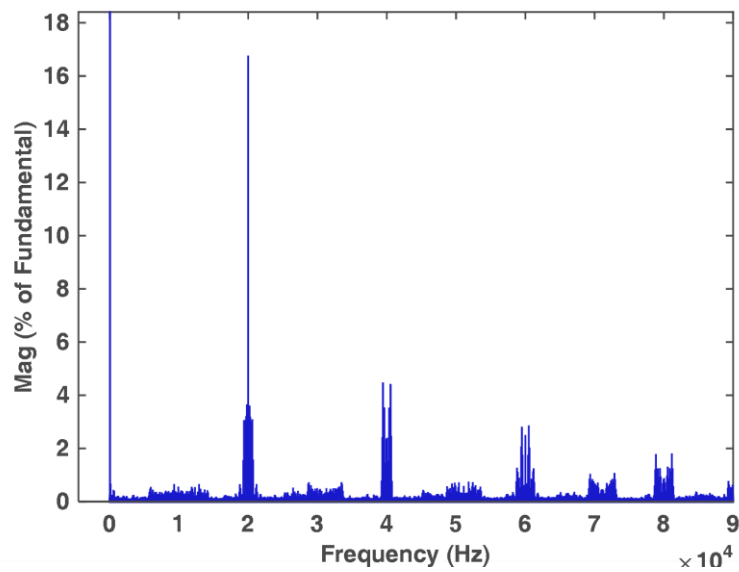
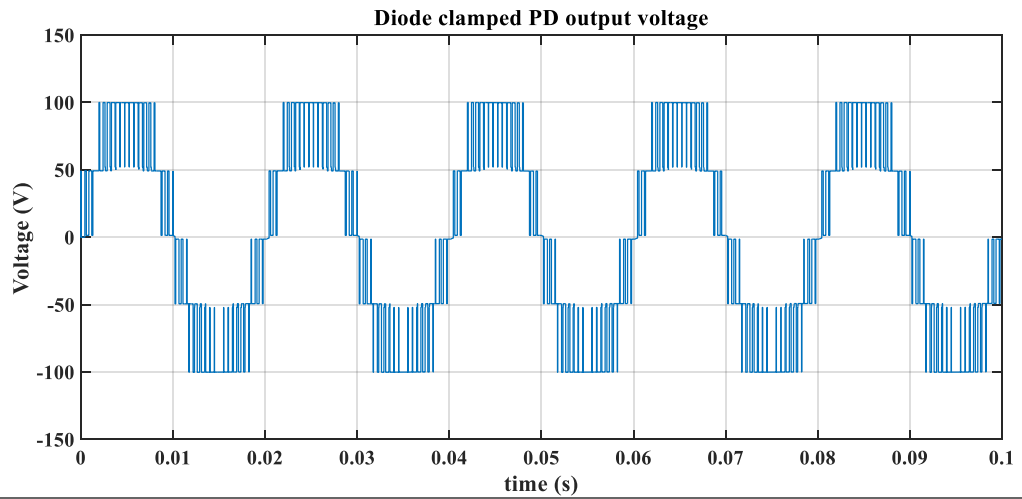


Figure 3.11. Diode Clamped 1 leg 5-level converter - Phase Disposition.

Phase Opposition Disposition (POD) PWM

The results of the simulation of the POD PWM is shown in Figure 3.12 the THD is 29.06%



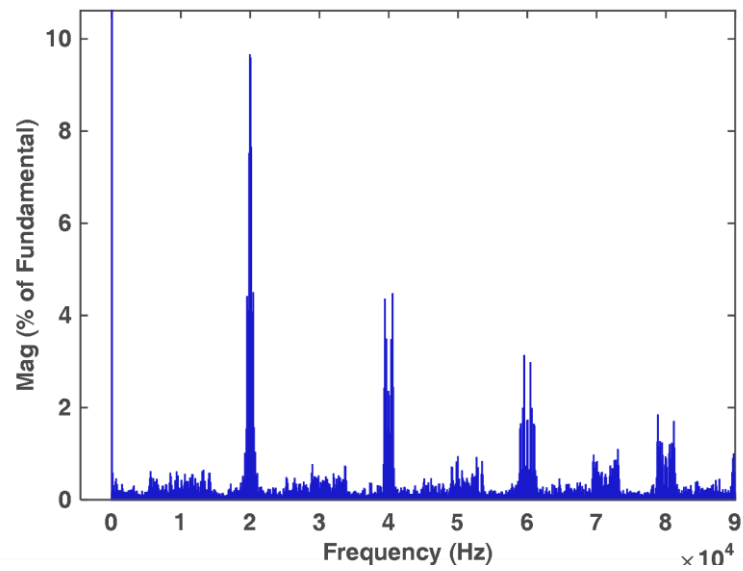
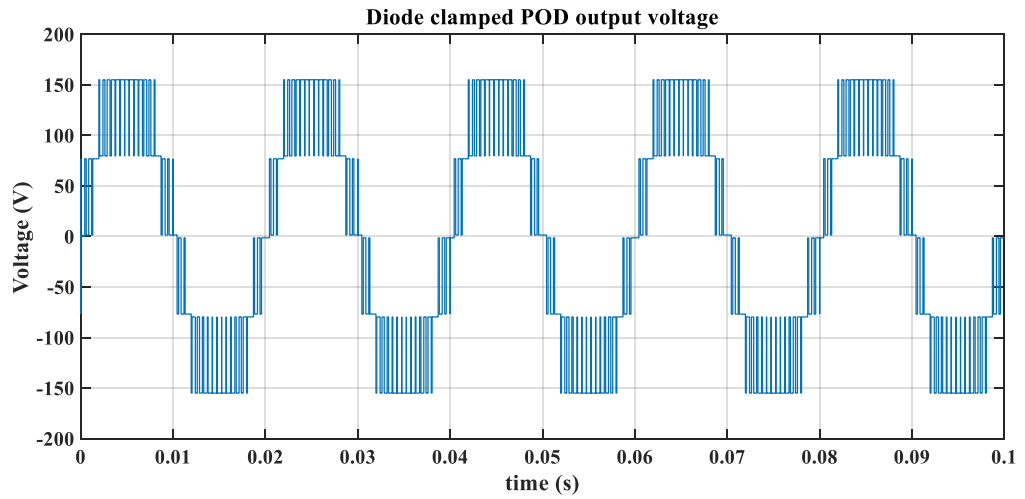


Figure 3.12. Diode Clamped 1 leg 5-level converter - Phase Opposition Disposition.

### APOD PWM

Simulation results for the APOD PWM is shown in Figure 3.13, indicating further improvements in THD with 24.92%.

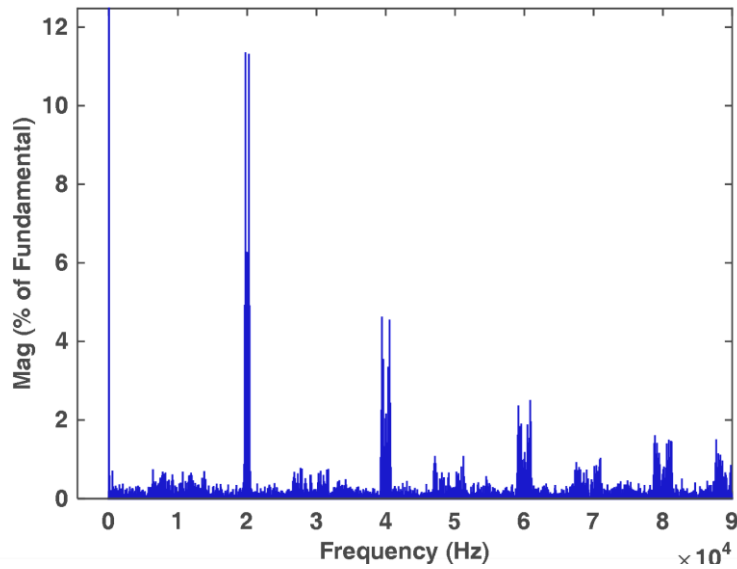
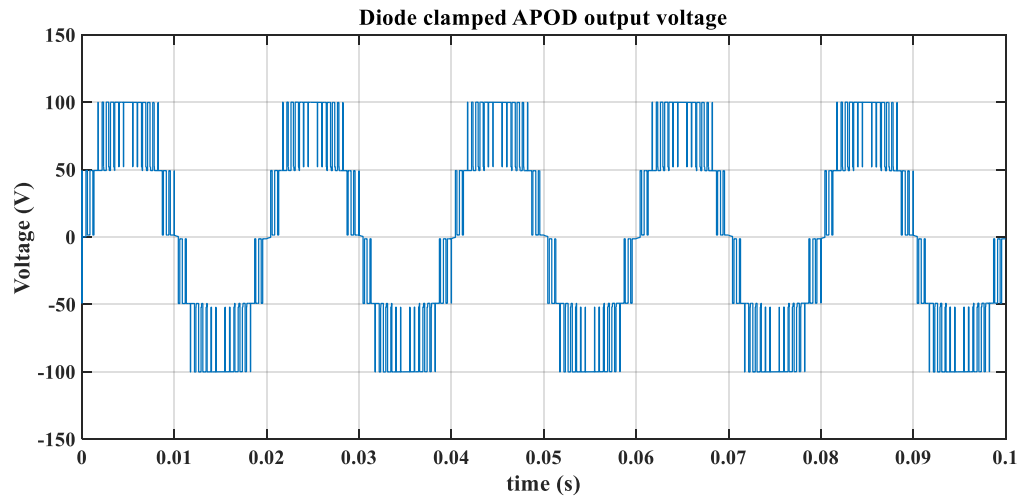


Figure 3.13. Diode Clamped 1 leg 5-level converter - Alternatively Opposition Disposition.

The results of the simulation for the 5-levels NPC converter in half bridge configuration using the three modulations introduced in the previous section show a slight improve in the THD when using APOD. The next section presents the results for FCC 5-levels in half bridge topology.

### 3.2.1.2 Flying Capacitor Half Bridge Simulation

The simulation results of the 5L-HB-FCC using the 3 forms of carrier based PWM are shown in this section. The model used is shown in Figure 3.14. The input DC voltage is

200V and a resistive load of 10 kΩ. The frequency of the triangular carrier signal is 20 kHz and the reference signal is sinusoidal of 50 Hz.

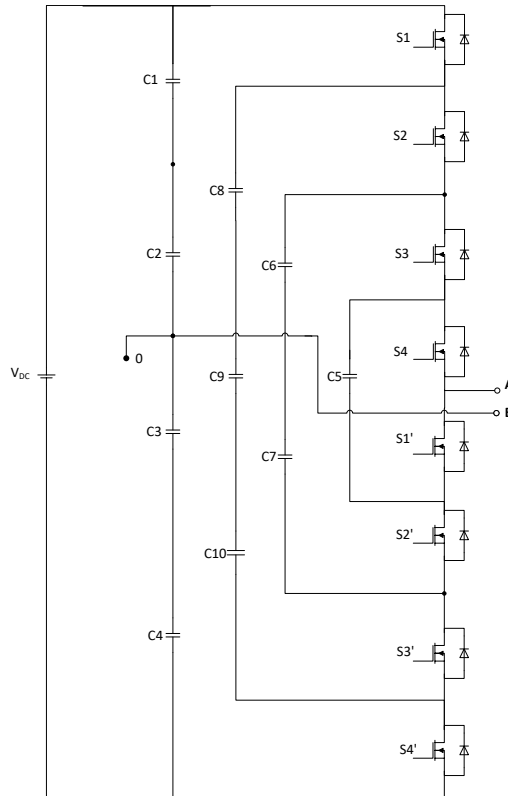


Figure 3.14. Flying Capacitor 5-level Single Phase Half Bridge.

The output voltage waveform is shown in Figure 3.15 for a PWM in PD, it can be seen the 5 levels balanced and the FFT analysis shows the frequency content accentuated in 20 kHz which is the switching frequency.

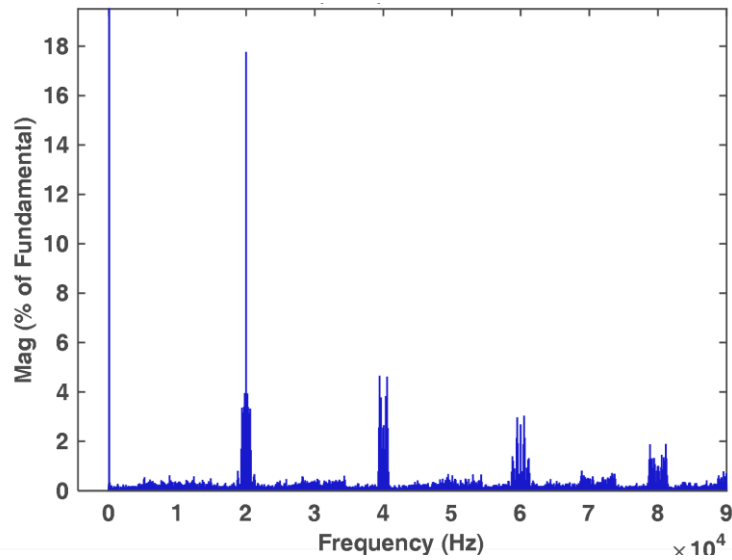
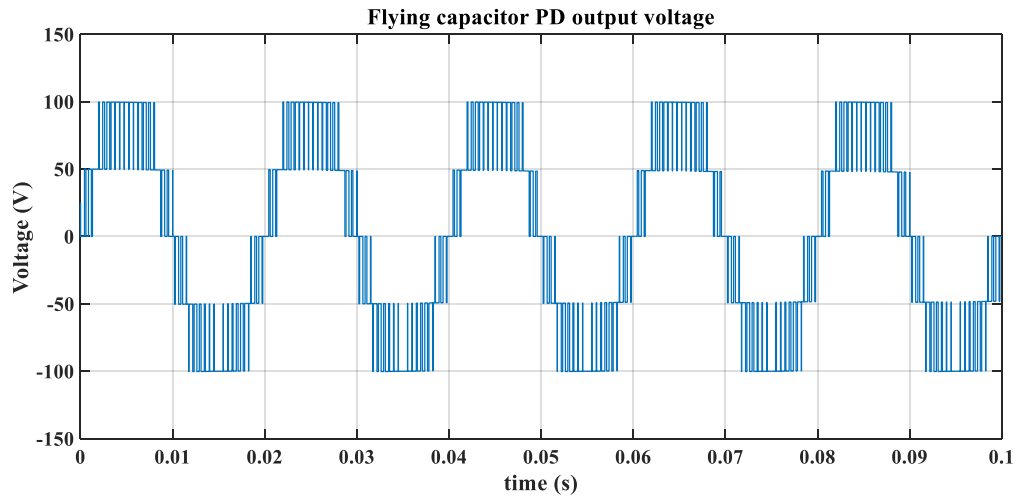


Figure 3.15. Flying Capacitor 1 leg 5-level converter - Phase Disposition.

Compared with the phase disposition, the phase opposition disposition modulation applied to the 5L-HB-FCC, the output voltage wave form and FFT analysis shown in Figure 3.16 the THD shows an improvement from 32.75% to 29.19% using POD and PD modulations respectively.

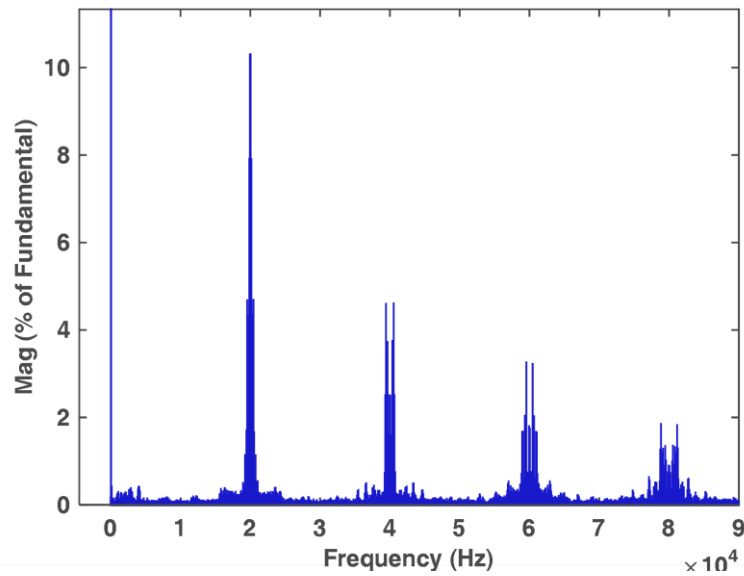
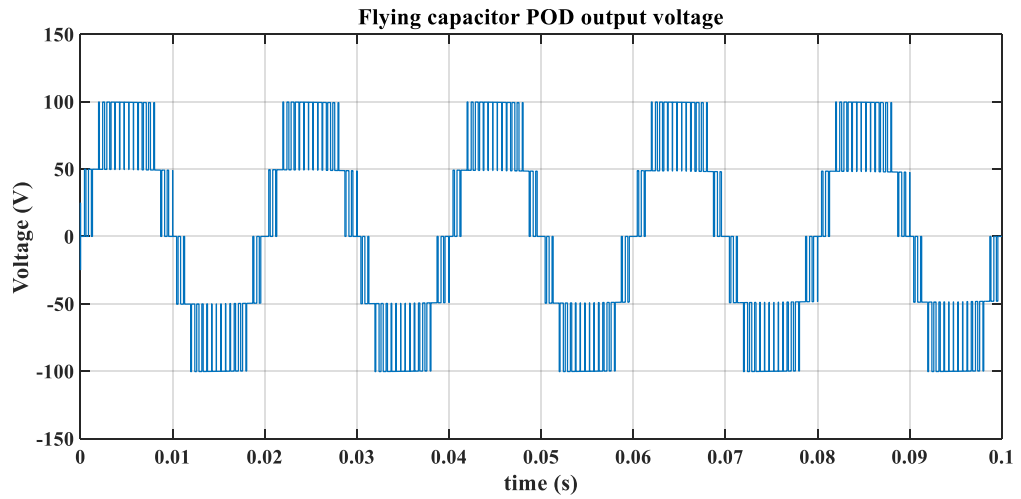


Figure 3.16. Flying Capacitor 1 leg 5-level converter - Phase Opposition Disposition.

As with the diode clamped model, the APOD modulation, Figure 3.17 shows the main component in 20 kHz reduced in amplitude but 2 components added at the side of the switching frequency component. The THD is 28.17% which is the lowest of the 3 tested in this section.

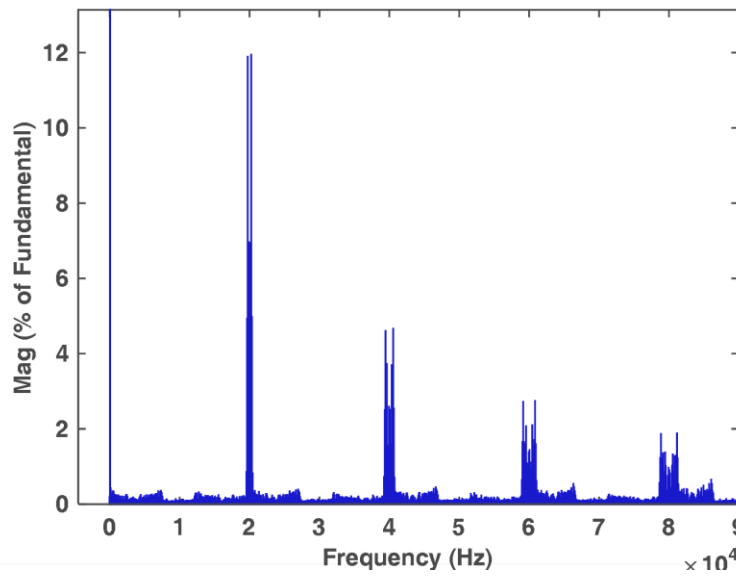
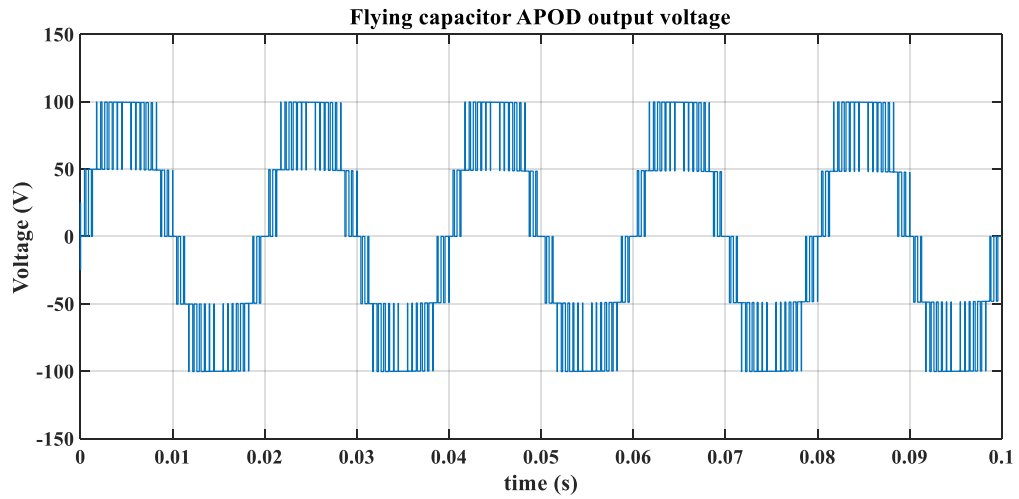


Figure 3.17. Flying Capacitor 1 leg 5-level converter - Phase Alternatively Opposition.

The results obtained in this section evaluating the three PWM techniques in the FCC topology in terms of THD are higher by approximately 1.5% to 3% compared with the results for the NPC converter in the previous section.

The THD for the different PWM techniques with half bridge converters in Table 3.1 shows that the PWM technique generating the less THD is the APOD in the NPC topology.

<i>Topology</i>	<b>PD</b>	<b>POD</b>	<b>APOD</b>
<b>Diode Clamped</b>	27.97%	29.06%	24.92%
<b>Flying Capacitor</b>	29.19%	32.75%	28.17%

Table 3.1. THD comparison for Different PWM techniques and topologies.

Therefore, considering that the THD didn't vary significantly, the evaluation of the full bridge topologies NPC and FCC as this will increase the number of levels and potentially reduce the THD. The following section presents the simulation results using APOD then an evaluation of the feasibility of the implementation of either topology is discussed.

### 3.2.1.3 9-level Full Bridge Diode Clamped Simulation

The 9L-FB-NPC was simulated using the APOD PWM to switch each leg as explained above and for the second leg using a reference signal shifted 180 degrees with respect to the other leg. The topology used for this simulation is shown in Figure 3.18. The simulation conditions are the same as the described at the beginning of this section.

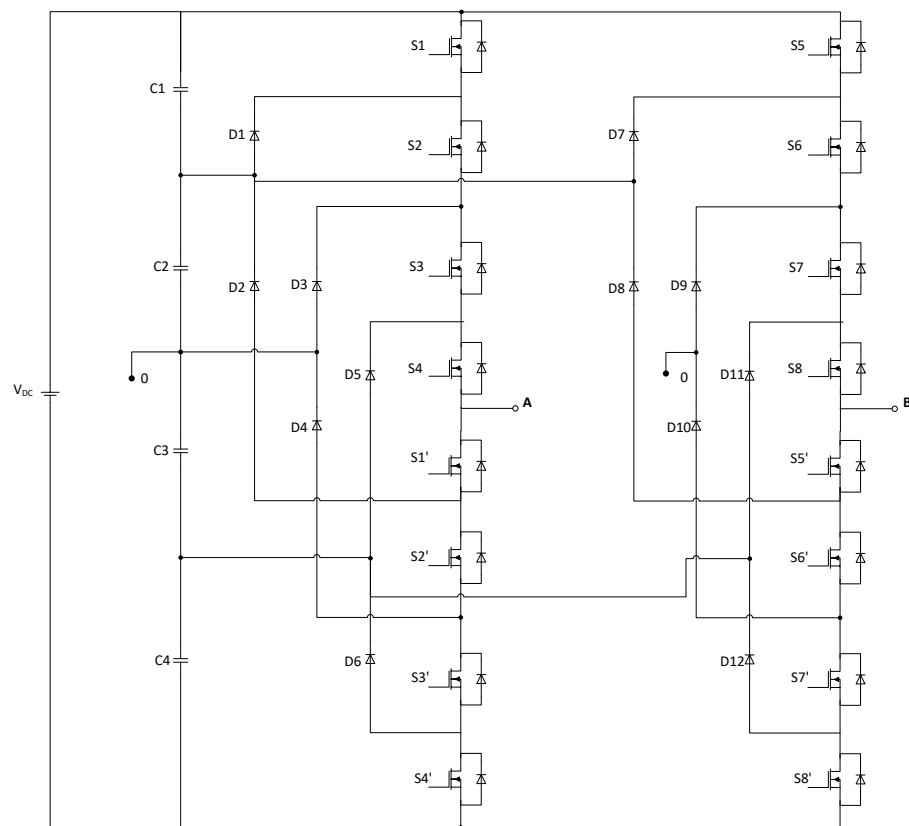


Figure 3.18. Diode Clamped 9-level Single Phase, Full Bridge.

The result of the simulation shows in Figure 3.19 an attenuated frequency content in 20 kHz, the component corresponding to the switching frequency is now in 40 kHz and 100 Hz due to the operation in full bridge. The 9-levels generated are balanced for a resistive load with the peak voltage level at the same level of the input voltage in DC.

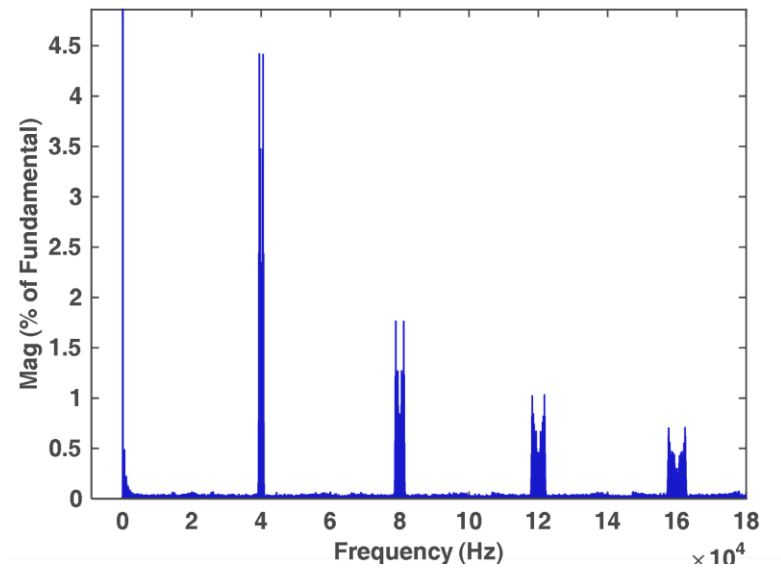
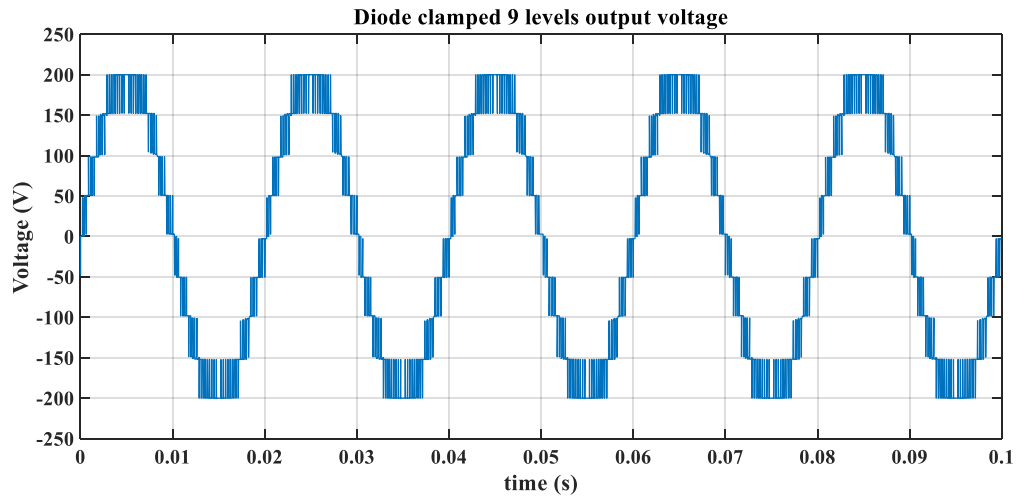


Figure 3.19. Diode Clamped Full Bridge 9-level converter.

The THD obtained in this configuration is 17.59%

### 3.2.1.4 9-level Full Bridge Flying Capacitor Simulation

The 9L-FB-FCC model used to simulate the performance of the topology with the APOD modulation is shown in Figure 3.20. The conditions are the same to the one in the previous section.



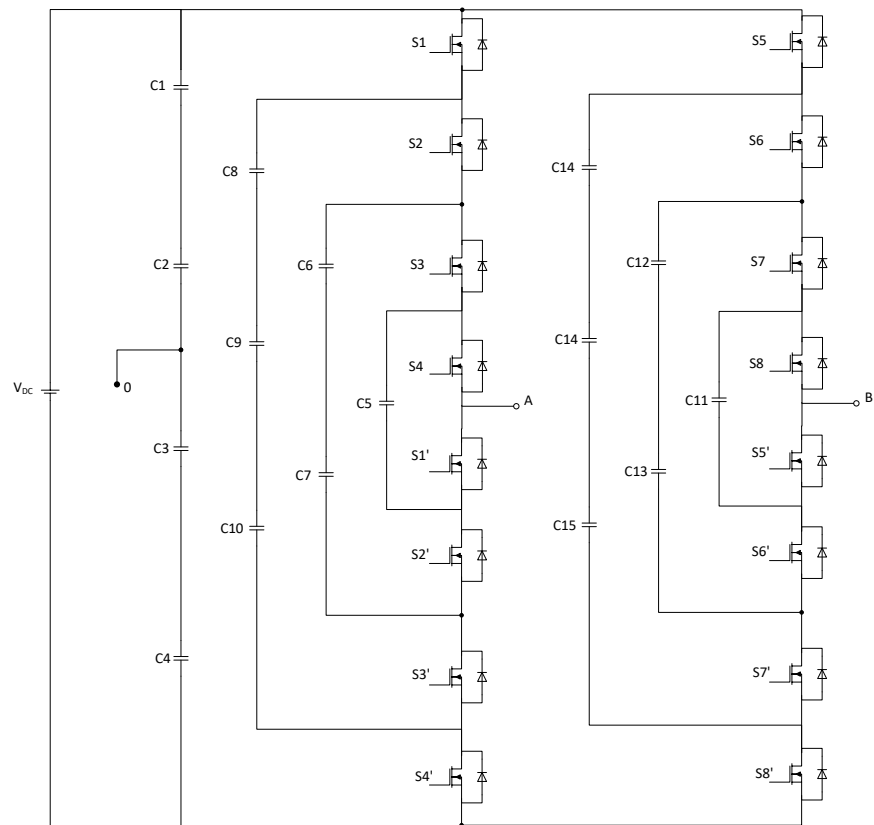


Figure 3.20. Flying Capacitor Full Bridge 5-level converter.

The output voltage waveform and FFT analysis presented in Figure 3.21 shows an unbalance of the levels due to the unbalance in the capacitors even with a resistive load, the maximum voltage level is also of the value of the DC input. The unbalance is present due to the open loop operation condition where no balancing algorithm is used. The FFT shows a similar frequency content to the results presented for the 9L-FB-NPC.

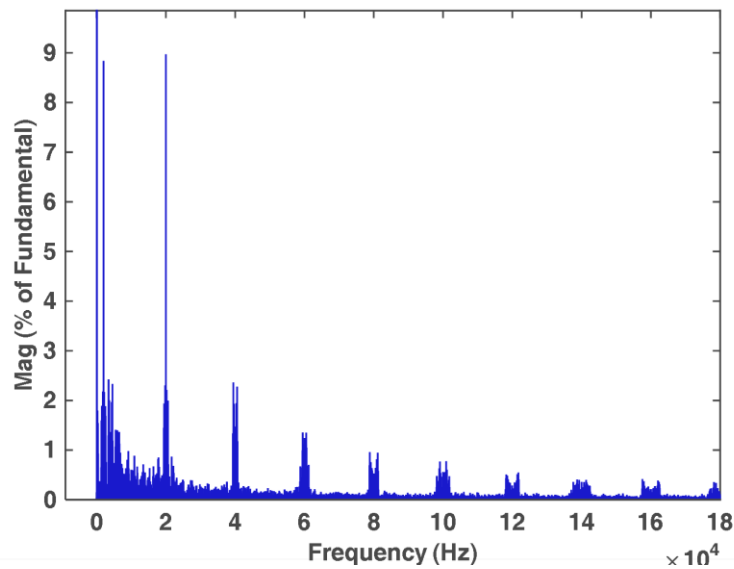
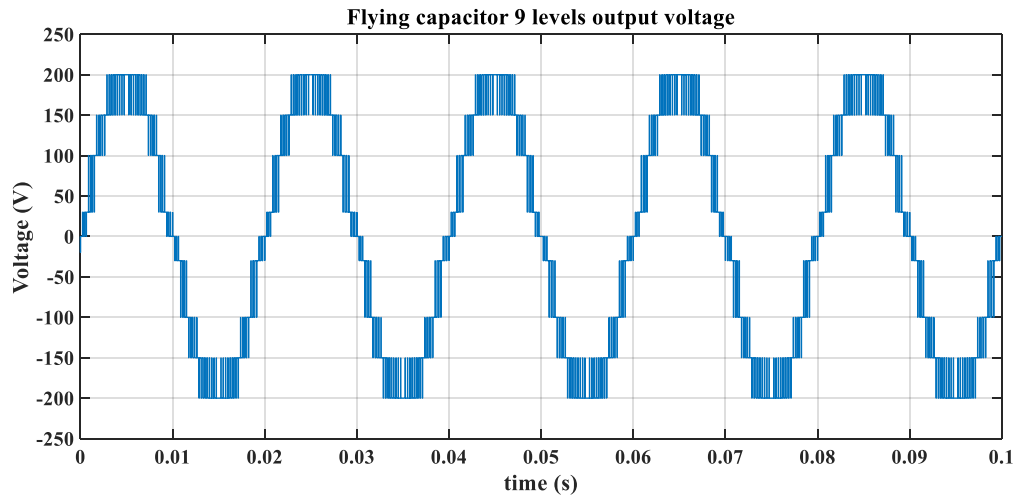


Figure 3.21. Flying Capacitor Full Bridge 9-level converter

The THD for the FB topology is 17.59% and 34.38% for the NPC and FCC topologies respectively. This is because the number of levels in full bridge are increased, generating a 9 level output waveform but it requires more components and more complex control.

Based on the simulation results, the topology selected is the 5 levels full bridge which produces the output voltage with a reduced THD, this will allow to minimise the filtering size and reduce the DC to DC conversion as the output voltage is of the same level as the DC input not halved as the level obtained if using the half bridge topology. NPC topology in full bridge is selected to further study. The number of levels selected is 5 and this can be achieved using two legs of a 3-level NPC. In the next sub section a simulation of the selected topology is presented highlighting the voltage level and the THD obtained.

### 3.2.1.5 Simulation SPWM 5 levels full bridge.

The topology presented in Figure 3.22 is the topology selected for further study in this thesis. The reasons to select this topology are the reduced THD achieved with full bridge topologies and the reduced number of switching devices and capacitors compared to the 9-levels and FCC topologies respectively.

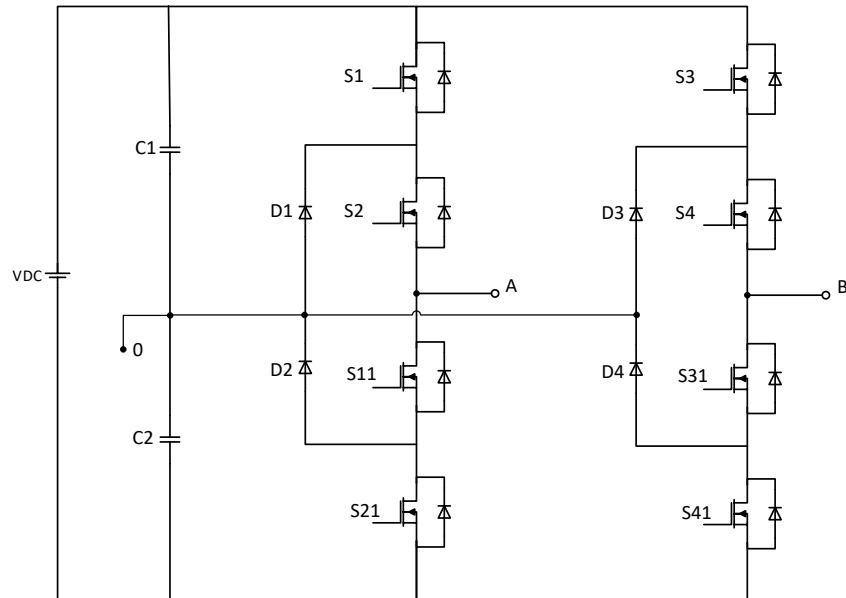


Figure 3.22 Diode Clamped Full Bridge 5-level converter

The waveform shown in Figure 3.23 corresponds to the simulation of the selected topology with APOD modulation with the same conditions as the series of simulations presented in the previous sections. It can be seen that the peak output voltage is of the same level value as the DC input instead of the  $V_{dc}/2$  normally obtained with a half bridge topology and the 5-levels are achieved.

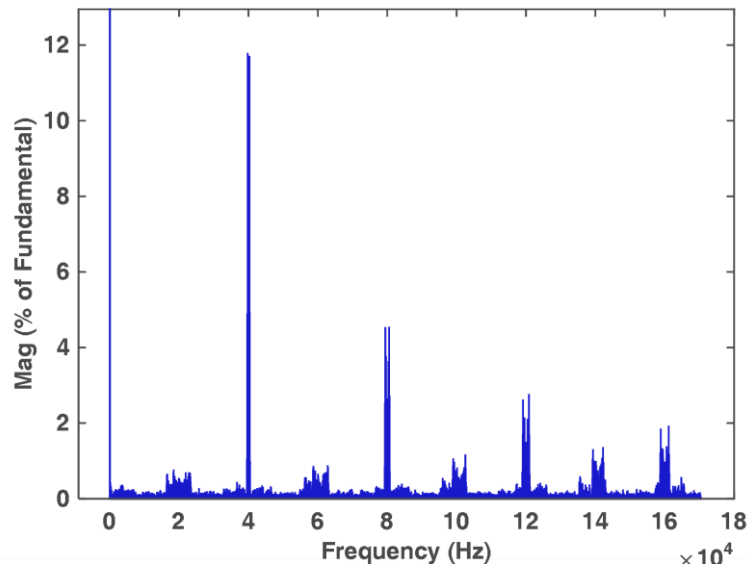
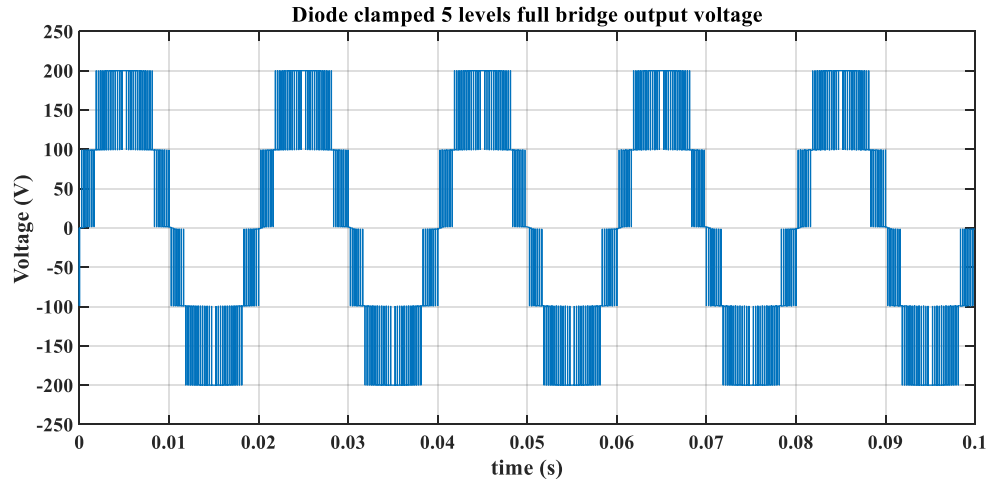


Figure 3.23 NPC Full Bridge 5-level converter waveform and FFT

The THD obtained is 26.87% which is slightly higher than that obtained with the 5-level half bridge topology presented in section 3.2.1.1, however the output peak voltage level will allow a reduced size of the DC-DC converter compared to the requirements if a half bridge topology is used for the application presented in the following chapters.

### 3.3 – 1-D Space vector modulation

Another approach to the control of the output of the converter is through the use of the Space Vector Modulation (SVM) technique. However, conventionally, the implementation of this modulator is more appropriate for converters of 3 levels or more and for 3-phase converters. In [3-10] a general form to implement SVM for a 3-phase

converter is presented. For single phase systems it can be implemented as a 1-Dimension (1D) form as explained in [3-11] where the topology, 5L-FB-NPC selected is explained using this modulation.

Using the redundant states in the diode clamped topology to generate the levels this technique can be implemented.

Steps to design a modulator.

1. Output vectors definition.
2. Separation plane identification.
3. Boundary plane identification.
4. Define switching sequence.

The last step represents a challenge in the implementation of this modulation strategy, and due to this and the advantages of this modulator is of great research interest in the MLC for the control and balancing.

### 3.3.1 Nearest 2 vectors modulation for 5-L-FB-NPC

A 5-level converter using the Nearest 2 Vectors (N2V) technique for the FB NPC topology is introduced in this subsection, it generates the output as a differential between the phase-A and phase-B, each of the leg or phase outputs as seen in Figure 3.22 are labelled A and B, this correspond to phase-A and phase-B. The vector selection is made based on a reference signal (sinusoidal), in this case a sine wave with an amplitude and frequency desired at the output, the amplitude will determine the modulation index. Once the reference is found the 2 vectors to generate one level and the duty cycles for each state is calculated.

$$V_{out} = V_a - V_b$$

For convenience a switching-state table is used as a reference for the modulator, Table 3.2. Considering just one phase (or leg) of the full-bridge, the phase voltage can exist in just one of three states ( $-V/2$ ,  $0$ ,  $+V/2$ ) and this is represented by the number 0, 1, 2 respectively. Since there are two phases in the full-bridge converter, there are a total 9 switching-states ( $3^2$ ). The first column (vector) indicates conduction states of both bridge legs  $AB$  such that the value 02 translates to phase A being in state 0 ( $V_A = -V/2$ ) and phase B being in state 2 ( $V_B = +V/2$ )  $V_{out} = V_A - V_B = -V$ . Columns S1, S2, ..., S41 explicitly shows conduction states of the individual switches where a value 0=off and 1=on.

Vector	S1	S2	S11	S21	S3	S4	S31	S41	Phase-A	Phase-B	Vout
02	0	0	1	1	1	1	0	0	$-V/2$	$V/2$	$-V$
01	0	0	1	1	0	1	1	0	$-V/2$	0	$-V/2$
12	0	1	1	0	1	1	0	0	0	$V/2$	$-V/2$
00	0	0	1	1	0	0	1	1	$-V/2$	$-V/2$	0
11	0	1	1	0	0	1	1	0	0	0	0
22	1	1	0	0	1	1	0	0	$V/2$	$V/2$	0
10	0	1	0	1	0	0	1	1	0	$-V/2$	$V/2$
21	1	1	0	0	0	1	1	0	$V/2$	0	$V/2$
20	1	1	0	0	0	0	1	1	$V/2$	$-V/2$	$V$

Table 3.2. Switching states for the 5-level full bridge NPC (5L-FB-NPC) converter in Figure 3.22.

The control region for the five-level converter is shown in Figure 3.24, this shows the voltage levels achieved with the vectors presented above. The control regions are numbered from 1 to 3 where the regions 2 and 3 correspond to redundant vectors.

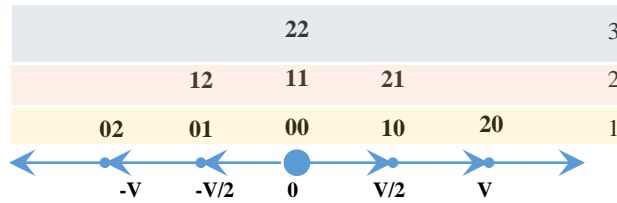


Figure 3.24. Control region for 5-level inverter.

As it can be seen, there are redundant vectors for the levels  $-V/2$ , 0 and  $V/2$ , regions 2 and 3, these vectors can be used to balance the DC-link capacitors or to optimise the switching sequence for switching loss reduction. The following sub-section presents the modulation algorithm without DC voltage balancing.

#### *Modulation algorithm without capacitor voltage balancing*

Under the assumption that the capacitors have infinite capacity then they will not lose any charge and therefore not require any replenishment and so capacitor voltage balancing is unnecessary. Under these conditions the gate signals for the converter switches are chosen from the vectors defined in Table 3.2 based on the nearest 2 vectors algorithm (N2V). With N2V the desired output is realised by the PWM of the two closest vectors to the desired output value. Here, a sinusoidal output at a specific frequency is desired and so a reference signal with the normalized magnitude of the reference signal ("a"), the nearest 2 vectors ( $A_1B_1$  and  $A_2B_2$ ) are selected to generate the levels at the output and the

duty cycle is defined by the same normalized magnitude of the reference signal to operate a PWM in the regions defined and detailed in Table 3.3.

<b>a</b>	<b>Duty Cycle</b>	<b>A<sub>1</sub>B<sub>1</sub></b>	<b>A<sub>2</sub>B<sub>2</sub></b>
<b>0 → 0.5</b>	$2*a-1$	00	10
<b>0.5 → 1</b>	$2*(a-0.5)-1$	10	20
<b>0 → -0.5</b>	$2*a+1$	00	01
<b>-0.5 → -1</b>	$2*(a+0.5)+1$	01	02

Table 3.3. States Sequence based on reference signal “a”

The duty cycle generated using the table presented above ranges from 0 to 1 or 0% to 100% respectively. The states corresponding to the low level are A<sub>1</sub>B<sub>1</sub> and the high level A<sub>2</sub>B<sub>2</sub> this will generate the pulses to the switches to generate the output level desired as shown in Figure 3.25 depending on the normalised reference signal “a”, to the left of the figure is are the vectors divided in the control regions 1 to 3 as presented above.

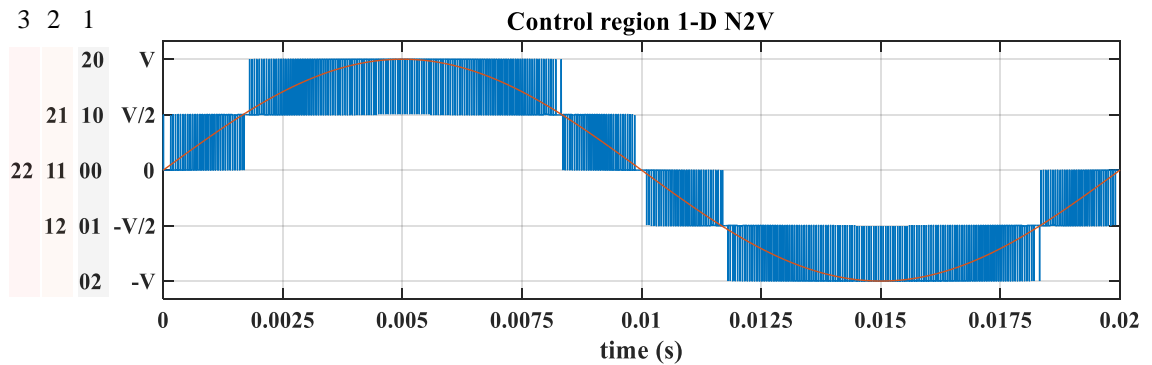


Figure 3.25 1-D Nearest 2 vectors control regions

For example for “a” in the range of 0 to 0.5, the vectors selected for the low state is 00 that generates voltage level 0 and the high state is 10 which generates the level V/2. This table is for generating the 5-level output without voltage balancing, in section 3.3.2 the algorithm with the redundant vectors is presented for DC-link capacitors voltage balancing.

### 3.3.2 Capacitor Voltage Balancing N2V.

Capacitor balancing is a great subject of study, depending on the number of levels in the converter, the complexity of the control varies. A great number of levels results in the use of more capacitors to split the voltage and create the levels. Self-balancing converters as a form to balance the voltage, a topology is introduced in [3-12], which proposes capacitor paths to balance the DC-link. SVM has been studied in the last years as a method to solve

this problem. Most of the studies carried out are for 3-phase systems diode clamped converters [3-13] [3-14]. A method to adapt the nearest three vectors to a single or multiphase system was introduced in [3-15] for a full bridge topology. Then the study of the effect of the states in the DC-link capacitors was presented in [3-16]. Considering the space vector technique for single phase, the method presented in [3-11] was implemented for the 5-levels converter, the results of the simulation is presented in this section.

### 3.3.2.1 Capacitor Voltage Balancing Method N2V 5-level single phase

The vectors using the capacitors C1 and C2 to generate the output and that charges or discharges them are the ones for  $V_{out} = -V/2$  and  $V/2$  shown in Figure 3.24, control regions 2, and 3. These are the redundant states that can be used to balance the voltage in the DC-link capacitors.

As described in [3-11], the states, charging the capacitors represented with an arrow up or discharging with an arrow down, and the effect on the voltage in the capacitors related to the output current in the load are shown in Table 3.4.

Vout	Vector	V <sub>C1</sub>		V <sub>C2</sub>	
		I <sub>out</sub> <0	I <sub>out</sub> >0	I <sub>out</sub> <0	I <sub>out</sub> >0
-V/2	01	↓	↑	↑	↓
	12	↑	↓	↓	↑
V/2	10	↑	↓	↓	↑
	21	↓	↑	↑	↓

Table 3.4. Voltage effect in the DC link capacitors for the 5-level converter.

As described in the previous section, the control regions 2 and 3 are used to balance the DC-link capacitors. Depending on the output current for the levels  $V/2$  and  $-V/2$  the redundant states are selected. Using the condition  $(V_{c1}-V_{c2})$  to determine which of the capacitors has the voltage increased and therefore it needs to be balanced, the states are selected. The level 0 has 2 redundant states but it does not contribute to discharge or charge the capacitors, therefore the vector 00 is assumed for the level 0.

In the following section the results of the simulation performed are presented for both algorithms, with and without capacitor balancing.



### 3.3.3 – Simulation space vector modulation

The model in Simulink in Figure 3.26 was implemented for the cases having the DC link capacitors unbalanced and balanced with an RL load of  $R=17$  Ohm and  $L=20$ mH. Battery Voltage= 100V.

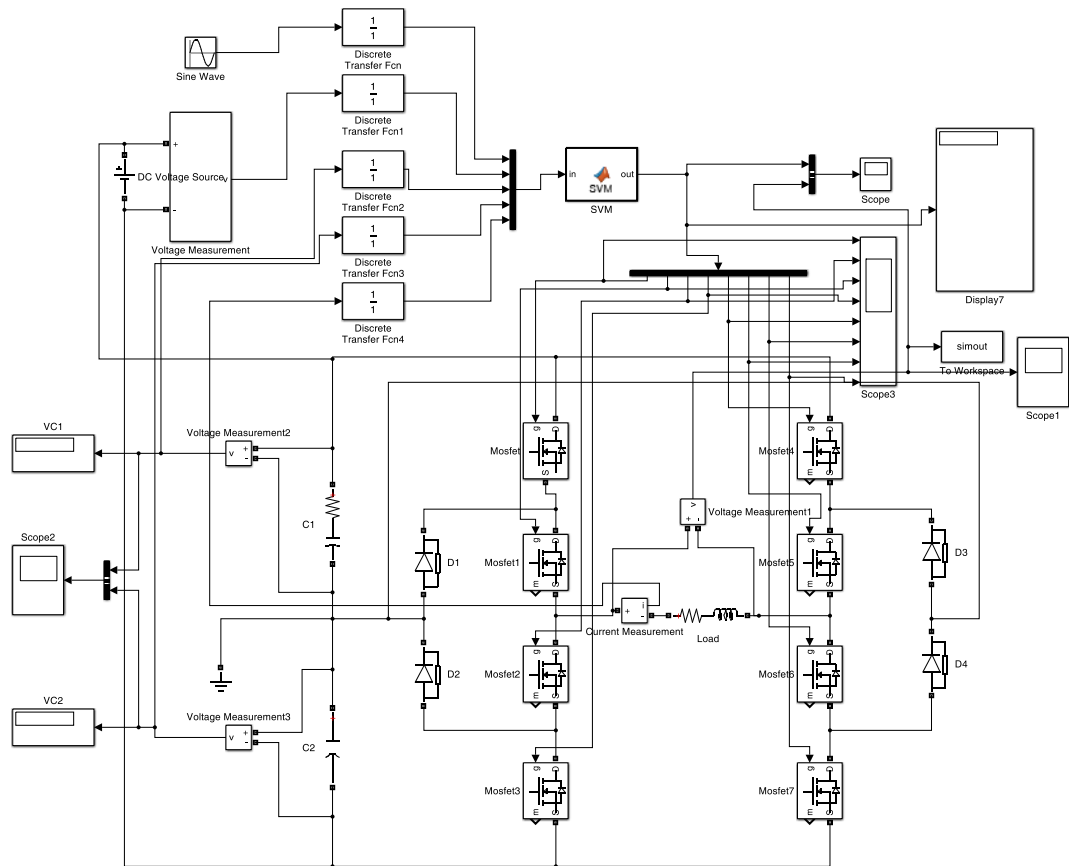


Figure 3.26. Simulink model of the 5-level converter.

The output voltage and voltage in the capacitors with no balancing algorithm is shown in Figure 3.27 and Figure 3.28 respectively. It can be seen that the levels are not even and as the time increases, the unbalance becomes larger. The capacitor voltage show the start of the voltage balanced and unbalancing with the time. This unbalance is due to the modulation employed selecting a sequence that unbalance the capacitors. With a feedback and the use of the redundant vectors this can be solved. In the next section the simulation with the balancing algorithm is presented.

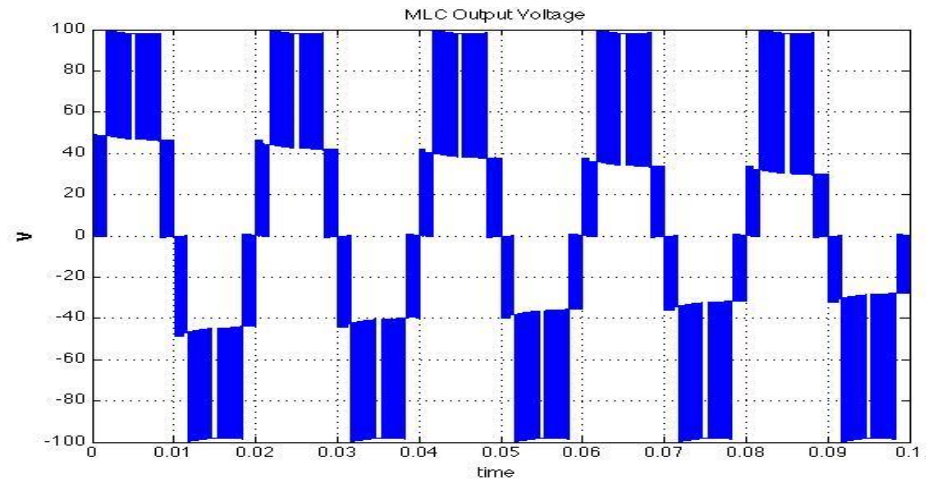


Figure 3.27 Output voltage with no balance algorithm implemented.

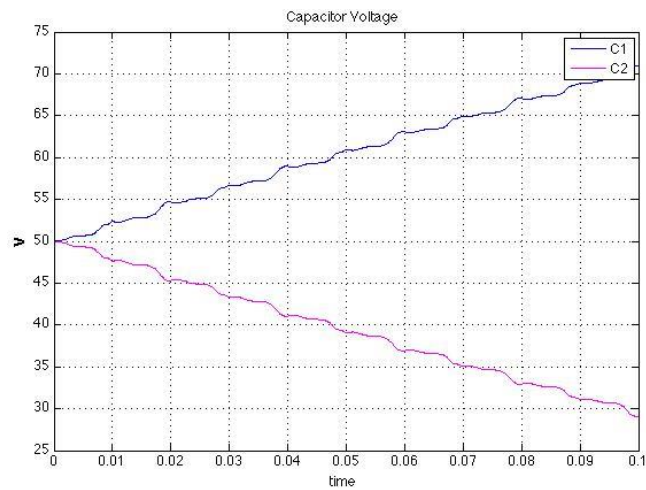


Figure 3.28 Voltage in the DC-link capacitors with no balance algorithm implemented.

The optimization using the redundant vectors to generate the output waveform to balance the DC link capacitors was implemented as explained in section 3.3.2.1 and the output voltage and voltage in the capacitors is shown in Figure 3.29 and Figure 3.30 respectively.

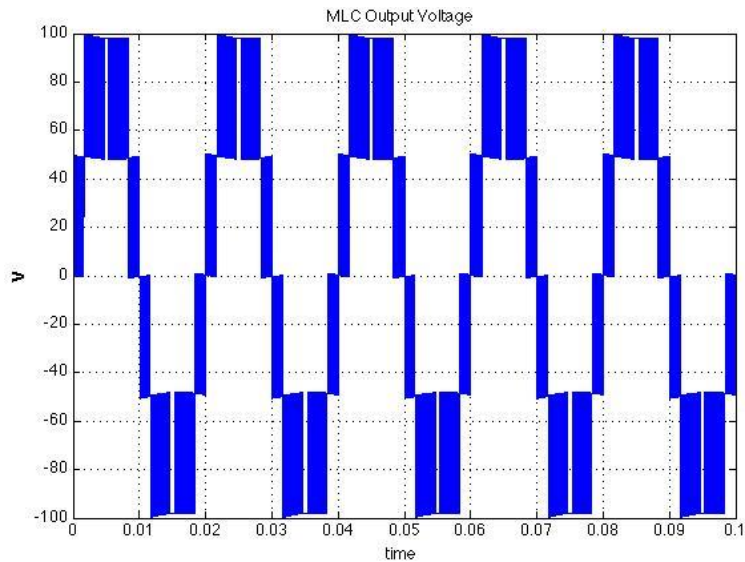


Figure 3.29 Output voltage with balance algorithm implemented.

In this case the capacitors C1 and C2 are initially pre-charged at 25V and 75V respectively to observe the balancing of the voltage in the capacitors using the previously described method.

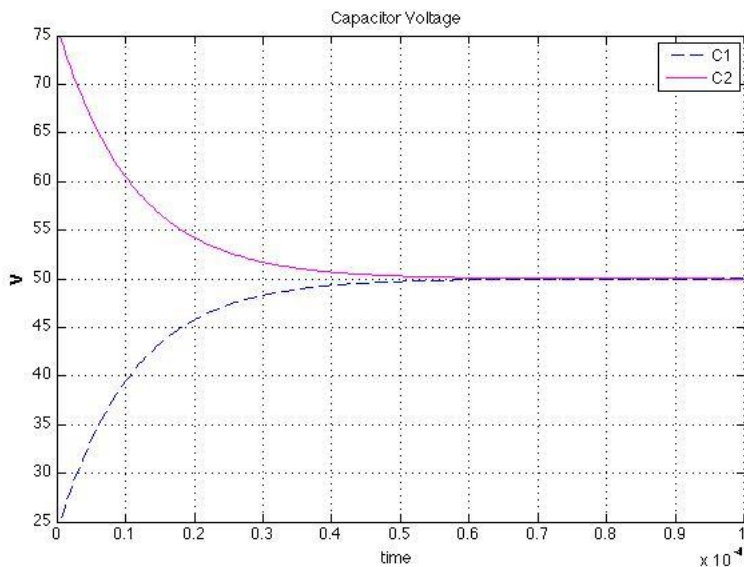


Figure 3.30 Voltage in the DC-link capacitors with balance algorithm implemented.

The results of the simulation presented in this section correspond to the modulation and topology selected. The control is implemented in an FPGA which gives a fast control response and once it has been proved that the algorithm works, the algorithm is coded in LabVIEW FPGA.

### 3.4 Chapter conclusion

In this chapter the modulation techniques for multilevel converters are discussed. Sinusoidal PWM is introduced and evaluated in simulation for different MLC topologies and the output voltage and FFT are presented for the different PWM techniques. After evaluating the sinusoidal PWM in the NPC and FCC for 5 and 9 levels, the topology to be used for the rest of these thesis is chosen based on the number of switching elements, voltage level and THD. The topology selected is NPC in full bridge to generate 5 levels.

Once the topology is chosen, an algorithm to balance the DC-link capacitors is studied. Due to the ease of implementation for a single phase converter a space vector modulation is introduced and chosen as the modulation to control the MLC capacitor balancing and control of the switching sequence. In order to evaluate the performance of the N2V modulation, a simulation with and without the voltage balancing algorithm is presented. The results show a good performance on balancing the capacitor voltage as well as producing the correct vector sequence to generate the 5-level voltage waveform.

The next chapter (4) presents the converter design followed by the implementation in chapter 5. Then in chapter 7 the introduction of an output filter to this converter is presented.

### 3.5 References

- [3-1] B. Mwinyiwiwa, Z. Wolanski, and B.-T. Ooi, "Microprocessor-Implemented SPWM for," *IEEE Trans. Ind. Appl.*, vol. 34, no. 3, pp. 487–494, 1998.
- [3-2] M. Calais, L. J. Borlel, and V. G. Agelidis, "Multicarrier PWM Methods for a Single-phase Five Level Inverter," *Proc. 32nd IEEE Power Electron. Spec. Conf. (PESC'01)*, pp. 1351–1356, 2001.
- [3-3] F. D. D. C. A. C. Converter, S. Busquets-monge, J. Bordonau, and J. Rocabert, "A Virtual-Vector Pulsewidth Modulation for the," *IEEE Trans. POWER Electron.*, vol. 23, no. 4, pp. 1964–1972, 2008.
- [3-4] E. Sambath, S. P. Natarajan, and C. R. Balamurugan, "Performance Evaluation of Multi Carrier Based PWM Techniques for Single Phase Five Level H-Bridge Type FCMLI," vol. 2, no. 7, pp. 82–90, 2012.
- [3-5] Franquelo, L. G., Rodriguez, J., Leon, J. I., Kouro, S., Portillo, R., & Prats, M. A. The age of multilevel converters arrives. *IEEE industrial electronics magazine*, vol. 2 no. 2. 2008

- [3-6] G. Carrara, S. Gardella, M. Marchesoni, R. Salutati, and G. Sciuotto, "A new multilevel PWM method: a theoretical analysis," *IEEE Trans. Power Electron.*, vol. 7, no. 3, pp. 497–505, Jul. 1992.
- [3-7] S. Busquets-Monge, S. Alepuz, J. Bordonau, and J. Peracaula, "Voltage Balancing Control of Diode-Clamped Multilevel Converters With Passive Front-Ends," *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 1751–1758, Jul. 2008.
- [3-8] H. Pinheiro, F. Botterbn, C. Rech, L. Schuch, R. F. Camargo, H. L. Hey, H. A. Gründling, and J. R. Pinheiro, "Space Vector Modulation for Voltage-Source Inverters : A Unified Approach," pp. 23–29.
- [3-9] J. I. Leon, S. Vazquez, J. a Sanchez, R. Portillo, L. G. Franquelo, J. M. Carrasco, and E. Dominguez, "Conventional Space-Vector Modulation Techniques Versus the Single-Phase Modulator for Multilevel Converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2473–2482, Jul. 2010.
- [3-10] J. I. Leon, R. Portillo, S. Vazquez, J. J. Padilla, L. G. Franquelo, and J. M. Carrasco, "Simple Unified Approach to Develop a Time-Domain Modulation Strategy for Single-Phase Multilevel Converters," vol. 55, no. 9, pp. 3239–3248, 2008.
- [3-11] J. I. Leon, R. Portillo, L. G. Franquelo, S. Vazquez, J. M. Carrasco, and E. Dominguez, "New Space Vector Modulation Technique for Single-Phase Multilevel Converters," *2007 IEEE Int. Symp. Ind. Electron.*, pp. 617–622, Jun. 2007.
- [3-12] F. Z. Peng, "A Generalized Multilevel Inverter Topology with Self Voltage Balancing," *IEEE Trans. Ind. Appl.*, vol. 37, no. 2, pp. 611–618, 2001.
- [3-13] C. Bharatiraja, S. Jeevananthan, R. Latha, and S. S. Dash, "A Space Vector Pulse Width Modulation Approach for DC Link Voltage Balancing in Diode-Clamped Multilevel Inverter," *AASRI Procedia*, vol. 3, pp. 133–140, Jan. 2012.
- [3-14] V. N. Reddy, C. S. Babu, and K. Suresh, "Advanced modulating techniques for diode clamped multilevel inverter fed induction motor," *ARPJ. Eng. Appl. Sci.*, vol. 6, no. 1, pp. 90–99, 2011.
- [3-15] O. Bouhali, E. M. Berkouk, C. Saudemont, and B. Francois, "A five-level diode clamped inverter with self-stabilization of the DC-link voltage for grid connection of distributed generators," *2004 IEEE Int. Symp. Ind. Electron.*, pp. 947–952 vol. 2, 2004.
- [3-16] J. I. Leon, L. G. Franquelo, R. C. Portillo, and M. M. Prats, "DC-link capacitors voltage balancing in multilevel four-leg diode-clamped converters," *31st Annu. Conf. IEEE Ind. Electron. Soc. 2005. IECON 2005.*, p. 6 pp., 2005.

## Chapter 4 – Converter design

### 4.1 Introduction

This chapter describes in detail the 5-level NPC multilevel converter (MLC) hardware platform used in this study. To provide a focus to the work, a bidirectional battery to 110VAC 50Hz converter is to be built, to act as a replacement for a petrol generator used as a construction site power supply. The battery is from a Hybrid Electric Vehicle (HEV) battery pack demonstrating the second life usage of EV, HEV and Plug-in Hybrid Electric Vehicle (PHEV) batteries. Although any battery with the appropriate rating or other DC source can be used, using repurposed batteries from EV can extend the usable time of a battery, contributing to a significant reduction in the environmental impact.

As mentioned in the previous chapters, there are three basic converter topologies: Neutral Point Clamped (NPC), Flying Capacitor Converter (FCC) and H-Bridge Converter (HBC). The cascaded H-bridge converter and full-bridge (FB) converters, as presented in previous chapters, are topologies of particular interest as their maximum output voltage can reach the level of the DC input, as compared to the maximum output of  $V_{DC}/2$  that the NPC and FC half bridge converters can achieve. A 5-level converter is studied here for the reduced THD compared to a 3 level converter and the reduced number of switching and clamping elements compared to those required in a 9-level converter with a single DC source. For this reason, the topology to be studied more in detail is the 5-level full bridge neutral point clamped 5L-FB-NPC similar to the system described previously in [4-1].

In this chapter the specification and design of the hardware platform is presented. Detailed simulation results of the subsystem in Simulink and then the integration of both subsystems (DC-DC and MLC) in LabVIEW Co-simulation with Multisim.

## 4.2 Platform system description and specification

The platform system is a bi-directional DC-AC converter based on a 5-level NPC full-bridge topology. A requirement of the system is that it operates from a 108V to 144V DC battery pack (Nickel metal hydride, NiMH, as found in a Honda insight HEV). Since the system is designed to operate with a 110VAC output, to operate in construction sites, a 2:1 step-down transformer is used to interface the unit the 220V AC mains for testing. The transformer is a typical 240:110V isolating transformer typically used on

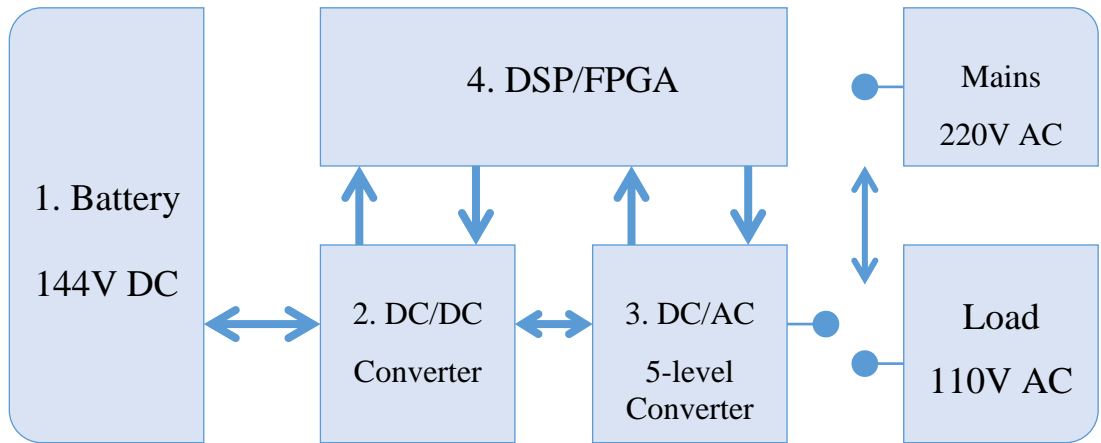


Figure 4.1 Block Diagram of the system.

construction sites. The voltage and power specifications are detailed in Table 4.1. The block diagram of the system used to test the MLC topology selected and the modulation technique for the construction site power supply is shown in Figure 4.1.

Construction Site Power Supply Electrical Specifications	
Output power	1500 W
Input voltage	108 -170 VDC
Output voltage (rms)	110 VAC
Maximum output peak voltage	171.1 VAC

Table 4.1 System specification

### 1. Battery

The DC source used for the presented circuit is a battery pack taken from a Honda Insight, rated at 144V DC, its characteristics are described in detail in Chapter 5. For the initial testing this voltage is simulated as a DC source considering 2 voltages, the minimum and nominal voltage, 108V and 144V respectively as the battery will not retain the maximum

voltage of 170V for a prolonged time. However, the converter is designed to work within the minimum and maximum voltages.

## *2. DC-DC converter*

A DC-DC converter is required to carefully manage the battery charge and discharge process and to provide the DC-AC converter with a relatively stable DC voltage. When the system is acting like a conventional building site generator and so the battery is being discharged, the voltage of the battery pack has to be increased (stepped-up) in order to meet the output voltage requirements. During charging mode the higher grid voltage is stepped-down to meet the battery voltage levels. Therefore, to meet these requirements a bidirectional buck-and-boost DC-DC converter is used.

## *3. DC-AC converter*

The DC-AC converter is a bidirectional 5L-FB-NPC topology. Its peak voltage DC voltage is the output voltage from the battery DC-DC converters. During battery discharge mode the load is taken to be a resistor for testing. During charging mode it is connected to the grid via a 220-110VAC step-down construction site transformer.

## *4. DSP-FPGA*

The control for the entire system including the DC-DC converter output voltage control, DC-link capacitor balance, MLC switching pulses to generate the output AC waveform and voltage level control are implemented in LabVIEW and runs on the single board RIO sbRIO-9607 with National Instruments NI 9683 mezzanine card platform. The controller board was selected as it provides a high speed and bandwidth processing of the signals to measure and control the system robustly and reliably. It also has a real-time processor and the parallel processing capabilities of the FPGA. Additionally, the mezzanine card has 16 analog inputs, 14 digital outputs, and other input and output ports.

The control system monitors the input and output voltages of the DC-DC converter and the AC grid voltage and current. A separate safety monitoring system implemented on an Arduino is used to protect the battery against overcharging and over discharging, and disconnects the battery using a relay should limits be reached, a signal is also sent to the LabVIEW controller to permit a controlled shut down.



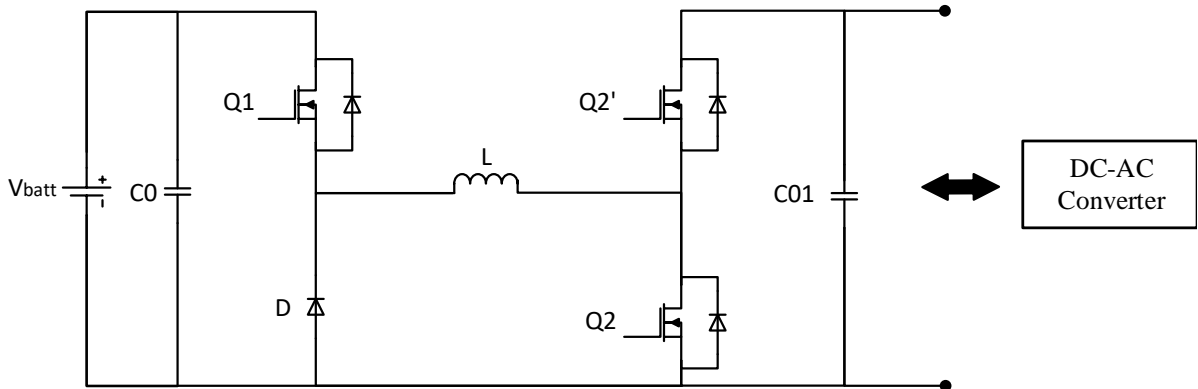
### 4.3 Converter Design

This section describes the operation and design of the DC-DC and DC-AC converters used within the platform.

As mentioned earlier, the basic concept is to use a bidirectional DC-DC converter to interface the battery to the DC-AC converter. The approach to integrating the DC-DC and MLC topology was proposed in [4-2] and [4-3], and this topology can operate in buck or boost mode in either direction (battery charging or discharging). For the purpose of the system designed here, a cascaded DC-DC converter stepping up the voltage from the battery, and stepping down the voltage from the mains to charge the battery, is introduced. The topology was first described in [4-4] and then a simplified version [4-5] to operate in the described form is used. In the following section, the design of the DC-DC converter is presented based on the simplified version of the converter.

#### 4.3.1 DC-DC converter design

Figure 4.2 shows the bi-directional buck and boost converter battery interfacing converter. It is formed with 3 controlled switches Q1, Q2 and Q2'. The purpose of the Q1 is to select the direction and the mode of the converter. If a '1' is applied to the gate, the converter



works as a boost converter to discharge the battery. In the case of '0' applied to the gate, the converter mode is buck to charge the battery. Switches Q2 and Q2' are used for the conversion in a complementary mode using a PWM signal to control the output of the converter.

Figure 4.2 DC-DC bidirectional converter

The specification for the power supply is a single phase AC supply 110 VAC (155 V peak). According to the UK specification the tolerances are +10% and -6% for a building site power supply following the standard BS7671 [4-6]. Thus the minimum and maximum output voltages the converter should supply are given by (4.1) and (4.2) respectively, the

peak voltage is used as this will define the output specification range for the DC-DC converter.

$$V_{grid (min)} = \sqrt{2} * V_{rms} * 0.94 = 146.22 \text{ V} \quad (4.1)$$

$$V_{grid (max)} = \sqrt{2} * V_{rms} * 1.10 = 171.11 \text{ V} \quad (4.2)$$

Taking the battery voltage  $V_{batt}$  as 144V and the maximum output peak voltage permitted as 170V. The maximum voltage is considered in the design of the converter as the output voltage  $V_{grid}$  in boost mode and for an output power of 1.5kW the current  $I$  is 10A. Using the maximum voltage will give the minimum requirements of the components, therefore the devices to use can go above that minimum.

The output of the converter in boost mode is given by (4.3) where the duty cycle  $D$  is applied to the switch  $Q2$  and the input voltage  $V_{batt}$  can vary from 170V and 108V which correspond to the maximum and minimum voltages respectively.

$$V_{out} = \frac{V_{batt}}{1-D_{boost}} \quad (4.3)$$

The values of duty cycle obtained evaluating for minimum battery voltage is 0.30 and for the maximum battery voltage, the duty cycle is approximately zero. The maximum duty cycle during the discharge operating mode used for the design is taken to be  $D_{boost}=0.30$ .

During charging the DC-DC converter operates in buck and the battery voltage to charge the battery is assumed to be 120V then the  $D_{buck}$  is found using (4.4)

$$D_{buck} = \frac{155 \text{ V} - 120 \text{ V}}{155 \text{ V}} = 0.22 \quad (4.4)$$

The value of the inductor  $L$  can be found using the expression described in (4.5) where  $\Delta_{iL}$  is the current ripple considered to be 5% of the output current  $I$  (10A) and  $f_{sw}$  is the switching frequency of the converter.

$$L = \frac{1}{2 * \Delta_{iL}} * \frac{V_{batt}^2}{I * V_{out} * f_{sw}} * \left(1 - \frac{V_{batt}}{V_{out}}\right) \quad (4.5)$$

The switching frequency of the DC-DC converter was selected to be 50 kHz as it is above the audible frequency range of 20 Hz to 20 kHz, and to reduce the inductor size. Using the battery nominal voltage and a switching frequency of 50 kHz for the initial design an

inductor of 406 $\mu$ H will be employed. This value of inductance will be used for the converter operating in boost and buck modes.

The RMS current in the inductor can be found using the equation (4.6), this current corresponds to the inductor operating in boost mode. The maximum current is given by the equation (4.6) and can be found with the maximum duty cycle.

$$I_L = \left( \frac{I_{out}}{1-D_{boost}} \right)^2 + \frac{1}{3} * \left( \frac{\Delta i_L}{2} \right)^2 \quad (4.6)$$

The current in the inductor for the boost mode is 14.08A.

The input and output capacitors will be used of the same value and it's given by the equation (4.7) where  $\Delta V_C$  is the output voltage ripple.

$$C = \frac{1}{2 * \Delta V_C} * \frac{I}{V_{out} * f_{sw}} * \left( 1 - \frac{V_{batt}}{V_{out}} \right) \quad (4.7)$$

For a voltage ripple of 1% the capacitance obtained is 100.38 $\mu$ F this represent the minimum capacitance required, a larger value of capacitor C=470 $\mu$ F is used to reduce the voltage ripple and to match the capacitance in the MLC.

The electrical ratings for the MOSFETs were chosen based on the maximum operating voltages and currents. The drain to source voltage  $V_{DS}$  is considered to be a maximum of 200V for both operation modes, and the current RMS current  $I_{sw}$  can be obtained for boost and buck modes with (4.8) and (4.9) respectively.

$$I_{sw \ boost} = I_L * \sqrt{D_{boost}} \quad (4.8)$$

$$I_{sw \ buck} = I_L * \sqrt{D_{buck}} \quad (4.9)$$

The current obtained is 6.56A and 7.66A. Therefore the rating for the MOSFETs in the DC-DC converter will be 200V  $V_{DS}$  and 7.66A minimum. To ensure the voltage doesn't exceed the limits the MOSFET used is FDH44N50 rated at 500V and 44A.

The current in the diode  $D$  can be found using (4.10) and (4.11) for each of the modes described.

$$I_{sw \ boost} = I_L * \sqrt{(1 - D_{boost})} \quad (4.10)$$

$$I_{sw \ buck} = I_L * \sqrt{(1 - D_{buck})} \quad (4.11)$$

The current values are 11.78 A and 12.43 for boost and buck modes respectively. As with the MOSFET, the higher value of current to ensure it works safely. The diode used is FES16JT rated at 600V and 16A.

#### 4.3.1.1 Bi-directional DC-DC converter simulation validation

In order to validate the circuit design the circuit in Figure 4.3 is implemented in Simulink using the model shown in Figure 4.4. The maximum voltage,  $V_{batt}$ , is 170VDC and 120VDC for discharging and charging modes respectively. In charging mode the battery becomes the load on the circuit. For the purpose of simulating this operating mode the load, is replaced by a DC source and the source is replaced with a resistor.

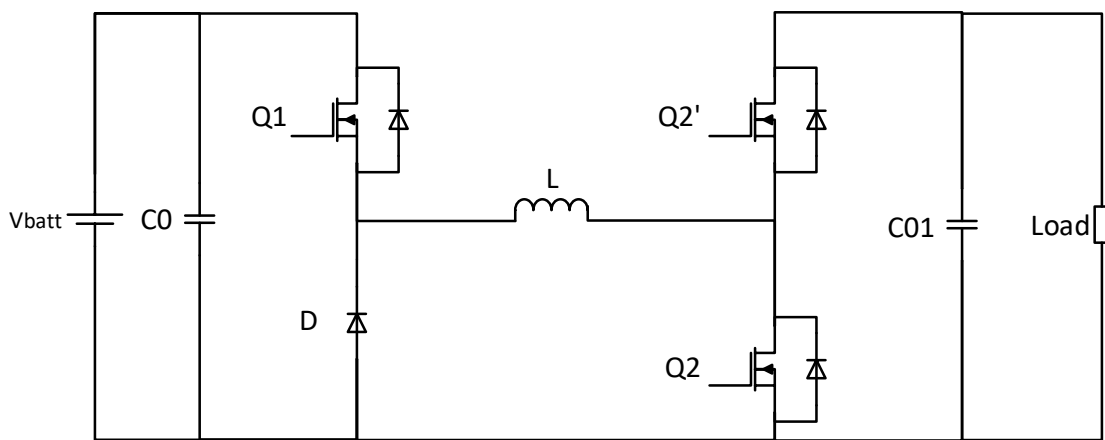


Figure 4.3 DC-DC bidirectional converter

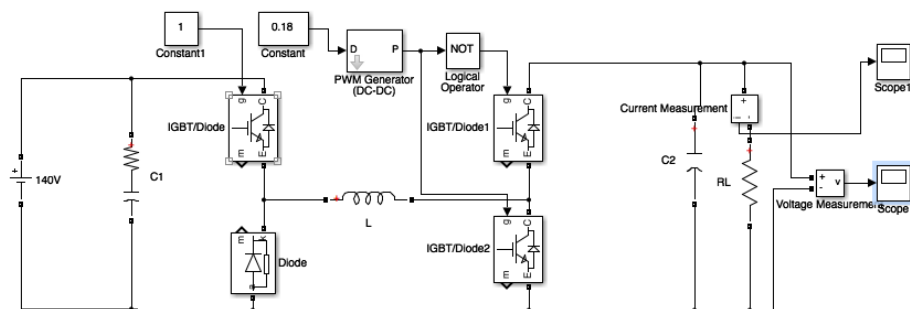


Figure 4.4 Simulink Model Boost Buck Converter

The converter was tested in discharging and charging modes, Figure 4.5 show the converter in boost mode and the output of the converter for both modes are shown in Figure 4.6.

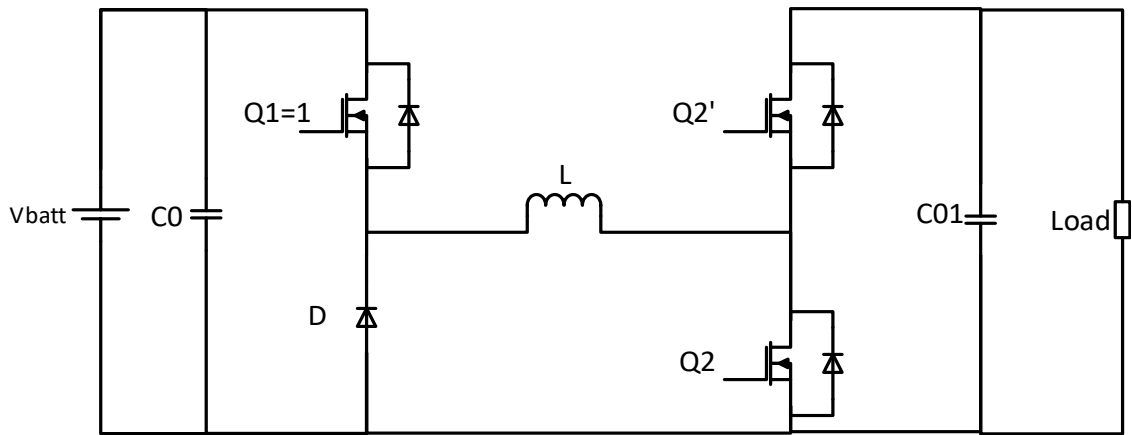


Figure 4.5 Boost Mode test circuit

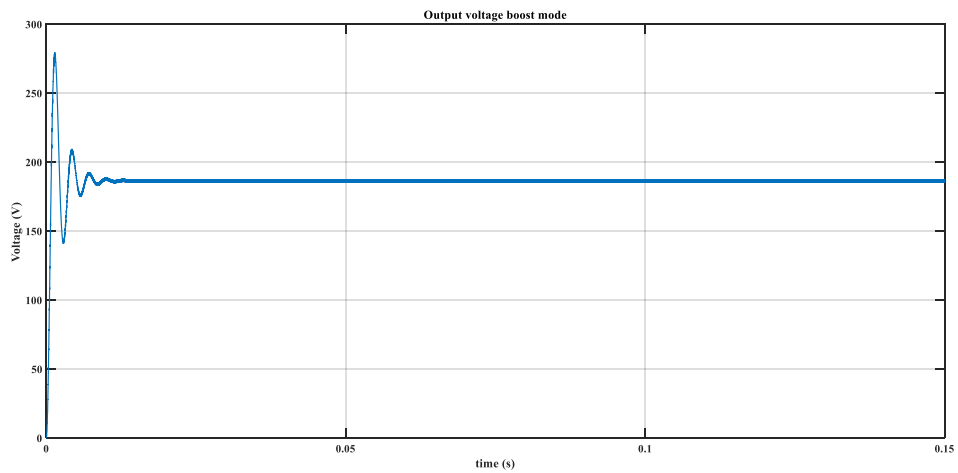


Figure 4.6 Boost (Discharge) Mode Output voltage

In Figure 4.7 the buck mode test circuit is shown and the output voltage measured in C0 is shown in Figure 4.8.

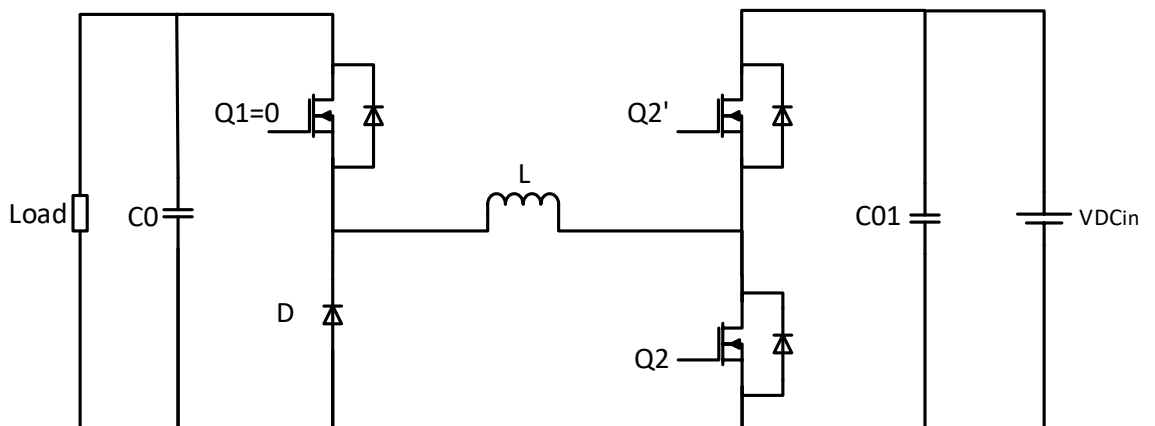


Figure 4.7 Buck Mode test circuit

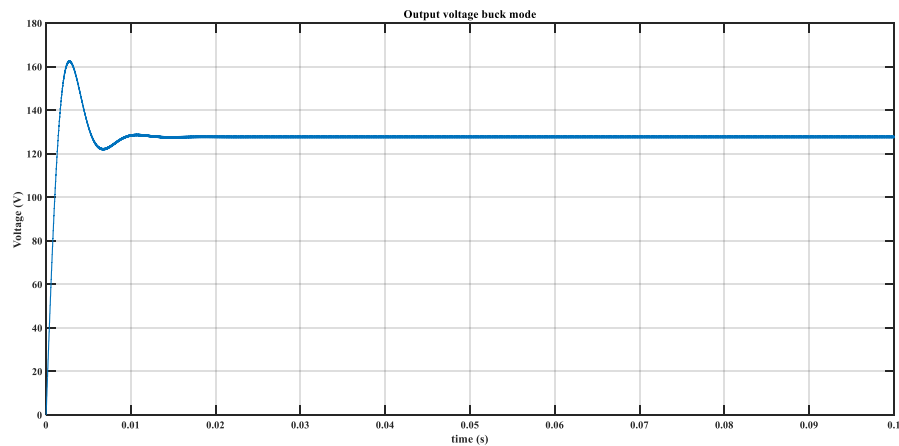


Figure 4.8 Buck (Charge) Mode Output

The output voltages for both modes operating in open loop show the converter working within the designed limits in open loop showing settling times of 15ms in buck mode and 25ms in boost mode. These simulation results were taken without limiting circuits and for the charge mode, a load resistor is used to represent the battery.

#### 4.3.2 Multilevel converter design

Although there are different implementations of the NPC topology reviewed in [4-7], for a single phase system, a topology with second leg or phase (leg B in Figure 4.9) [4-8] can be used where the output is taken from nodes A and B making the 5-level Full-Bridge NPC (5L-FB-NPC) topology with output voltage levels defined as  $V$ ,  $V/2$ ,  $0$ ,  $-V/2$  and  $-V$ . The bi-directional DC-AC is formed by a 5-level MLC which is based on a full-bridge topology where each leg consists of a 3-level Half-Bridge Neutral Point Clamped (3L-HB-NPC), see Figure 4.9.

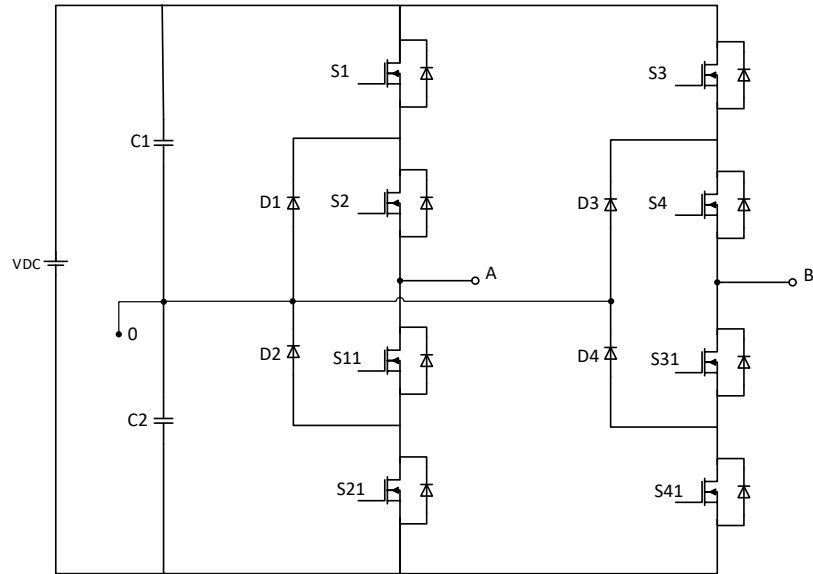


Figure 4.9 5-level NPC converter in full bridge topology.

The DC-link is smoothed by two capacitors C1 and C2 where the dc voltage (VDC) is divided in 2 discrete levels ( $V/2$  and  $-V/2$ ). Considering leg A, the output is taken from node A and 0, where 0 is the neutral point between the 2 capacitors. The leg output voltage  $V_{A0}$  can take on one of three levels  $-V/2$ , 0, or  $V/2$ .

The output voltage of phase A, phase B, and AB is shown in Figure 4.10. The phase voltages A and B are referenced to 0V and the output voltage with 5 levels is taken from nodes A and B for an input voltage of 155V.

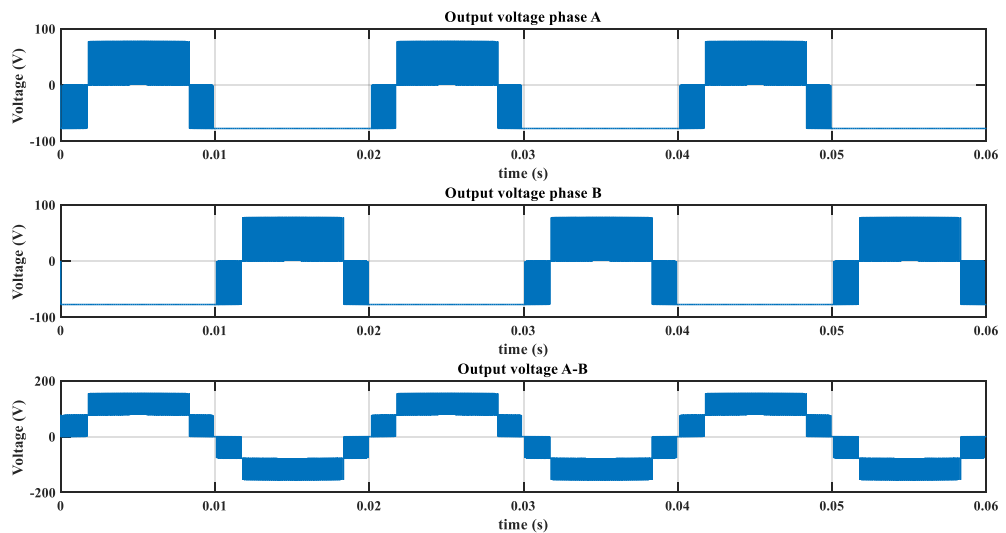


Figure 4.10 Output voltage per phase and total

As described previously the topology chosen can generate an output peak voltage at the level of the DC-link voltage when the output voltage is supplied by the two legs. The capacitor voltages are balanced using the algorithm presented in Chapter 3.

The advantage of MLC is the reduced semiconductor size compared to conventional two-level inverters. The topology used is formed of 2 legs of a 3-level NPC. The voltage rating of the MOSFETs in a MLC can be found using (4.12) for an m-level converter, for this design m=3.

$$V_{DS\ MLC} = \frac{V_{batt}}{m-1} \quad (4.12)$$

The voltage rating of the MOSFET is half the DC-link considered for this design as 170V maximum. The current rating is also halved, then the voltage and current rating of the MOSFETs are 85V and 5A respectively. The closest device available through the university suppliers with low  $R_{DS\ on}$  at the time of the design was an FDP04N10A rated at 100V and 164A, a margin has been left for safety reasons and this MOSFET also features a low  $R_{DS\ on}$  of 4.5m $\Omega$  to reduce conduction losses, increasing overall system efficiency.

The clamping diodes block the voltage of one of the capacitors at a time, for the topology presented, the voltage on a capacitor is 85V considering the maximum voltage of 170V in the DC-link and half the output current of 10A. Therefore, the same diode used in the DC-DC converter is used for the DC-AC converter.

The value of the capacitors forming the DC-link,  $C_{DC}$  (4.13), can be found as described in [4-9] considering the voltage ripple in the capacitor  $\Delta V_C$  expressed in percentage, the output current  $I_{out}$ , the maximum voltage in each capacitor  $V_C$  and the frequency  $f$  at which the MLC is generating the output voltage, for this design is 50Hz.

$$C_{DC} = \frac{\Delta V_C}{V_C} * \frac{I_{out}}{f} \quad (4.13)$$

The capacitor value found using the expression above is 2,000 $\mu$ F, the next capacitor available is 2,200 $\mu$ F at 250V was used.

#### 4.3.2.1 Multilevel converter simulation

The DC-DC and MLC converters integrated are shown in Figure 4.11. The programming of the FPGA in LabVIEW with the same algorithm described in Chapter 3 was



implemented. The reference signal generation, vector selection and PWM generation functions are used. First, in open loop, without considering the voltages of the DC link capacitors, to generate the switching pulses using the Half-Bridge Digital Output in the FPGA mezzanine board, once the pulses were generated, the capacitor balancing algorithm was added to the program adding analogue input reading for the capacitor voltages and output voltage and current.

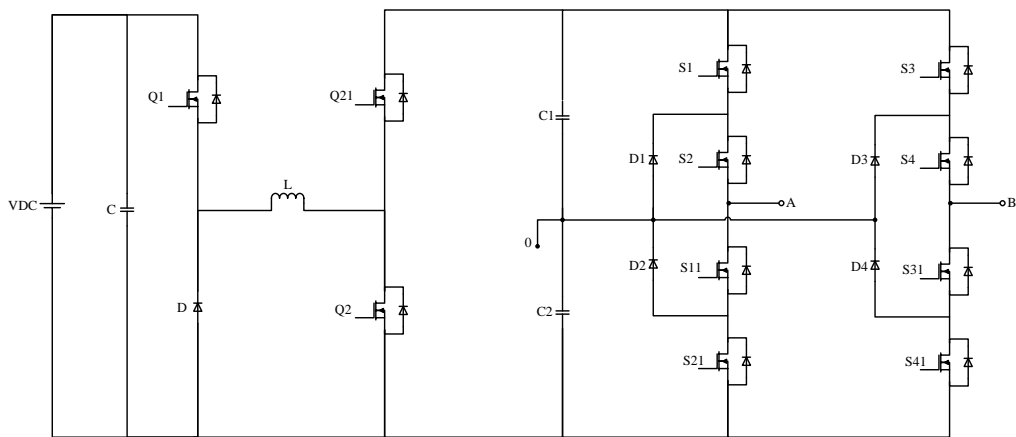


Figure 4.11 DC-DC and MLC converter integrated.

LabVIEW and Multisim provides a convenient environment for co-simulating control systems with power electronic circuits, and so can be used to accelerate the design process by using LabVIEW to simulate the FPGA program and Multisim to simulate MLC design in Multisim where the MLC is placed as an external model in LabVIEW to test the model's response to the FPGA program. The Co-simulation requires adaptations of the actual FPGA program and in the Multisim model as well, some of these adaptations are the use of SubVIs and the adaptation to the limitation to use functions as flat sequences, timed loops and numeric representations. Then, the simulation was done for both, charging and discharging modes with the DC-DC converter integrated.

The MLC Multisim model used in the simulation is shown in Figure 4.12. With the Co-Simulation model in discharging mode, the Power Spectrum and the Harmonic Distortion Analyser functions were used to calculate the FFT and THD respectively. Modifications and collection of the data to be used by the mentioned blocks was also necessary to obtain the desired result.

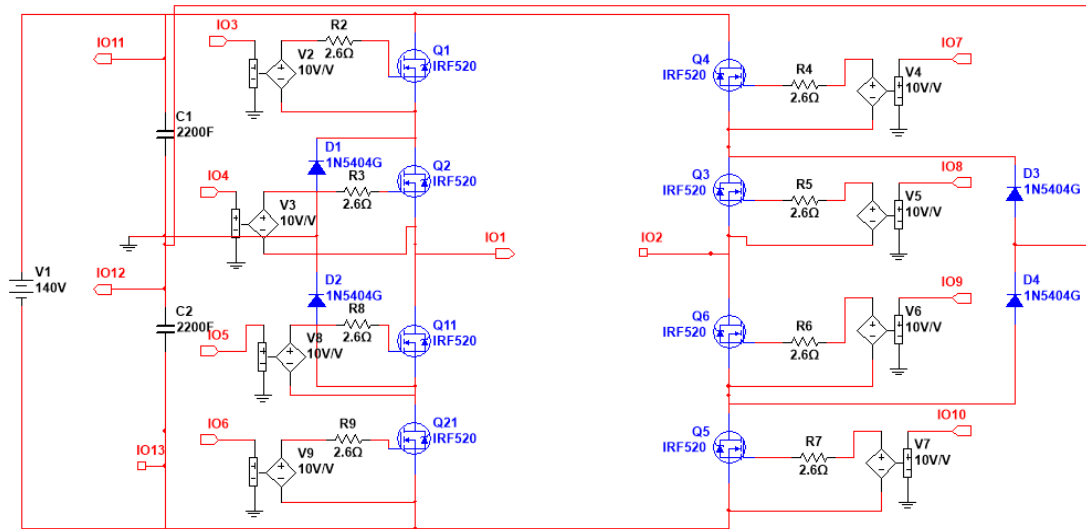


Figure 4.12 5-level NPC single phase full bridge converter Multisim model.

The front panel used for this simulation is shown in Figure 4.13, as explained above, co-simulation allows an interaction between the LabVIEW program and the model to visualise the output in the model as the parameters are changed in the program. This feature is useful to evaluate the effect of different loads connected to the system in a graphical interface.

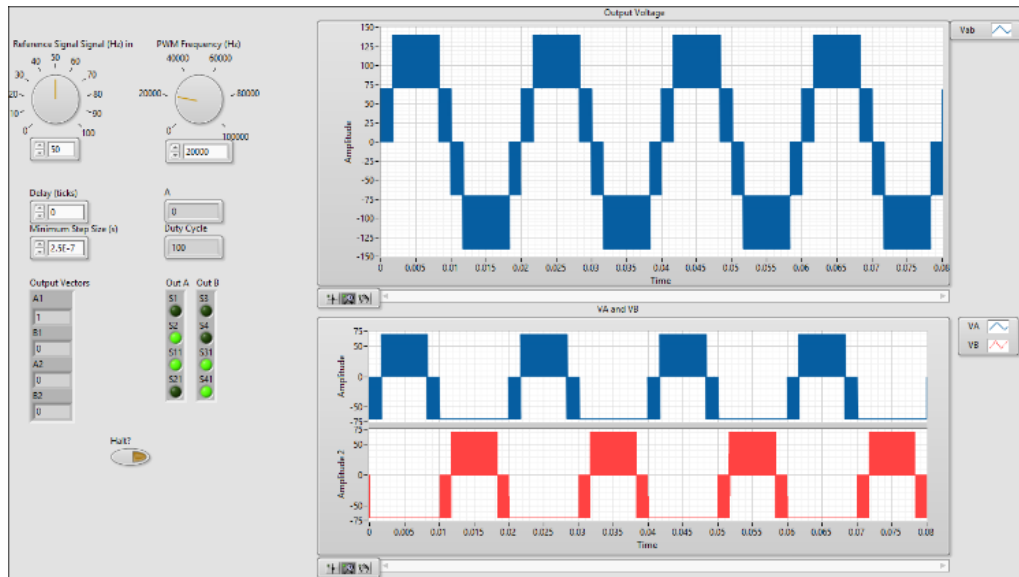


Figure 4.13 Co-Simulation Front Panel Output Voltage and phase voltages.

The block diagram of the co-simulation system is shown in Figure 4.14, it can be seen that a simulation loop is used instead of the while loop used normally in a LabVIEW

program. The simulation loop allows the use of external models to communicate with the LabVIEW code.

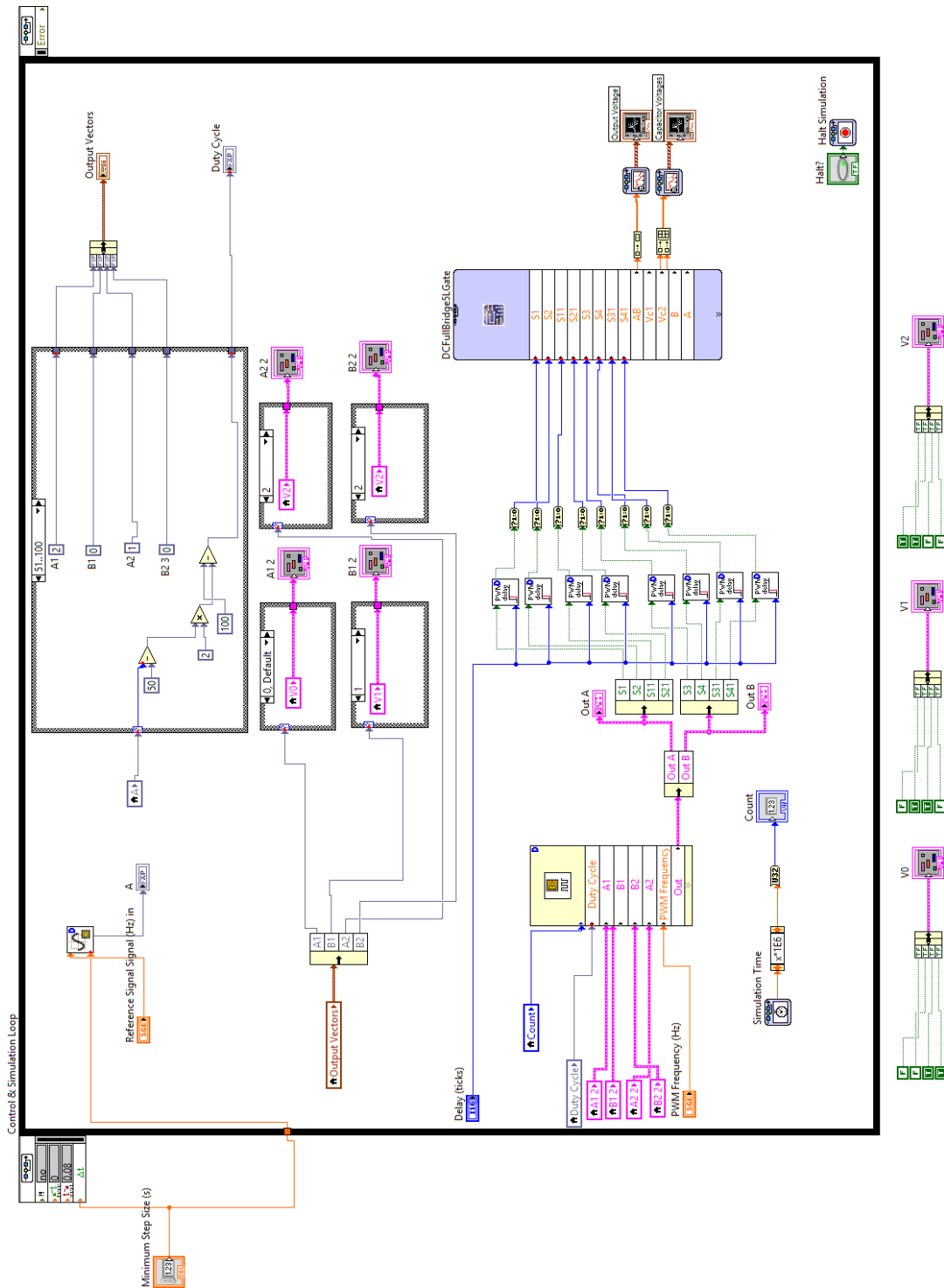


Figure 4.14 CoSimulation block diagram.

#### 4.4 System Simulation Results

This section presents simulation results of the integrated converters in Figure 4.15 operating in charge and discharge modes.

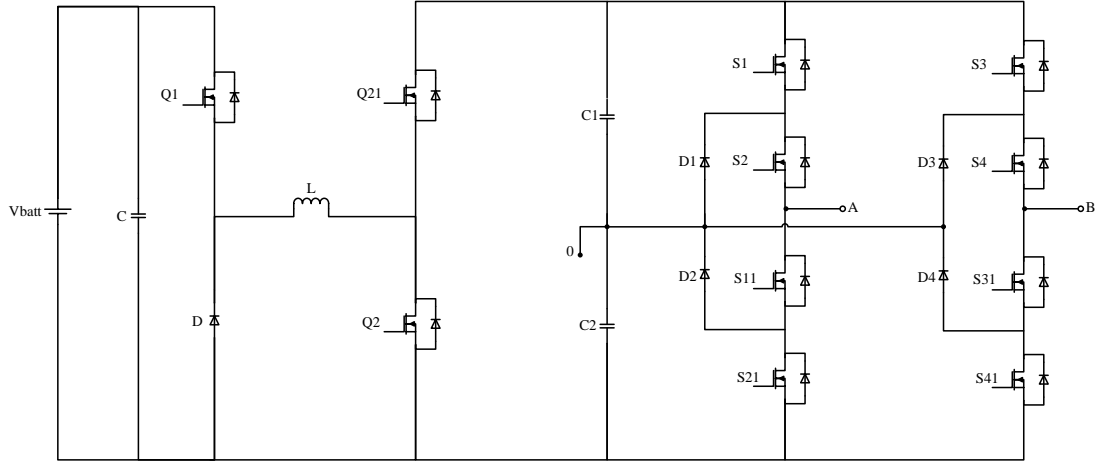


Figure 4.15 DC-DC and MLC integrated

The operating conditions simulated are the minimum and nominal battery voltages and the maximum and minimum tolerances on the AC side, the switching frequency of the MLC is 30kHz and the sinusoidal reference signal is 50 Hz. The switching frequency is 30 kHz for the DC-DC converter, operating in open loop with a fixed duty cycle for both battery voltage levels. In the discharging mode the load tested is  $R=100\ \Omega$ ,  $L= 10\mu\text{H}$  and in charging mode the load used to simulate the battery as a load is  $100\Omega$ .

The THD is calculated for the discharging simulations using using equation 4.14

$$THD = \frac{\sqrt{V_{trms}^2 - V_1^2}}{V_1} * 100 \quad (4.14)$$

Where  $V_{t rms}$  is the output RMS voltage, and  $V_1$  is the voltage of the fundamental component.

#### 4.4.1 Discharging mode with nominal battery voltage

The results of the system's simulation in discharging mode with the nominal battery voltage are presented in this section. In Figure 4.16 the DC side, battery voltage and the

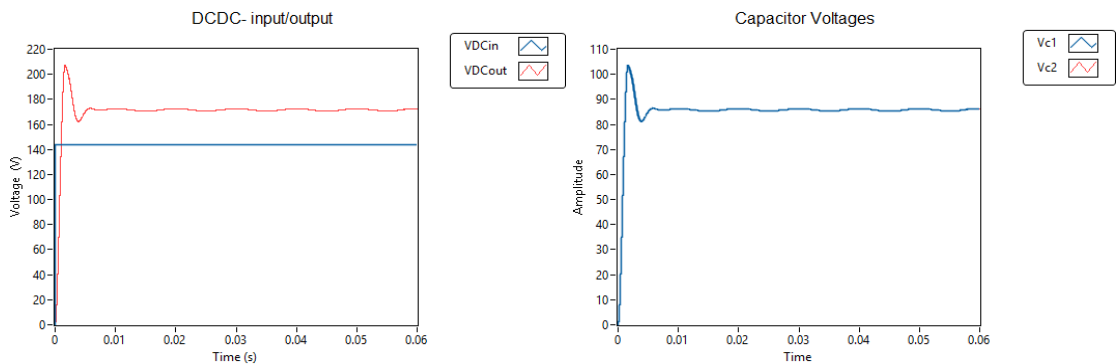


Figure 4.16 DC-DC converter input and output waveforms. On the right graph the DC link capacitor voltages

output of the DC converter is shown and the capacitor voltages forming the DC-link to the MLC. The voltages are balanced and the output of the DC-DC converter presents a ripple within the specified design.

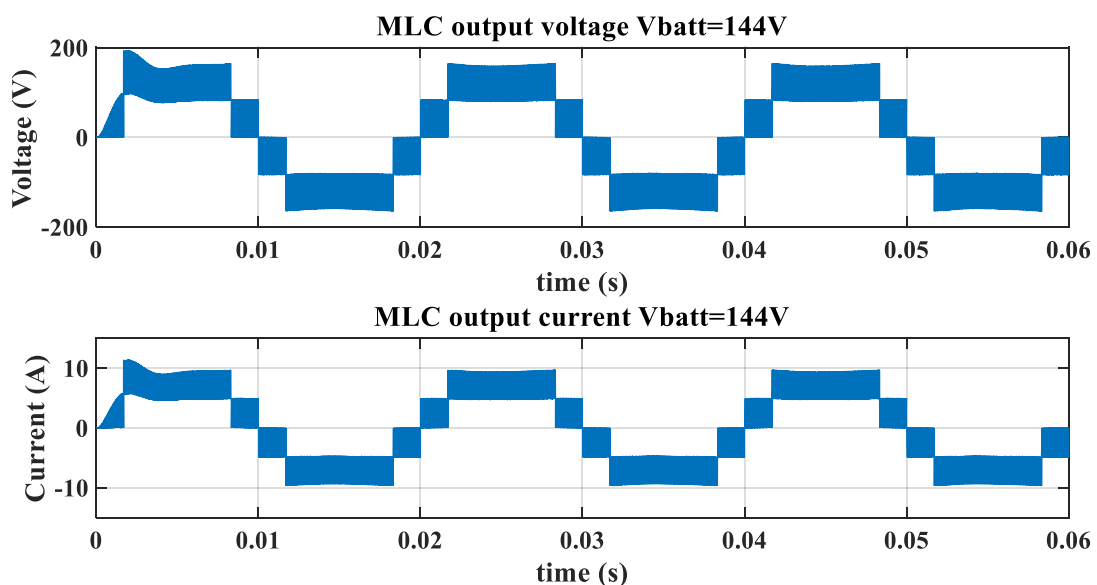


Figure 4.17 Output Voltage and Current waveforms with  $V_{batt}=144V$

The output voltage and currents on the AC side of the converter are shown in Figure 4.17, the MLC provides a maximum output of  $V_{grid(max)}= 185VAC$ .

The THD of the output voltage and current is obtained from the the FFT analysis shows the following result,  $THD= 26.91\%$ , the FFT power spectrum is shown in Figure 4.18

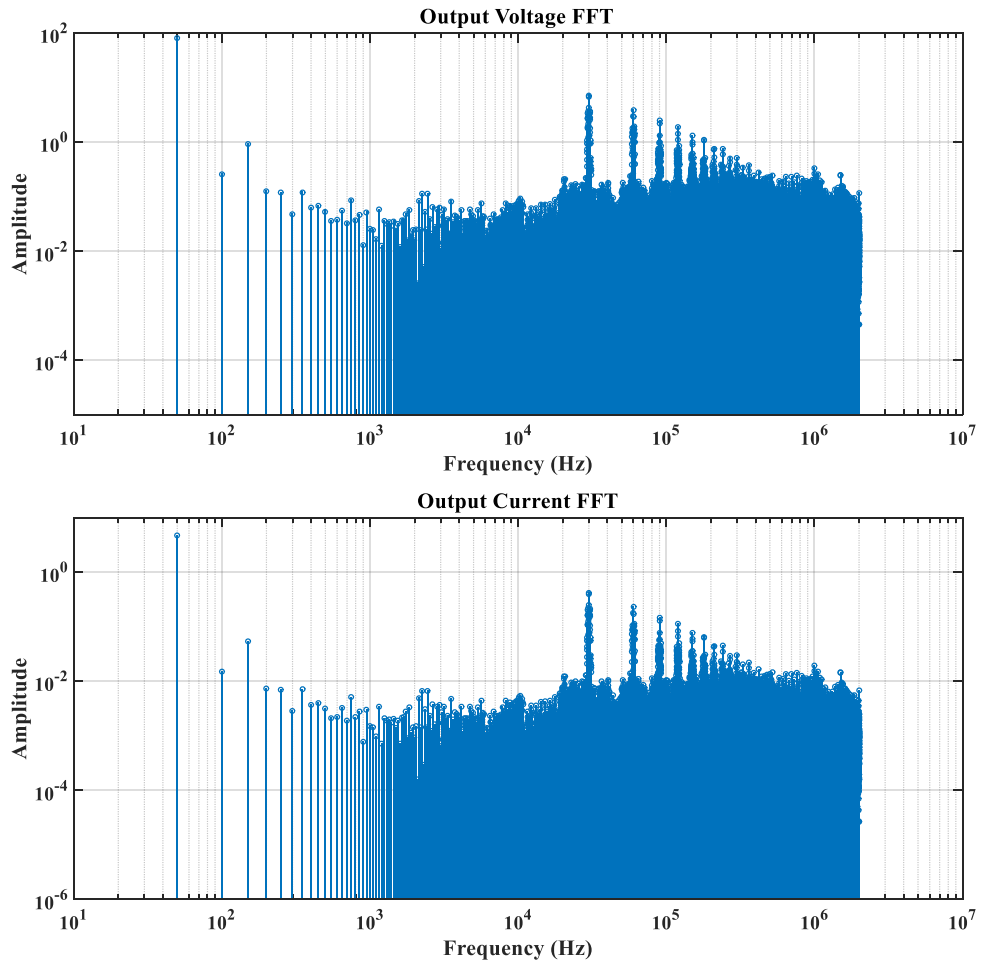


Figure 4.18 Current and Voltage FFT in discharging mode with  $V_{\text{batt}}=144\text{V}$

The frequency components represent the frequency of 50 Hz in the AC side and the switching frequency of the converters.

#### 4.4.2 Discharging mode with minimum battery voltage

The simulation result of the converter at the minimum battery voltage in the DC side conversion are shown in Figure 4.19, the voltage in the capacitors show an increased time to balance compared to the response obtained in the previous battery voltage tested.

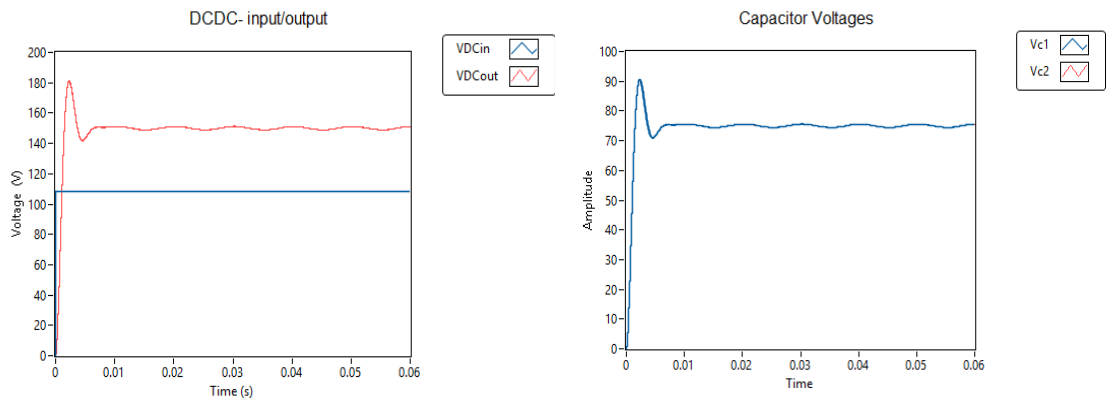


Figure 4.19 Generator Mode DC-DC converter input and output waveforms. On the right graph the DC link capacitor.

The AC output of the converter is shown in Figure 4.20 the peak-voltage is 148V, and this voltage is within the limits established in the regulations on building sites power supplies.

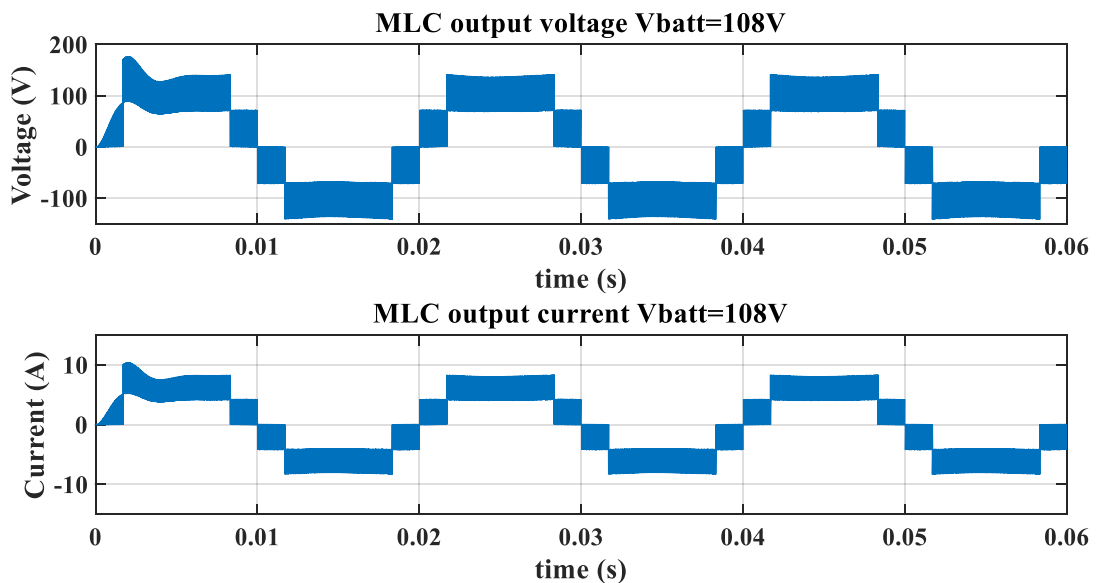


Figure 4.20 Output Voltage and Current waveforms with  $V_{batt}=108V$

The harmonic distortion obtained for the conditions in this simulation, the FFT is shown in Figure 4.21 the THD of the current and voltage outputs is THD= 26.83%

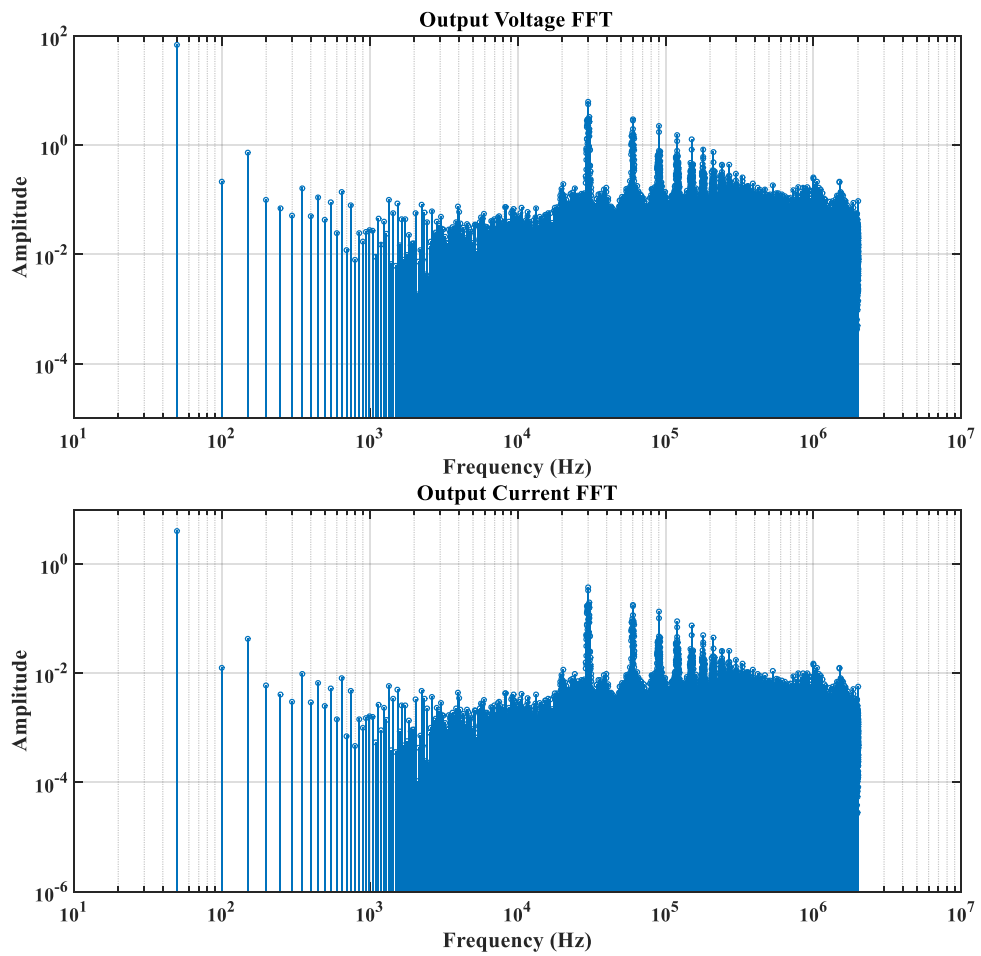


Figure 4.21 Current and voltage FFT

The frequency components under these conditions on the output current show an increased amplitude of the 50Hz component and showing the same high frequency components described for the previous simulation conditions.



#### 4.4.3 Charging mode with maximum grid voltage

As described in Section 3.4, the converter is designed to work in bidirectional mode, the converter can convert the AC current coupled with a transformer to charge the battery. The first test condition with the AC side as the input is 171.1 VAC, representing the maximum voltage in the AC side expected and a load in the DC side to represent the battery. The output voltage on the DC side of the converter is shown in Figure 4.22, it can be seen that the output voltage is 144V, the maximum voltage to charge the battery. The capacitor balance is achieved following the same voltage levels on both capacitors from the start.

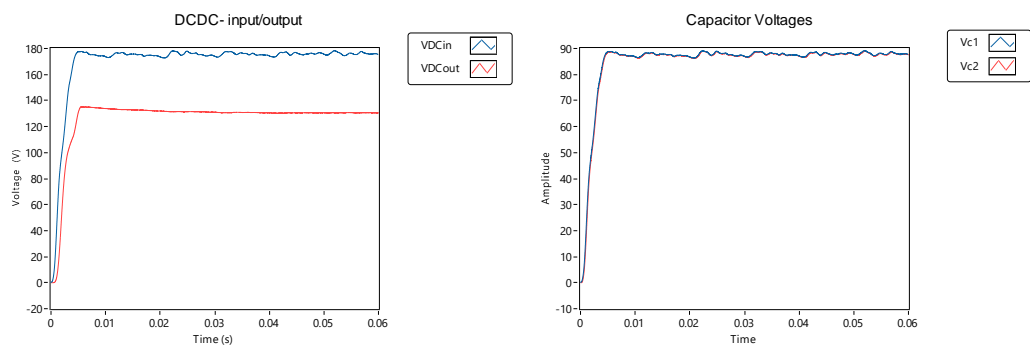


Figure 4.22 Charging Mode DC-DC converter input and output waveforms. On the right graph the DC link capacitor voltage.

#### 4.4.4 Charging mode with minimum grid voltage

In this section, the simulation of the charging mode of the converter with the minimum voltage expected in the AC side. The output in the DC side and the voltage in the capacitors is shown in Figure 4.23. It can be seen that the overshoot goes to the same

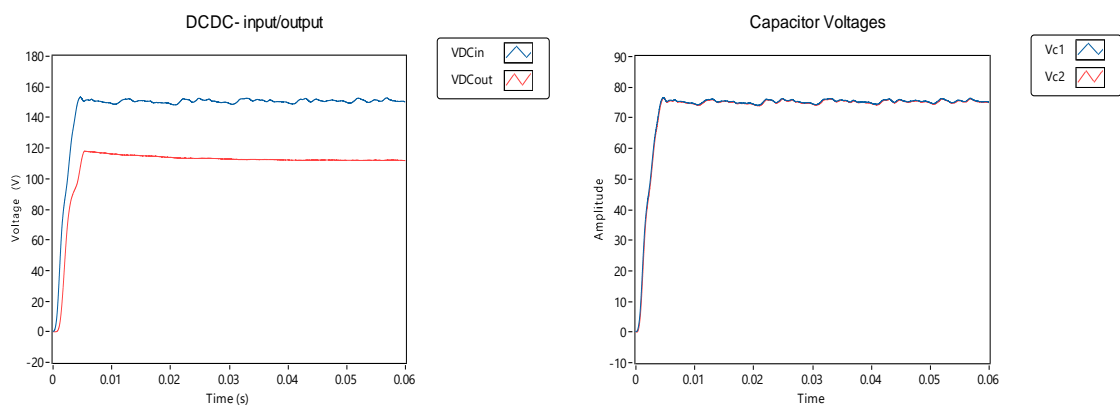


Figure 4.23 Charging Mode DC-DC converter input and output waveforms. On the right graph the DC link capacitor voltage.

levels as in the previous test but it stabilises in the same period of time. This is because the same duty cycle is used for both and the operating mode is in open loop. The simulation of the different battery voltages and the grid proved to be working without exceeding or going below the maximum and minimum voltages for the charging mode, in discharging mode with nominal battery voltage the output maximum voltage is exceeded when operating at fixed duty cycle. The next stage is to evaluate the system in closed loop of the DC-DC converter to regulate the output voltage in discharging mode.

#### 4.4.5 Closed loop evaluation

The results obtained after the evaluation in open loop of the integration of the DC-DC and MLC for the two cases, minimum battery voltage give an output within the permitted limits, however for the nominal battery voltage, the limit is exceeded then, the implementation of a PI controller in simulation results are presented in this section. In Figure 4.24 a block diagram of the system show the interconnection of the subsystems and the measurement of the voltage and current for the closed loop. For the DC-DC, the battery voltage and the DC- link voltage is measured to control the DC output and AC voltage level. In the MLC, the voltage of the capacitors, output voltage and current is measured to balance the capacitors and for the AC waveform generation. All the control and signal measurements are done in the FPGA, then the PWM signals are sent to the gate drivers in the converters.

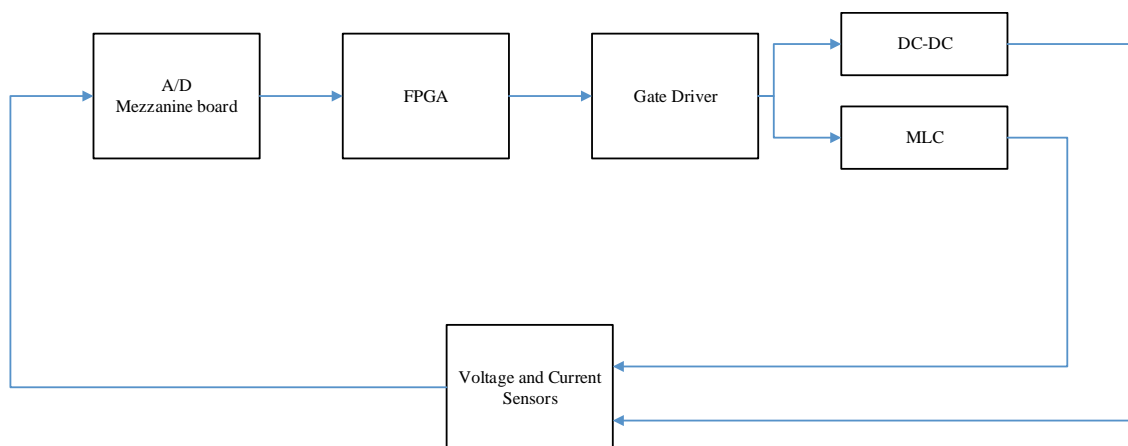


Figure 4.24 Control loop block diagram

The controller is used to regulate the output voltage at the DC-link assuming that there are minimal losses in the MLC it can set the voltage to regulate at the output of the DC-DC converter to be at 155V which corresponds to the peak voltage of the 110VAC. The

controller was manually tuned for this stage to prove that by regulating the DC-link voltage the output of the MLC can be controlled accordingly.

The results of the simulation are presented in Figure 4.25 and Figure 4.26 for an input voltage of 108V that corresponds to the minimum battery voltage DC-link and MLC output voltage respectively.

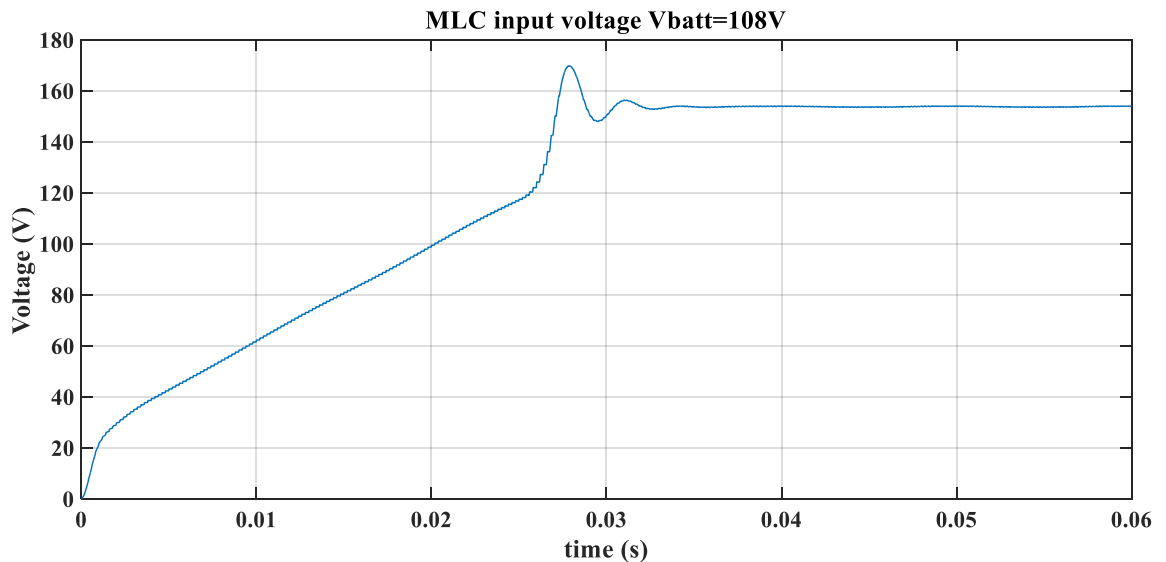


Figure 4.25 DC-link voltage in closed loop with  $V_{batt}=108V$

These figures show the voltage regulation to a set voltage of 155V, Figure 4.25 shows the regulation on the DC link voltage, and this is the output of the DC-DC converter and the MLC input.

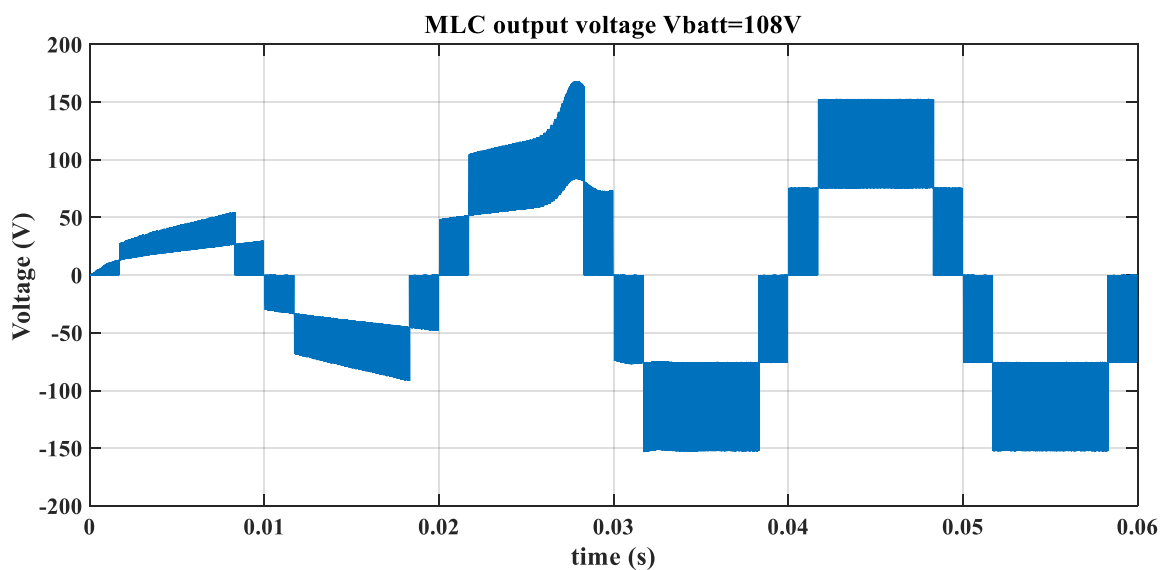


Figure 4.26 MLC output voltage in closed loop with input voltage  $V_{batt}=108V$

The evaluation results at nominal battery voltage, 144V are presented in Figure 4.27 showing the DC-link voltage and Figure 4.28 the MLC output voltage.

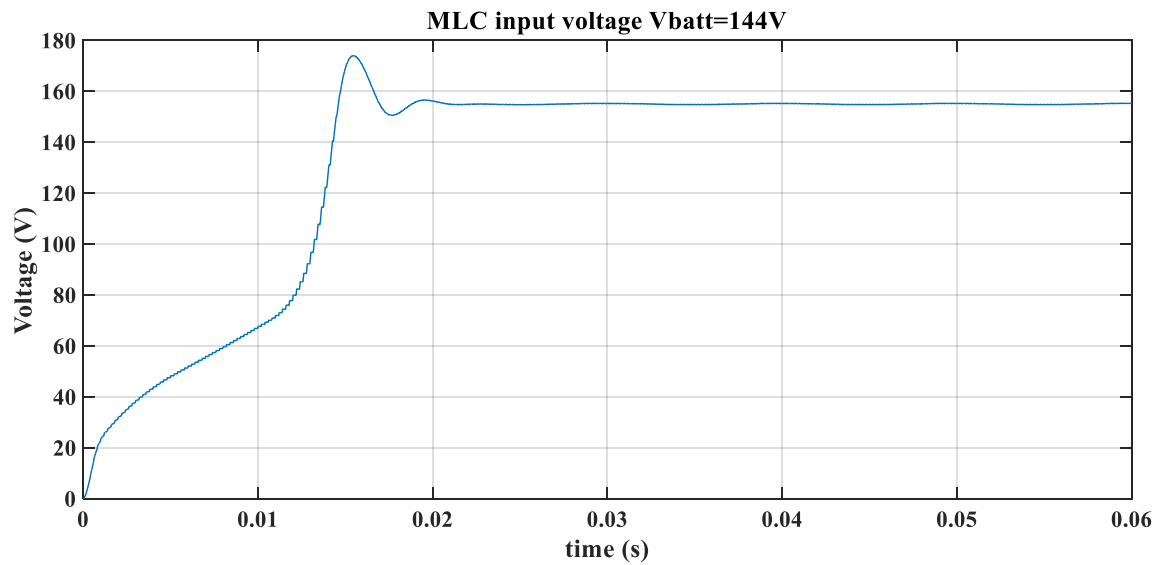


Figure 4.27 DC-link voltage in closed loop with  $V_{batt}=144V$

Figure 4.27 show the DC-link voltage, as in the previous case for the minimum battery voltage, this is the output of the DC-DC converter and the input of the MLC, the voltage reaches the set-point faster than the previous case due to the higher input voltage from the battery. Figure 4.28 presents the AC output of the MLC following the level of the DC-link voltage.

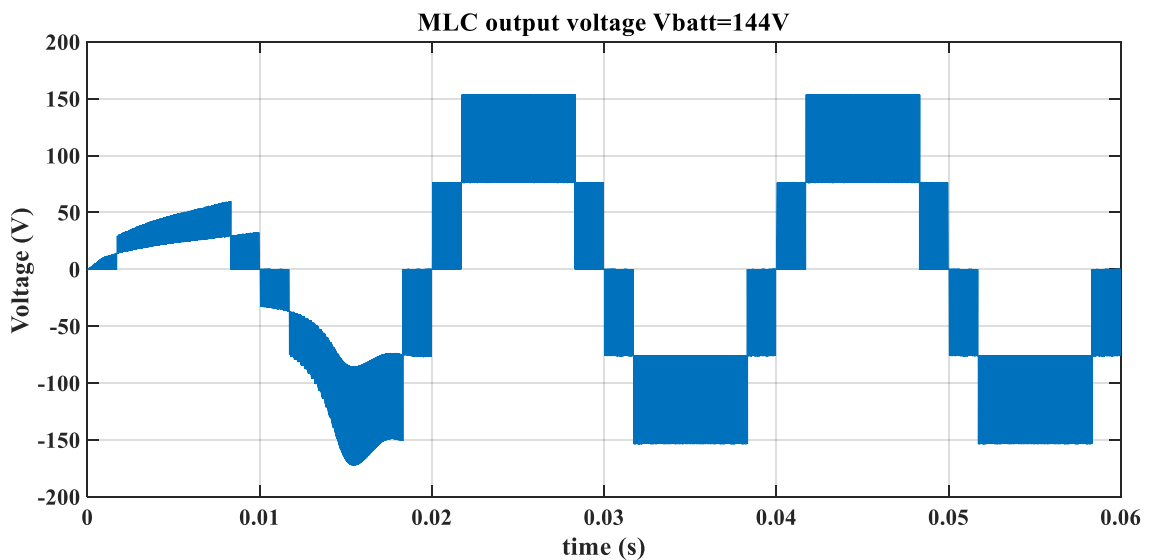


Figure 4.28 MLC output voltage in closed loop with input voltage  $V_{batt}=108V$

It can be seen from the results presented in this section that the controller implemented for the DC-DC converter can regulate the voltage at the output of the MLC at the specified set point. The settling time for both input voltages is between 25 ms and 35 ms, less than

one cycle of a 50 Hz MLC output voltage. The MLC can handle these transients but for the experimental evaluation an MLC turn on delay should be considered in order to protect the semiconductors from large  $dV/dt$ . The converter has been evaluated without output filter in this chapter, the output filtering is presented in Chapter 7 where the THD in MLC is studied.

#### 4.5 Chapter conclusion

This chapter presented the system's description detailing the applications of the MLC and battery as a battery charger, building site power supply and EV's battery second life. The description and design of the DC-DC converter and MLC is presented and the simulation results in isolation of the DC-DC and MLC. The integration of the converters is evaluated through simulation and the feasibility to use the proposed topologies in the intended application is evaluated. The following chapter will cover the experimental evaluation describing the technical requirements for the hardware construction including driving requirements and converter's characterisation.

#### 4.6 References

- [4-1] J. Lai and F. Z. Peng, "Multilevel Converters-A New Breed of Power Converters," *IEEE Trans. Ind. Appl.*, volume 32, no. 3, pp. 509–517, (1996).
- [4-2] D. C. Erb, O. C. Onar, and A. Khaligh, "An integrated bi-directional power electronic converter with multi-level AC-DC/DC-AC converter and non-inverted buck-boost converter for PHEVs with minimal grid level disruptions," in *2010 IEEE Vehicle Power and Propulsion Conference*, 2010, pp. 1–6.
- [4-3] I. Patrao, E. Figueres, F. González-Espín, and G. Garcerá, "Transformerless topologies for grid-connected single-phase photovoltaic inverters," *Renew. Sustain. Energy Rev.*, vol. 15, no. 7, pp. 3423–3431, Sep. 2011.
- [4-4] F. Caricchi, F. Crescimbeni, F. G. Capponi, and L. Solero, "Bi-Directional Buck-Boost Converter Topologies for Application in Electrical Vehicle Motor Drives 17.," in *APEC '98. Conference Proceedings 1998*, 1998, pp. 287–293.
- [4-5] M. Gonzalez Valencia and A. Alzate Gomez, "Diseño estático de un convertidor DC / DC reductor-elevador bidireccional," *Rev. Tecnura*, vol. 4, no. 26, pp. 7–14, 2009.
- [4-6] BS7671, British Standard. Requirements for Electrical Installations. *IEE Wiring Regulations*, 2008.

- [4-7] J. Rodriguez, S. Bernet, P. K. Steimer, and I. E. Lizama, "A Survey on Neutral-Point-Clamped Inverters," *IEEE Transactions on Industrial Electronics*, volume 57, no. 7, pp. 2219–2230, (2010).
- [4-8] J. I. Leon, R. Portillo, L. G. Franquelo, S. Vazquez, J. M. Carrasco, and E. Dominguez, "New Space Vector Modulation Technique for Single-Phase Multilevel Converters", *IEEE Int. Symp. Ind. Electron.*, pp. 617–622, (2007).
- [4-9] S. Burusteta, J. Pou, S. Ceballos, I. Marino and J. Á Alzola, "Capacitor voltage balance limits in a multilevel-converter-based energy storage system," *Power Electronics and Applications (EPE 2011), Proceedings of the 2011-14th European Conference on*, Birmingham, 2011, pp. 1-9.

## Chapter 5 – System experimental evaluation

### 5.1 – Introduction

Following on from the simulation presented in Chapter 4, this chapter describes prototype converter used during the course of the research and its control platform including the grid synchronisation using a phase-locked loop (PLL). The basic operating concepts of bidirectional converter are described alongside experimental results. Throughout the work, LabVIEW was used as a co-simulation development system to expedite the design by allowing the FPGA based control system to be developed within a simulation environment before hardware testing, and then downloaded onto the hardware platform once it performed satisfactorily.

The control of the DC-DC and MLC converters can be implemented by using a microcontroller, Digital Signal Processor (DSP), Field Programmable Gate Array (FPGA) or a combination of them. The FPGA option enables the parallel execution of methods by assigning dedicated hardware in an integrated circuit, the paralleling facilitates the control response to be faster. Nowadays, graphical programming languages such as LabVIEW greatly simplify the programming of an FPGA, which is usually programmed in VHSIC Hardware Description Language (VHDL), by creating a seamless translation of LabVIEW code directly to the FPGA. Moreover, it allows the use of FPGA to implement more elaborated and time critical calculations, and so enhances its usage.

The system hardware platform is introduced in this chapter, it will be used as a base system to test different control schemes and execution methods in the FPGA. Then based on the obtained results, the advantages and disadvantages are evaluated. Furthermore, the platform is sufficiently versatile to permit the evaluation of different power switches using emerging technologies for the fabrication of the MOSFETs, such as SiC and GaN. Once the results of the tests are obtained, comparisons can be made with Si components highlighting the adaptations required and possible novel modulation techniques for the control and the advantages or disadvantages of using emerging semiconductor technologies.

An extended work to the base test platform introduced here is the interconnection with the grid, to aid with demand side management of power on the grid. A description of the characteristics benefits and future trends is presented in [5-1] [5-2]. A review of on board

chargers used in EVs [5-3] presents an evaluation of the different topologies, such as full bridge, half bridge in diode clamped, capacitor clamped and the integration with the DC-DC converter.

Finally, an integration with other systems, for example energy billing and state of charge of the battery is more easily enabled through the LabVIEW interface.

## 5.2 – FPGA control platform

An FPGA is a reconfigurable integrated circuit, where the hardware configuration is defined after the fabrication of the device. This gives a unique characteristic over the Application Specific Integrated Circuits (ASICs) of being able to configure the hardware according to the application, while the ASIC is limited to the resources and functions determined by the designer during fabrication. The FPGA can be adapted to the specific task in hardware by assigning and configuring the internal gates, this gives the real parallelism when executing a function as the resources are configured and not divided as it happens in ASIC [5-4].

An FPGA is composed of Logic Blocks (LBs) positioned in a matrix, programmable routing to interconnect the different blocks, and an Input / Output interface. The use of the LBs can be to form a simple logic gate, or an elaborated arithmetic function. Flip-flops and Look-Up Tables (LUTs) along with LBs make for a truly versatile computing engine and as a result they can be found in a wide variety of applications ranging from set-top boxes to power electronic converters.

Depending on the manufacturer the characteristics vary, but for this work a National Instruments (NI) Single-Board RIO is used. The NI 9606 board has a 400MHz processor with 512 MB of non-volatile storage and 256 MB of DRAM. The FPGA is a Xilinx Spartan-6 LX45. A mezzanine I/O board NI 9683 provides the half bridge digital outputs and the fast simultaneous capture of analogue inputs.

The NI FPGA system is programmed with LabVIEW using the FPGA application and a VI file created in LabVIEW, which offer provision for the interconnection of LBs, or LUTs as required. The NI system has a number of useful built- in functions including PID control, waveform generators, and signal processing blocks to implement FFTs. Interactive communication is provided between a Real-Time target and a host computer to visualize and process the data. The advantage of using a high-level graphical



programming environment such as LabVIEW is that the program can be transferred to other NI solutions with minimal changes and the compiler will optimize and create the intermediate files and bitfile to download to the FPGA in a single step.

Multisim, National Instruments' circuit simulation tool, can interact to test the code to be implemented in the FPGA connected to the physical elements in a circuit using Co-simulation. This enables the simulation of the complete system and so one can evaluate the different operating conditions such as input voltage and load variations, together with the simulation of perturbations to the system or different responses of the system to a given input or condition.

The literature contains a number of documented investigations on the use of FPGA to control MLC, most of the work presented is on SPWM [5-5], 3-phase with SVM modulation NPC [5-6], and multi-phase cascaded converter [5-7], the programming used on the previous investigations is done in VHDL. A few publications using the LabVIEW FPGA [5-8] [5-9] [5-10] were also found. The study presented in [5-8] is on a 3-phase conventional (2-level) converter, simulation results showing a fast and accurate control. In [5-9] a 7-level cascaded H-bridge for an application on wind energy conversion uses a multi-carrier phase-shifted PWM showing simulation and practical results that proved to be simple to implement with LabVIEW's graphic interface. Finally, in [5-10] a hybrid MLC based on H-bridge topology presented both simulation and experimental results with a reduction in the execution speed using the FPGA.

### 5.2.1 FPGA implementation.

A systematic design and validation process was used to ensure consistency with Multisim and LabVIEW FPGA Co-simulation environment introduced in the previous chapter (4). The PWM pulses for each switch (S1, S11, S2, S21, S3, S31, S4, and S41) in Figure 5.1 to generate the 5-level is presented in this section in both Co-Simulation and experimental.

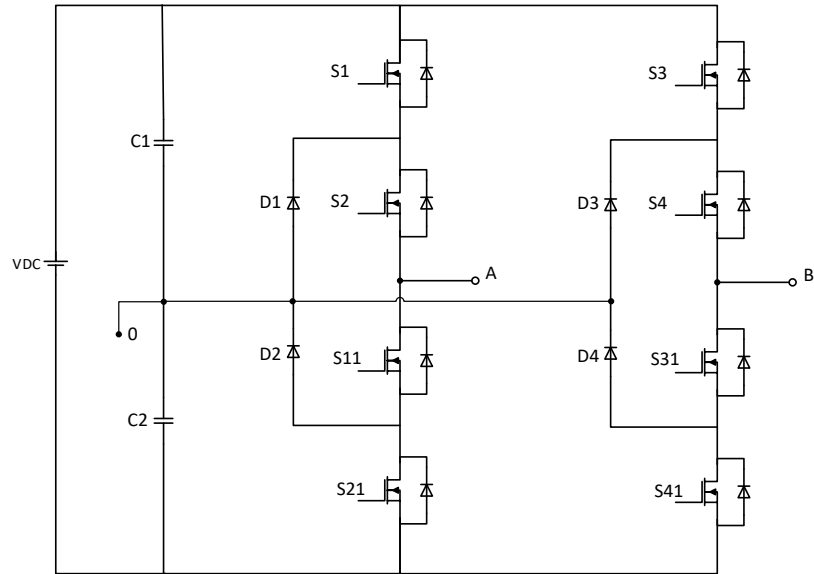


Figure 5.1 5-level NPC converter in full bridge topology.

Co-simulation and practical results of the pulse generation on the FPGA for the MLC are shown in Figure 5.2 and Figure 5.3, representing the pulses applied to the MOSFET gates of S1 and S3 to generate the levels  $\pm V_{dc}/2$  and  $\pm V_{dc}$ .

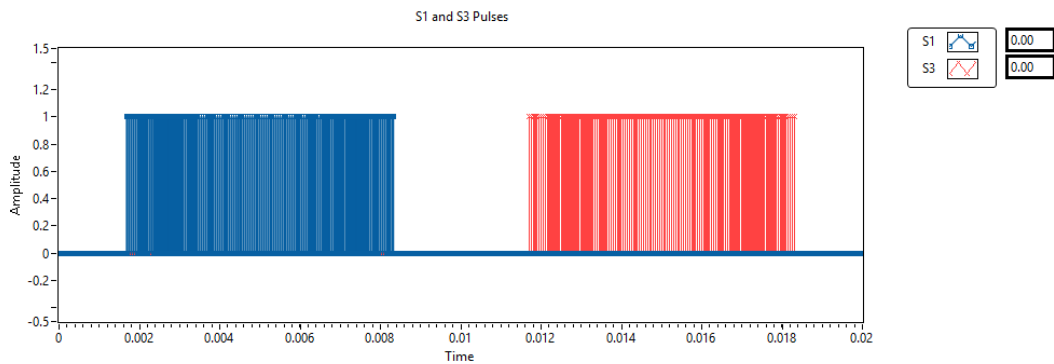


Figure 5.2 S1 and S3 pulses Co-Simulation output.

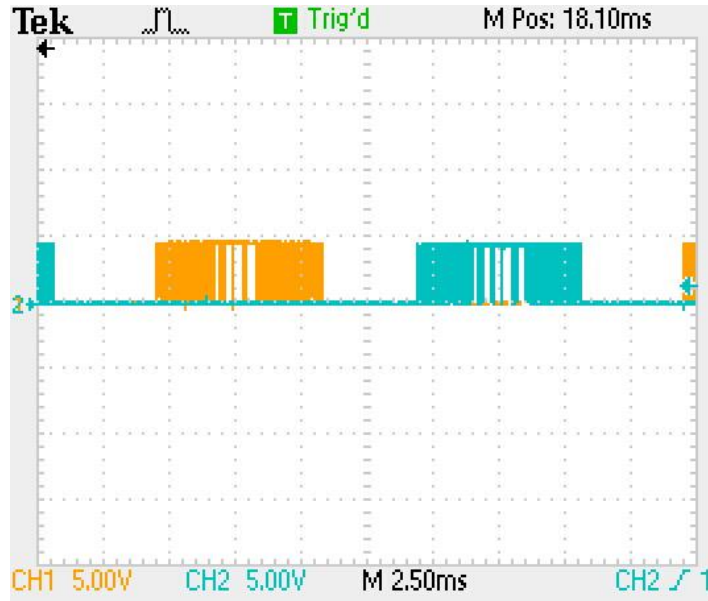


Figure 5.3. S1 and S3 Digital Output FPGA.

The complements of the pulses shown above are shown in Figure 5.4 and Figure 5.5.

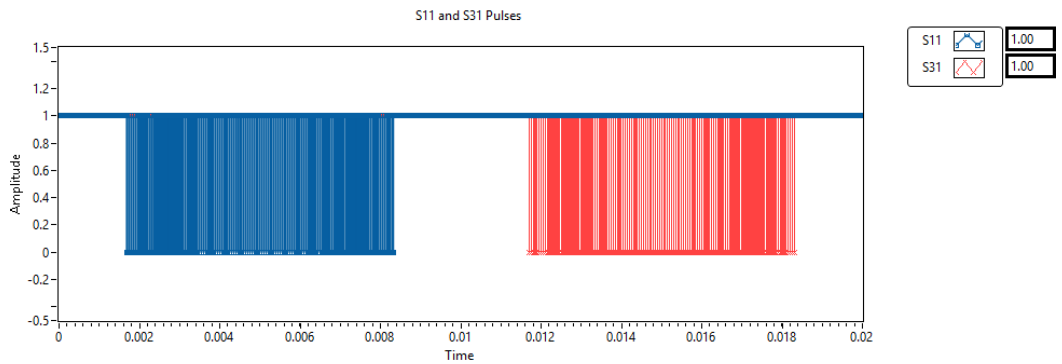


Figure 5.4 S11 and S31 pulses Co-Simulation output.

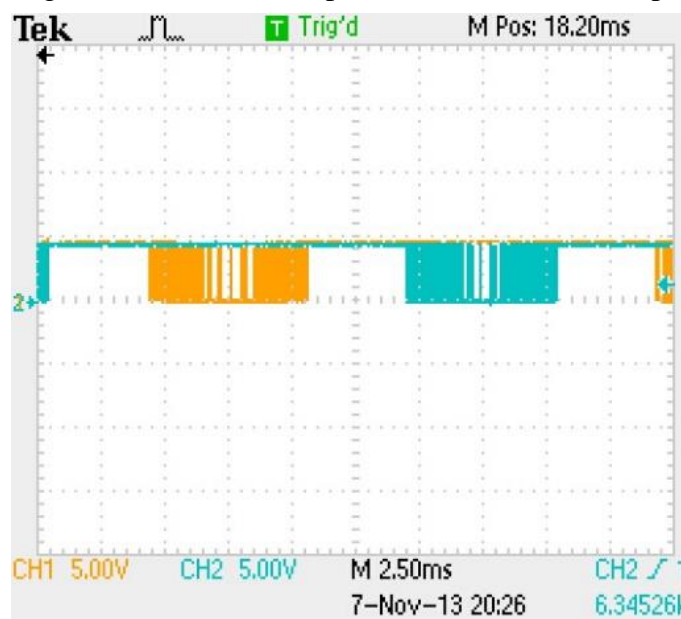


Figure 5.5. S11 and S31 Digital Output FPGA.

The pulses to generate the levels 0 and  $\pm V_{dc}/2$  are shown in Figure 5.6 and Figure 5.7.

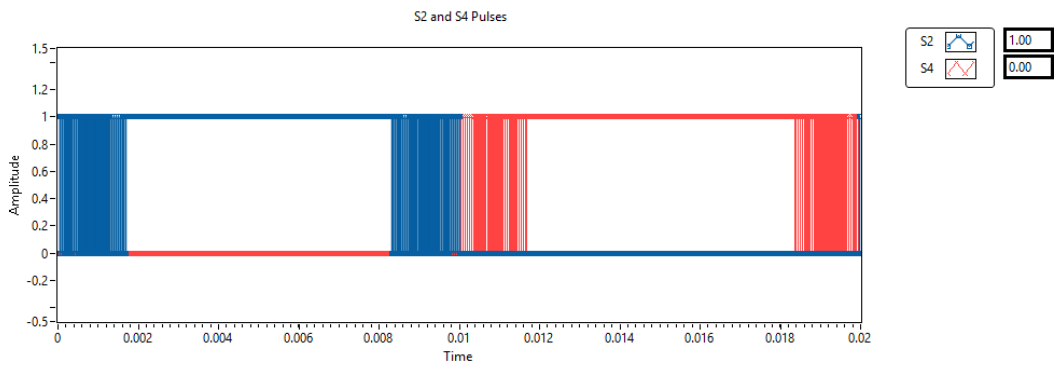


Figure 5.6 S2 and S4 pulses Co-Simulation output.

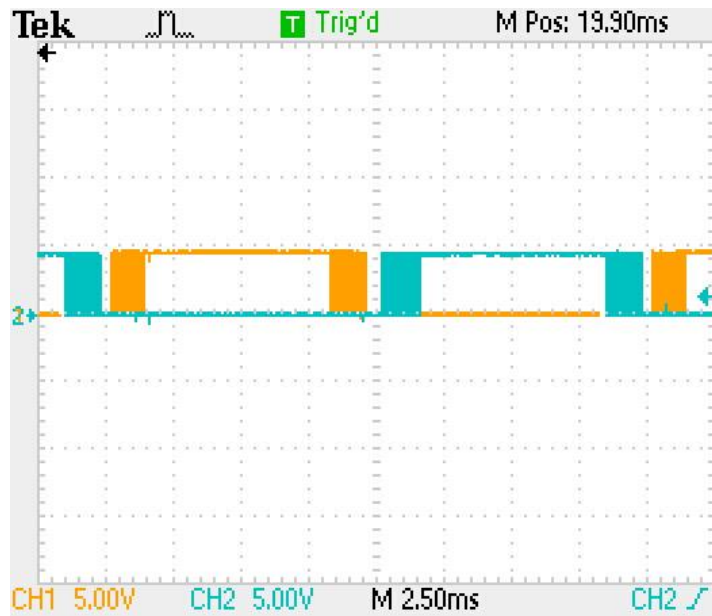


Figure 5.7 S2(CH1) and S4(CH2) Digital Output FPGA.

In Figure 5.8 and Figure 5.9 the pulses generated for the complement of the switches described above are shown.

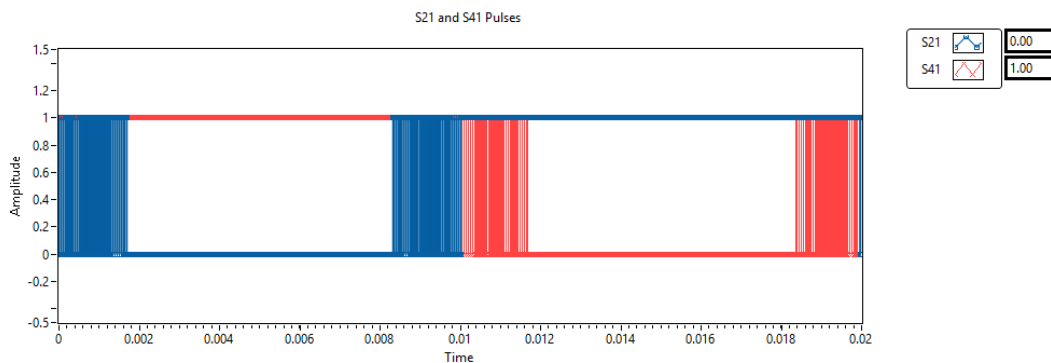


Figure 5.8 S21 and S41 pulses Co-Simulation output.

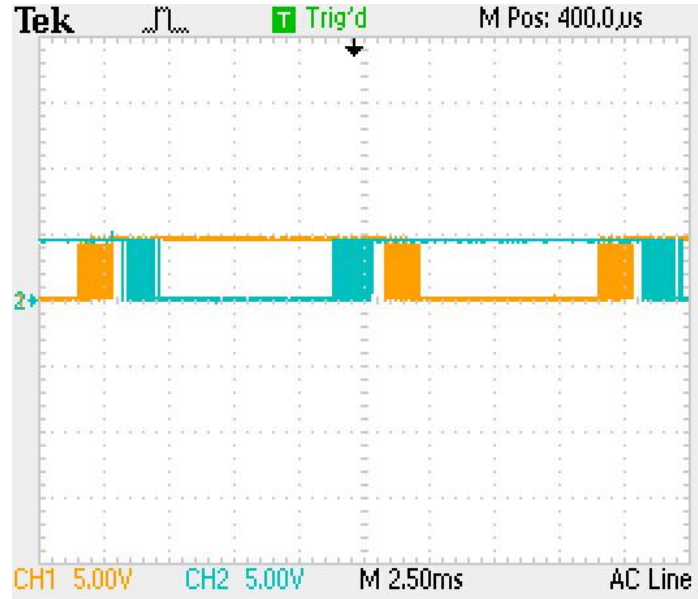


Figure 5.9 S21(CH1) and S41(CH2) Digital Output FPGA.

Having proven the operation of the FPGA and comparing the co-simulation and experimental results, the experimental waveform's voltage level is from 0-5V as this is the output obtained from the digital output, for switches S1 and S3 and its respective complement waveforms, some of the pulses when the duty cycle approaches zero doesn't appear in the experimental waveforms due to the added dead time. No dead time was considered for this initial testing as no MOSFETs were switching at this stage, only the pulse generation was validated in this section. The remainder of this section describes the design of the prototype platform

### 5.3 Gate driver circuit design

In order to drive the MOSFETs presented in Chapter 4 for the MLC and the DC-DC converters, in this section the gate driver circuit design is presented. The current required to turn on the gate is calculated using 2 parameters, the total gate charge and the transition time.

$$I_G = \frac{Q_{G(total)}}{t_{transition}} \quad (5.1)$$

$$I_G = \frac{54nC}{25ns} = 2.16A \quad (5.2)$$

According to the current obtained, the maximum peak current of the gate driver should be greater than 2.16A. FOD3120 gate drive IC has a maximum peak current of 3A.

Equation (5.3) is used to calculate the minimum resistance to obtain the required current to drive the MOSFET.

$$R_G = \frac{20V}{2.16} = 9.25\Omega \quad (5.3)$$

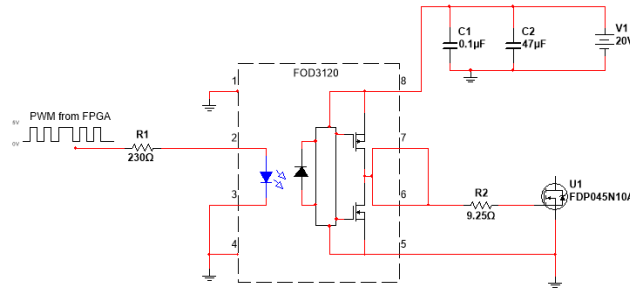


Figure 5.10 Gate Driver Circuit interface with MOSFET.

The circuit diagram shown in Figure 5.10 shows the gate driver for each MOSFET used in the converters, the output voltage from the FPGA is 0 and 5V for the low and high levels respectively. The power supply on each gate driver is isolated and the gate resistor value is the closest available to the calculated above which is 10  $\Omega$ . The MOSFET FDP04N10A rated 100V and 164A was selected as it is the closest to the voltage specification available through the university suppliers featuring low  $R_{DS\ on}$  of 4.5m $\Omega$ .

#### 5.4 Isolated voltage and current input and output

To implement the control, feedback needs to be employed, hence to close the loop of the converters, the voltage and current readings of the output are required. Along with the gate driver circuits, the voltage and current measurement circuits have to be isolated to protect the FPGA from the high voltage in the converter. The voltage and current reading circuits are presented in this section.

### 5.4.1 Isolated voltage transducer.

The voltage transducer (LV 25-P) uses the Hall Effect to operate which gives electromagnetic isolation and can be used in measurements from 10 to 500V. The design of the components of the voltage reading circuit shown in Figure 5.11 is presented in this section.

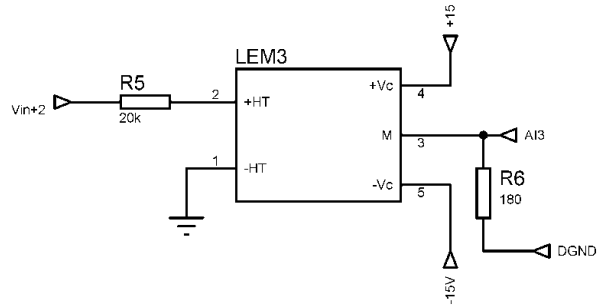


Figure 5.11 Voltage transducer circuit.

The voltage should be passed through a resistor R5 calculated to give a 10mA in the primary of the transducer.

In this case the maximum voltage to be read is 200V.

$$R_5 = \frac{200V}{10mA} \quad (5.14)$$

$$R_5 = 20 \text{ k}\Omega \quad (5.15)$$

Then the transducer output voltage is obtained from output terminal M, measured across resistor R6. The maximum voltage in the output of the amplifier is given by

$$V = (R_S + R_M) * I_S \quad (5.16)$$

$$V = (110\Omega + 180\Omega) * 25mA \quad (5.17)$$

$$V = 7.25V \quad (5.18)$$

Where  $R_S$  is  $110\Omega$  and  $I_S$   $25mA$ . The value of  $R_M$  can be of any value between  $100$  and  $190\Omega$ .

#### Characterisation

The characterisation of the transducer was carried out measuring voltages from 0 to 200V in steps of 5V, the characteristic curve is shown in Figure 5.12. The trend curve provided the gain applied to the code in LabVIEW to calibrate the readings.

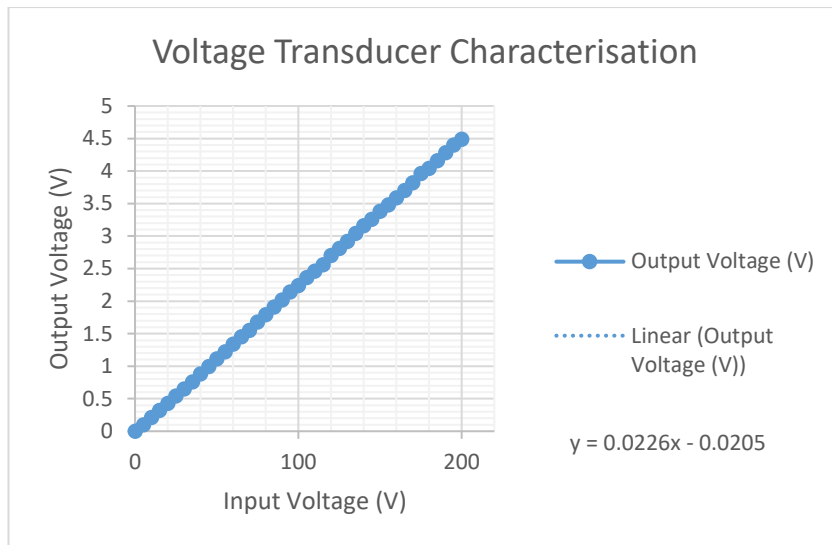


Figure 5.12 Voltage transducer characteristic curve.

As specified by the manufacturer, the voltage reading is more accurate for high voltages, for the application in the converter this does not represent a problem. The calibration factors are shown on the right hand side of Figure 5.12.

#### 5.4.2 Isolated current transducer.

The current transducer HX 10NP, like the voltage transducer, relies on the Hall Effect. This transducer is capable to read up to  $\pm 10A$  rms. It outputs a voltage from 0 to 4V. The current transducer circuit is shown in Figure 5.13.

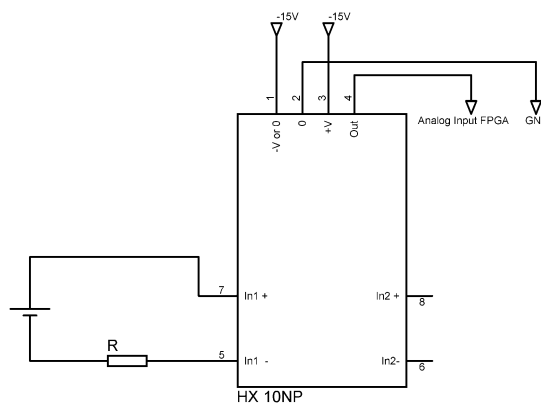


Figure 5.13 Current transducer circuit.

### Characterisation



The characterisation of the current transducer was done by varying a current from 0 to 15 A in steps of 0.5A. The output of the transducer was measured using a multimeter and an oscilloscope, the characteristic curve is shown in Figure 5.14 with the calibration factors are shown on the right hand side of the figure.

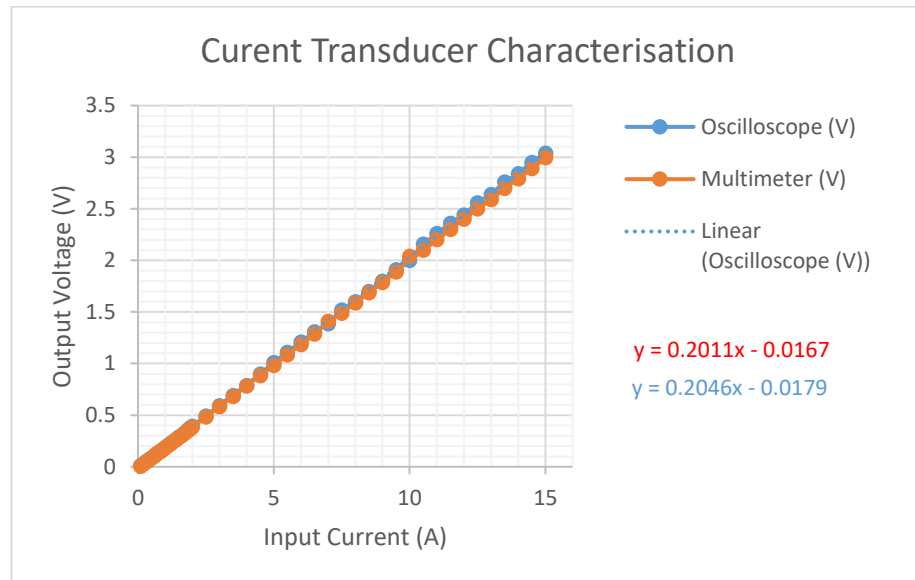


Figure 5.14 Current transducer characteristic curve

The characterization of the current transducer gives important information about the gain of the sensor to then process its signal and adapt it in the controller.

In order to implement closed loop control of both converters, current and voltage transducers circuits were selected and employed to interface with the FPGA. The initial tests of the converters were carried out using Silicon (Si) MOSFETs and the appropriate gate drivers, and the next stage is the test with SiC and GaN components as detailed in the subsequent chapters.

### 5.5 DC-DC converter evaluation

The first stage of the multilevel converter is the DC-DC converter shown in Figure 5.15 to step up (boost) the voltage from the battery to a DC voltage at a sufficient level to support the required output voltage in the Multilevel Converter of 110 VAC rms, and to also step down (buck) the voltage to charge the battery when operating in a grid to battery charging mode.

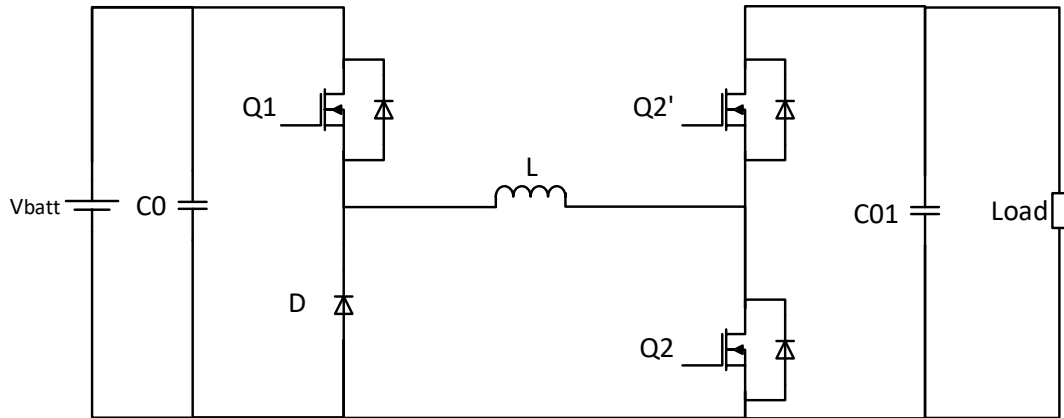


Figure 5.15 Bidirectional DC-DC converter

This section provides experimental validation of prototype platform when operating under specific conditions. The DC-DC converter prototype is shown in Figure 5.16

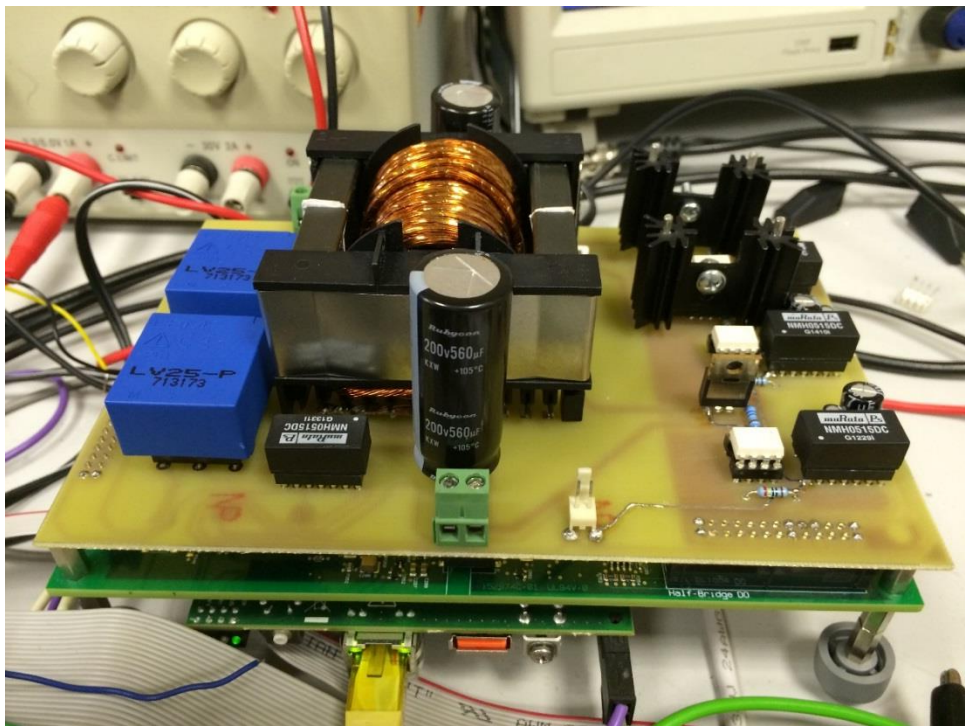


Figure 5.16. DC-DC converter PCB and FPGA.

### 5.5.1 Inductor

In order to fit the inductor in an ETD core, the switching frequency of the converter was set to 50 kHz and the value for the inductor was determined to be 0.4mH.

For the switching frequency of 50 kHz, 3C90 ferrite material was selected as it can be used in frequencies below 200 kHz. From the  $I^2L$  table in the Ferroxcube Data Handbook the appropriate core to use is ETD59 with an effective area ( $A_e$ ) of 368 mm<sup>2</sup>

Considering a maximum saturation  $B_s$  of 300mT. The minimum number of turns is calculated from (5.4) for an inductor (L) of 0.4mH and an output current of 13A.

$$N_{min} = \frac{L \cdot I_o}{B_{max} \cdot A_e} \quad (5.4)$$

$$N_{min} = \frac{0.4mH \cdot 13}{300mT \cdot 368mm^2} = 47.10 \approx 47 \text{ turns} \quad (5.5)$$

For the number of turns, the air gap length is calculated using (5.6)

$$l_g = \frac{N^2 \cdot \mu_0 \cdot A_e}{L} \quad (5.6)$$

$$l_g = \frac{47^2 \cdot 4\pi \times 10^{-7} \cdot 368mm^2}{0.4mH} = 2.55mm \quad (5.7)$$

The area of the conductor required is given by (5.8)

$$A_{Cu} = \frac{k_{Cu} \cdot A_w}{N_{min}} \quad (5.8)$$

$$A_{Cu} = \frac{0.6 \cdot 368mm^2}{47} = 4.69mm^2 \quad (5.9)$$

Where  $K_{Cu}=0.6$  is the packing factor for the winding

The diameter of the conductor is therefore 2.44mm

#### *Skin Depth*

For the frequency of 50 kHz the skin depth of a copper wire at 70°C is 0.34 mm, and the area of the wire that can be used at that frequency is 0.36mm<sup>2</sup>. Thus, a cable with at least 13 twisted wires of 0.68 mm in diameter can be used.

#### 5.5.2 DC-DC converter testing

The test results of the DC-DC converter at full voltage in boost and buck modes are presented in this section.

### 5.5.2.1 Boost Mode Test

Under battery operation the DC-DC converter should provide the 5 level DC to AC converter with an adequate DC link voltage. The specification for construction site power supply voltage is 110 VAC (+10%, -6%). To step up the battery voltage, the boost mode of the converter is used, the circuit is shown in Figure 5.17

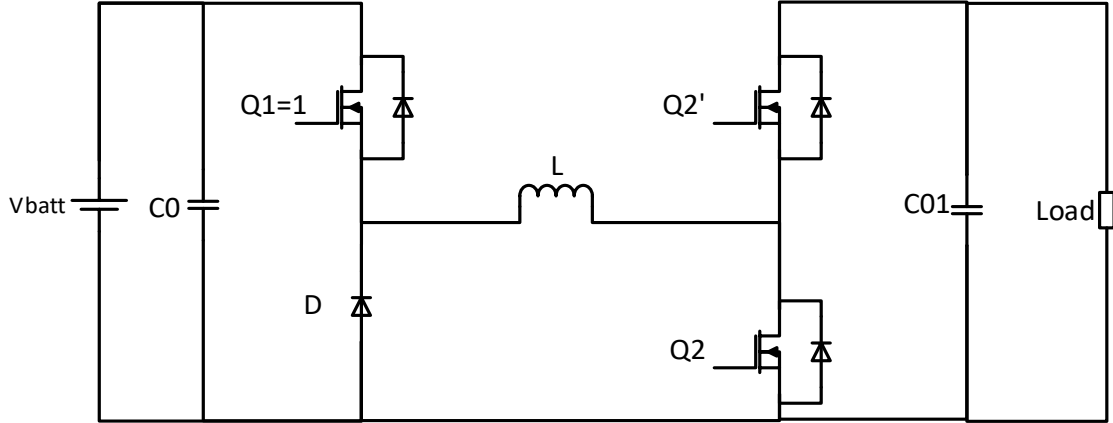


Figure 5.17 Boost mode test circuit

The maximum and minimum battery voltage is 170V and 108V respectively. The test specifications and conditions for the boost mode are detailed in Table 5.1.

$V_{batt \min}$	108V
$V_{batt \text{ nom}}$	144V
$V_{batt \text{ max}}$	170V
$R_{load}$	130 $\Omega$
frequency	50 kHz

Table 5.1 Test conditions

Output voltage required is 155.56V<sub>peak</sub> (+10%, -6%); (170.1V, 146.22V).

*Test at minimum battery voltage.*

$$V_{out \min} = 146.22V$$

$$I_{out \min} = 1.32A$$

$$efficiency = \frac{P_{out}}{P_{in}} = \frac{146.22V * 1.32A}{108V * 1.8A} = \frac{193.01W}{194.4W} = 99.28\%$$

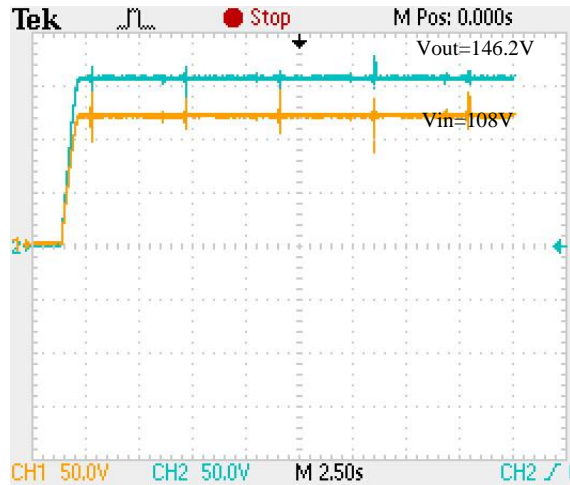


Figure 5.18 Input and output voltages in boost mode with minimum battery voltage.

The waveform in Figure 5.18 and Figure 5.19 show the input and output voltages measured with the oscilloscope.

*Test at maximum battery voltage.*

$$V_{out \max} = 169.4V$$

$$I_{out \max} = 1.54A$$

$$efficiency = \frac{P_{out}}{P_{in}} = \frac{169.4V * 1.54A}{144V * 1.85A} = \frac{260.87W}{266.4W} = 97.92\%$$

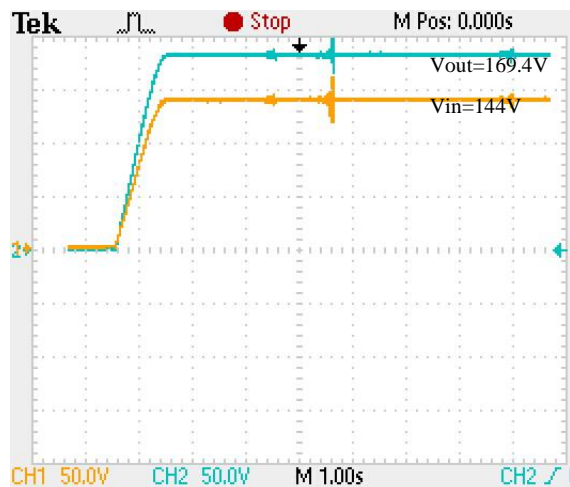


Figure 5.19 Input and output voltages in boost mode with maximum battery voltage.

The output voltage complies with the specification in boost mode for both minimum and maximum voltages described in previous sections.

### 5.5.2.2 Buck Mode Test

To charge the battery from a site transformer, the DC-DC needs to be operating in buck mode to step down the voltage to ~120V for battery charging. The circuit in buck mode is shown in Figure 5.20. The results of the test in buck mode are shown below.

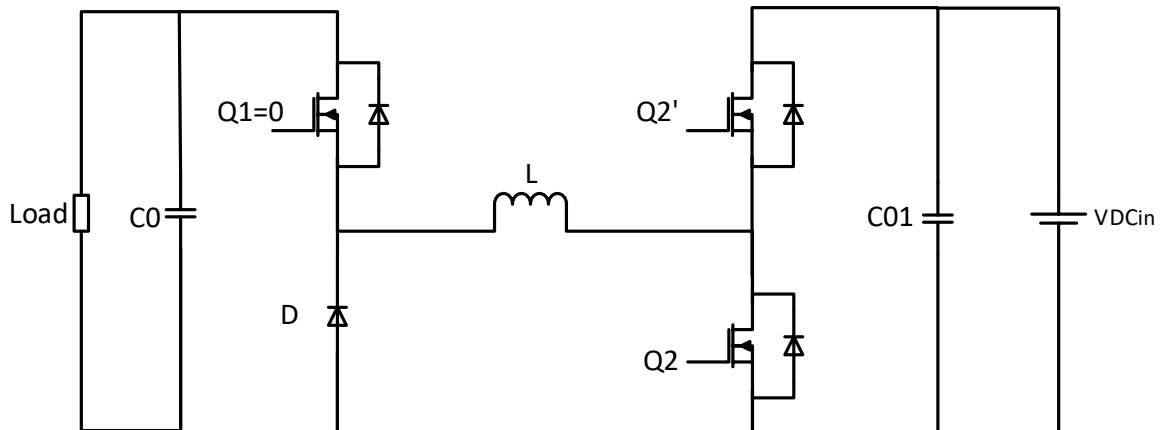


Figure 5.20 Buck mode test circuit

The specifications of the test in buck mode are described in Table 5.2

$V_{DCin}$	155.5 V
$V_{out\ min}$	108 V
$R_{load}$	100 $\Omega$
$I_{out}$	1.2 A

Table 5.2 Specifications buck mode

$$efficiency = \frac{P_{out}}{P_{in}} = \frac{108V * 1.3A}{155V * 0.95A} = \frac{144W}{147.9W} = 97.36\%$$

In Figure 5.21 the input and output voltages waveforms are shown as measured in the oscilloscope for the buck mode test.

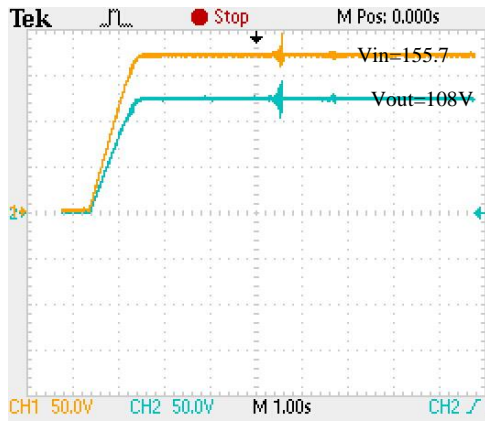


Figure 5.21 Input and output voltages in buck mode.

The full voltage test in open loop of the DC-DC converter proves that the system work within the limits established by the tolerances specified by the UK regulations. However, a full current and low voltage test has to be done before connecting the system to the battery to evaluate the performance of the system.

### 5.6 Multilevel converter testing

This section describes the evaluation testing performed on the 5L-FB-NPC, shown in Figure 5.22. The results presented here are for Phase A, one leg of the full-bridge, Figure 5.23, with the input voltage set at 100V. A resistive load ( $R=200\Omega$ ) connected to the terminals A and GND. The figures shown below correspond to the models in NI Multisim used to evaluate the control algorithm described in Chapter 3 in LabVIEW.

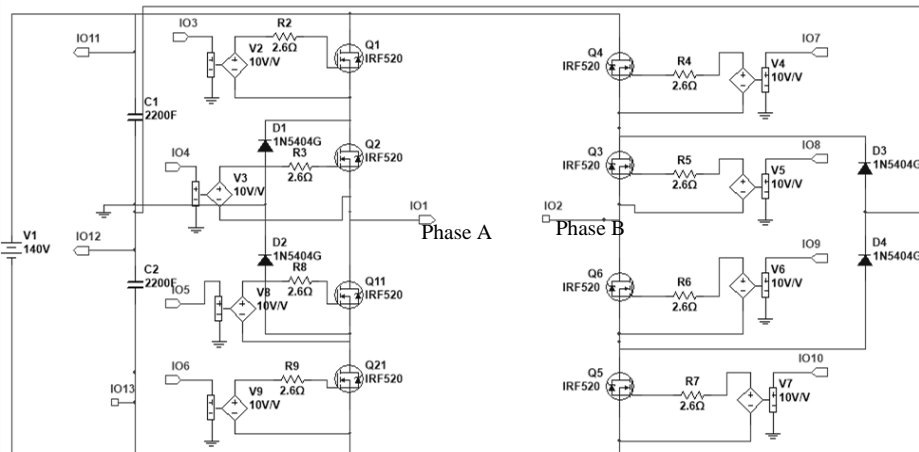


Figure 5.22. 5-level diode clamped full bridge converter.

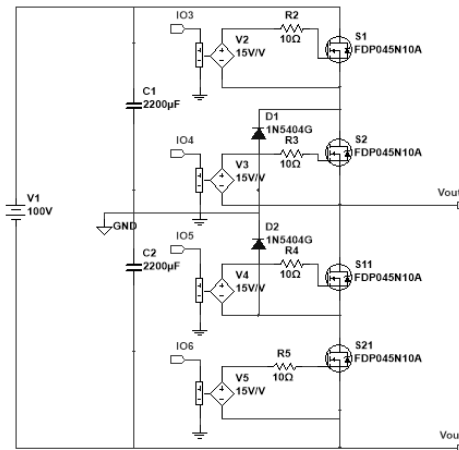


Figure 5.23 Phase A (3-level) converter circuit.

The simulation results and the tested waveforms are shown in Figure 5.24 and Figure 5.25 respectively.

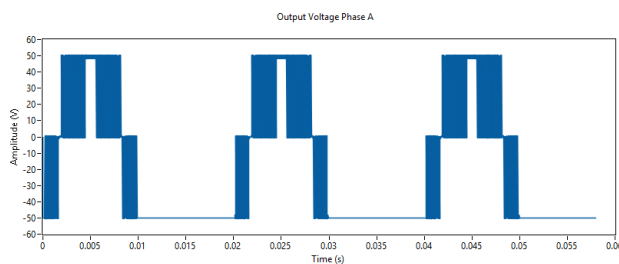


Figure 5.24 Output voltage of phase A, Co-simulation.

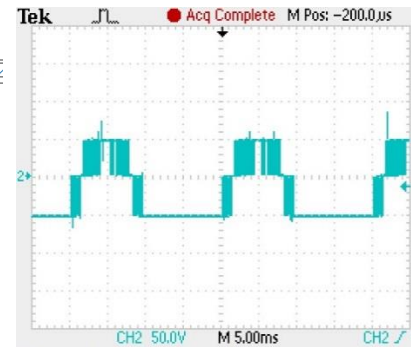


Figure 5.25 Phase A output voltage tested.

The prototype performs as expected with the output voltage taking on the 3-level (-50V, 0V and 50V) waveform. The output filter will eliminate the high frequency components and the output voltage waveform will approximate a sinusoid.

### 5.6.1 Multilevel converter full bridge operation and capacitor voltage balancing

The experimental operation of the full bridge converter compared with the simulation results are presented in this section. Here, the result is shown with 50V input voltage and load 200Ω. The output voltage obtained and measured with the oscilloscope is shown in Figure 5.27 and compared with the simulation result in Figure 5.26. Good agreement



between the results can be seen although experiment waveform does show some deviations which includes noise, again, this will be cleared up by the output filter.

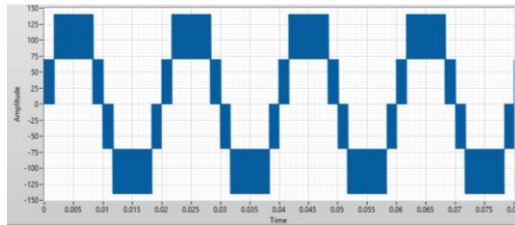


Figure 5.26 Co-simulation front panel output voltage and output voltages per phase.

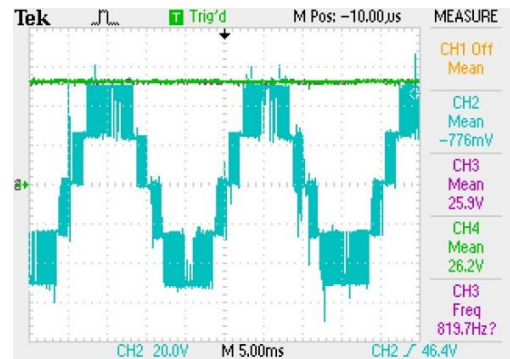


Figure 5.27. 5-level converter output test at 50V input.

The voltage on the DC-link capacitors was also monitored so the performance of the voltage balancing algorithm can be observed during a start-up transient, Figure 5.28. As can be seen the voltages are well balanced from the start-up and responding as well as to changes in the load current step change from 1 to 1.5A

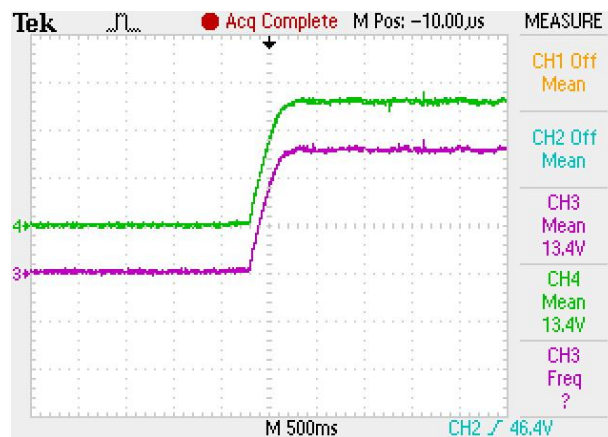


Figure 5.28 DC-link capacitor voltage balanced.

### 5.6.2 Full-bridge 5-level converter operation

In this section, the practical evaluation of the integrated converters, DC-DC and MLC is presented. The circuit diagram used is shown in Figure 5.29

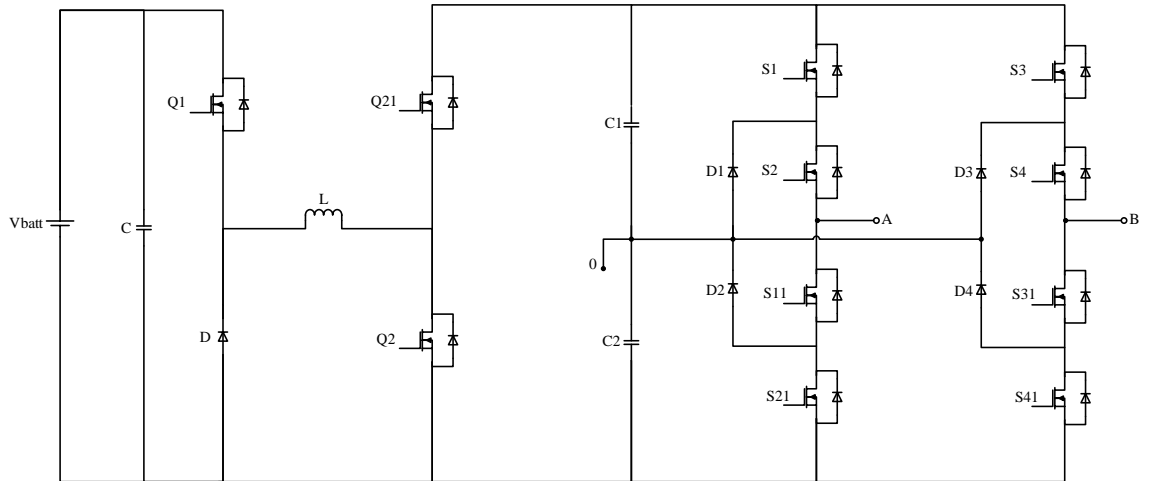


Figure 5.29 DC-DC and MLC integrated

The output voltage waveforms before filtering and filtered are shown in Figure 5.30 and Figure 5.31 respectively. This is using the same dead time for all MOSFETs in the MLC. The input voltage is 120V DC and both converters, DC-DC and MLC, are operated in closed loop.

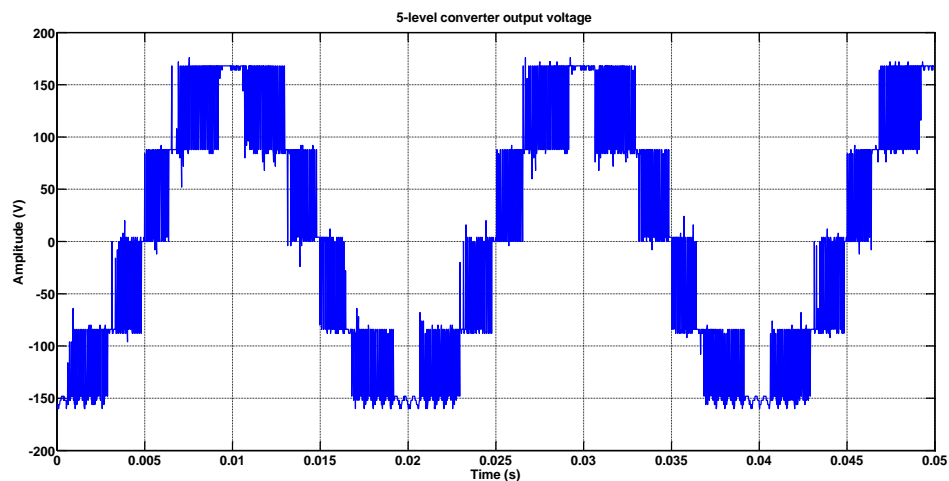


Figure 5.30 5-level output voltage before filtering

The output filter is based on a low pass LCL filter with cut-off frequency of 5 kHz. The filtered waveform is shown here to demonstrate the sinusoidal waveform obtained when testing the MLC in full voltage. The output filter is only required when the converter interfaces with the grid. Further detail of the filter added is presented in Chapter 7 where the power quality of the voltage generated by the MLC is analysed.

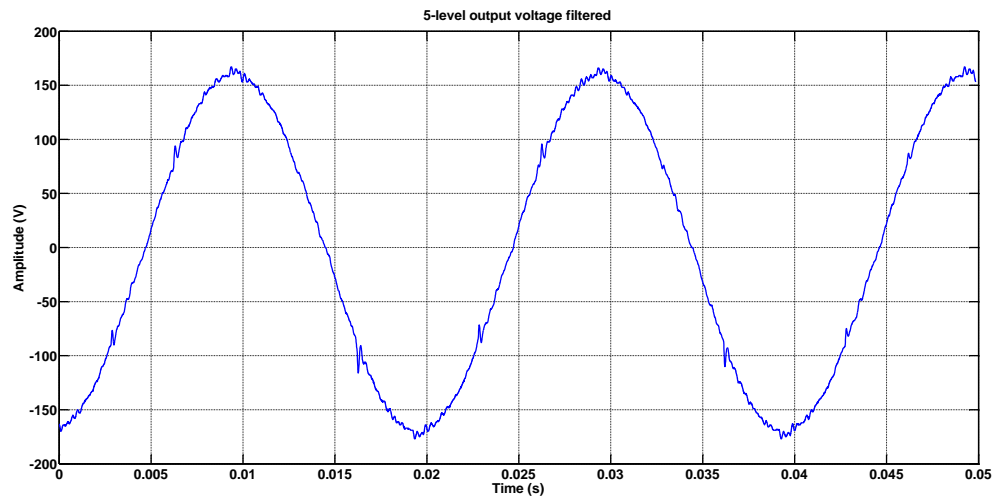


Figure 5.31 5-level output voltage filtered

More improvements to the control can be done by adjusting the dead time for each switch and using the filtered output current signal for the feedback.

Further investigation on reduction of dead time and other parameters in the control of the converters is presented in the following chapters

### 5.6.3 Transformer

A transformer was required to operate the whole converter system from the 230VAC mains. This transformer provided two functions, namely safety isolation and stepping down of the mains voltage to 110VAC expected on construction sites. Figure 5.32 shows a block diagram of the whole test system.

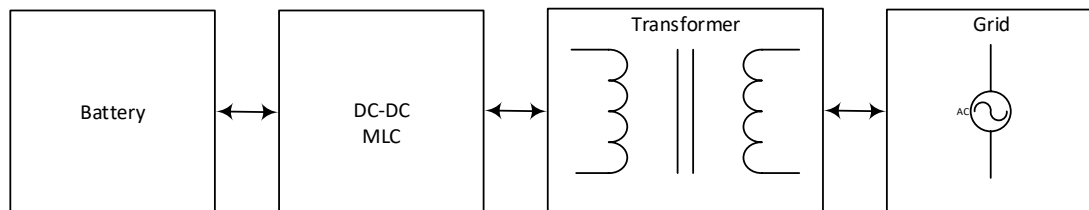


Figure 5.32 Block diagram of the grid interface.

### 5.7 Phase locked loop with grid

To implement the interface with the grid, the reference signal used to form the 5-levels in the DC-AC converter should be in phase with the mains and operating at the same frequency. The synchronisation of the single phase converter with the mains frequency and phase was implemented in LabVIEW FPGA with a phase locked loop (PLL). The

output of the PLL will therefore be used to generate the AC voltage at the correct phase and frequency.

### 5.7.1 PLL to generate reference signal for MLC

The reference signal in the MLC has to be synchronised with the mains to test the charging mode of the converter. First, a sinusoidal was generated with the FPGA to simulate the grid voltage at a lower level and 50 Hz and read back in an analogue input to generate the reference signal. Figure 5.33 show the results of this first approach, the signal in blue corresponds to the signal generated in the FPGA and acquired back into the system to generate the reference signal in green. The reference signal generated is in phase with the sinusoidal generated.

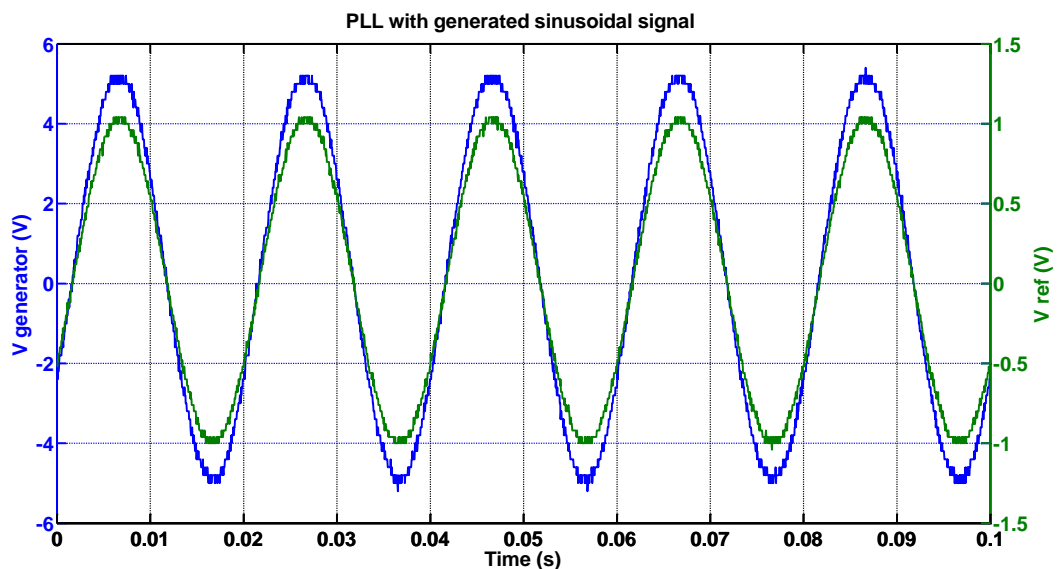


Figure 5.33 PLL with sinusoidal generated in FPGA Vgen(blue) and Vref(green).

Once the reference signal was generated with the previous method, the voltage from the actual grid supply, taken through an isolating transformer, is read via the analogue input in the FPGA. The reference signal similarly generated with the actual grid voltage, as shown in Figure 5.34.

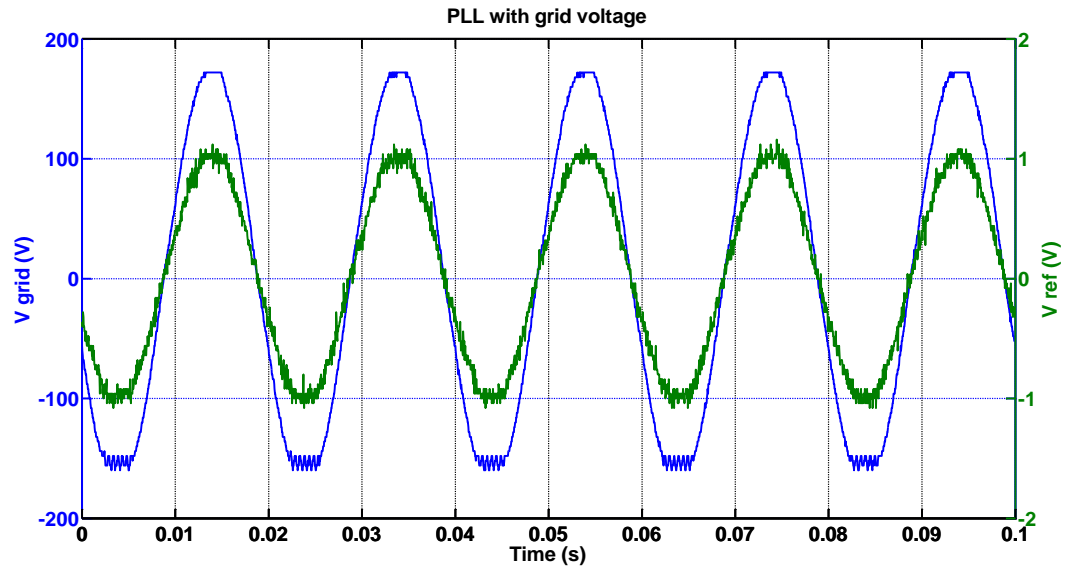


Figure 5.34 PLL with grid voltage  $V_{grid}$ (blue) and  $V_{ref}$ (green)

Debugging is being carried out to use the output of the PLL as the reference signal in the MLC to achieve the synchronisation of the mains and the MLC.

## 5.8 Safety and protection circuit

### 5.8.1 Fuse selection

Considering 150% of the  $I_{RMS}$  value of the input and output currents as maximum limit values. The fuse for the input of the converter or battery side is a slow blow fuse rated at 250VAC and 15A, and the output fuse or multilevel converter input side is a slow blow fuse 250VAC at 20A.

### 5.8.2 Battery protection circuit

In order ensure safe operation of the system and to prevent damage occur to the battery an external circuit was used to monitor the battery voltage. This was composed of a relay and a microcontroller, in this case an Arduino. The function of the monitoring system is to measure the voltage on the battery to ensure that it is not discharged below 108V and also to prevent overcharge beyond 170V. The battery protection circuit of the system is shown in Figure 5.35.

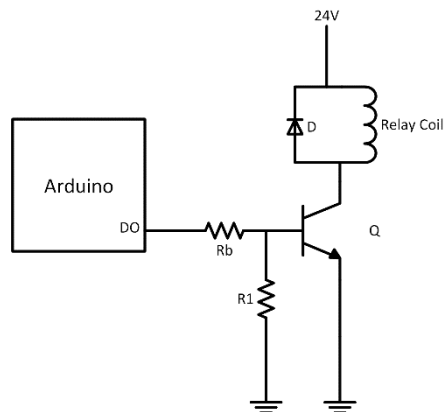


Figure 5.35 Battery protection circuit.

If the system detects violation of the safe operating conditions, then the battery is disconnected from the converter and the FPGA based control system is informed of a fault and so stops the gate signals for the system performing a shutdown.

### 5.8.3 Safety enclosure

The converter was installed in a safety enclosure to comply with the departmental safety regulations. The enclosure contains the DC-DC and MLC converters along with the FPGA and battery protection circuit. The addition of 2 fans to the box is in order to reduce the operational temperature within the enclosure. A photograph of the final system is shown in Figure 5.36

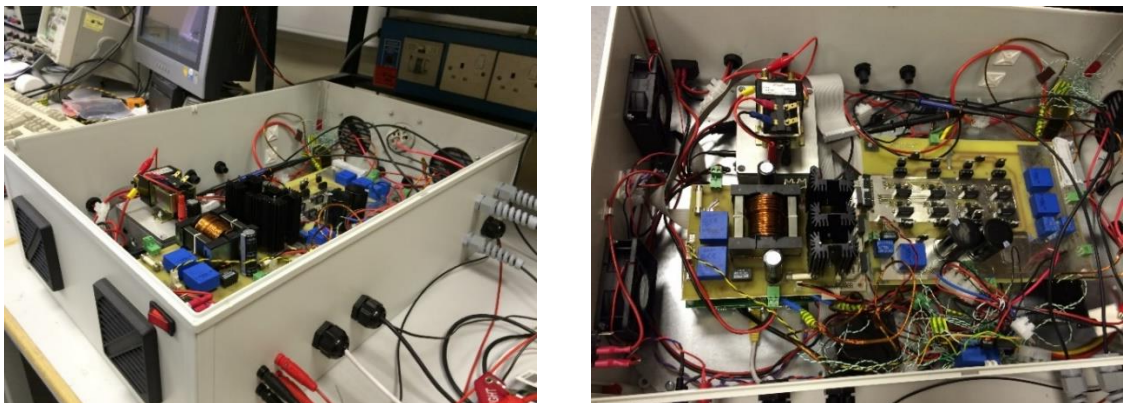


Figure 5.36 Enclosure safety box

## 5.9 Chapter conclusion

This chapter covers the experimental evaluation of the base platform converter that is used to evaluate performance at different operating conditions, i.e. temperature, harmonic distortion and also to evaluate emerging semiconductor technologies. The converter is controlled with an FPGA from National Instruments and it is programmed in LabVIEW. The first part show the implementation in the FPGA and the circuits and sensors required for the experimental evaluation. The next part presented the test of the DC converter, followed by the MLC evaluation in isolation. The test of both converters integrated is shown from section 5.6.2. The following part of this chapter introduces the PLL function of the converter to interface it with the grid.

The last part of the chapter focuses on the safety measures taken for the safe operation of the experimental setup from fuses to a battery protection circuit developed to operate as a separate system interconnected to the FPGA.

In the next chapter (6), the thermal performance of the MLC evaluated in this section is presented and compared when using Si an SiC MOSFETs.

## 5.10 References

- [5-1] C. Hinkle, a. Millner, and W. Ross, “Bi-directional power architectures for electric vehicles,” *2011 8th Int. Conf. Expo Emerg. Technol. a Smarter World*, pp. 1–6, Nov. 2011.
- [5-2] S. S. Hosseini, A. Badri, and M. Parvania, “The plug-in electric vehicles for power system applications: The vehicle to grid (V2G) concept,” in *2012 IEEE International Energy Conference and Exhibition (ENERGYCON)*, 2012, pp. 1101–1106.
- [5-3] N. Wong and M. Kazerani, “A REVIEW OF BIDIRECTIONAL ON-BOARD CHARGER TOPOLOGIES FOR PLUGIN VEHICLES,” in *IEEE Canadian Conference on Electrical and Computer Engineering (CCECE)*, 2012, pp. 0–5.
- [5-4] M. Lanzagorta, S. Bique, and R. Rosenberg, *Introduction to Reconfigurable Supercomputing*, vol. 4, no. 1. University of Wisconsin, Madison: Morgan & Laypool publishers, 2009, pp. 1–103.
- [5-5] N. . Salgado-Herrera, A. Medina-ríos, A. Ramos-Paz, and J. R. Rodriguez-Rodriguez, “Generation of a Multilevel SPWM Technique of 3 , 9 and 21 Levels with FPGAs,” *North Am. Power Symp.*, pp. 1–5, 2013.

- [5-6] H. Hu, W. Yao, and Z. Lu, "Design and Implementation of Three-Level Space Vector PWM IP Core for FPGAs," *IEEE Trans. POWER Electron.*, vol. 22, no. 6, pp. 2234–2244, 2007.
- [5-7] Ó. López, J. Álvarez, J. Doval-gandoy, and F. D. Freijedo, "Multilevel Multiphase Space Vector PWM Algorithm," *IEEE Trans. Ind. Electron.*, vol. 55, no. 5, pp. 1933–1942, 2008.
- [5-8] C. Wang, T. Tian, and Y. Ye, "Research on Three-Phase Inverter SVPWM Modulation Based on FPGA," in *2013 5th International Conference on Intelligent Human-Machine Systems and Cybernetics*, 2013, no. 1, pp. 222–225.
- [5-9] P. Samuel, N. Chandrashekhar, and R. Gupta, "Wind energy conversion based on seven-level cascaded H-bridge inverter using LabVIEW FPGA," in *2010 International Conference on Power, Control and Embedded Systems*, 2010, pp. 1–6.
- [5-10] S. Gautam, S. Kundu, P. Basu, and R. Gupta, "FPGA implementation of generalized modulation for hybrid multilevel inverter with fixed ratio DC link voltage," *2012 IEEE Int. Conf. Power Electron. Drives Energy Syst.*, pp. 1–5, Dec. 2012.



## Chapter 6 – Evaluation of 5L-FB-NPC MLC featuring wide bandgap semiconductor devices

### 6.1 – Introduction

In previous chapters, the topology studied has been presented including the modulation techniques in Chapter 3. In Chapter 4 the application system is described in detail followed by the experimental evaluation of the converter in Chapter 5. Motivated by the increasing general interest on wide bandgap devices, the evaluation of the performance of SiC devices in this topology is presented in this chapter.

The work presented in this chapter focuses on a evaluating the performance of alternative power devices when deployed in single phase 5-level Neutral Point Clamped converter(NPC), Figure 6.1.The underlying operation of the circuit is similar to the previous chapters where a form of space vector modulation (N2V) is used to derive the switching states to generate the output voltage and provide capacitor voltage balancing control to ensure the voltage at the midpoint of C1 and C2 is steady.

Motivated by the impetus to reduce the use of electrical energy produced from fossil fuel

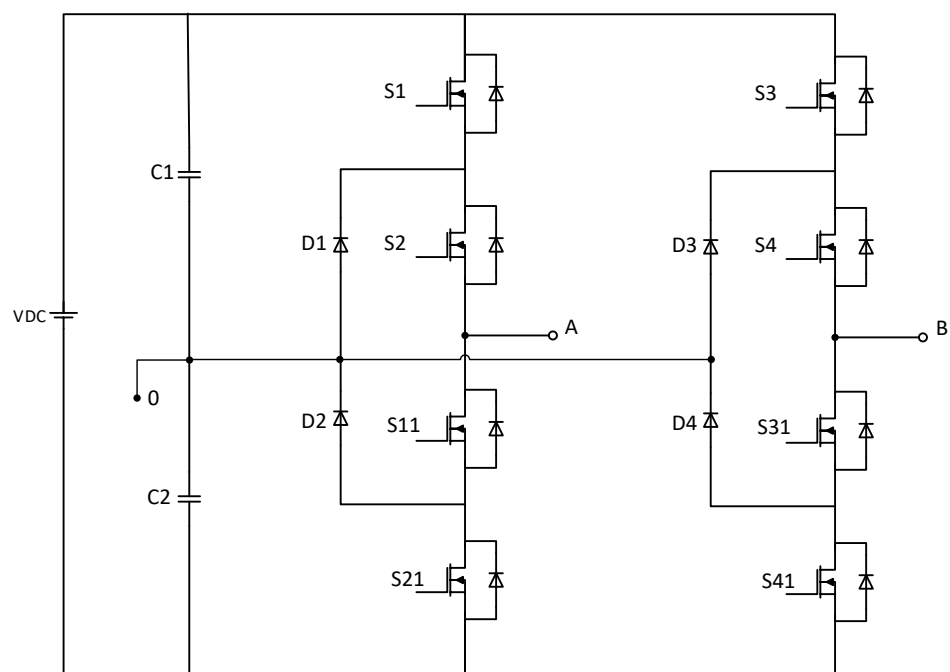


Figure 6.1: Circuit diagram for the 5-level single-phase converter

resources and the continued increased in electric powered equipment, has led to the increased deployment of alternative energy resources. A power converter is often required

to ensure its energy is supplied to the load in the most efficient manner. A MLC is able to produce output waveforms featuring a much lower harmonic distortion compared to the typical 2 level converter. In a MLC lower distortion is achieved by reducing the voltage step-size that occurs during a commutation event.

Operating the MLC at high frequency, enables the reduction of filter size, nevertheless, this leads to higher switching losses reducing overall converter efficiency. The development of new semiconductor devices, such as Silicon Carbide (SiC) MOSFETs, allows high switching frequencies and permits operation at higher temperatures, thus reducing the requirements in both filtering and a thermal management when compared to their silicon (Si) counterparts. In addition to these characteristics, the converter can be scaled up for high power as the SiC MOSFETs voltage and current rating is higher than SiC devices.

In the literature, performance comparisons between Si and SiC in MLC topologies have been found in [6-1] to [6-5]. In these works, evaluations in performance of Si IGBT and diode over SiC MOSFET and SiC JFET are made respectively, when used in a modular multilevel converter. The evaluation was based on a series of simulation results. In [6-2] a comparison in a medium power 3-level switched neutral point converter was carried out considering efficiency and operating temperatures by supplanting the Si IGBT and Si antiparallel diode with their SiC equivalents. The work undertaken in references [6-3] and [6-4] study a similar impact on the performance in a 3-level NPC topology. Reference [6-3] presents the evaluation of SiC diodes (antiparallel and clamping) performance in simulation by comparing the average junction temperature and losses differences with a converter employing Si devices. A simulation based study in reference [6-4] concentrates on a 3-phase converter, it evaluates a diversity of PWM methods and the power quality in terms of the Total Harmonic Distortion (THD) for various gate resistor values.

In this chapter the results of an experimental study on the performance of SiC MOSFETs and SiC anti-parallel diodes operating as the switching devices in a 5-level NPC MLC are presented. The performance of the MLC with SiC devices is contrasted with that of standard Si devices, the comparison is based on the devices temperature rise and the total efficiency of the converter. In Section 6.2 a description of the complete system and converter is presented followed by Section 6.3 with a description of the semiconductor devices used in the evaluation. In Section 6.4 the experimental evaluation of the switching

devices is presented, emphasizing the differences in efficiency, operating temperature of the switching components along with voltage waveforms and spectrum analysis of the output.

## 6.2 – 5-level NPC Converter

The evaluation platform for this work was a 5-level NPC intended for use as a construction site battery power supply. The block diagram of the complete system is presented in Figure 6.2. The work presented here concentrates on the DC to AC 5-level converter. The entire system is designed to provide bi-directional power flow and the control of the system is implemented in LabVIEW, with a FPGA providing gate control signals to the MOSFETs as presented in Chapter 3 and 5 of this thesis.

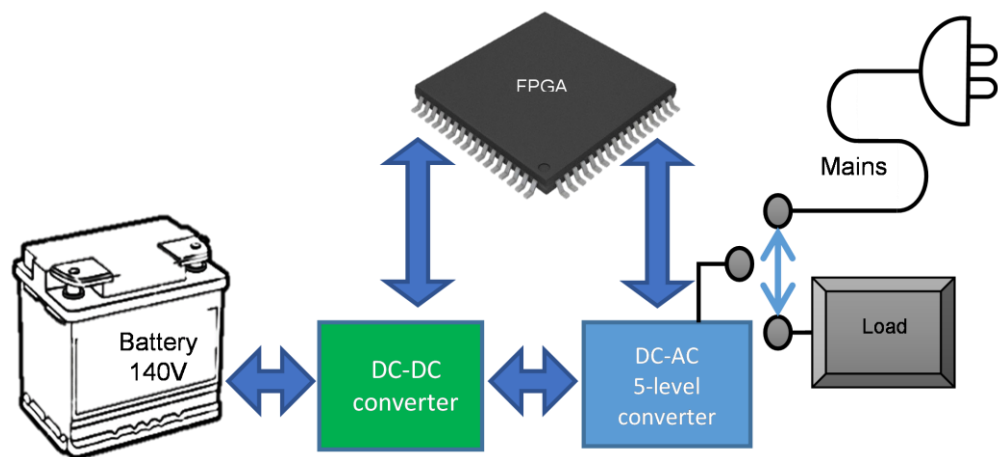


Figure 6.2: Block diagram of MLC system

A review found in [6-6] considers different implementations of the NPC topology, for a single phase system, a topology with an additional leg or phase can be added, taking the output from nodes A and B making the 5-level Full-Bridge NPC (5L-FB-NPC) topology with output voltage levels defined as  $V$ ,  $V/2$ ,  $0$ ,  $-V/2$  and  $-V$ , this has been described in detail in Chapter 3. The redundant switching states to generate the output voltage allow the individual divider capacitor voltages to be balanced.

## 6.3 – Wide bandgap semiconductor devices

Wide bandgap (WBG) semiconductor materials such as SiC or Gallium Nitride (GaN) are enabling unprecedented performance to be obtained with power electronic switching devices allowing power electronic converters to operate at higher frequencies, higher voltage stress, higher temperatures, and with reduced size.

In the last decade, SiC has been of particular interest in the power electronics industry with a large amount of research carried out to evaluate its performance. An interesting application of this novel semiconductor material is in the More Electric Aircraft (MEA) where it permits the operation at higher temperatures, reducing the weight of the electronic systems due to the reduced size of heatsinking, and it also improves the reliability of the systems.

Motivated by the previously discussed advantages of WBG switching components, the temperature rise in the converter studied in this thesis using SiC and Si is evaluated to show the differences when operating as part of a multilevel converter.

Reference [6-7] presents a review of a series of SiC and Gallium Nitride (GaN) devices including SiC MOSFETs in the range from 1.2kV to 10kV and provides details on the latest improvements in the technology including the MOSFETs in the 1.2kV range from CREE and ROHM. It has been demonstrated in [6-8] that the 2<sup>nd</sup> generation of Cree MOSFETs (C2M) can provide long term reliability, based on a stress of 1000 hours and 150°C and 175°C for a  $V_{GS}$  of -15V and 20V respectively. This chapter builds on the previous work by demonstrating the deployment of SiC devices within a 5L Neutral Point clamped full-bridge multilevel converter.

### 6.3.1 – Si and SiC evaluation devices

SiC power MOSFETs were selected for the evaluation due to their high temperature operation, and the recent improvements in the normally-off n-channel devices that are now readily available in the market.

The power electronic devices evaluated in this study are listed in Table 6.1. The silicon MOSFET N95 was chosen as its ratings are comparable to the range of the SiC devices being evaluated. MOSFETs SiC 040 and SiC 280, were chosen for comparison due to their low  $R_{DS(on)}$  and low current rating respectively.

Another parameter considered when choosing which specific semiconductor devices to test was the input capacitance ( $C_{ISS}$ ) since it gives a measure of how the switching devices will perform at high frequency, the smaller the capacitance the faster it will charge enabling the MOSFET to switch faster.

For the Si MOSFETs, Si N95 has the lower value of capacitance but also has the highest  $R_{DS(on)}$  and Si FDP has the lowest  $R_{DS(on)}$  with the highest capacitance.

Name	MOSFET	Manufacturer	V <sub>DS</sub> (V)	I <sub>DS</sub> (A)	R <sub>DS(on)</sub> (mΩ)	C <sub>ISS</sub> (pF)
Si N95	Si	ST	950	10	680	1620
Si FDP	Si	Fairchild	100	164	4.5	3960
SiC 040	SiC	CREE	1200	60	40	1893
SiC 280	SiC	CREE	1200	10	280	259

Table 6.1 Switching devices for performance evaluation in 5-level single phase converter

For the SiC MOSFETs, SiC 040 has the lowest R<sub>DS(on)</sub> with the highest capacitance in the range of Si N95 and SiC 280 has the lowest capacitance of all the devices at 259 pF.

The SiC devices described in this section were selected from the manufacturer CREE for its market leading innovation reputation and for the availability from the university suppliers. Cree’s solution offered at the time of evaluation was the newest technology available, being the second generation of the firm’s products.

#### 6.4 – Experimental evaluation

The test was carried out under the conditions listed in Table 6.2 with the DC input being provided by a bench power supply. The MLC controller is set to give an output of 110 V AC and the load is connected to the terminals A and B of the MLC, see Figure 6.1.

V <sub>DC</sub>	120V
V <sub>AB rms</sub>	110 V
R <sub>load</sub>	8 Ω
I <sub>out</sub>	13.75 A
P <sub>out</sub>	1.5kW

Table 6.2 Experimental evaluation test conditions

The input and output powers are calculated using the measurements of voltage and current at the input and output. Then the efficiency of the converter is found.

The converter is controlled using the FPGA controller described previously to give the PWM to the converter to both balance the DC link, and control the output voltage. In order to keep the operating conditions comparable in all cases, the gate driver used is suitable to drive Si and SiC MOSFETs and the control parameters are the same for both Si and SiC tests.

#### 6.4.1 – Hardware setup

In order to effectively evaluate the performance of the switching devices, an external antiparallel SiC diode and a blocking diode was used to minimize the effect of the body diode of the MOSFETs, as shown in Figure 6.3. The diode characteristics are detailed in Table 6.3. The diodes were selected to match the specification of the converter and they were mounted on the same heatsink as the switching devices. The terminals shown as G, D and S in Figure 6.3, represent the actual terminals (gate, drain and source) connected to the converter topology presented in the previous section. The external antiparallel diode is a SiC diode from Cree’s 4<sup>th</sup> generation of SiC technology and has very low capacitance, allowing the MOSFET to switch faster.

For each device under test, its temperature was measured by using thermocouples attached to the heatsink. The ambient temperature in a laboratory was also measured and subtracted from the measured device temperatures to provide measurements for the temperature rise caused by the losses. The efficiency is determined by measuring the input and output power of the converter.

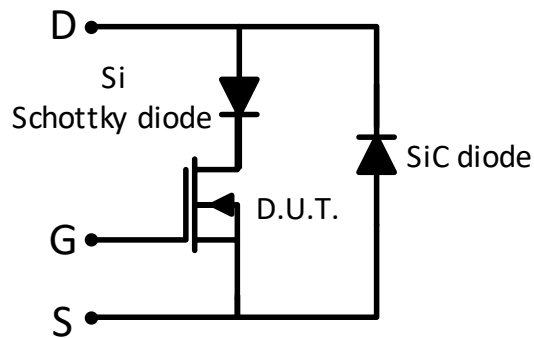


Figure 6.3: MOSFET with external SiC antiparallel diode and blocking diode.

Name	Device	Manufacturer	$V_{RRM}$ (V)	$I_F$ (A)
Blocking Diode	Si Schottky diode	IXYS	600	50
Antiparallel diode	SiC Diode	CREE	1200	11

Table 6.3: Characteristics of blocking diode and antiparallel diode

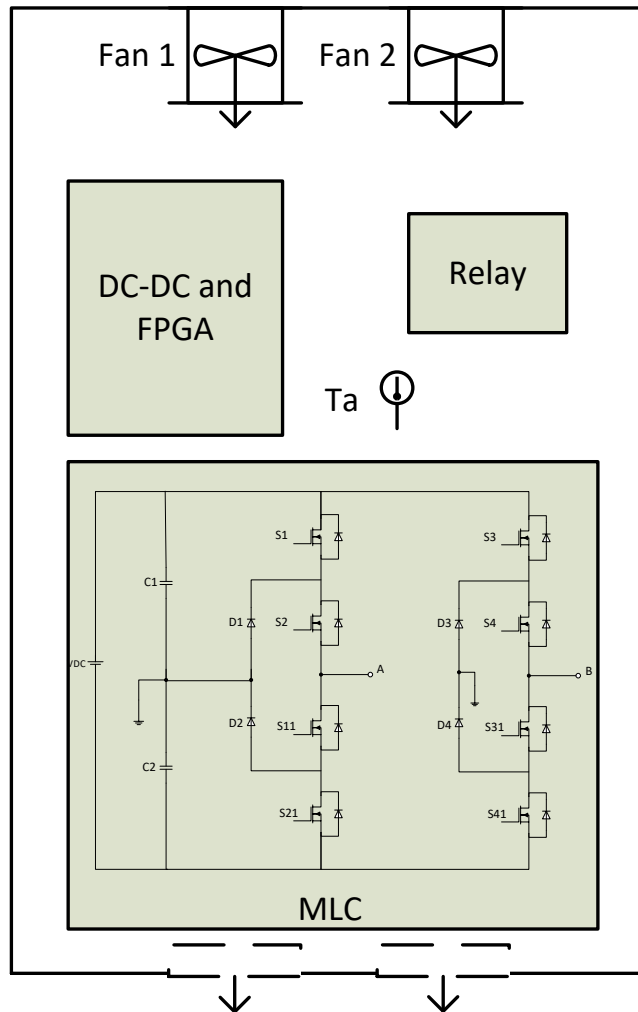


Figure 6.4 Converter enclosure component

The experimental apparatus, Figure 6.4, is housed inside an enclosure with forced air provided by fans blowing from the S1 and S3 devices to S21 and S41. Since S1 and S3 are located closest to the fans they receive greater cooling. Labels S1-4 and S11-41 show the locations of the heatsinks fitted with the power devices and C1, C2 are the DC

capacitors. The heatsinks have a thermal resistance of  $R_{th} = 4^{\circ}\text{C}/\text{W}$ . The operating

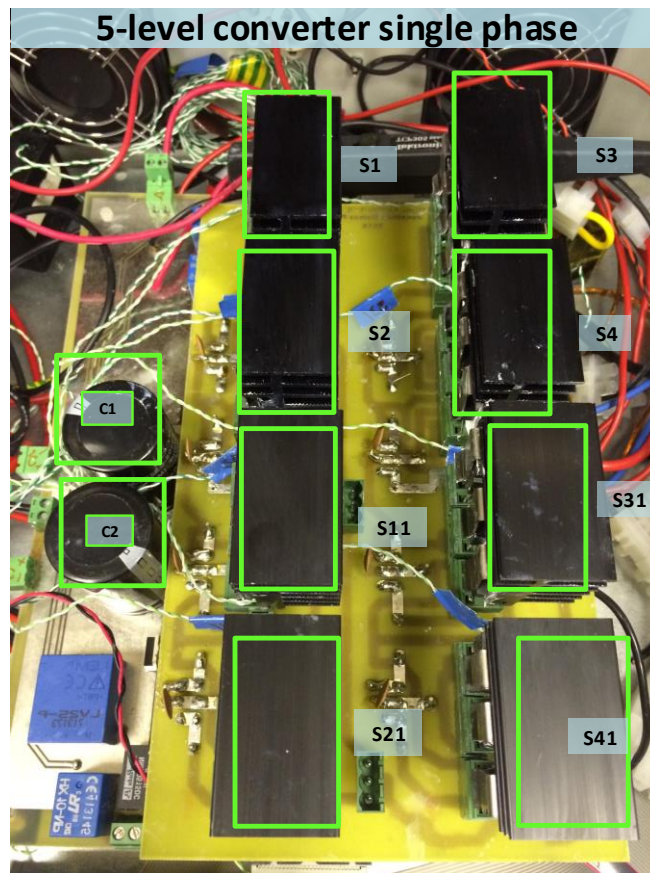


Figure 6.5 Hardware of converter evaluated

conditions for the experiment were the same, with the evaluation MOSFETs being the only change made during the experiments.

The temperature was measured using thermocouples attached to the heatsink of each of the MOSFETs (S1, S2, S11, S21, S3, S4, S31 and S41). Figure 6.4 shows the location of the components in the enclosure and the position of the fans and the air flow direction. To measure the ambient temperature, a thermocouple was placed and it is denoted as  $T_a$ . The real distribution of the components is shown in Figure 6.5.

#### 6.4.2 – Temperature rise and efficiency results

The temperature and efficiency results are presented in this section. As previously described, the MLC was tested at the range of frequencies from 20 kHz to 80 kHz. The figures below show the temperature rise for each device labelled as presented in the previous section.



The results of the Si devices are presented first followed by the SiC devices. The average temperature of the eight switching devices is calculated to give a clearer picture of the effect of the different devices when evaluated in the MLC.

The results for the Si devices evaluated in the experiments are shown in Figure 6.6. and Figure 6.7. From these it may be seen that for the N95 devices, the temperature rise sits in the range from 50°C to 110°C and for the FDP from 15°C to 37°C, for the range of frequencies in the test.

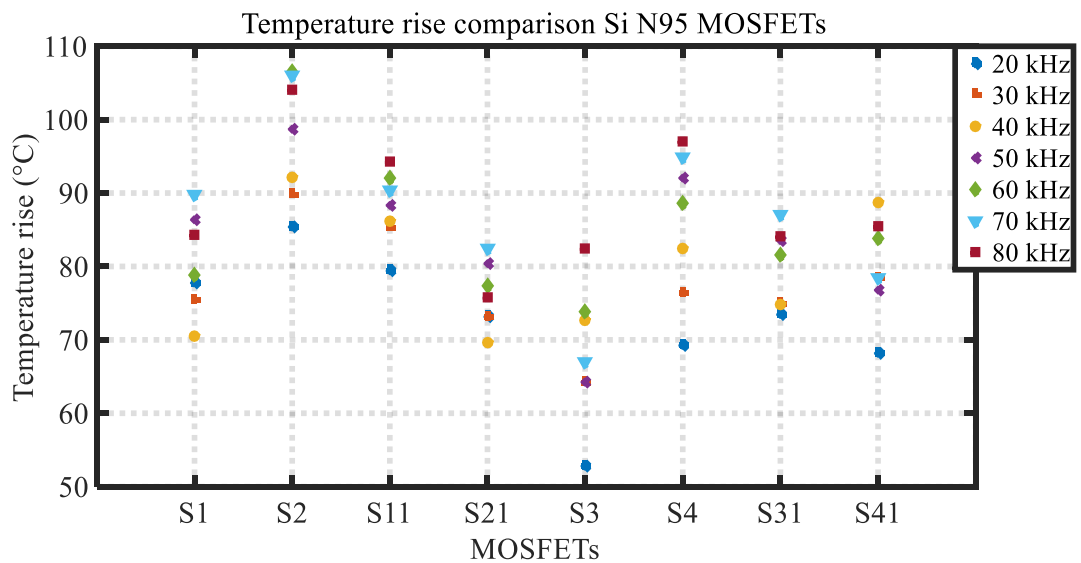


Figure 6.6: Temperature rise of Si N95 MOSFETs in MLC

For the specific devices the temperature rise variation for Si N95 is between 12°C and 30°C and for Si FDP is 5°C to 12°C.

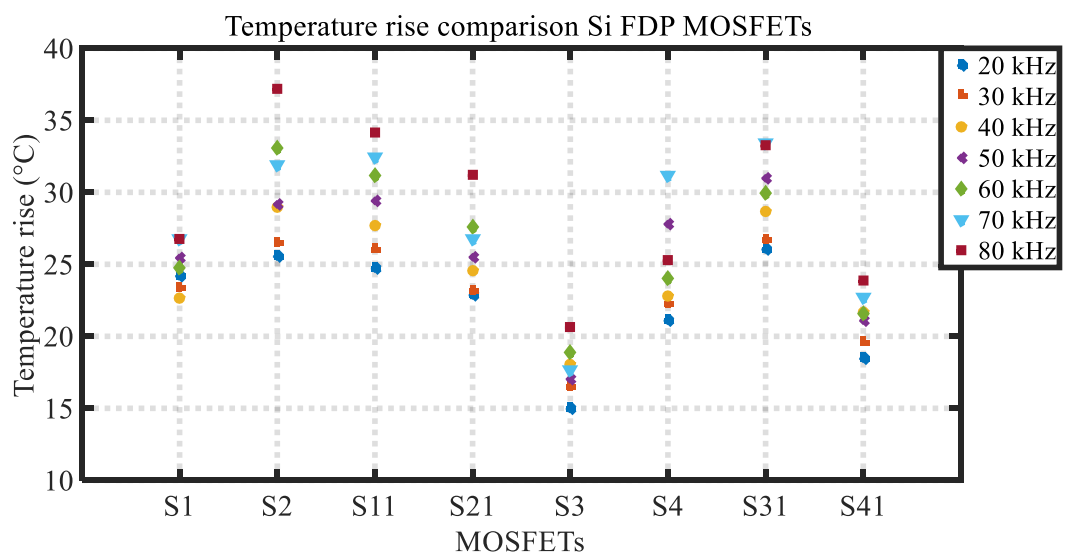


Figure 6.7: Temperature rise of Si FDP MOSFETs in MLC

The results presented in Figure 6.8 and Figure 6.9 correspond to the SiC devices 280 and 040 respectively. The temperature rise is in the range from 25°C to 55°C for 280 MOSFETs and from 12°C to 40°C for the 040 MOSFETs.

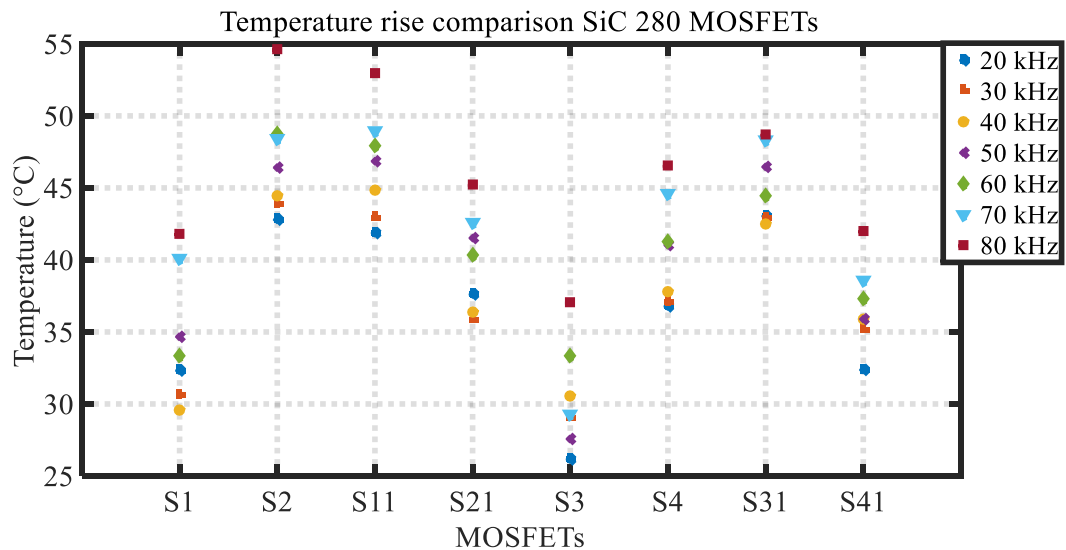


Figure 6.8: Temperature rise of SiC 280 MOSFETs in MLC

The distribution of the temperature rises seems to vary for certain frequencies but is generally consistent. The fluctuation between the minimum and maximum temperature rises of the SiC280 is between 8°C and 12°C. While for SiC 040 is between 4°C and 8°C.

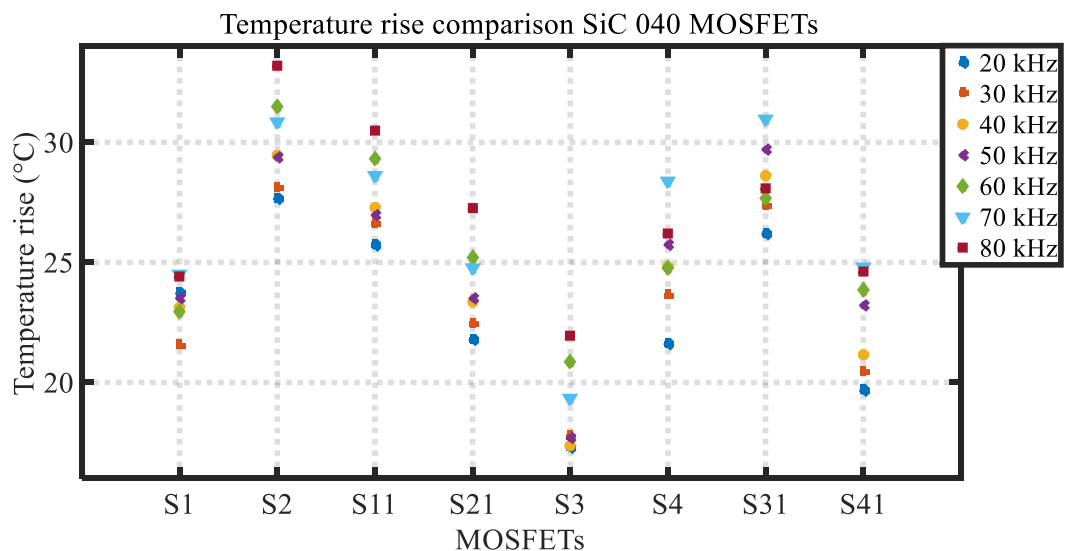


Figure 6.9: Temperature rise of SiC 040 MOSFETs in MLC

Considering the variation of temperature rise in the different devices across the frequency range, it is evident that smallest span between measurements is for the SiC devices with 4°C between the minimum and the maximum for both SiC 280 and SiC 040. Whereas the

Si devices showed a difference of 7°C for Si FDP and 18°C corresponding to Si N95. This shows the good performance of SiC devices at both higher temperature and frequencies.

Despite the distribution of the temperatures between the devices, the average temperature rise of all the devices increases with frequency. In Figure 6.10 the mean temperature of all the devices for a given frequency is taken and plotted to show the average temperature rise as a function of frequency for the Si and SiC devices.

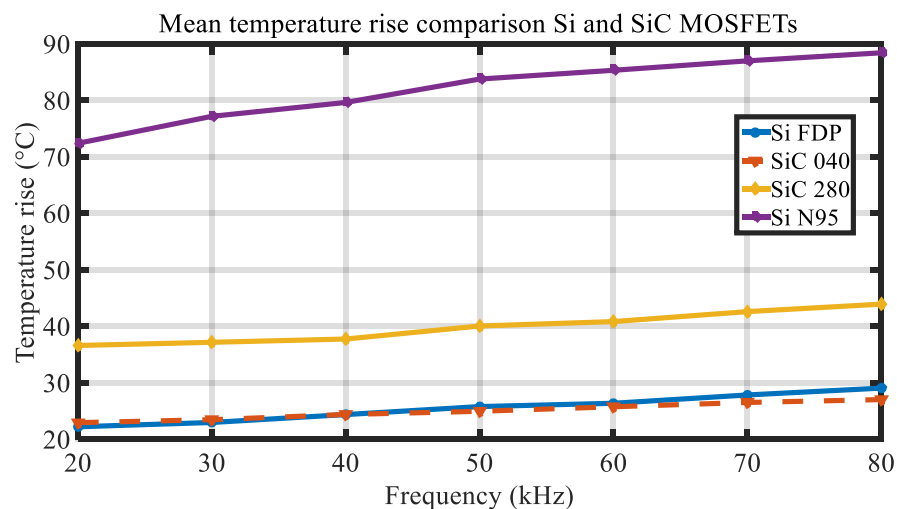


Figure 6.10: Average temperature as a function of frequency for the Si and SiC devices

It can be seen that the device having the larger temperature increase is the Si N95, followed by the SiC 280 but there is a difference of approximately 40°C. This is to be expected since the  $R_{DS(on)}$  of these devices is quite large which leads to higher conduction losses. Comparing SiC 040 and Si FDP reveals some interesting behaviour. At low-frequencies the FDP devices provide better performance due to their lower on-state resistance. However, at higher frequencies the 040 devices give slightly better performance where the switching losses incurred by the Si FDP devices begin to take effect. Indeed, one can observe the gradient is shallower for the 040 devices indicating superior high-frequency behaviour.

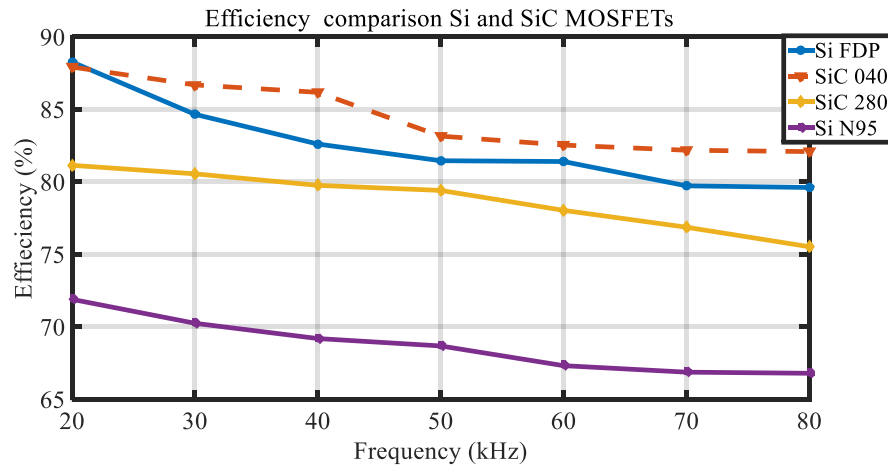


Figure 6.11: Efficiency comparison as a function of frequency

Efficiency measurements for the MLC fitted with the four types of MOSFETs is shown in Figure 6.11. As expected the converter with the SiC 040 devices installed performs the best with efficiencies of 88% to 83%, then the Si FDP gives the next highest efficiency with 88.5% to 80%. SiC 280 gives an overall efficiency of 81% to 75% and finally the device giving the lowest efficiency is the N95 with 72% to 66%.

The results clearly show the impact that  $R_{DS(on)}$  and operating frequency on the performance of the converter. This is clearly seen in the efficiency measurements, as the converter fitted with the 040 devices exhibits the highest efficiency for the range of frequencies considered. The addition of the isolating diodes can lower the overall efficiency of the converter as there is a voltage drop across them.

#### 6.4.3 – Voltage and current waveforms comparison

In this section, the voltage and current waveforms are presented for a particular switching frequency of 30 kHz with the same evaluation parameters presented at the beginning of this section to evaluate the filtered output waveforms produced with each device.

In Figure 6.12 the voltage and current waveforms corresponding to Si N95 are shown. Both voltage and current are sinusoidal. Although the figure shows the filtered voltage and current waveforms, it can be seen that certain noise still appears in the waveforms.

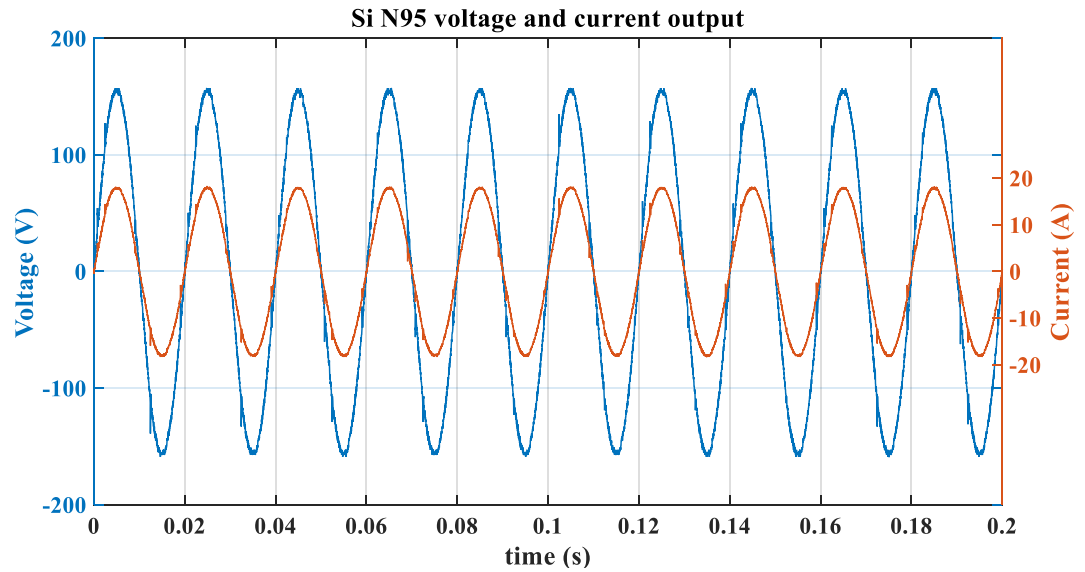


Figure 6.12 Si N95 voltage and current waveforms

Figure 6.13 shows the FFT of the voltage waveform for the Si device. The FFT helps to illustrate the noise. Only the voltage FFT is taken as it will give a measurement needed for the comparison. From the figure below it can be seen that the noise floor is around  $10^{-2}$ . The component at 50 Hz corresponds to the output voltage generated by the MLC and the high frequency spectra lines in 30 kHz and 60 kHz correspond to the switching frequency.

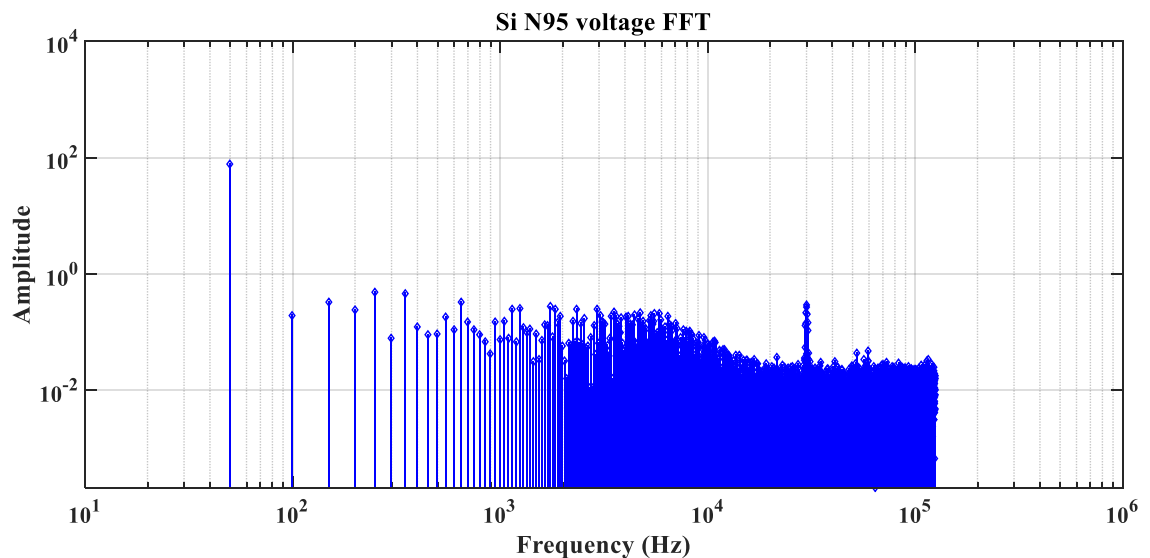


Figure 6.13 Si N95 voltage FFT

In Figure 6.14 are the waveforms corresponding to Si FDP, it shows a ripple slightly bigger than the Si N95 for both voltage and current.

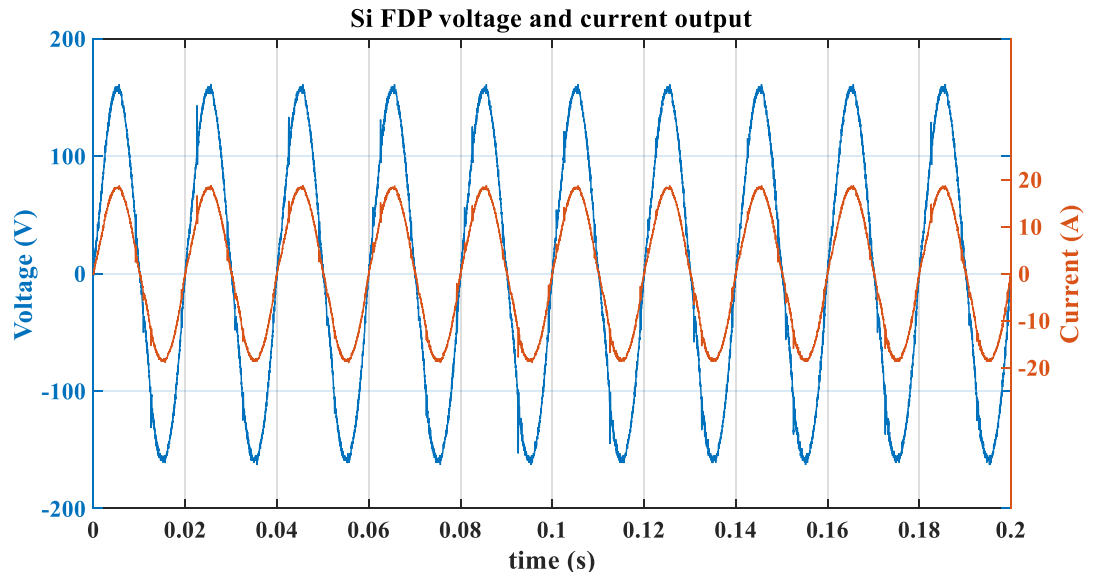


Figure 6.14 Si FDP voltage and current waveforms

The spectrum shown in Figure 6.15 are the voltage components in frequency for the Si FDP. Comparing the FFTs for both Si devices, it can be seen that Si N95 has the lowest magnitude in the harmonics of the fundamental 50 Hz. For this example, the third harmonic is larger than the component with Si N95.

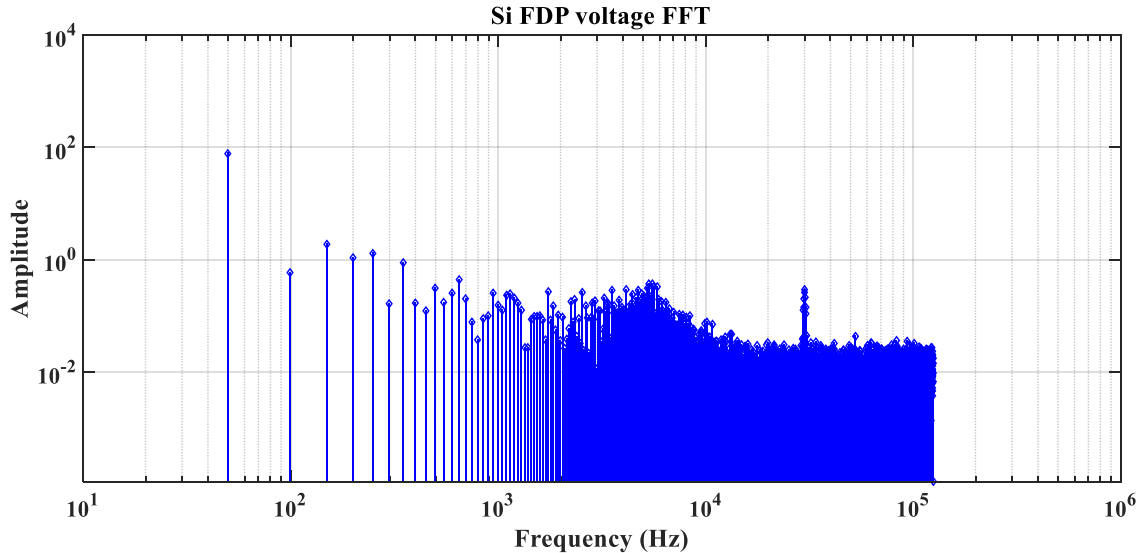


Figure 6.15 Si FDP voltage FFT

In Figure 6.16 the voltage and current waveforms corresponding to SiC 280 are shown. Both voltage and current are sinusoidal. Compared with the Si devices waveforms this seems less distorted.

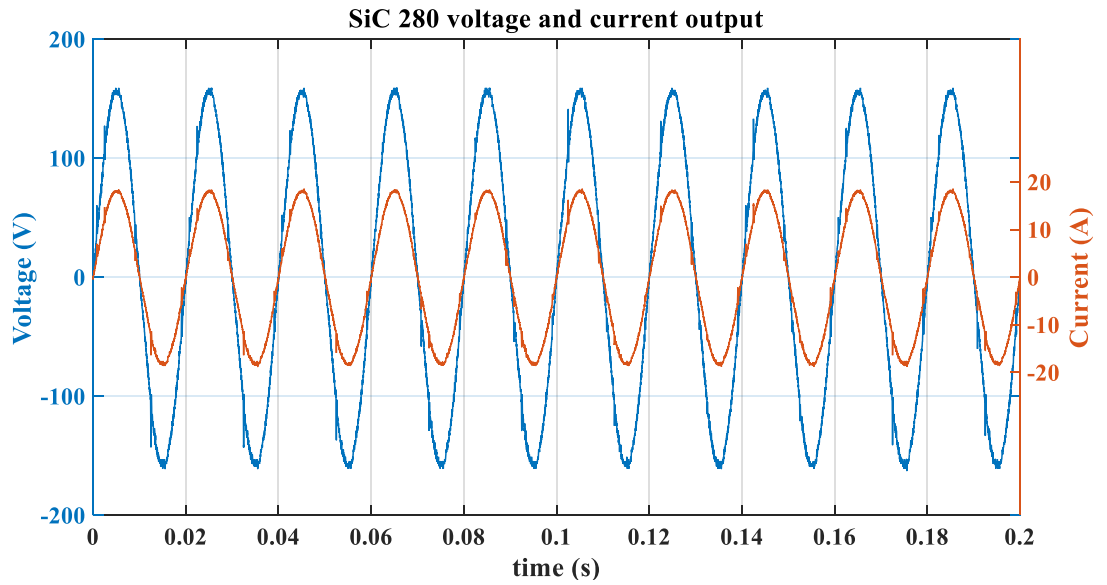


Figure 6.16 SiC 280 voltage and current waveforms

In Figure 6.17 the frequency components of the voltage are shown corresponding to SiC 280. Compared to the lowest Si device (N95), SiC 280 shows higher amplitude components up to the 5<sup>th</sup> harmonic, then lower amplitude components at the higher harmonics than given by Si N95.

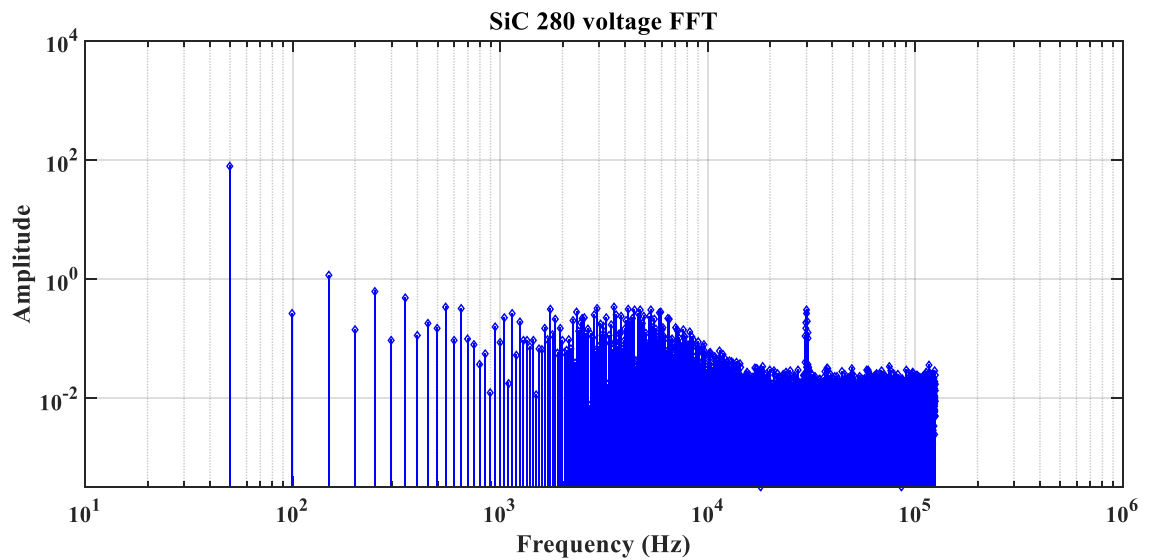


Figure 6.17 SiC 280 voltage FFT

The waveforms in Figure 6.18 are the voltage and current for SiC 040. The ripple and noise is similar to that obtained for SiC 280.

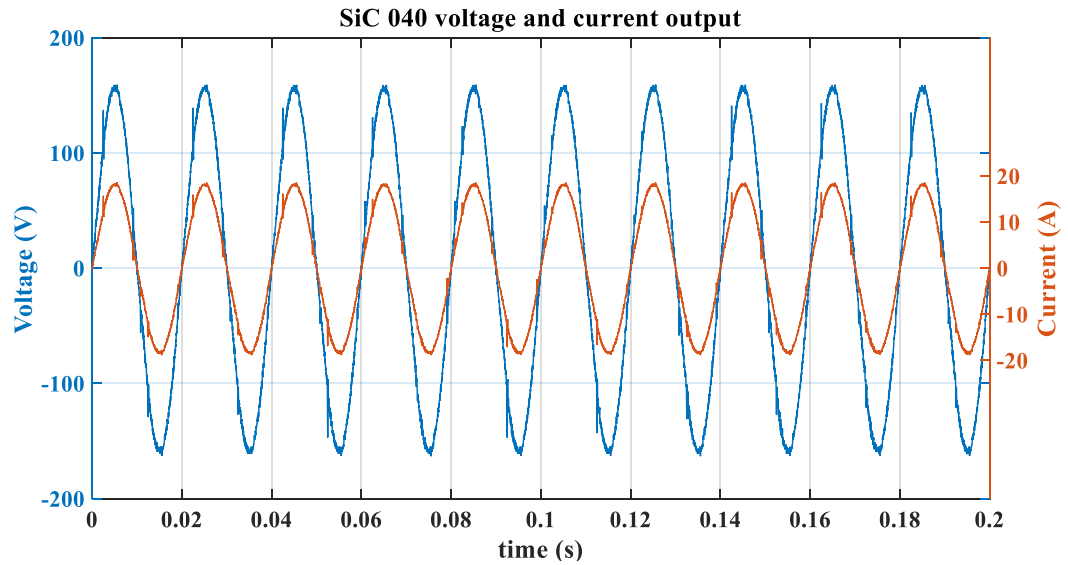


Figure 6.18 SiC 040 voltage and current waveforms

Figure 6.19 shows the FFT of the voltage obtained with SiC040. The harmonic content with this device is slightly higher in magnitude for each harmonic achieved with SiC 280 but lower than Si FDP.

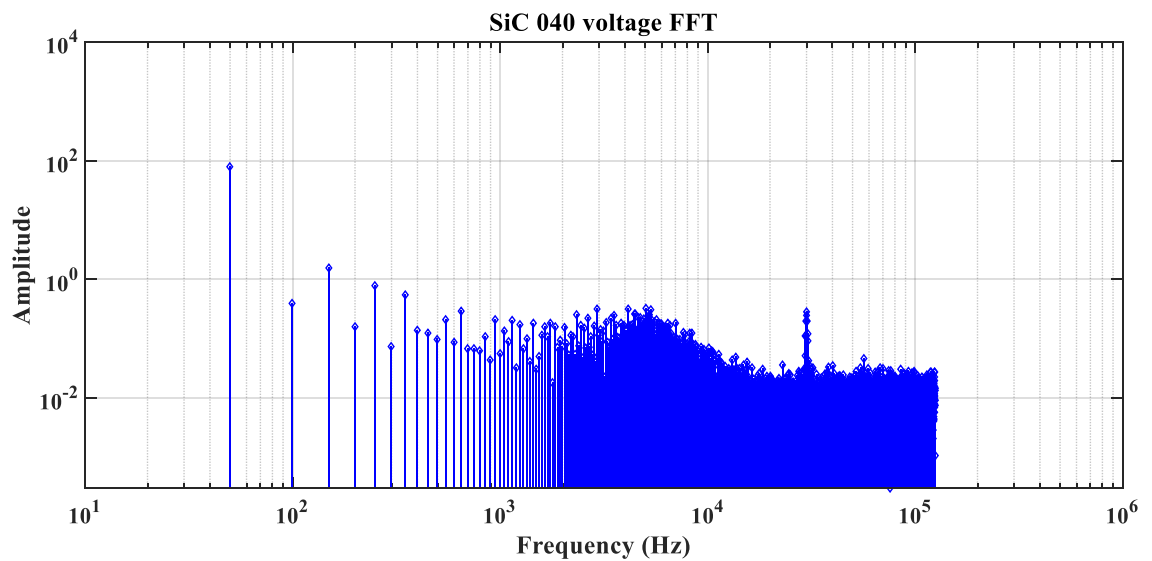


Figure 6.19 SiC 040 voltage FFT

A summary of the harmonics magnitude in Table 6.4, after analysing and comparing the FFT of the different devices, Si N95 shows the lowest magnitude in the lower harmonics but SiC 280 gives lower magnitude followed by SiC040 of the higher harmonics up to the 9<sup>th</sup> harmonic analysed in this section.



MOSFET	Harmonic number and voltage magnitude								
	1 <sup>st</sup>	2 <sup>nd</sup>	3 <sup>rd</sup>	4 <sup>th</sup>	5 <sup>th</sup>	6 <sup>th</sup>	7 <sup>th</sup>	8 <sup>th</sup>	9 <sup>th</sup>
<b>N95</b>	77.97	0.06	0.27	0.05	0.49	0.24	0.57	0.14	0.15
<b>FDP</b>	77.89	0.65	1.79	1.04	1.23	0.22	0.85	0.07	0.14
<b>SiC040</b>	77.9	0.38	1.38	0.12	0.73	0.16	0.54	0.07	0.09
<b>SiC280</b>	77.91	0.31	1.01	0.11	0.67	0.13	0.53	0.06	0.12

Table 6.4 Harmonics voltage FFT magnitude

The results obtained in this section are consistent with the input capacitance, SiC 280 has the lowest  $C_{ISS}$  with 259 pF followed by Si N95 with 1620 pF. This illustrates that the lower capacitance in the MOSFET enables a better operation in higher frequency

### 6.5 – Conclusion

The evaluation of performance of SiC compared to Si devices in the 5-level MLC presented in this chapter shows the effect of the  $R_{DS(on)}$  on the temperature rise of the devices and efficiency. The second generation of SiC MOSFETs and Si MOSFETs evaluated were chosen for their low  $R_{DS on}$  (SiC 040 and Si FDP) and for the similarity in current and voltage ratings (SiC 280 and Si N95).

The overall performance of SiC devices evaluated in the converter is significantly higher, the low temperature rise with SiC devices would allow the reduction of size as the cooling systems required by these devices are smaller and operating at higher frequencies implies a reduction in filter component's dimensions. Although the temperature rise with Si FDP and SiC 040 appears to be close, the SiC competitor gives lower temperature rise at higher frequencies. Furthermore, the reliability of the SiC devices should be greater as the Si N95 operates at 85% of its voltage rating compared to less than 10% of SiC 040 rating.

It should be noted that the control and modulation scheme remained unchanged for the experiments presented here. It may be possible to modify the control to decrease switching losses for the different frequencies considered which could reduce the temperature rise in the devices and improving the overall efficiency and is currently under investigation.

Following the last section in this chapter, in the next chapter, the effect of SiC on the THD when used in the MLC will be presented considering the dead time and switching frequency.

## 6.6 – References

- [6-1] L. Wu, J. Qin, M. Saeedifard, O. Wasynczuk, and S. Krishna, “Efficiency Evaluation of the Modular Multilevel Converter Based on Si and SiC Switching Devices for Medium / High-Voltage Applications”, *IEEE Trans. Electron Devices*, volume 62, no. 2, pp. 286–293, (2015).
- [6-2] D. Debashis, et al. "An all SiC MOSFET high performance PV converter cell", *Power Electronics and Applications (EPE), 15th European Conference on. IEEE*, (2013).
- [6-3] F. Filsecker, R. Alvarez, and S. Bernet. "Comparison of 6.5 kV silicon and SiC diodes", *Energy Conversion Congress and Exposition (ECCE), IEEE*, (2012).
- [6-4] Jahdi, Saeed, Olayiwola Alatise, and Phil Mawby. "On the Performance of Voltage Source Converters used on Silicon Carbide Technology." *Telecommunications Energy Conference Smart Power and Efficiency'(INTELEC), Proceedings of 2013 35th International. VDE*, (2013).
- [6-5] Pefitsis, Dimosthenis, et al. "High-power modular multilevel converters with SiC JFETs." *Power Electronics, IEEE Transactions,*” pp. 28-36, (2012).
- [6-6] J. Rodriguez, S. Bernet, P. K. Steimer, and I. E. Lizama, “A Survey on Neutral-Point-Clamped Inverters,” *IEEE Transactions on Industrial Electronics*, volume 57, no. 7, pp. 2219–2230, (2010).
- [6-7] P. Godignon and X. Perpi, “A Survey of Wide Bandgap Power Semiconductor Devices,” *IEEE Transactions on Power Electronics*, volume 29, NO. 5, vol. 29, no. 5, pp. 2155–2163, (2014).
- [6-8] B. Hull, S. Allen, Q. Zhang, D. Gajewski, V. Pala, J. Richmond, S. Ryu, M. O. Loughlin, E. Vanbrunt, L. Cheng, A. Burk, J. Casady, D. Grider, and J. Palmour, “Reliability and stability of SiC power MOSFETs and Next-Generation SiC MOSFETs,” *Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, pp. 139–142, (2014).

## Chapter 7 – Power quality evaluation in 5L-FB-NPC MLC

### 7.1 – Introduction

In the previous chapter (6) an evaluation of wide band-gap devices in the MLC topology described in chapter 4 and 5 was presented. In this chapter, a study of the harmonics in the converter will be covered based on the modulation technique presented in chapter 3.

The use of power converters to supply and drive large machinery and electronic appliances introduces unwanted disturbances (noise and distortion) to the systems to be powered and even onto the grid in grid connected applications. The main sources of disturbances introduced to the grid from power converters are from the control system and the modulator, and include PWM, space vector modulation used mainly to control the output of the converter and the technique used to balance DC-link capacitor voltages.

The appliances or loads connected to the grid are also responsible of generating disturbances in the form of harmonics. Inductive loads in particular can introduce a large amount of disturbance as they commutate diodes during dead time periods.

The harmonics in question are voltage or current frequency components that are a multiple of the grid frequency. The output waveform of a MLC possesses unwanted harmonics as a result of the operation of the switching devices. The total harmonic distortion (THD) is a parameter used to measure how far a waveform is with respect to the ideal waveform, in this case a sinusoid.

In [7-1] an algorithm to calculate the THD of a sinusoid is presented along with results evaluation. The study of THD on MLC minimisation with different switching angles is presented in [7-2]. Further studies on the calculation of the THD on H-bridge topologies with equal and unequal DC-sources are have been presented in [7-3] and [7-4].

A publication on NPC class D audio power amplifiers [7-5] analyses the effect of the clamping diode in this topology and how it affects the THD showing that the reverse time recovery of the clamping diode ( $t_{tr}$ ) has influence on the output distortion.

Additionally, in [7-6] a model to predict the harmonics due to the dead time in class D amplifiers is presented. Moreover, the cited publication states that the harmonic levels are a function of load impedance, modulation depth, dead time and switching frequency.

Based on this, the effect of dead time in the MLC studied in this thesis will be evaluated as a function of frequency.

In order to minimise the harmonics, and to obtain a purer sinusoidal output waveform, a filter is employed which will be presented in section 7.2, then the total harmonic distortion is presented in section 7.3 including a comparison with the THD obtained with the same WBG devices presented in the previous chapter.

## 7.2 – Multilevel converter (MLC) filter

The output filter is used in a MLC to generate a sinusoid with the least noise and harmonic content. The filter should be able to attenuate the harmonic components with the minimal attenuation of the fundamental component. The goal is to maintain the THD at a low value while ensuring the size of the filter is not too physically large. There are several filters that can be used, a comparison of passive filters is presented in [7-7] and for its ease of design and the good results it provides, an LC filter was deemed sufficient. A study analysing the harmonics and filter design is presented in [7-8]. Since there are different passive filters that can be used as low pass filter for a MLC a short review of the most commonly used filters is provided in the following section.

### 7.2.1 – L filter

An L-filter is a filter formed with an inductor connected in series with the output of the converter as shown in Figure 7.1. A resistor in series is normally considered in this circuit as the inductor can possess a winding resistance which affects its performance. The attenuation of this first order filter is 20 dB/dec.

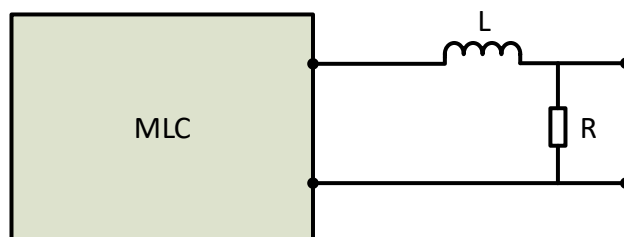


Figure 7.1 L-filter

The corner frequency of this filter is given by

$$f_c = \frac{R}{2\pi L} \quad (7.1)$$

### 7.2.2 – LC filter

The filter shown in Figure 7.2 corresponds to the LC low pass filter. It is a second order filter with an attenuation of 40 dB/dec.

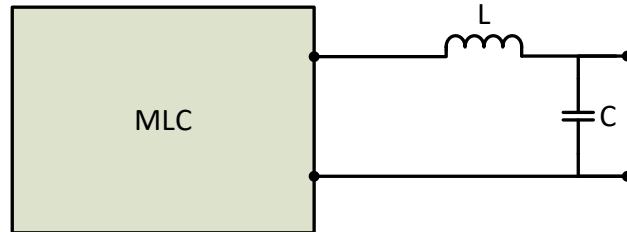


Figure 7.2 LC-filter

The corner frequency of this filter is given by:

$$f_c = \frac{1}{2\pi\sqrt{LC}} \quad (7.2)$$

And the transfer function of the LC filter is given by the equation 7.3

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{(2\pi f_c)^2}{s^2 + 2\zeta(2\pi f_c)s + (2\pi f_c)^2} \quad (7.3)$$

Where  $\zeta$  is the damping ratio and the quality factor  $Q$  can be expressed as:

$$Q = \frac{1}{2\zeta} \quad (7.4)$$

The characteristic of this filter is that is simple to design and implement. For frequencies lower than the corner frequency it has no gain. However, at the corner frequency,  $f_c$ , the gain peaks and a damping circuit is required to minimise this effect.

### 7.2.3 – LCL filter

The LCL filter, shown in Figure 7.3 can be seen as the LC filter presented before with another inductance ( $L_g$ ) in series

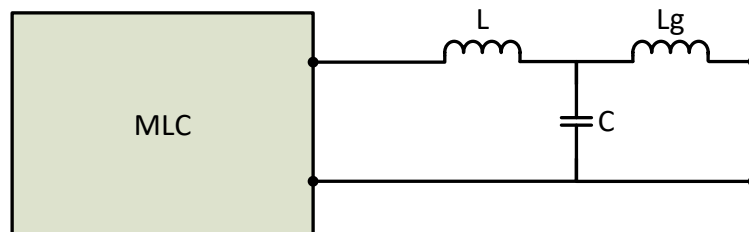


Figure 7.3 LCL filter

The corner frequency of the LCL filter is given by (7.5).

$$f_c = \frac{1}{2\pi} \sqrt{\frac{L+L_g}{L*L_g*C}} \quad (7.5)$$

This filter has an attenuation of 60 dB/dec. The LC and LCL filter have similar responses around the corner frequency that can cause disturbances at that particular frequency.

#### 7.2.4 – Damping circuit

The use of the low pass filter can be aided by a damping circuit to reduce the components at corner and higher frequencies. There are two different damping circuits presented in this section, both applied to a LCL filter. Simulation results with R and RC damping circuits are therefore presented in this section. The complete circuit diagram of the MLC and the filter is shown in Figure 7.4 Simulations were performed with VDC=155V that corresponds to the peak voltage to generate a 110VAC, LfA=LgA=LfB=LgB = 100μH, CA=CB=20μF and Rload=50Ω and fsw=40kHz.

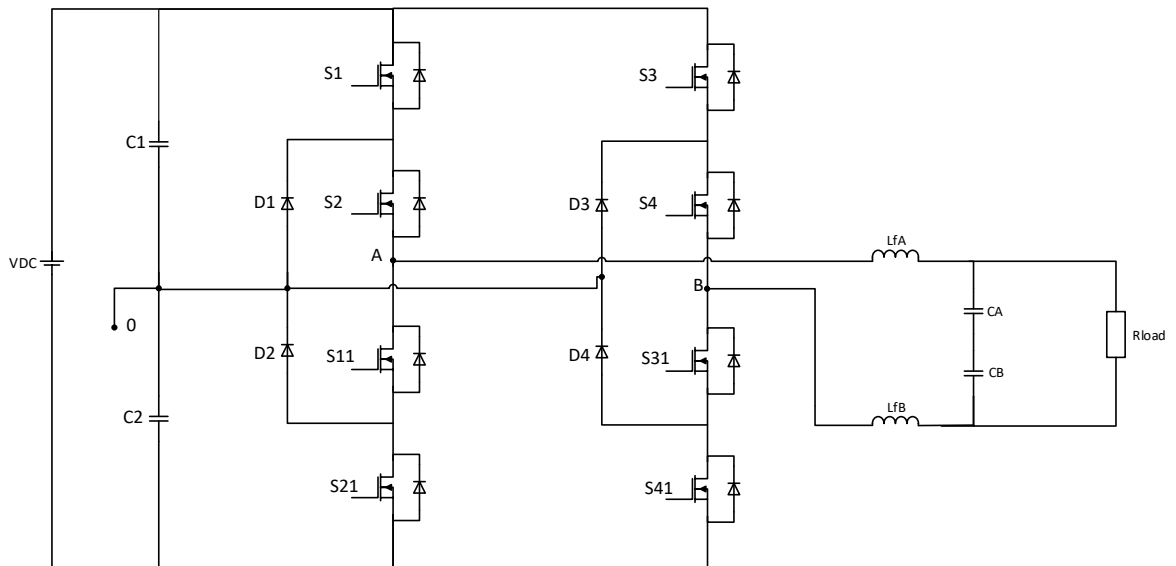
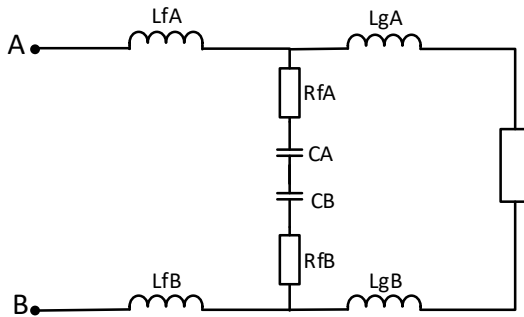


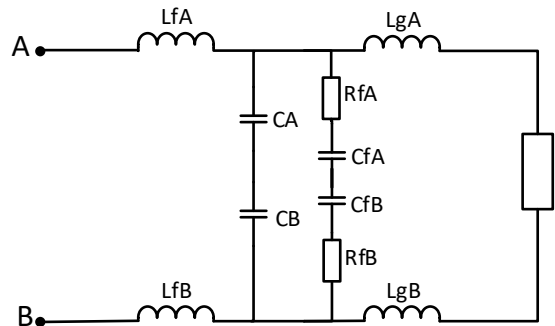
Figure 7.4 MLC with LC filter

To reduce the peak at the resonant frequency, two passive damping circuit were tested to evaluate their performance. The R damping circuit shown in Figure 7.5, a resistor is

connected in series with the LCL filter capacitor. In Figure 7.6, the RC damping circuit is presented, it connects in parallel with the LCL capacitors. The values of  $R_{fA}$  and  $R_{fB}$  to be evaluated range from 0 to  $2.5\Omega$  and for  $C_{fA}$  and  $C_{fB}$  from  $1.5\mu\text{F}$  to  $2.5\mu\text{F}$ .

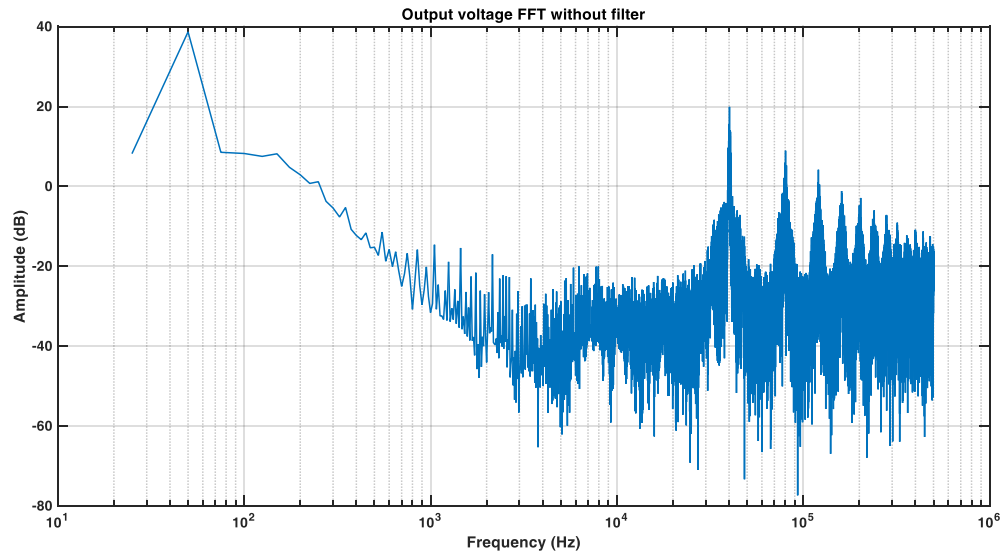


**Figure 7.5 R damping circuit**



**Figure 7.6 RC damping circuit**

The output voltage FFT in Figure 7.7, shows the frequency components of the signal without filter. The components of interest are at 50 Hz and 40 kHz with their respective harmonics.



**Figure 7.7 Output voltage FFT without filter**

In Figure 7.8, the simulation results for the R damping circuit is presented using different resistor values  $R_{fA}=R_{fB}$ . It can be seen that the 40 kHz component is attenuated as the value for R increases but the higher frequency components are poorly attenuated.

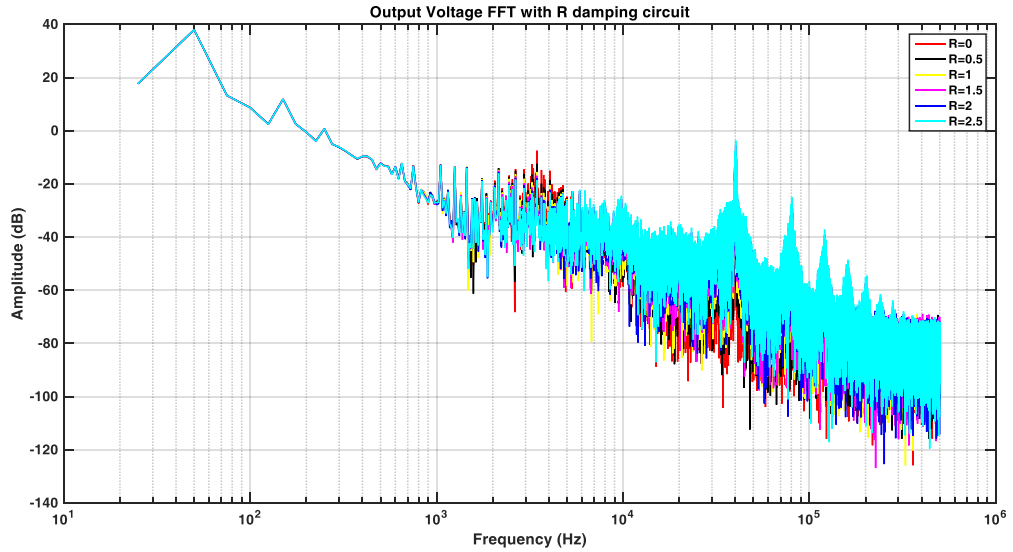


Figure 7.8 Output voltage FFT for the R damped LCL filter with  $R_{fa}=R_{fb}=0\Omega, 0.5\Omega, 1\Omega, 1.5\Omega, 2\Omega$  and  $2.5\Omega$

The results presented in Figure 7.9 correspond to the simulation with the RC damping circuit, it can be seen that the behaviour is almost the same for 4 of the cases. At higher frequencies, as the value of R and C increases, the amplitude of these components is more attenuated.

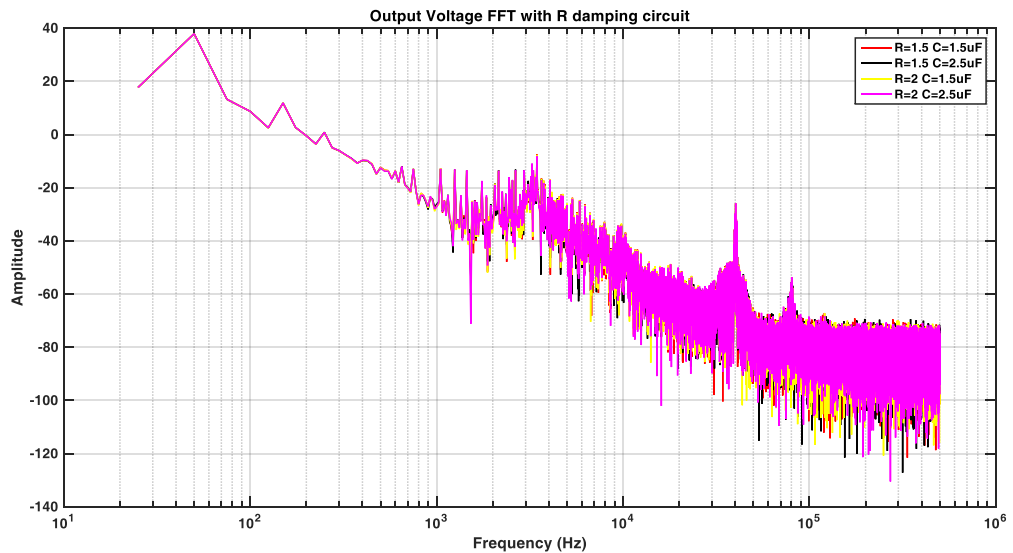


Figure 7.9 Output voltage FFT for the RC damped LCL filter with  $R=1.5\Omega C=1.5\mu F, R=1.5\Omega C=2.5\mu F, R=2\Omega C=1.5\mu F, R=2\Omega C=2.5\mu F,$



A comparison of both circuits, R and RC is presented in Figure 7.10 taking the higher values of R and RC evaluated during these set of simulations and it can be concluded that the best result is obtained with the RC damping circuit at high frequencies.

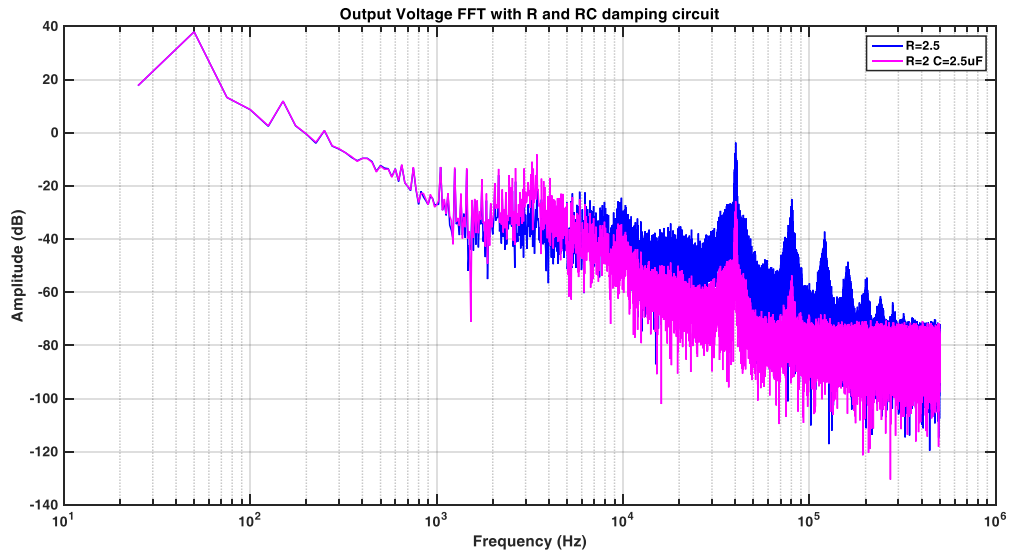


Figure 7.10 Output voltage FFT with  $R=2\Omega$   $C=2.5\mu F$  and  $R=2.5\Omega$

### 7.3 – Power Quality

One of the main aims when designing a power supply, in this case an inverter, is the reliability of the converter. As important as the reliability is the power quality that the converter will provide specially when employed in critical areas such as hospitals, avionics, production lines and any other where poor power quality may damage or affect the operations that are critical. Power quality refers to the voltage level, frequency and harmonics.

There are external factors like weather adversities, power cuts or the ones due to the power distribution which affect power quality, but these are out of scope for this study. However, there are also distortions caused by the loads or appliances connected to the local network. These loads demand non-sinusoidal currents from the grid, and they can be classified in 2 groups [7-9]. First group is the known loads such as high power converters and rectifiers. The second group is the unknown loads, in this group there are domestic appliance power supplies, computers, lighting and in general any electronic device connected to the grid found in a regular home. The second group is of particular interest because they generate greater effects and distorts the power line quality than the known loads.

The power demanded by the unknown loads introduces harmonics to the power grid. The increase of low order harmonics in the grid like those dominant harmonics introduced by these loads can create problems for other devices connected to the same node in the grid. The most common problems due to the harmonics are device overheating, insulation defects, and faults on measurement, control and protection systems.

Due to this, it is essential to design power converters that introduce less disturbances to the grid in order to improve the power quality of the grid. The use of MLC can reduce the amount of harmonics introduced to the power grid with a higher number of levels which leads to the use of smaller filters compared to the 2-level inverters.

The Total Harmonic Distortion (THD) gives a measure of how different is a waveform from its fundamental component and it is defined as follows.

$$THD = \frac{\sqrt{V_{t_{rms}}^2 - V_1^2}}{V_1} * 100 \quad (7.6)$$

The term  $V_1$  is amplitude of the fundamental,  $V_{t_{RMS}}$  is the RMS voltage and the result is given as a percentage. The lower the value, the closer the waveform is to the fundamental component.

### 7.3.1 Norms and standards

The energy clients, or the end users of the electricity expect to receive or buy good quality energy in terms of a constant voltage level, frequency and low harmonic content. This can be compared to an actual product or service, where buyers look for high quality, reliable, reasonable cost while protecting the environment. Therefore, requirements are placed on electrical equipment manufacturers to ensure their system do not substantially affect energy quality.

In recent years, more emphasis has been made on the power quality. Specialised institutions like IEEE (Institute of Electrical and Electronic Engineers), IEC (International Electrotechnical Commission), CENELEC (Comite Europeen de Normalisation Electrotechnique) and BSI (British Standards Institution) among others have developed standards and measurement methods to evaluate products in the power industry.

The BSI norm that regulates the Electromagnetic Compatibility (EMC) is the BS EN 61000. The compatibility is defined as the ability of an equipment to work properly in an

electromagnetic environment and not to induce any intolerable interference to it. The interference is an emission produced by an equipment, in this case a power supply producing an AC waveform at 50 Hz with the related harmonics, the distortion caused by the harmonics polluting a signal is given by the THD. This norm is presented in three main parts [7-10]. Part 2 is referred as the EMC environment, describes the environment and different perturbations on different applications. Part 3 covers the limits divided in different categories. Lastly, part 4 describes the testing and measuring techniques.

For this work, part 3 and 4 are applicable. BS EN 61000-3-2 is the section of part 3, presents the emission limits applicable to electrical and electronic devices with input current of less than 16 A per phase and designed to connect to the grid. The devices are then classified into 4 different groups. The MLC designed for this work, falls into the class A devices. The THD limit according to the norm must be equal or less than 8% up to the 40<sup>th</sup> harmonic (N=40).

Part 4 provides details on the measuring techniques for the range of voltages that the MLC designed to work, the requirement is that the observation period is a short cyclic of 10 or more cycles and the repeatability must be of  $\pm 5\%$ .

### 7.3.2 MLC harmonic evaluation

In order to evaluate the THD of the output voltage and current, the LC low pass filter was added to the output of the converter as shown in Figure 7.11. The voltage at the load resistor waveform is captured and the THD is calculated for 10 cycles of 50 Hz sinewave according to the norm presented in the previous section.

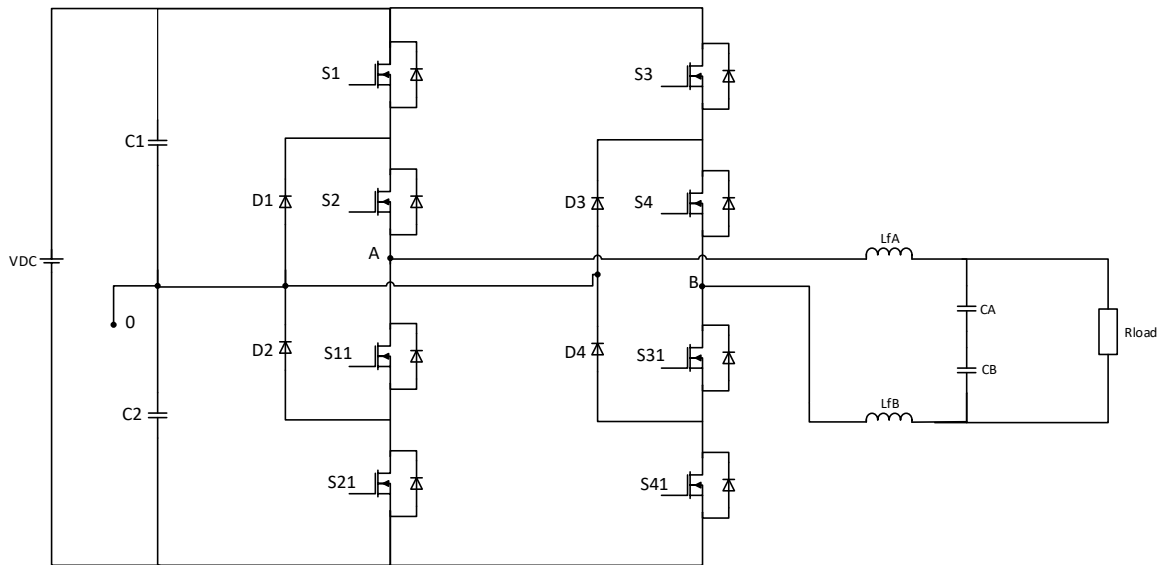


Figure 7.11 MLC with LC filter

The waveform shown in Figure 7.12 is the output voltage without filter. Using the low pass filter described previously the output of the MLC is presented in Figure 7.13

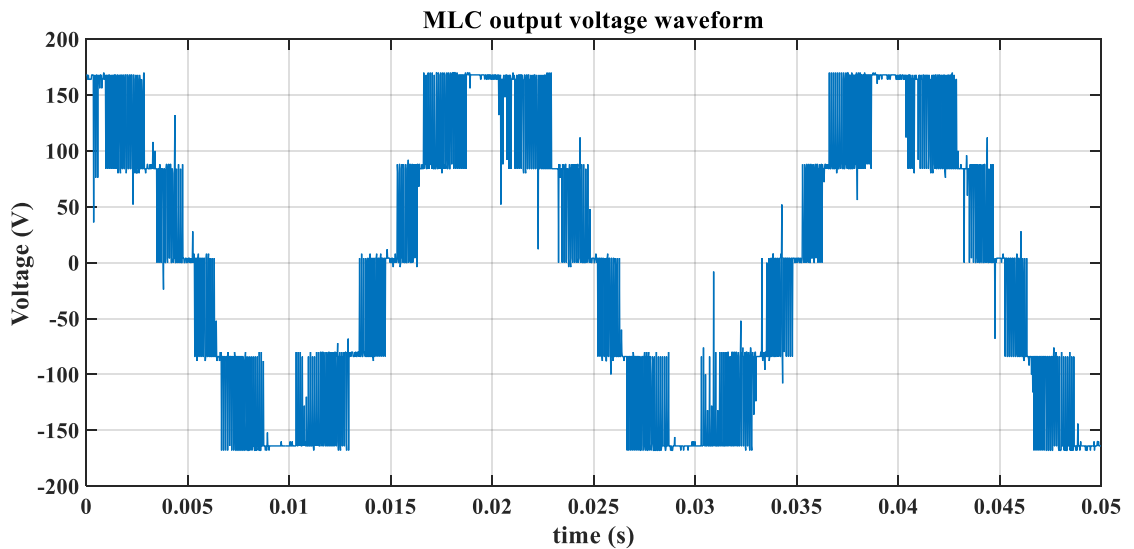


Figure 7.12 Output voltage waveform

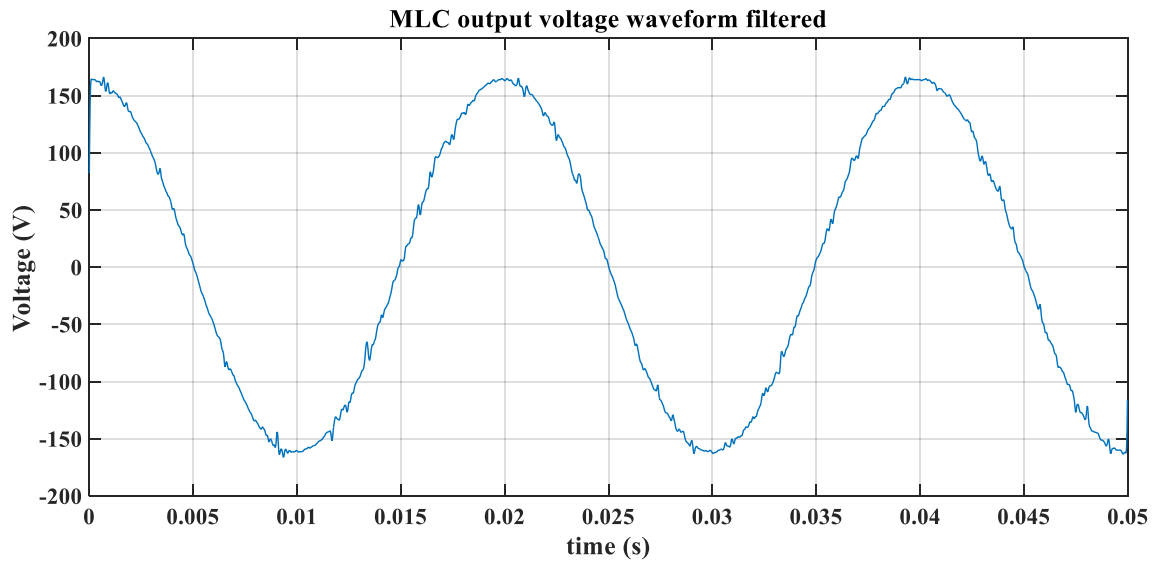


Figure 7.13 Filtered output voltage waveform

It can be seen from Figure 7.13 that the filter has attenuated the high frequency switching compared to the voltage waveform in Figure 7.12. The voltage level is 110 V rms and the THD for this particular waveform is 2.85% which complies with the norm.

### 7.3.1 THD comparison Si and SiC

Motivated by the requirement of greater power quality, an evaluation of the THD for the MLC designed was carried out. A set of tests were used to determine the THD at different dead time intervals and operating frequencies. The MLC is controlled with an FPGA providing the PWM using space vector modulation presented in previous chapters.

The dead time to prevent two switches operating at the same time in a leg of the converter is also controlled by the FPGA. The FPGA works with a 40 MHz clock, so the minimum interval time that can be applied is 5 ticks of the FPGA clock (125ns).

Si and SiC devices are evaluated in this work as described in the previous chapter. Table 7.1 details the switching characteristics of the MOSFETs evaluated.

Device	Turn-on delay time (ns)	$V_{DS}$ rise-time (ns)	Turn-off delay time (ns)	$V_{DS}$ fall time (ns)
N95	18	16	50	21
FDP	23	26	50	15
SiC040	15	52	26	34
SiC280	5.2	7.6	10.8	9.9

Table 7.1 Switching times of the devices evaluated

It can be seen that the fastest device according to the turn-on delay is SiC 280 followed by SiC040 and N95 then FDP. In terms of the rise-time, SiC 280 has the best timing followed by N95 then FDP and SiC040. For the turn-off delay time SiC280 has the shortest delay followed by SiC 070 and finally N95 and FDP with the same delay. SiC280 has the shortest fall time followed by FDP then N95 and finally SiC040.

The MOSFETs are operated under the same conditions except for the dead time that will vary according to the conditions described. The test was performed for the range of frequencies from 20 kHz to 100 kHz in steps of 10 kHz. The voltage waveform is captured with an oscilloscope then the THD is computed in MATLAB.

The results of these tests are presented in the following section for different adjusted dead time, minimum (5 ticks) and maximum (9 ticks).

#### 7.3.1.1 THD with different dead time

According to the table above, the dead time was calculated and applied to the MLC, the dead times are detailed in Table 7.2 The dead time was obtained by adding the rising and falling times then rounded to the nearest integer number of FPGA clock ticks that the system can generate effectively, starting from 5 ticks (125ns).

<b>Device</b>	<b>Dead time (ns)</b>	<b>Dead time in ticks</b>
SiC 280	125	5
SiC 040	225	9
Si FDP	205	8
Si N95	175	7

Table 7.2 Dead time in ns and ticks

The results presented in Figure 7.14 correspond to the evaluation of the THD with the different dead times presented above.

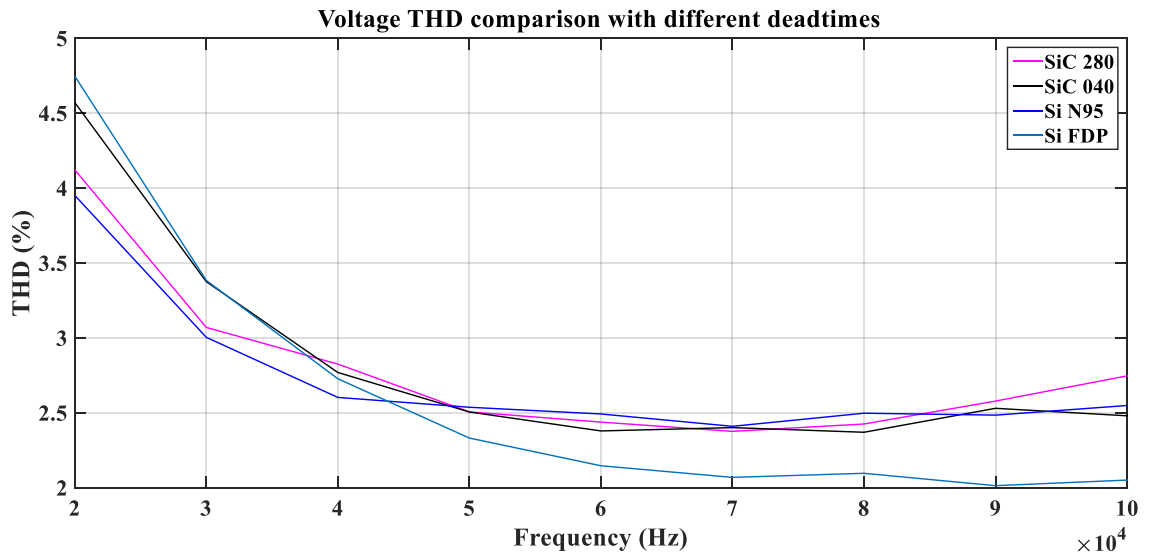


Figure 7.14 THD comparison with different dead time.

For the range of frequencies from 20 kHz to 40 kHz, the largest THD corresponds to Si FDP, followed closely by SiC 040 with a THD of 4.6 to 4.7 % and with a THD of 3.9% to 4.1% is Si N95 and SiC 280 respectively. For the highest frequencies Si FDP gives the lowest THD with 2% compared to the others with a THD of between 2.5 % and 2.7%. Si FDP gives the lowest THD at high frequencies this is possibly due to reduced susceptibility to fast transients compared with the other MOSFETs.

The set of results presented in this subsection correspond to an evaluation with an different dead time. In the following section, a set of tests with minimum and maximum dead time is presented.

### 7.3.1.2 THD with minimum dead time

After the test with different dead times, a test with the minimum dead time that the FPGA can effectively generate of 5 ticks which corresponds to 50 ns. The results for this series of tests are presented in Figure 7.15.

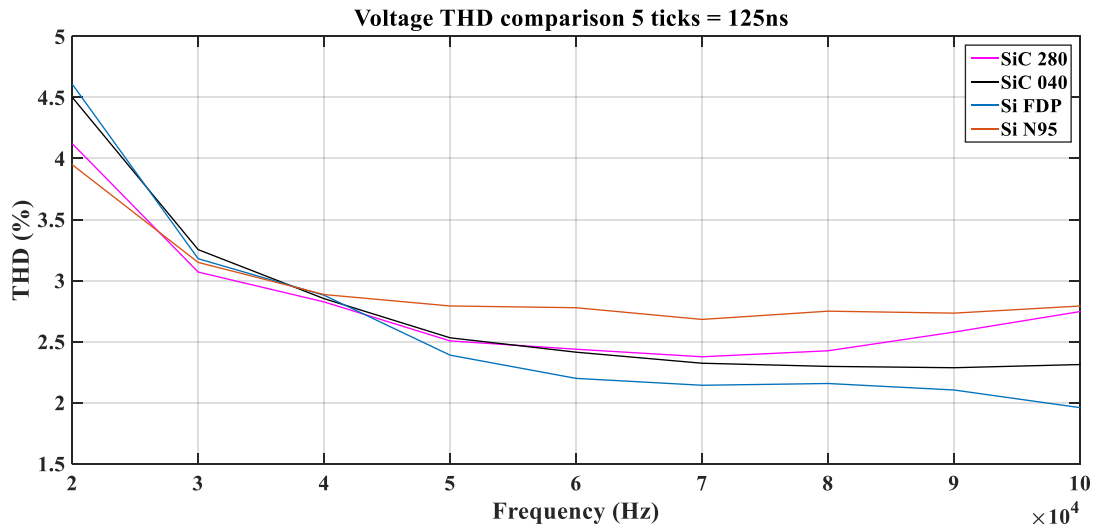


Figure 7.15 THD comparison with 5 ticks

Here it can be seen that for the frequencies from 20 kHz to 50 kHz Si FDP and SiC040 give a THD of 4.6% and 4.4% respectively. The THD for the highest frequencies Si FDP gives the lowest THD with 2.2% followed by SiC040 with a difference of only 0.1%. The THD for SiC 280 and Si N95 is the largest for these range of frequencies with THDs of 2.6% and 2.7% correspondingly.

### 7.3.1.3 THD with maximum dead time

Followed by the minimum dead time, a series of test with the maximum dead time was performed. The dead time used is 9 ticks of the FPGA clock that gives an effective dead time of 150 ns. The results are presented in Figure 7.16

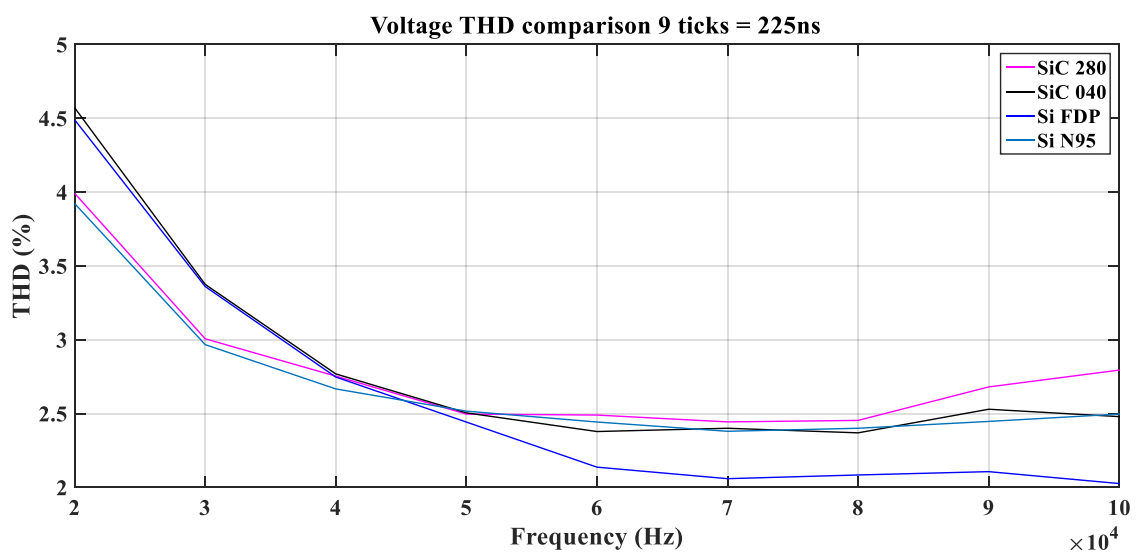


Figure 7.16 THD comparison with 9 ticks



The THD obtained at the range of frequencies from 20 kHz to 40 kHz of 4.6% and 4.5% with SiC040 and Si FDP respectively followed by SiC280 and Si N95 with a THD of 4% and 3.9%. For the higher frequencies Si FDP provides the lowest THD of 2% followed by SiC040 with 2.4% followed closely by Si N95 and SiC 280 with a THD of 2.7%

#### 7.3.1.4 THD with minimum and maximum dead time

In this section, the results obtained are presented as a comparison of the THD generated with the minimum and maximum values of dead time for each device.

The device SiC 280 shows in Figure 7.17 for higher frequencies a lower THD of 2.25% with the minimum dead time compared to 2.4% with the maximum dead time.

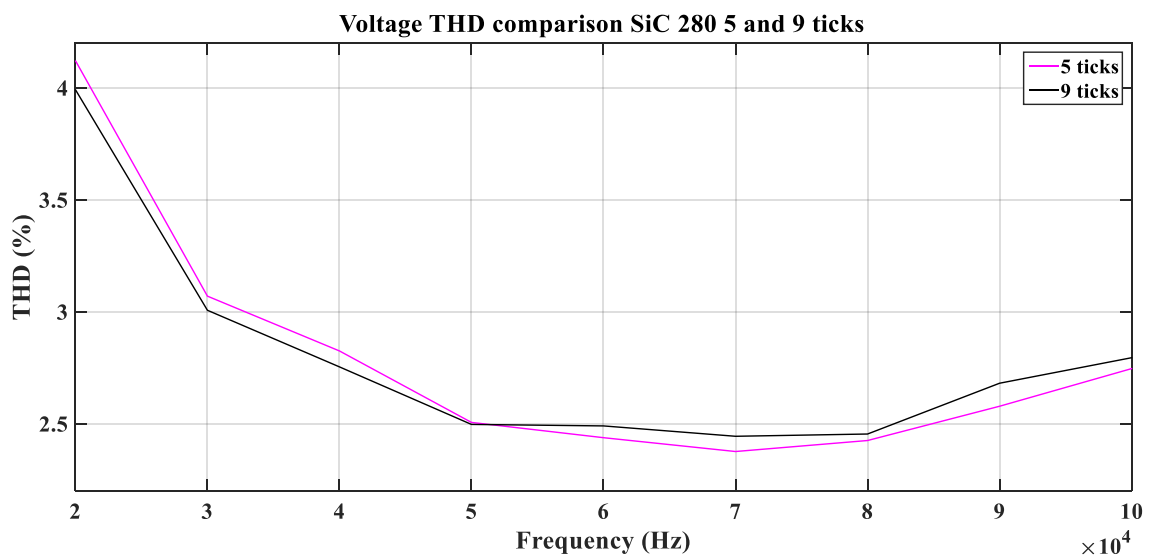


Figure 7.17 SiC 280 THD comparison

Figure 7.18 shows the comparison results of SiC 040 which similar to SiC 280 the THD at higher frequencies is lower with the minimum dead time with a value of 2.2% compared to 2.5% found with the maximum dead time at 90 kHz.

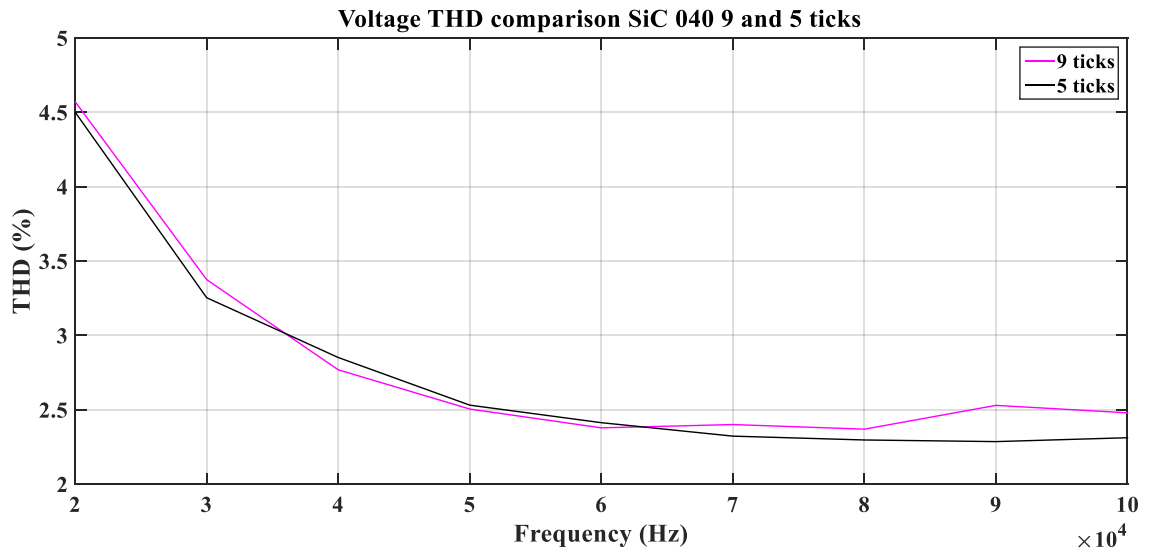


Figure 7.18 SiC 040 THD comparison

The silicon counterparts' results are presented next. In Figure 7.19 the comparison for Si FDP the THD found was followed closely for both minimum and maximum dead times. For most of the frequencies tested, the lowest THD obtained was with the maximum THD of 9 ticks.

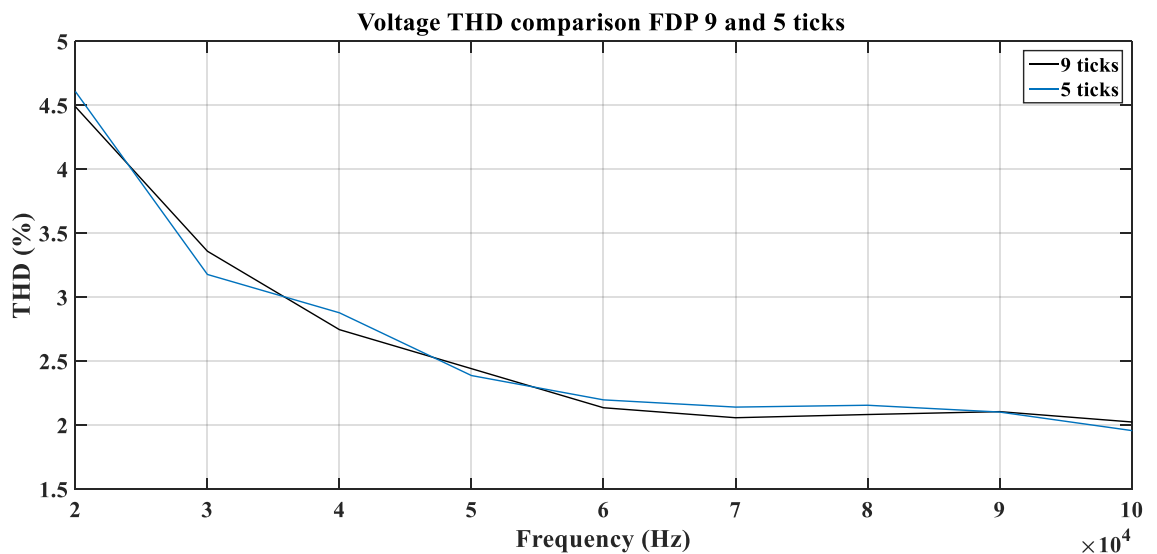


Figure 7.19 Si FDP THD comparison

The Si MOSFET N95 results are presented in Figure 7.20 for this device, the lowest THD obtained was with 9 ticks that corresponds to the maximum dead time with a lowest value of 2.39% compared to 2.7% at 70 kHz for the minimum dead time.

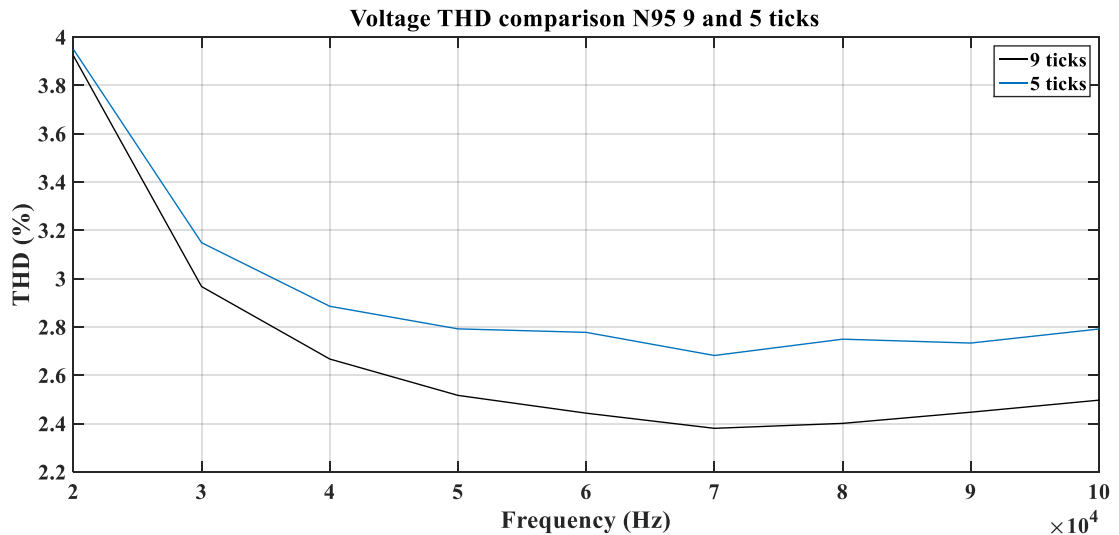


Figure 7.20 Si N95 THD comparison

The results obtained in the comparison with the different dead time and maximum and minimum dead times showed that Si FDP gives the lowest THD followed alternatively by SiC 040 or SiC 280. Looking at the output capacitance of the Si FDP device it was found that the value of 925 pF may be influencing the results obtained for these series of THD evaluation tests. The output capacitance value for the other devices ranges from 23 pF for SiC 280, 117 pF for Si N95 and 150 pF for SiC 040. Moreover, Si FDP has the lowest  $R_{DS(on)}$  and highest input capacitance compared to the other devices.

Evaluating the comparison of the THD with minimum and maximum dead time for each device it was found that for the SiC devices, the lowest THD obtained is with the minimum dead time. Whereas for the Si devices, the lowest THD was generated with the maximum THD. This proves that the SiC devices can operate faster and perform better with lower dead times. In general the THD with SiC devices show a trend to decrease and then increase with frequency, this can possibly be due to SiC devices susceptibility to transients introduced by fast changes in drain to source voltages resulting in a wrong switching behaviour. This can be minimised with the use of high-frequency optimised gate driver.

#### 7.4 – Conclusion

In this chapter, the evaluation of the THD of the topology studied is discussed. The requirement of a filter in the output of the MLC is necessary to reduce the harmonic content and to keep the THD as low as possible to deliver a clean signal. There are multiple implications of a high harmonic content that increase the operating temperature

of the switching components, cables or even the appliances the converter is connected to, consequently reducing the reliability of the system.

The evaluation of the THD as a function of frequency for different values of dead time has been presented in this chapter. It has been found that the THD is a function of dead time and frequency considering the results obtained and discussed in the previous sections.

It has also been proved that the THD can also be reduced using different semiconductors as SiC, these devices have shown to generate lower THD at lower dead times. This can represent a benefit not only to the system powered with the MLC but also to the overall efficiency of the converter.

In the following chapter, a conclusion of the work presented in this thesis will be presented and the future work will also be discussed.

## 7.5 – References

- [7-1] Mog, G. E., & Ribeiro, E. P. (2004, November). Total harmonic distortion calculation by filtering for power quality monitoring. In *Transmission and Distribution Conference and Exposition: Latin America, 2004 IEEE/PES* pp. 629-632
- [7-2] Yousefpoor, N., Fathi, S. H., Farokhnia, N., & Abyaneh, H. A. (2012). THD minimization applied directly on the line-to-line voltage of multilevel inverters. *IEEE Transactions on industrial electronics*, 59(1), pp. 373-380.
- [7-3] Farokhnia, N., Vadizadeh, H., Kadkhoda, F., & Vahabzadeh, A. (2010, June). Formulation of the line voltage THD, case I: Multilevel inverter with equal DC sources. In *Power Electronics Conference (IPEC), 2010 International* pp. 1244-1251
- [7-4] Farokhnia, N., Vadizadeh, H., Fathi, S. H., & Anvariasl, F. (2011). Calculating the formula of line-voltage THD in multilevel inverter with unequal DC sources. *IEEE Transactions on Industrial Electronics*, 58(8), pp. 3359-3372.
- [7-5] Sala, V., Salehi, R., Moreno-Eguilaz, M., Salehifar, M., & Romeral, L. (2012, October). Clamping diode caused distortion in multilevel NPC Full-Bridge audio power amplifiers. In *IECON 2012-38th Annual Conference on IEEE Industrial Electronics Society* pp. 4941-4948
- [7-6] MOSELY, I. D.; MELLOR, P. H.; BINGHAM, C. M. Effect of dead time on harmonic distortion in class-D audio power amplifiers. *Electronics letters*, 1999, vol. 35, no 12, p. 950-952.

- [7-7] LETTL, Jiri; BAUER, Jan; LINHART, Libor. Comparison of different filter types for grid connected inverter. En *PIERS Proceedings*. 2011. pp. 1426-1429.
- [7-8] KIM, Soo-Hong, et al. Harmonic analysis and output filter design of NPC multi-level inverters. En *37th IEEE Power Electronics Specialists Conference (PESC '06)*. 2006. p. 1-5.
- [7-9] H. Akagi, (1994). Trends in Active Power Line Conditioners, *IEEE Transactions on Power Electronics*, Vol. 9, No. 3, pp. 263-268
- [7-10] IEC, B. S. 61000. *Electromagnetic compatibility (EMC)*, 1998

## Chapter 8 – Conclusion and further work

### 8.1 Conclusion

The thesis has presented the systematic analysis, design and experimental validation of a grid connected Five Level Full Bridge Neutral Point Clamped (5L-FB-NPC) multilevel converter. The intended application for this is a battery-powered inverter to for use on a construction site with the expectation of using 2<sup>nd</sup> life electric vehicle battery packs. The work also included a comparative study of the effects of using SiC power devices, the findings of which has been presented at IET PEMD 2016.

Chapter 2 explored the background literature to the field of research reviewing the different multilevel converter topologies and comparing their relative merits in terms of complexity, number of switching devices & capacitors, voltage range, etc. From this investigation, although the Cascaded H-bridge (CHB) can generate the same number of levels with the same number of switching devices and no clamping elements, it requires separate DC-sources per level. The 5L-FB-NPC was selected as the desired MLC topology for the intended application because it offered reduced number of switches and output voltage range with a single battery pack. This chapter also introduced the concepts of modulation to generate specific output voltage waveforms.

A detailed description of modulation techniques for various multi-level converters was provided in Chapter 3. The purpose of this work was to review current state of the art techniques and compare their total harmonic distortion (THD) performance and voltage level balancing when used to provide the gate signals for the main multilevel converter topologies. Simulink simulations were used throughout the investigations to evaluate performance. Sinusoidal PWM was used to introduce the main concepts of modulation, output voltage level generation and waveform spectra. However, due to the ease of implementation in the FPGA for a single-phase converter, a space vector modulation (SVM) is introduced. SVM provided a greater control for the MLC capacitor balancing and control of the switching sequence. A detailed simulation investigation of the nearest two vectors (N2V) modulation technique was given and the results showed good performance on balancing the capacitor voltage as well as producing the correct vector sequence to generate the low-distortion 5-level voltage waveform. The findings of this chapter informed the design and the implementation of the modulator used in the hardware platform.

The design and implementation of the hardware platform used for the experimental investigations presented later in the thesis was described in Chapter 4. The chapter discussed the requirements for the construction site battery powered inverter system and its functionality. For the system to provide bi-directional power flow between the battery and the grid and/or power tool the system AC-DC conversion stage to provide high-power factor low distortion grid currents and a buck-boost converter stage for battery management. A description of the systems operation and the design of the individual conversion stages is presented alongside simulation results to validate their design.

The integration of the converters is evaluated through simulation and the feasibility to use the proposed topologies in the intended application is evaluated. A major contribution of this chapter is the Co-Simulation of the power electronic circuitry and controller using the National Instruments (NI) Multisim and its following implementation using the NI LabVIEW platform which incorporated a FPGA to provide fast and accurate timing control for the modulator and analogue signal acquisition. Multisim Co-Simulation provided a robust platform for the evaluation of the MLC, this platform enables the test of both, the circuits in the converter using high-fidelity models of the components, including gate driver and MOSFETs, and the FPGA code. This feature allows to simulate the analog and digital parts of the system in a single simulation to obtain accurate simulation results.

The NI co-simulation platform required a somewhat different approach to Simulink as the loop time required consideration when developing control algorithms. It is worth mentioning the protracted time taken to compile the LabVIEW FGPA code to VHDL. For example, a single LabView FGPA code change would take over 1 hour to compile successfully. However, once a design has been finalised changing parameters such as PWM frequency, dead-times and reference levels is very easy and the system would operate reliably.

Chapter 5 covered the systematic experimental evaluation of the base platform converter when operating under different battery and grid voltage. The individual conversion stages were evaluated in isolation and then integrated and then operated together. Comparison with simulation results from NI Multisim co-simulation and the experimental results demonstrated that whole system operated as expected.

Chapter 6 compared the performance of the converter platform when operated with different power device technologies. Second generation devices of SiC MOSFETs and Si MOSFETs evaluated were chosen for their low  $R_{DS\ on}$  (SiC 040 and Si FDP) and for the similarity in current and voltage ratings (SiC 280 and Si N95). Overall, the performance of SiC devices was significantly better with lower temperature rise, which would allow the reduction of size as the cooling systems required by these devices are smaller. Although the temperature rise with Si FDP and SiC 040 appears to be close, the SiC competitor gives lower temperature rise at higher frequencies. Furthermore, the reliability of the SiC devices should be greater as the Si N95 operates at 85% of its voltage rating compared to less than 10% of SiC 040 rating. For the work presented here, the control and modulation scheme remained unchanged and therefore it may be possible to modify the control to decrease switching losses for the different frequencies considered which could reduce the temperature rise in the devices and improving the overall efficiency and is currently under investigation. The findings of work described in this chapter was presented at IET PEMD 2016.

Finally, Chapter 7 investigate the THD performance of the converter with the different switching devices for a range of switching frequencies. The norms and standards associated with power quality and THD are introduced alongside the commonly used input filter topologies. Simulation was used to evaluate the performance of the different input filters and damping circuits. An experimental evaluation of the THD as a function of frequency for specific values of dead time was presented and it was found that the SiC devices could offer improved THD performance at higher frequencies with lower dead times. This can represent a benefit not only to the system powered with the MLC but also to the overall efficiency of the converter.

## 8.2 Further work

The research described in the thesis has revealed a number of opportunities for further work. Below is a description of a number of avenues suitable for further investigation.

### *Modulation improvements*

As has been described in the review chapters and demonstrated using both simulation and experiments, the chosen modulation techniques can have a significant impact on the performance of the converter. Research in this area falls into three categories: i) reducing the number of switching events; ii) improve output waveform (lower THD) and iii)



provide better capacitor balancing. All of these are inter-related and it may be possible to improve all three aspects by developing new space-vector algorithms. A final consideration is the possibility of redistributing the losses of the power devices to homogenize the loss distribution and also minimize power cycling, both of which could improve the reliability of the converter.

#### *High-frequency operation*

Operating at high-frequencies would allow the size of the reactive components (filter and DC link and voltage level capacitors) to shrink thereby reducing volume and weight and so increasing power density. In order to do this the thesis has shown that low-loss high-frequency power devices are needed. This work has also shown that the dead-time and modulation will be needed to be optimized.

#### *Comparison of SiC and Si with GaN power devices at high-frequency*

GaN represents another attractive device technology in terms of its high-speed performance. The experimental investigation presented in Chapter 6 could be extended to include GaN devices to see the relative merits of each technology when operating at high frequencies (>250kHz).