Device Modelling of Silicon based High-Performance Flexible Electronics

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***Abstract*— The area of flexible electronics is rapidly expanding and evolving. With applications requiring high speed and performance, ultra-thin silicon-based electronics has shown its prominence. However, the change in device response upon bending is a major concern. In absence of suitable analytical and design tool friendly model, the behavior under bent condition is hard to predict. This poses challenges to circuit designer working in the bendable electronics field, in laying out a design that can give a precise response in a stressed condition. This paper presents advances in this direction and investigates the effect of compressive and tensile stress on the performance of NMOS and PMOS transistor and a touch sensor comprising a transistor and piezoelectric capacitor.**

Keywords— Flexible Electronics; Ultra-thin silicon; E-Skin; Device Modelling; CMOS

I. INTRODUCTION

Miniaturisation led growth in microelectronics over last five decades have transformed our lives through fast communication and computing. However, recent advances push More than Moore concept in the field dominated by applications such as Internet-of-Things, mobile healthcare, smart cities, energy autonomous appliances etc.[1, 2] Very often, these applications require electronics to conform over 3D surfaces and this calls for new methods to realise devices on unconventional substrates such as plastics as illustrated in Fig.1. For example, in the electronic skin, various types of sensors and electronics need to be integrated over flexible substrates so that it can be placed over curvilinear body surface of a robot or prostheses[3-5].

Intrinsically flexible materials like organic semiconductors and 2D materials have extensively been used for realizing large area flexible electronics. Nevertheless, the associated low mobility and nascency in development stage has restricted their usage where high-performance is needed. On the contrary, Complementary metal-oxide-semiconductor (CMOS) technology dominates the field of high-speed electronics, with frequency of operation reaching up to tera-hertz. But due to mechanical rigidity of standard silicon wafer, it cannot be used in the application, which demands mechanical flexibility. In this scenario, ultra-thin silicon obtained by thinning down silicon from bulk wafer to ultra-thin regime (< 50 µm) provides an interesting avenue for addressing the need of high performance in flexible and stretchable electronics [6, 7]. The fabrication and performance evaluation of bendable silicon-based circuits

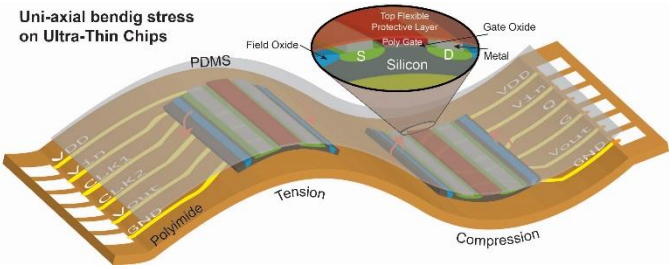

Figure 1: Illustration of ultra-thin chip on flexible substrate undergoing tensile and compressive strain

received significant attention during last decade[8, 9]. The various reports of device and simple circuit realized on thin silicon has shown deviation in response from standard or defined response upon bending. This change is mainly credited to stress, which is experienced by device during bending [10]. Therefore, when thin chips are placed over 3D surfaces, due to bending stress, their response is different from their bulk counterpart. Although, theoretical modelling of internally generated stresses like strained silicon, STI effect etc. have been extensively studied, effects due to externally applied stress and its implementation in theoretical model have less been studied [8]. A quantitative evaluation of stress-induced split of conduction band edge, its effect on effective mass of carriers and experimental demonstration of changes in effective mass has been presented in [11]. There have also been reports of analytical models defining the effect of stress on electronic transport of devices comprising mainly of changes in threshold voltage and mobility. The relation between normalized variation in mobility as a function of stress, device orientation and piezo resistive coefficient has been presented by Bradley et al. [12]. These shifts can change the performance of the system and lead to unreliability in its functioning. Similarly, a sensor which is using a semiconductor platform for sensing can give unexpected output under bending, if the effect of bending is not properly compensated. Therefore, for easing complex circuit design and predict their response under different bending condition precisely, it is necessary to understand these variations and develop improved design tools.

In this direction, [13] presents a SPICE based model for static and dynamic performance for amorphous silicon-based thin film transistor. Focusing more on material properties and considering the change in valence and conduction band structure during externally applied stress, [14] terms these changes as an

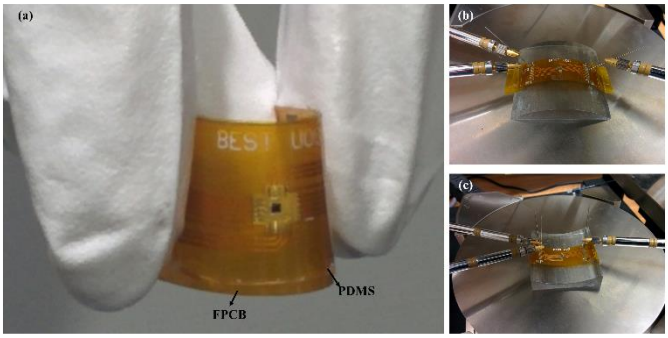

Figure 2: (a) Ultra-thin chip embedded between polyimide based PCB and PDMS layer (b) Device characterization under tensile bending condition (c) Device characterization under compressive bending condition

effective change of material itself. In another study, effects of self-heating and stress are included in Verilog-A for PSP 103.1[15]. However, a compact model, which can easily be implemented in design tools like Cadence, is presented and discussed in this paper. Furthermore, it is validated using experimental measurements on thin silicon based devices. The major advantage of this model is that once implemented in a design tool, it can be used for simulating any transistor-derived sensor or composed circuit.

This paper is organised as follow: Section II discusses in brief about the fabrication and packaging scheme employed for realising ultra-thin chips. The proposed model and its validation with the experimental results is presented in detail in Section III and finally concluding remarks are given in Section IV.

II. Fabrication & Characterization

A. Fabrication

The chips used in this work are fabricated in a standard CMOS technology in an external foundry. The channel width and length of NMOS and PMOS are (W_n/L_n = 4 µm/0.35 µm) and (W_p/L_p = 8 µm/0.35 µm), respectively. Once the front-end fabrication is over, die is partially diced to cut depth of 20 µm. This is followed by glueing the chip on grinding tape front-side down and coarse and fine grinding till the grinding depth reaches the cut depth. At this stage, ultra-thin bendable chips get separated and picked up for packaging on flexible printed circuit board (FPCB).

B. Packaging

Thin chips are picked up using vacuum pick tool and glued on FPCB using low-stress adhesive. After curing of glue at 60 degrees for 2 hours, thin chip experience combination of stresses, majorly arising due processing steps and packaging steps. Stress experience by a thin chip placed over a flexible substrate can be calculated from Stoney's formula:

$$\sigma_{chip} = \frac{E_s h_{sub}^2}{6h_{chip}(1-\vartheta_f)R} \quad (1)$$

where h_{sub} and h_{chip} are thickness of substrate and chip respectively, ϑ_f and E_s are substrate Poisson's ratio and Young's modulus respectively and R is bending radius. As can be observed that choice of substrate for packaging and position of chip plays an important role in defining the stress level. For reducing this stress, neutral plane concept has been used in this work [16]. After wire bonding, we cover the connection pad of FPCB with Kapton tape and spin coated PDMS over the exposed surface. Spin time of 30 sec and speed of 1000 rpm gives a thickness of around 25 µm. This soft material bring the chip near to the neutral plane of package and thus helps in increasing the bendability of package as shown in Fig.2(a).

C. Characterization

Electrical characterization of the flexible NMOS and PMOS devices in strained conditions is performed by adhering FPCB with a thin chip over 3D printed plastic structures, which replicates tensile and compressive bending condition as shown in Fig.2(b)-(c). Change in carrier mobility (Table I) and the threshold voltage is observed during the characterization in bent condition when compared to that of in planar condition.

III. Modelling and Validation

Most of the circuit simulators like PSpice, Cadence uses BSIM parameters which are geometry-independent parameters and their prediction is valid only for zero stress. Therefore, derivation of stress-dependent analytical equations and implementation on circuit simulation environments is essentials for understanding and predicting the behaviour of bendable devices. For the simulation of transistors under stress, it is important to identify those parameters which get affected due to stress and defining them as a function of stress magnitude and sensitivity to stress. Among major DC parameters of the transistor, threshold voltage and mobility play very important role in fixing the current level and can be written as a function of the magnitude of stress (σ) and sensitivity to stress (Π) [17].

$$\mu_{(stress)} = \mu_o\left(1 \pm \Pi_\mu \ .\sigma_\mu \ \right) \quad (2)$$

$$V_{th(stress)} = V_{th_0}\left(1 \pm \Pi_{V_{th}}.\sigma_{V_{th}}\right) \quad (3)$$

The current equation under stress is given by:

$$I_{D(stress)} = I_{D_0}\left(1 \pm \Pi_{I_D}.\sigma_{I_D}\right) \quad (4)$$

Here, Π is piezoresistive coefficient and represent the sensitivity of mobility/threshold/drain current to stress. Since, piezoresistive coefficient depends on direction of current flow, or channel orientation (θ), and direction of stress application (π), it can be written as:

$$\Pi = 1 - 2 \times \pi.\sin(\theta) \quad (5)$$

The bending stress magnitude can be calculated from chip's Young's modulus (E), thickness (h), bending radius (R) and geometry variation factor (ΔG):

$$\sigma = E.\frac{h}{2R}.\Delta G_{I_{D0}}(1 + \frac{\Delta G_{I_D}}{G_{I_D}}) \quad (6)$$

The above mathematical equations along with extracted parameters from BSIM4 are implemented in Verilog-A which enables circuit simulation in ASIC design process using Cadence. To validate the model, we compared the experimental

measurement of ultra-thin chip based NMOS and PMOS characteristics to the simulated data as shown in Fig. 3(a)-(d).

TABLE I: CARRIERS' MOBILITIES UNDER DIFFERENT BENDING CONDITIONS

	Planar	Tension 40mm	Tension 20mm	Compression 40 mm	Compression 20mm
NMOS	1229	1241	1251	1167	1159
PMOS	438	451	455	452	460

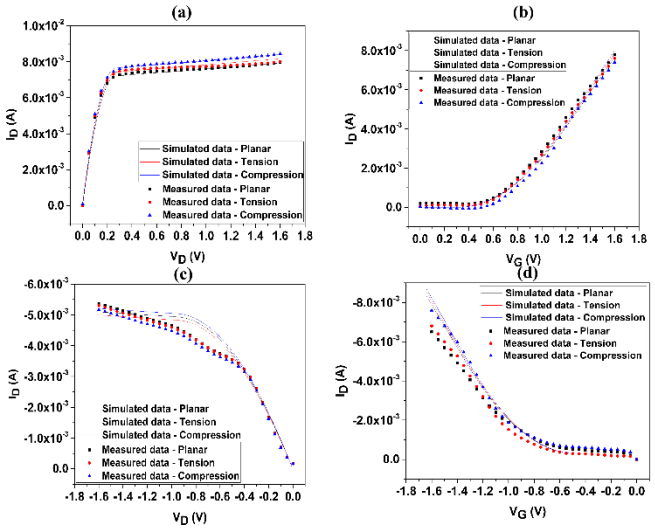

Figure 3: (a) Output characteristic of NMOS (b) Transfer characteristic of NMOS (c) Output characteristics of PMOS (d) Transfer characteristics of PMOS

To further extend the applicability of the bendable MOSFET model, we simulated the behaviour of CMOS-based touch sensor, which uses MOS transistor in combination with a piezoelectric layer over the gate area. This structure is termed as Piezoelectric Oxide Semiconductor Field Effect Transistor (POSFET), and can be used for detecting force/pressure using piezoelectric property of PVDF-TrFE [18, 19] as shown in Fig.4(a). The current equation of POSFET is obtained by modifying the standard current equation of transistor. In this equation there is a series combination of oxide capacitance (C_{ox}) and PVDF-TrFE capacitance (C_{PVDF}) represented as C_{stack}. An effective threshold voltage ($V_{th_{eff}}$), is formulated based on polarization charges and transistor's actual threshold voltage arising due to shift of remnant polarization charges (P_s, P_r) in piezoelectric material [20].

$$I_{ds} = \begin{cases} \mu_n C_{stack}\left(\frac{W}{L}\right)\left\{\left(V_{gs} - V_{th_{eff}}\right)V_{ds} - \left(\frac{1}{2}\right){V_{ds}}^2\right\} \\ \mu_n C_{stack}\left(\frac{W}{2L}\right)\left(V_{gs} - V_{th_{eff}}\right)^2 \end{cases} \quad (7)$$

where $$V_{th\_eff} = V_{th} - \left(\frac{P_s + P_r}{C_{ox}}\right) \quad (8)$$

On application of force, the piezoelectric layer of POSFET generates charge, which in turn modulates the gate voltage of the transistor. For empirical modelling of this response, POSFET is considered to comprise of two fully decoupled stages: electronic stage, which is the underlying bendable transistor, and electro-mechanical stage, which is a PVDF-

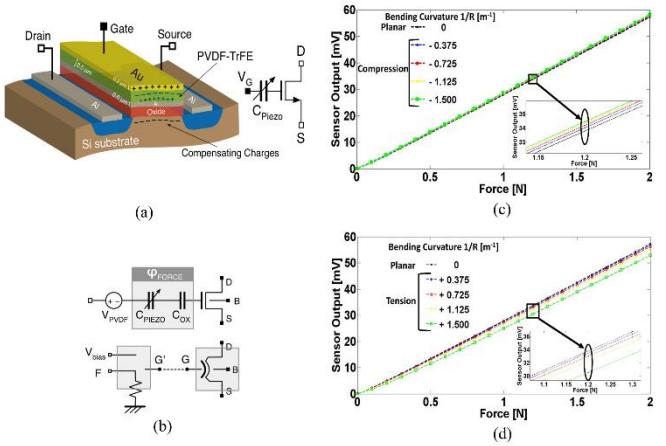

Figure 4: (a) Illustration of bendable POSFET (b) Verilog-A macro model of POSFET (c) Sensor output variation in compressive bending condition (d) Sensor output variation in tensile bending condition

TrFE layer. However, this assumption does not follow the condition of charge neutrality of the POSFET structure, given by:

$$\sigma_I + \sigma_P + \sigma_S = 0 \quad (9)$$

where σ_I, σ_P, and σ_S are the charge densities at the interface of gate electrode - piezoelectric polymer, in the bulk of the piezoelectric polymer, and in the semiconductor, respectively. Usually σ_s is much smaller than σ_I and σ_{P_S}, and constant with respect to the applied force, and therefore Eq. (9) reduces to:

$$\sigma_I + \sigma_P = 0 \quad (10)$$

With this assumption, the electronic stage can be considered as fully uncoupled from the electro-mechanical stage.

The effective gate voltage on application of force can be written as:

$$V_{gs_{eff}} = V_{gs} + \frac{d_{33}F}{C_{PVDF}} = V_{gs} + \Phi_{Force} \quad (11)$$

Due to change in gate voltage, the current level gets change and can be written as:

$$\Delta I_{ds} = \mu_n C_{stack}\left(\frac{W}{2L}\right)\left(V_{gs_{eff}} - V_{th_{eff}}\right)^2 - \mu_n C_{stack}\left(\frac{W}{2L}\right)\left(V_{gs} - V_{th_{eff}}\right)^2 \quad (12)$$

The output produced by sensor can be recorded as voltage by passing the current through a resistor [20].

To simulate the sensor response in Cadence environment, the voltage produced by PVDF-TrFE (denoted as Φ_{Force} in Fig. 4b) can be modelled as a linear voltage-controlled voltage source, whose value depends on the applied force and the C_{PVDF}. The macro-model shown in Fig. 4(b) is defined as two sub-circuit blocks. Pins V_{bias}, G', G, B, S, D stands for the top electrode bias voltage, the connection towards the gate of the transistor, the bulk, gate, source and drain of strained transistor, respectively. Terminal F is for force-dependent voltage source connected to a dummy transistor [21].

The proposed model for bendable POSFET sensors implemented in Verilog-A was used to simulate the sensor

response under compressive and tensile stress conditions, as is shown in Fig. 4 (c) and (d), respectively. The radius of curvature varies from 0 to 1.5 m^{-1} in both directions and an increase in sensitivity up to 7% is observed with respect to planar condition.

IV. CONCLUSION

Emerging applications in the field of flexible electronics require high performance to match the level of current computation and communication speed. In order to meet this demand, time-tested traditional silicon-based electronics can be the most attractive candidate. Thinning of silicon to the ultra-thin regime and heterogeneous integration with a flexible substrate provides an interesting path for realising high-speed electronics, which can also conform to 3D surfaces. However, the change in device response upon bending is scarcely researched. Therefore, improved models compiled in simulating environments need to be developed to capture the effect of bending. This paper presents our work in this direction by proposing a compact model that can be compiled in Cadence Virtuoso environment. This model is a combination of mathematical equations along with extracted parameters from BSIM4. The fabricated ultrathin chips are packaged in neutral plane using FPCB and PDMS layer. During the experimental characterization, changes in mobility's value of transistors and output voltage of POSFET sensor are observed as per the theoretical prediction. The change in current level and output voltage during tensile and compressive bending condition shows close matching with the simulated model data. Thus, overall this study presents the thorough investigation of bending effect on device and sensor performance.

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