Al-Ameri, T., Georgiev, V.P. , Adamu-Lema, F. and Asenov, A. (2017) Variability-aware Simulations of 5 nm Vertically Stacked Lateral Si Nanowires Transistors. International Workshop on Computational Nanotechnology, Windemere, UK, 5-9 June 2017.

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Deposited on: 11 October 2017

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Variability-aware Simulations of 5 nm Vertically Stacked Lateral Si Nanowires Transistors

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Abstract—**In this work, we present a simulation study of vertically stacked lateral nanowires transistors (NWTs) considering various sources of statistical variability. Our simulation approach is based on various simulations techniques to capture the complexity in such ultra-scaled device.**

I. Introduction

Gate all around nanowire transistors (GAA NWTs) promise an improved transistor's electrostatics, offering better performance at lower supply voltages and significantly reducing the short channel effects. Arranging multiple GAA NWTs in vertically stacked lateral (VSL) configuration is a promising structure to increase the drive current for 7nm CMOS technology and beyond [1]. Also in current technology nodes, the variability is becoming important in nanoscale transistors due to process deviation and intrinsic properties of materials and interfaces. There are numerous sources of statistical variability (SV) such as Random Discrete Dopants (RDD), Wire Edge Roughness (WER) and Metal Gate Granularity (MGG), which dominate the NWT behaviour. Due to the inherited SV related to doping and gate patterning, it is very important to include SV information in process design kits (PDKs). Accurate statistical reliability (SR) information is crucial in defining the reliability criteria, and for supporting reliability-aware statistical design. For example, NBTI and PBTI degradations are associated with injection and trapping of carriers in defect states in the gate stack during device operation [2].

II. Methodology

In this work, we study the SV of Si n-channel GAA NWTs with an elliptical cross-section of 7 nm x 5 nm. The device has a 0.4nm interfacial SiO2 and 0.8nm HfO_2 (High-k) layers as shown in Fig.1. The doping concentrations are as follows: channel - $10^{14}/cm^3$, source/drain extensions - $10^{20}/cm^3$, and source/drain contacts - $4x10^{20}/cm^3$. In our recently published work [3] we investigated the performance of vertically stacked lateral (VSL) NWTs. In this work, we examined the effects of SV and SR on the performance of VSL configured NWT. For this work two computational methods have been used: a Poisson-Schrödinger model (PS) coupled with Monte Carlo (MC) technique and quantum corrected drift-diffusion model. The flowchart in fig 2, illustrates the overall simulation methodology. The quantum corrections obtained from the Poisson-Schrödinger solution is used in the MC simulations to deliver predictive simulation results. Then the drift-diffusion simulator is calibrated against the MC result and used for efficient SV and SR simulations. An ensemble of 1000 devices has been simulated for the statistical analysis.

III. Results and Discussion

The simulated statistical I_D-V_G characteristics are shown in Fig 3(top). The correlation between different FOM as a function of trap density is shown in Fig. 4. The simulation data presented in Fig.5 include the main sources of SV and the interplay between interface traps and the FOM correlation. For example, the anti-correlation coefficient is lower (-0.95) between Ion and V_T compared to when SV is not considered (-1) for VSL NWT with the double channels. Moreover, the distribution of I_{ON} and I_{off} also shows more variability when both interface traps and sources of SV are considered as shown in Fig 5. Fig. 6 (top left) shows DIBL distribution for 1000 devices at five different scenarios. The average of the distribution is almost the same for all devices that include sources of SV (blue, red and black curves). The standard deviation is also very similar for those three cases and does not follow entirely the Gaussian distribution the two cases. When we consider only interface traps in the uniformly doped device, the DIBL has a lower value than in the other three scenarios where variability sources are included. Also for all cases, the average value increases with increasing trap density in the oxide. Similarly, the distribution does not follow an entirely Gaussian distribution. Fig. 6 (bottom) present the I_{on} and I_{OFF} current distribution for the ensemble of 1000 devices with and without sources of statistical variability and traps in the oxide, correspondingly. Like before the average value of both Ion and I_{off} is shifted to higher values. Moreover, for all devices with included statistical variability, values of I_{on} and I_{off} follow a Gaussian distribution. For the devices with interface traps only and no variability sources, the distribution is very similar in both cases. Fig. 6 (bottom right) reveals the threshold voltage distribution for all five scenarios. As expected when only the devices with statistical variability are considered, the average value of the distribution increases because of increasing the charge trapping but the standard deviation is almost identical in all cases. Like the data presented above the uniformly doped devices with just charge trapping in the oxide shows different behaviour than the other three cases. In those two cases, the average value of V_T also moves to higher values when the trap concertation is increased. Fig. 7 shows the distributions of threshold voltage subject to a combination of VS and ITC for both two & three VSL NWTs.

IV. Conclusions

Detailed simulation of SV and SR study of 5 nm NWT-based CMOS technology at 5nm is presented. Local variability sources including RDD, GER, WER and MGG are considered in this studying in addition to ITC. The presence of SV sources in the simulations affects the SR results dramatically.

References

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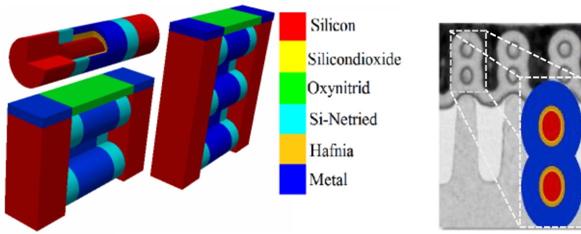

Fig. 1 (right) 3D schematic view a Si nanowire transistor (NTW) an material information for the two channel Si NWT(left), Cross-section TEM [1] image of two channel Si NWT.

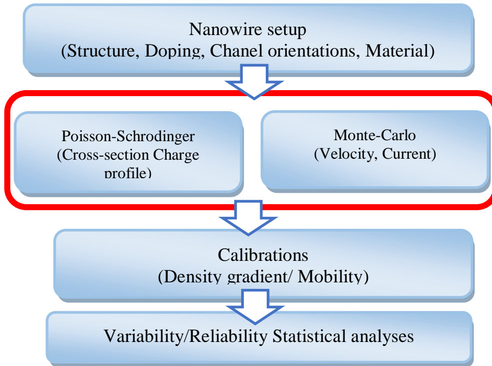

Fig 2: The simulation tool calibration flow chart

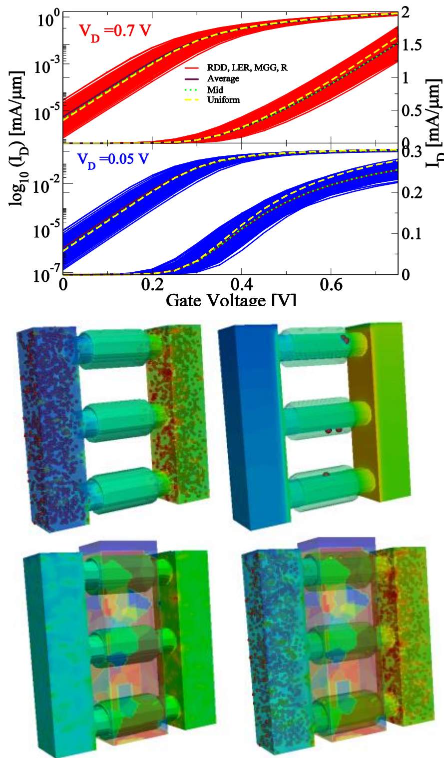

Fig. 3(top) Linear transfer characteristics for the ensemble with RDD, LER and MGG for double channel Si NWT at L_G=12 nm calibrated DD methods. (Bottom) 3D schematic of effects of SV and SR on the potential

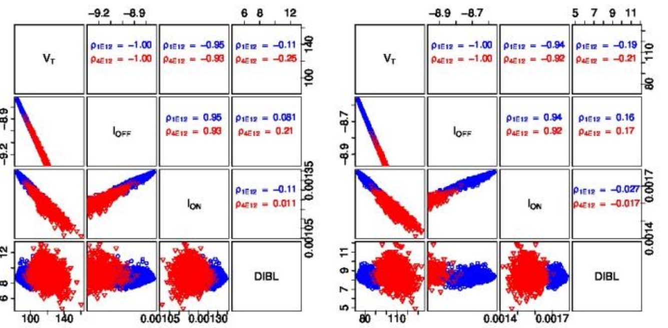

Fig. 4 Distribution of and correlations between extracted FOM from the TCAD simulations of individual ITC $1x10^{12}$ cm^{-1} and $4x10^{12}$ cm^{-1} for double NWT (left) and triple NWT (right).

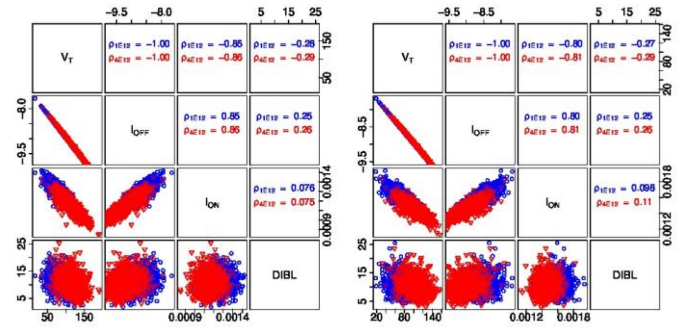

Fig. 5 Correlations between extracted FOM from the TCAD simulations for both ITC and VS effect (RDD, WER, MGG and R) for double NWT (left) and triple NWT (right).

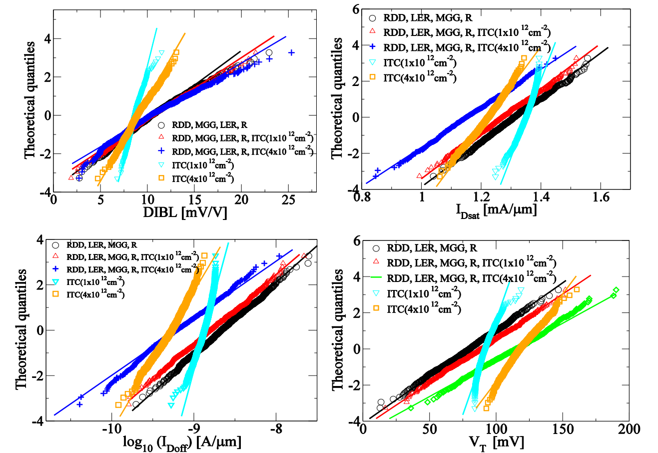

Fig. 6 Normal probability QQ-plot of DIBL, I_{dsat}, I_{off}, and V_T distributions due to individual VS effect of (RDD, LER, MGG, and R), and in their combination with $1x10^{12}$ cm^{-1} and $1x10^{12}$ cm^{-1} ITC .

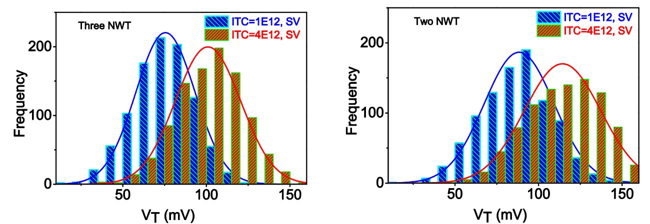

Fig. 7 Distributions of threshold voltage subject to VS effect of (RDD, LER, MGG, and R), and in their combination with $1x10^{12}$ cm^{-1} and $1x10^{12}$ cm^{-1} ITC 4x1012 cm-1 ITC for three VSL NWTs(left), and Two VSL NWT (right)