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Position-Dependent Performance in 5 nm Vertically Stacked Lateral Si Nanowires Transistors

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Abstract—**In this work, we investigated the performance of vertically stacked lateral nanowires transistors (NWTs) considering the effects of series resistance. Also, we consider the vertical positions of the lateral nanowires in the stack and diameter variation of the lateral NWTs as new sources of process variability.**

I. Introduction

Vertically stacked lateral nanowire transistors (VSL - NWTs) also called gate-all-around (GAA) nanowire transistors can enable the next generation 5nm CMOS technology and beyond [1]. However, the performance of these is affected by the nanowire stack position dependence of the drain current in addition to the complexity of controlling the diameters of lateral NWTs in the stack. In our recent publication [2], we investigated the performance VSL – NWTs. Our results show a noticeable position-dependent current density degradation through the identically sized lateral NWTs in the vertical stack. Hence, the upper lateral nanowires closer to the source/drain contacts carry more current than that one that is farther away (middle, bottom) due to the series resistance related voltage drop.

Also, the variability of NWTs position has a significant effect on I_{ON} and in combination with other sources of statistical variability (SV) such as Random Discrete Dopants (RDD), Wire Edge Roughness (WER) and Metal Gate Granularity (MGG) determines the NWT behaviour. The variability of diameters of lateral NWTs in the same stack will enhance the SV and affects the electrostatic confinement. In addition to all sources of SV the reliability which also plays an important role. It is possible that the nearest NWT to the S/D contacts may become weak point suffering extensive ageing. One possible solution is to increase the diameter of lower nanowires concerning the upper nanowires in the stack. However, although the drain current is increasing with increasing of NWT cross-sectional area, the voltage drop will increase across the highly doped S/D regions. The idea of decreasing the doping concentrations near the top lateral NWT and increasing it gradually near the middle and the bottom lateral NWTs, would decrease the total I_{on}. Such solutions are unsatisfactory.

II. Methodology

The simulated device has a three lateral Si NWTs with an elliptical cross-sectional shape (5nmx7nm) and (7nmx5nm) with 110 channel orientation as shown in Fig1. In this work, we employed the Poisson-Schrödinger (PS) quantum corrections coupled with Monte Carlo (MC) module of GARAND [2] as a reference point. We calibrate the GARAND drift-diffusion simulations to this reference MC simulations.

In this work, test the idea of slicing the S/D contact. The slice up is from the top of contact and the second slice up to the middle of the stack as shown in Fig 4. Also, we have tested position dependent performance 500 and SV of diameters of 729 (VSL NWTs) devices.

III. Results and Discussion

The simulated I_D-V_G characteristics of single NWTs with channel orientation 110 shown in Fig 2. The (5nmx7nm) has more quantum charge than (7nmx5nm) NWT, while (7nmx5nm) has less footprint than (5nmx7nm). Fig (3) shows the current density of stack NW with three lateral NWTs with the flowing dimensions: top NWT has 7nm×5nm, 7.4nm×5nm for the middle, and 8.0nm×5nm for the bottom. The upscaling diameter of lower nanowires with respect to the upper nanowires in the stack is not satisfactory to balance the current density in the stack. Fig 3 (B, C, D) shows that even if we use single NWT the position of NWT in the stack directly affects the current. Fig 4 shows that slicing the S/D contact, can satisfactory balance the current distribution in the stack. Fig 5 shows the distributions of I_{ON} subject to lateral NWT position along the vertical stack considering +/- 3nm deviation from the initial position. Fig. 5 shows the correlations between extracted device performance and cross-section profile for both 5nmx7nm and 7nmx5nm stacks, considering 730 atomistic devices.

References

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[2] T. Al-Ameri et al., IEEE Nanotechnology Materials and Devices Conference (NMDC). 2016
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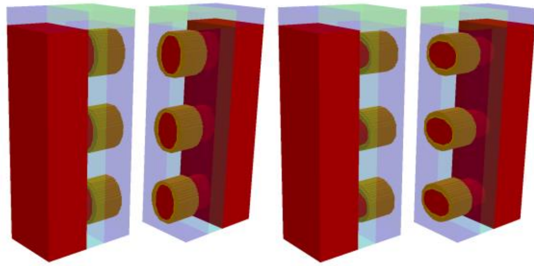
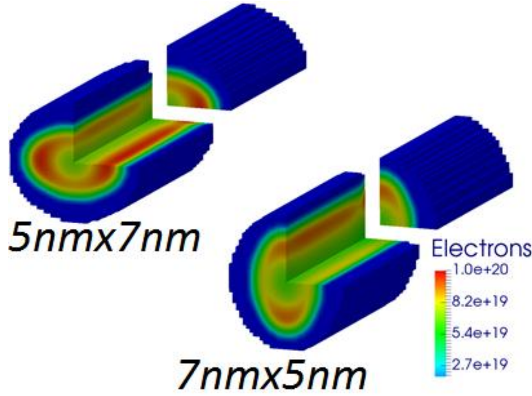


Fig. 1 3D schematic view a Si nanowire transistor (NTW). (Left) 7x5 nm and the (right) one in 5x7nm.



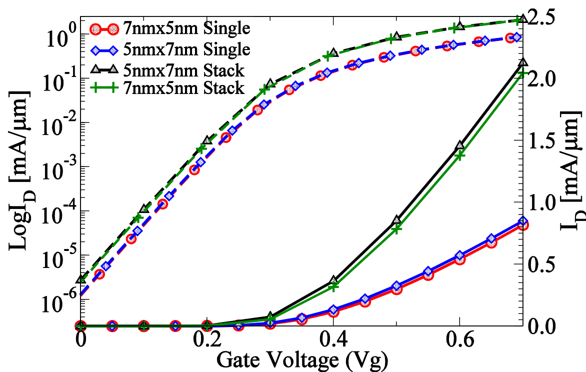


Fig. 2 (Top) Quantum charge distributions of a 5nmx7nm, and 7nmx5nm (NTW) (channels only) with effective gate length Lg=12nm. (Bottom)Id - Vg curves for single and stack NWTs.

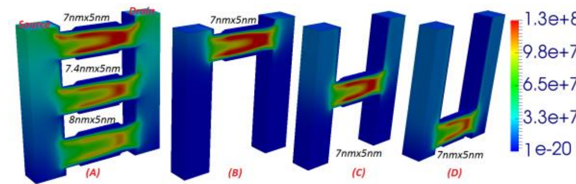


Fig 3 (A) the current density of stack with three lateral NWTs: top 5nmx7nm, 5nmx8.6nm (middle), and 5nmx9.4nm bottom. (B, C, D) the current density of single (5nmx7nm) NWT in the top, middle, the bottom of the stack.

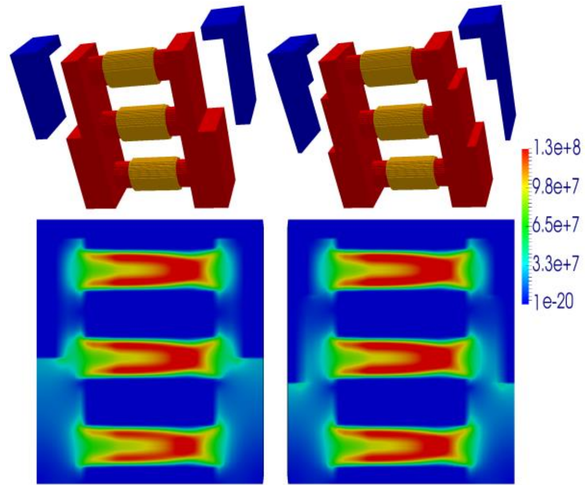


Fig 4 (Bottom) Slicing the S/D contact, the up slice is from the top of contact and the second slice up to the middle of the stack. (Top) the current density of longitudinal cross-section.

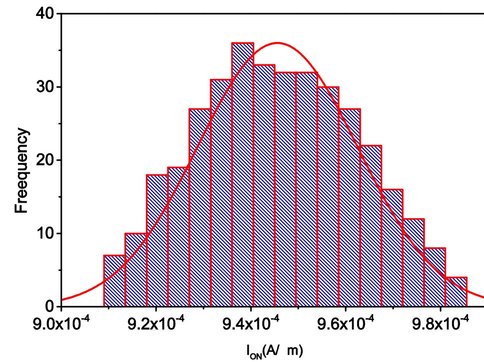


Fig. 5 The distributions of I_{ON} subject to lateral NWT position in the stack.

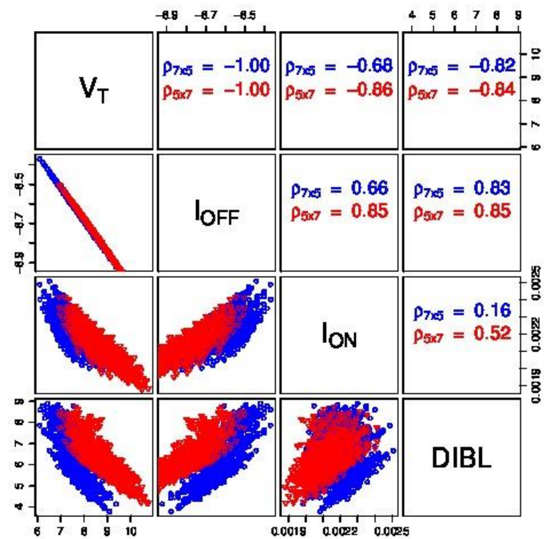


Fig. 6 Correlations between extracted Figure of Merit from the TCAD simulations for both 5nmx7nm and 7nmx5nm stacks with s diameter variability of 729 devices.