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Simulation Based DC and Dynamic Behaviour Characterization of Z2FET

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Abstract: This work presents a TCAD investigation of the operation of a Z2FET device for memory application, where the TCAD model is well calibrated to experimental hysteresis curves. The DC operation of the Z2FET has been analyzed for 4 cases, based on the permutations of the front and back gate biases, to identify and compare different modes of operation. The memory mode of operation is under the "*Thyristor*" like scenario with positive and negative biases applied to the front and back gates respectively. The dynamic property of Z2FET as a memory device is shown and its operation mechanism is described.

Keywords: Hysteresis; 1T-DRAM; Thyristor, DRAM; partioning; Z2FET

I. INTRODUCTION

The Z2FET memory architecture is particularly complex and its operation has promise for application in memory cells without connection to external charge storage components-1T-DRAM [1][2]. Since its inception [3 - 6] and experimental demonstrations [7][8], important progress has been made in analyzing its transient properties through experimental characterization. However, the carrier dynamics and device operation within the distinct regions of the device under a range of DC operating conditions is still not well understood. This paper describes the DC characterization of the Z2FET, from different angles, including a brief description of its transient (dynamic) properties. In this work, we mainly concentrate how the current-voltage characteristics behave in different bias conditions or modes of operation and investigate the carrier distributions during the operation of the device.

II. TCAD CALIBRATION AND METHODOLOGY

The Structure editor and Device simulator from the Synopsys TCAD tool Sentaurus [9] were used to design the device and perform the device simulation respectively. The schematic of device structure is illustrated in Fig.1. For this work, we focused on the relatively small set of device data available at the time of the calibration process. Ungated region (Region A) is 200nm in length and the SOI (Region B) section is 200 nm as well. The significant dimensions used of the device structure are documented in Table 1. The channel doping is very low, which results in a configuration similar to a *P-i-N* diode [10]. The nominal back gate (V_{BG}) and front gate (V_{FG}) bias conditions used for calibration of the TCAD deck are -1.0V and 1.2V respectively. The cathode voltage (V_K) is kept at 0 V while sweeping the anode voltage (V_A). The mobility and SRH recombination and generation models are calibrated against the experimental I_a-V_a data so that the simulation deck can reproduce the hysteresis characteristics at the nominal biasing conditions.

The systematic calibration is conducted in a way to achieve an accurate matching of the simulation result with the experimental data. This was done by means of sensitivity analysis of I_a-V_a curves with different front gate voltages and various mobility model parameters. During the sensitivity analysis, we also probed the effect of the gate work function (ϕ_m) to see how it impact the memory window. Since carrier lifetime plays important roles in determining hysteresis, various carrier life time ($\tau_{e,h}$) values have been used in the SRH recombination and generation model during the calibration process in order to gauge the behaviour of the hysteresis width. For completeness, we also activated the band to band tunneling (B2BT) model during the calibration stage although it has only a marginal impact on. It doesn't modify the hysteresis window, which means B2BT has no significant effect on Z2FET operation.

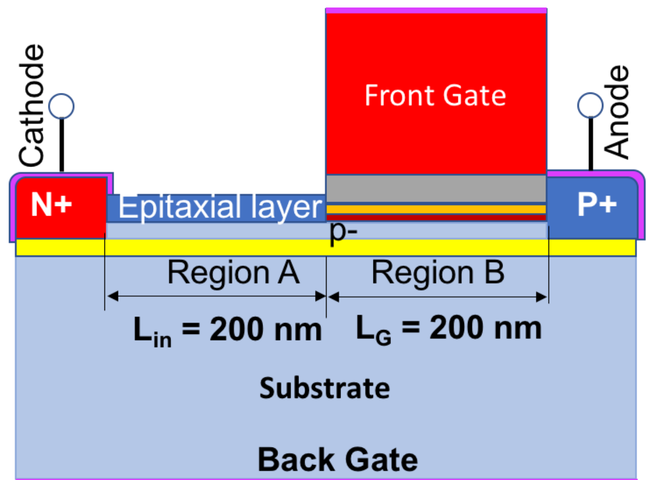

Fig. 1 Illustration of used device structure with *Lin*=*Lg*=200 nm

Finally, Fig. 2 shows a good agreement between the TCAD simulation and experimental data. Following

calibration process, the calibrated TCAD deck was used as the basis for all subsequent simulations, which differ through the variation of V_{FG} and V_{BG} as required.

Table 1: Important physical and doping information

Parameter	Value	Parameter	Value
L_g	200 nm	**$t_{ox\text{-}HK}$**	1.785 nm
L_{in}	200 nm	**t_{Box}**	25 nm
t_{epi}	15 nm	**N_{ch}**	$1\text{x}10^{15}$ cm^{-3}
t_{Si}	7 nm	**$N_{S/D}$**	$5\text{x}10^{20}$ cm^{-3}
$t_{ox\text{-}SiO2}$	0.711 nm	**N_{BG}**	$1\text{x}10^{18}$ cm^{-3}

III. Z2FET Operation and Analysys

A. Operation

As a device, the operation mechanism of Z2FET is manifested on the positive feedback [4][5] which is triggered because of a chain of carriers' injections. The increase in V_A increases injections of holes from the anode (which is the drain) towards source region. The increase in drain bias reduces the potential barriers formed by V_{BG}. The injection of holes across the channel initiate the return injection of electron from the source (cathode) back to the two channel regions, which reduces V_{FG}. These cascades of injections of electrons, holes and the near collapse of the two barriers lead to an abrupt increase (sharp switch) of drain current as shown in Fig. 2 below.

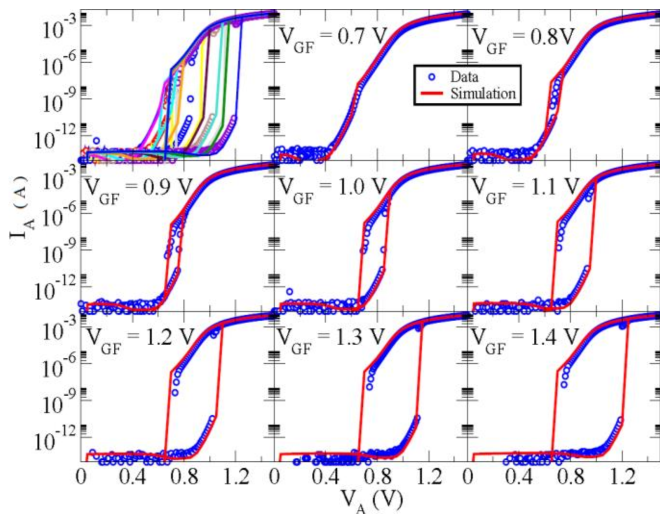

Fig. 2 Calibration of TCAD stationary simulation. Points are from experimental data and lines are simulation results. In all cases the carrier life time are the same for electrons, ($\tau_{maxh} = 3 \times 10^{-8}\ s$) and for holes, ($\tau_{maxh} = 5 \times 10^{-9}\ s$). The back-gate voltage is fixed to -1.0 V and the cathode terminal is grounded.

As shown in Fig. 2, the hysteresis window depends on the level of V_{GF} applied among other deciding factors. High V_{GF} shifts the triggering point of the drain voltage (V_{ON}) to the right. This is the point where the drain current exhibit sharp increase. On the other hand, the reverse sweep remains practically unchanged. Applying large V_{GF} will enhance the memory window. The main drawback of increasing the front gate voltage is an increase in the power consumption.

B. Z2FET Operation Based Partition

Taken from another perspective, the operation of the Z2FET device can be understood by a systematic partitioning of the overall process into 4 biasing regions assuming the scenarios listed in Table 2 and the listed polarities of V_{BG} and V_{FG}. These setups are used throughout this work to understand the functionality of the Z2FET operating conditions. The possible partitions, based on the permutations of the front and back gate bias, are illustrated in Fig. 3

Table 2 Possible scenarios during Z2FET operation:

V_{BG} (V)	V_{FG}(V)	Cathode	Region **A**	Region **B**	Anode	Scenarios	
-	-	n	p	p	p	D R_A R_B	1
+	-	n	n	p	p	R_A R_B	2
+	+	n	n	n	p	R_A R_B	3
-	+	n	p	n	p	D R_A R_B	4

From the list of scenarios given in Table 1, the Z2FET operates as memory device in only one of these conditions, which is listed as *scenario 4*. In the remaining three cases, the DC behaviour replicates that of a diode with the combination of access resistance $R = R_{C1} + R_{C2} + R_A + R_B$, where R_{C1} and R_{C2} are the access resistors. The back-bias V_{BG} and the front gate bias V_{GF} can influence the values of R_A and R_B and change the position of the diode in the Z2FET structure as depicted in Fig 6. Therefore, combinations of V_{BG} and V_{GF} can create one (in three different location) or three diodes as in Fig 4.

For example, in *scenario 1*, The negative gate bias creates accumulation of holes in the *gated* channel region. This lead to the lowering of the resistivity of the SOI channel region (R_B decreases) thus the forward diode current increases. For $V_{BG} >> 0$ and $V_{FG} < 0$ bias condition, namely *scenario 2*, the access epitaxial region (ungated) will be inverted and the two diodes will disappear as a result. As shown in Table 1, for *scenario 3,* the biasing condition is $V_{BG} >> 0$ and $V_{FG} > 0$. At this condition, the epitaxial region and the gated SOI region are inverted creating an *N-n-n-P* configuration and the two diodes disappear leaving the one near the neighborhood of the anode contact. In *scenario 4,* determining the memory operation state, the *gated* channel is biased at inversion mode and the epitaxial access region is biased at accumulation mode. In this condition, there are alternating regions of *N-p-n-P* configuration in the thin silicon body resulting in three p-n junction formation, hence three diodes as shown in Fig.3. This resembles a "*Thyristor"*, [11] [12] represented as a back to back bipolar transistors.

The carrier distribution for this configuration (*scenario 4*) indicate that three *p-n* junction regions (Fig. 5 circled) are formed for a bias condition of V_{BG} << 0 and V_{FG} >> 0. As expected, the DC characteristics in this case exhibit hysteresis (Fig. 2). On the other hand in Fig. 6 the carrier density plot shows a single *p-n* junction coresponding to *scenario 1* (a), *scenario 2* (b), and *scenario 3* (c). The representative ("equivalent") circuits are illustrated in Fig.6(top), where the diodes are placed in three different position of the Z2FET during its operation phase. The location of the three diodes is reflected in the carrir distribution plot (Fig. 6).

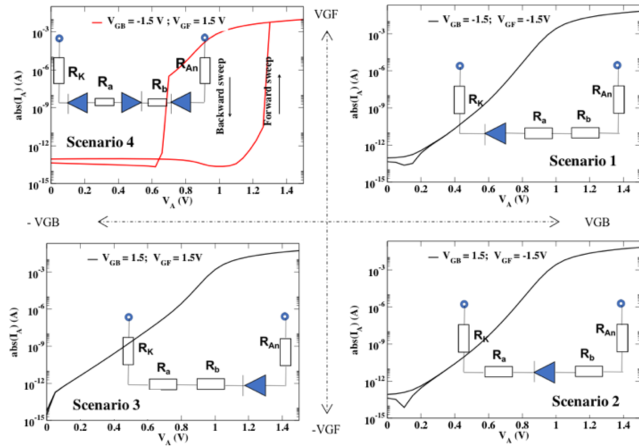

Fig.3 Partisioned regions of Z[2]FET and corresponding I_A-V_A characteristics, of proposed Cenarios. Arange of V_{FG} and V_{BG} between (+/-1.5: +/-1.5) V is used in the simulations. Only simulations from the boundary values of the range are shown

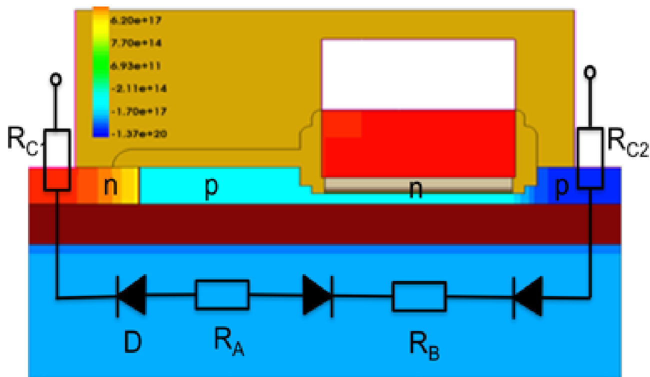

Fig.4 Possible working state of Z[2]FET as a memory device for V_{FG} >> 0 and V_{BG} <<0. At this phase of operation, the devise forms an *N-p-n-N* configuration by inverting the two channel regions. The three *P-N* junctions form a representative "equivalent circuit" with 3 diodes and resister elements.

The carrier distribution is constantly evolving (changing) in the system during the operation phase, and it is hard to estabilish the condition and position of the diodes. However, visualising both electron and hole carrier distributions, which are extracted from the cross-section along the longtudnal direction of the device as shown in Fig. 5 and Fig. 6, clearly indicate that the formation of the *p-n* junctions.

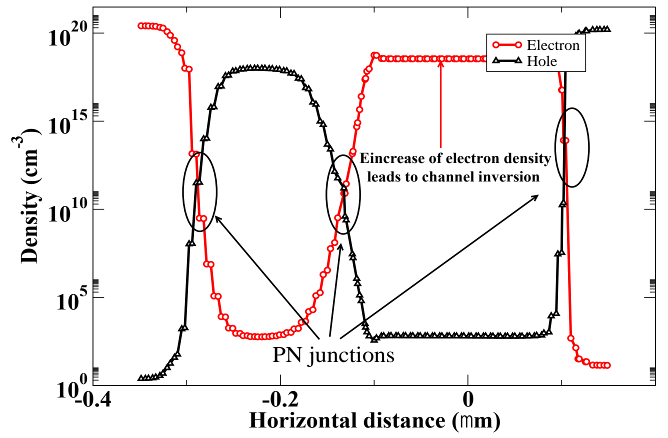

Fig 5. Carrier distribution extracted at the same bias conditions as in the conditions where the device state of operation three diodes

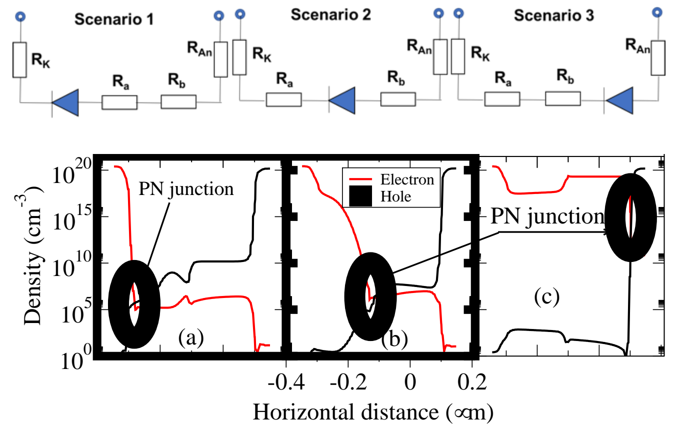

Fig 6. Carrier density plot showing the PN junctions and the circuit representation involving the diods and resistors are illustrated top. The three Diodes are placed in different positions of the Z[2]FET during its operation pheses. The coresponding carrier density profiles of scenario1, scenario 3, and scenario 3 are illustrated in (a), (b) and (c) respectivly.

C. Memory operation

The Z2FET operates as a memory device only under scenario 4, where *n-p-n-p* configuration has been established in the device. Only this bias condition allows Z2FET to perform a fast switching in combination with appropriate hysteresis width.

The waveforms shown in Fig. 7 are chosen to study the operation of the Z2FET as a memory device, where it is understood that successful DRAM operation requires the right bias condition and is sensitive to timing. All expected normal operations including program '0' (P0), hold '0' (H0), read '0' (R0), program '1' (P1), hold '1' (H1), and read '1' (R1) are covered in the simulation trace where the complete operation cycle is presented in Fig. 6. The dependence of I_A – as a function of time (*time-diagram*) is presented in Fig. 7. This shows the typical output result of the memory operation of the Z2FET. Furthermore, when '1' is written as shown in Fig. 8 the holes are stored under the ungated region and electrons are stored under the

gated SOI region. This lowers the potential barrier and allows injection of further holes into the ungated epitaxial access region when V_A is lifted.

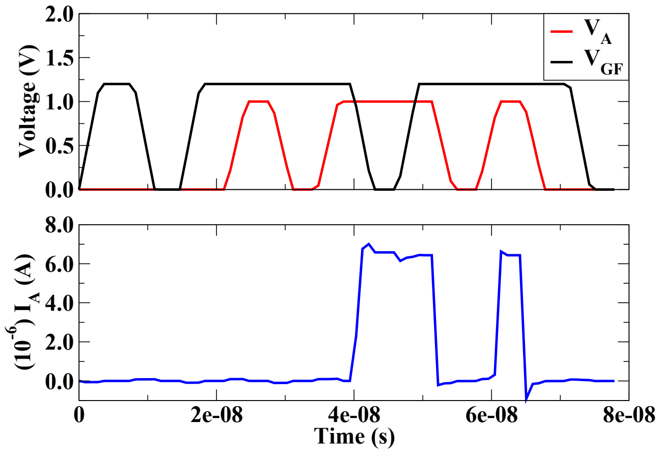

Fig. 7 Waveform for Z²FET used as DRAM device. As shown in (left), both '1' and '0' can be successfully written in and read out on this device when biased at scenario 2 (in this example, V_{FG}=1.2 V and V_{BG} = -1.0 V are applied).

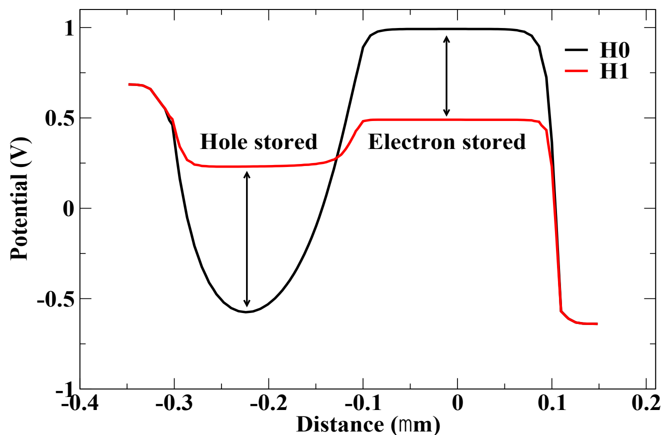

Fig. 8 shows where the stored information is located with respect to the potential distribution in the system.

IV. Conclusion

The operation of the Z2FET when biased to act as a memory device has been investigated. The main operation bias points of Z2FET have been analyzed. From DC operation point of view, 4 *scenarios* have been considered based on a given domain determined by the combination of both V_{BG} and V_{BF}. The switching condition of Z2FET emulate a *Thyristor* operation when -V_{BG} and +V_{GF} bias conditions are meet. The dynamic property of Z2FET as a memory device and it's working mechanism has been described.

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