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# Development of a Reference Wafer for On-Wafer Testing of Extreme Impedance Devices

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**Abstract**—This paper describes the design, fabrication, and testing of an on-wafer substrate that has been developed specifically for measuring extreme impedance devices using an on-wafer probe station. Such devices include carbon nano-tubes (CNTs) and structures based on graphene which possess impedances in the  $k\Omega$  range and are generally realised on the nano-scale rather than the micro-scale that is used for conventional on-wafer measurement. These impedances are far removed from the conventional  $50\text{-}\Omega$  reference impedance of the test equipment. The on-wafer substrate includes methods for transforming from the micro-scale towards the nano-scale and reference standards to enable calibrations for extreme impedance devices. The paper includes typical results obtained from the designed wafer.

**Index Terms**—Calibration, on-wafer measurement, nano-scale, co-planar waveguide, RF nanotechnology, extreme impedance measurement.

## I. INTRODUCTION

New nano-scale device and material technologies are rapidly emerging to support the Internet-of-Things (IoT), wearable electronics and quantum computing. These new devices derive their advantages from material properties and physical dimensions. Universal high-frequency techniques and standards are required to measure accurately and characterize these devices for their further use in new applications. The intrinsic high impedances ( $k\Omega$ ) of these devices are significantly higher than the  $50\text{-}\Omega$  reference impedance of the measurement equipment [1]. This is the main barrier to characterize accurately such devices using the available test equipment, as a highly sensitive system will be required to account for the high reflections generated by these devices [2]. In addition, the dimensions of these devices are three orders of magnitude smaller than the available microwave probes. This paper describes a reference wafer that contains access structures and calibration standards that deal with the change in mechanical dimensions to enable reliable on-wafer metrology of nano-scale devices.

Research has been published to date on physically accessing nano-scale devices, using conventional measurement systems, via a co-planar waveguide (CPW) that is tapered down to a few  $\mu\text{m}$  [3]- [5]. The reference wafer described in this paper includes similar access structures. The wafer also includes calibration standards that enable the reference planes of the measurements to be moved to the device-under-test (DUT). The standards enable several calibration techniques to be investigated for high-frequency characterization at this scale.

## II. DESIGN

The design of the access structures is based on a ground-signal-ground (GSG) CPW transmission line similar to [3]. Fig. 1 shows the dimensions of an open-circuit structure used as one of the calibration standards. Going from left to right in Fig. 1, the signal conductor width is  $100\ \mu\text{m}$  and the separation between the signal and ground conductors is  $66\ \mu\text{m}$ . The signal and ground conductors are then tapered so that the signal conductor width is reduced to  $4\ \mu\text{m}$ . The same methodology can be extended to narrower lines, however the dimensions were limited by the uncertainty of the fabrication process. This provides a position where a nano-scale device can be placed and subsequently measured. The conductor metal used is gold (Au) of  $500\ \text{nm}$  thickness on a  $400\ \mu\text{m}$  gallium arsenide (GaAs) dielectric substrate. A  $25\ \text{nm}$  titanium (Ti) layer was used beneath the Au to enhance adhesion to the substrate. The dimensions of the CPW were chosen to preserve a  $50\text{-}\Omega$  characteristic impedance ( $Z_0$ ) at all places along the CPW line. This minimizes reflections originating from the structures, and thus transfers the maximum amount of the signal to the DUT.

The calibration standards included on the fabricated wafer are five lines having lengths of  $0.5\ \text{mm}$ ,  $1\ \text{mm}$ ,  $2\ \text{mm}$ ,  $3\ \text{mm}$  and  $5\ \text{mm}$ , five offset shorts with different phase delays designed for  $15\ \text{GHz}$ , open, short,  $50\text{-}\Omega$  load, and thru. In addition, empty one-port and two-port structures with gaps between  $2\ \mu\text{m}$  and  $20\ \mu\text{m}$  were included to enable nano-scale devices to be placed and measured. Calibration standards were designed to perform a two-tier calibration moving the

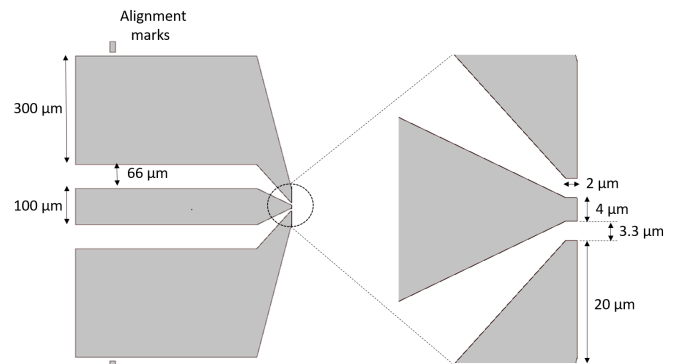


Fig. 1. Open-circuit calibration standard included in the fabricated wafer. The dimensions shown were selected to achieve a  $50\text{-}\Omega$  characteristic impedance across the entire structure.

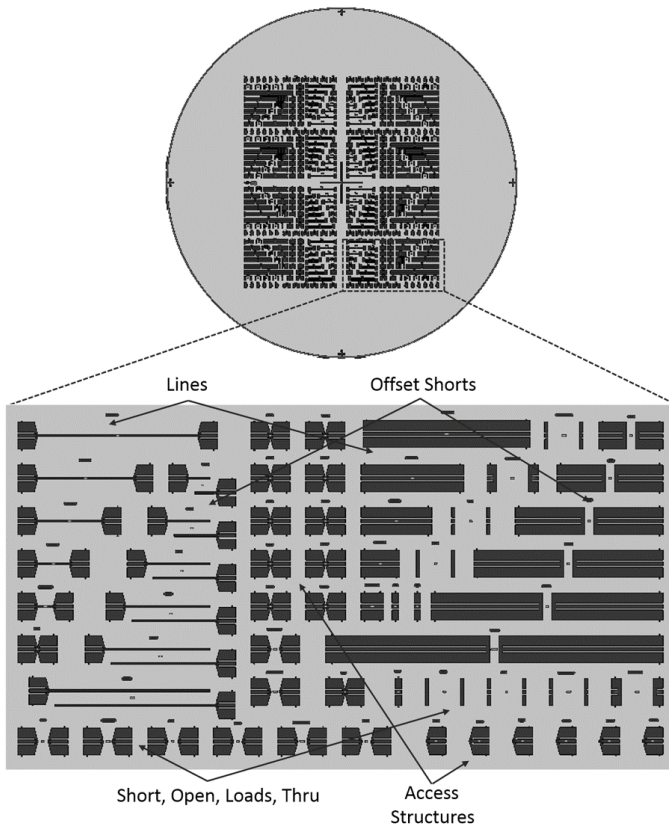


Fig. 2. Layout of the fabricated 3 inch wafer including all the access structures and calibration standards.

reference plane of the measurement from the tips of the microwave probes to the end of the tapered conductor line of the CPW.

### III. FABRICATION

The fabrication of the wafer was performed at the Institute of Electronics, Microelectronics and Nanotechnology (IEMN, RENATECH). The resistive layer (Ti) used for the load standards has thickness of 23 nm. The process flow is based on conventional optical lithography, metal evaporation and liftoff steps. Scanning electron microscope (SEM) based images show a dispersion of the structure dimensions over the full wafer less than  $\pm 300$  nm. The variation in the thickness of the metallic layers, obtained by atomic-force microscopy (AFM) measurements, is between  $\pm 10$  nm and  $\pm 1.5$  nm for Au and Ti layers respectively. Fig. 2 shows the 3 inch wafer designed and it includes eight copies of the access structures and calibration standards.

### IV. MEASUREMENT SET-UP

Initial measurements were performed on the fabricated structures to verify, by comparing with electromagnetic simulations, that they have been designed and fabricated correctly. For the S-parameter measurements, a Keysight N5247A PNA-X Vector Network Analyzer was used. The on-wafer probes used were MPI Titan 26 GHz GSG probes with  $150 \mu\text{m}$  pitch.

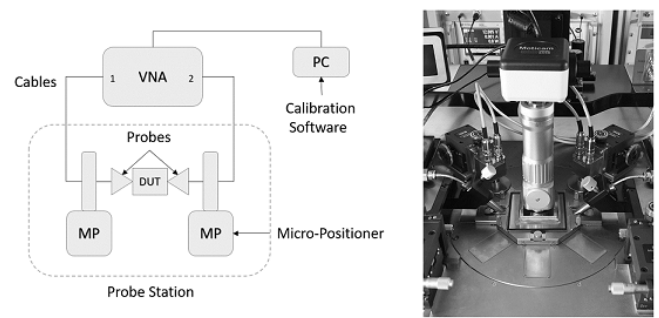


Fig. 3. (Left) Simplified block diagram of the two-port test set-up, (Right) Photograph of the measurement set-up at n3m-labs.

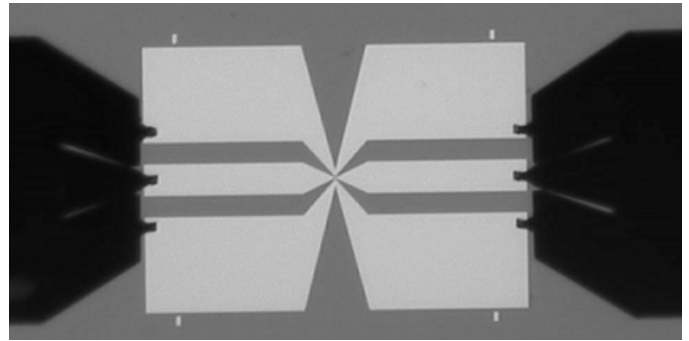


Fig. 4. Back-to-back access structure measured using two GSG probes.

The system was calibrated up to the probe tips by the short-open-load-thru (SOLT) calibration method using an MPI AC-2 impedance standard substrate [6]. The measurement configuration using an MPI TS-2000 probe station located at n3m-labs<sup>1</sup> is shown in Fig. 3. QAlibria software was used to calibrate the VNA and to obtain the corrected results [7]. The frequency range of the measurement was set to 0.1-26 GHz with 100 Hz IF bandwidth.

### V. STRUCTURE MEASUREMENTS

Measurements were performed on two different back-to-back access structures included in the fabricated wafer. This structure will be used as a thru calibration standard when measuring a nano-scale device in order to move the reference plane of the measurement to the end of the tapered line. One of these back-to-back structures is shown in Fig. 4.

The reflection ( $S_{11}$ ) and transmission ( $S_{21}$ ) coefficients obtained for the measurements and electromagnetic simulation of these back-to-back structures are shown in Figs. 5 and 6 respectively. The simulation and design of the structures was performed using *em* from Sonnet Software [8]. For the simulation  $50\text{-}\Omega$  ports were used in a single mode CPW structure. The simulated structure includes a 500 nm Au

<sup>1</sup>n3m-labs is the joint NPL/University of Surrey Nonlinear Microwave Measurement and Modeling Laboratories, n3m-labs.org.

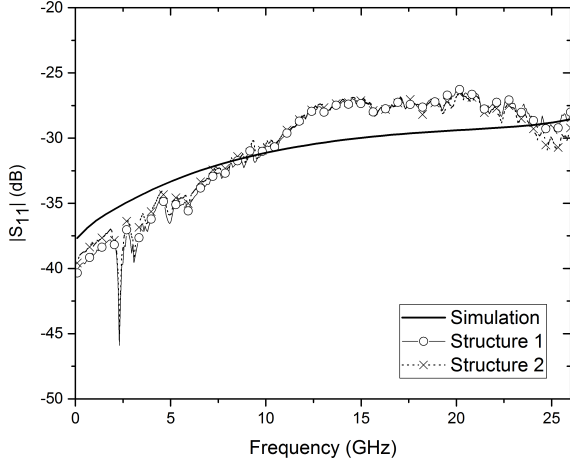


Fig. 5. Simulated and measured reflection coefficient of the back-to-back access structure.

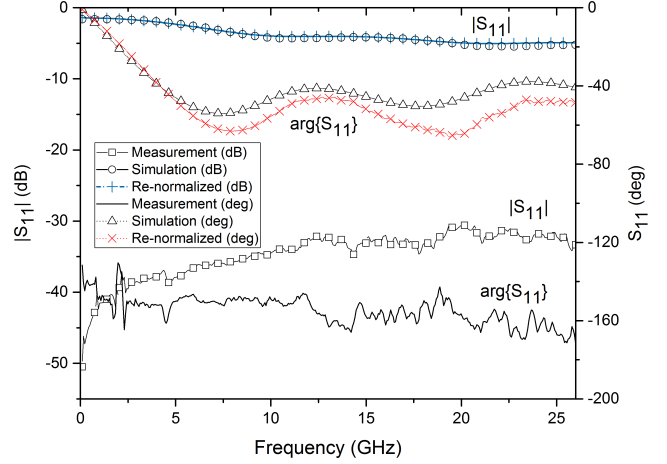


Fig. 7. Measured and simulated reflection coefficient of the 5-mm line.

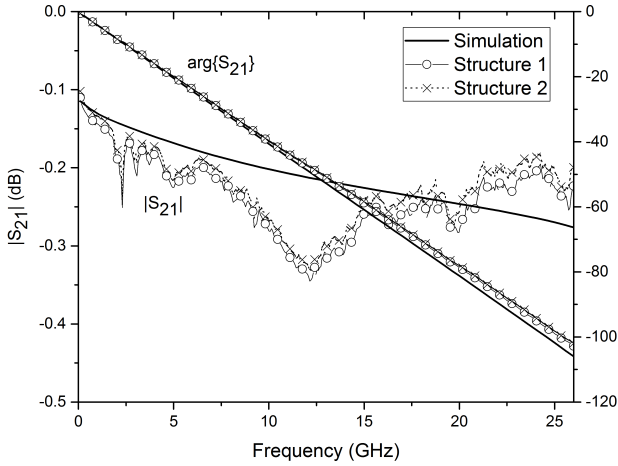


Fig. 6. Simulated and measured transmission coefficient of the back-to-back access structure.

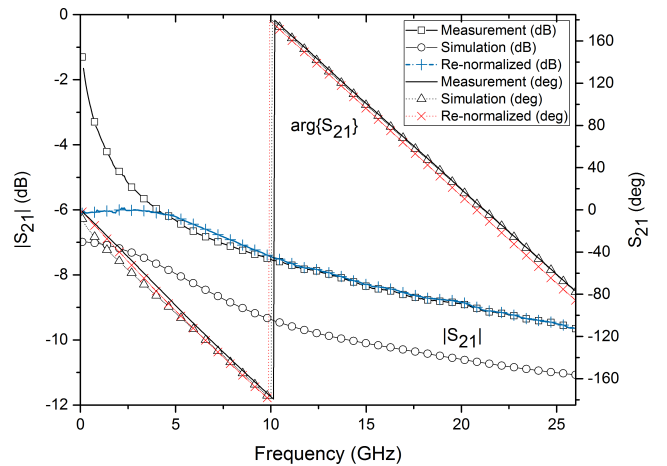


Fig. 8. Measured and simulated transmission coefficient of the 5-mm line.

metallization with conductivity of  $3.8 \times 10^7$  S/m on a  $400 \mu\text{m}$  GaAs dielectric with a relative dielectric constant ( $\epsilon_r$ ) of 12.9 and resistivity of  $1 \text{ M}\Omega\cdot\text{m}$ .

The measurement results show that the reflection coefficient is lower than  $-25$  dB at all frequencies and therefore the designed structures have an approximately  $50\text{-}\Omega$  characteristic impedance. Moreover, there is good agreement between the simulated and measured data. A plot of the reflection coefficient's phase is not included because phase becomes indeterminate when the magnitude of a signal is relatively small (i.e. compared to the measurement system noise floor).

## VI. DEVICE MEASUREMENTS

Since the S-parameter measurements of the access structures have shown that they behave as expected, a measurement of a device was implemented using the access structures and

calibration standards included on the reference wafer. The same measurement set-up as before was used. A multi-line thru-reflect-line (TRL) [9], [10] calibration was conducted to move the reference plane of the measurement to the DUT. One of the back-to-back structures measured was used as the thru standard, an open was used as the reflect standard and four lines with lengths of 0.5 mm, 1 mm, 2 mm and 3 mm as the line standards. A 5-mm line included on the wafer was used as the device to be measured.

The line standards, due to the small physical dimensions at the sub-micro scale, are very lossy having a high characteristic impedance [11] expressed by  $Z_0 = (R + j\omega L)/(G + j\omega C)$  where  $R$  is the resistance per unit length,  $L$  is the inductance per unit length,  $G$  is the conductance of the dielectric per unit length,  $C$  is the capacitance per unit length and  $\omega$  is the angular frequency.

Through simulation the characteristic impedance of one of the line standards was calculated. This impedance has to be accounted for as it is a critical parameter for an accurate TRL calibration. Using (1) and (2) [12] the measured S-parameters were re-normalized to the 50- $\Omega$  reference impedance of the system.

$$S_{NORM} = (S_{MEAS} - XI)(I - S_{MEAS}X)^{-1} \quad (1)$$

$$X = (Z_{Line} - Z_{REF}) / (Z_{Line} + Z_{REF}) \quad (2)$$

where  $S_{NORM}$  are the re-normalized S-parameters,  $S_{MEAS}$  are the measured S-parameters,  $I$  is the identity matrix,  $Z_{Line}$  is the characteristic impedance of the line standard and  $Z_{REF}$  is the reference impedance of the measurement system.

The S-parameter measurements of the 5-mm line are shown in Figs. 7 and 8. The measured data do not match the simulated data because they are referenced to the characteristic impedance of the line standard, whereas the simulated data are referenced to 50  $\Omega$ . The re-normalized S-parameters of the measured data match the simulation data more closely. This indicates that the reference plane of the measurement has been successfully moved to the DUT due to the calibration.

## VII. CONCLUSION

The design and fabrication of a reference wafer containing access structures and calibration standards enabling the measurement of nano-scale devices at microwave frequencies has been presented. The structures presented are based on a CPW design, moving the reference plane of the measurement from the conventional micro-scale to the sub-micro scale.

Now that the structures and standards have been verified, they will be utilized in the near future to develop a new method which transforms the 50- $\Omega$  reference impedance of the test equipment to the k $\Omega$  range for the accurate characterization of extreme impedance nano-scale devices. In addition, the validity of different calibration techniques for nano-scale microwave measurements will be investigated using the calibration standards included on the wafer.

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