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Interaction between Hot Carrier Aging and PBTI Degradation in nMOSFETs: Characterization, Modelling and Lifetime Prediction

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Abstract

Modelling of the interaction between Hot Carrier Aging (HCA) and Positive Bias Temperature Instability (PBTI) has been considered as one of the main challenges in nanoscale CMOS circuit design. Previous works were mainly based on separate HCA and PBTI instead of Interacted HCA-PBTI Degradation (IHPD). ***The key advance of this work is to develop a methodology that enables accurate modelling of IHPD through understanding the charging/discharging and generation kinetics of different types of defects during the interaction between HCA and PBTI.*** It is found that degradation during alternating HCA and PBTI stress cannot be modelled by independent HCI/PBTI. Different stress sequence, i.e. HCA-PBTI-HCA and PBTI-HCA-PBTI, lead to completely different degradation kinetics. Based on the Cyclic Anti-neutralization Model (CAM), for the first time, IHPD has been accurately modelled for both short and long channel devices. Complex degradation mechanisms and kinetics can be well explained by our model. Our results show that device lifetime can be underestimated by one decade without considering interaction.

Introduction

In advanced nanoscale CMOS technology, reliability is one of the main concerns for circuit design and modelling [1-6]. Both Hot Carrier Aging (HCA) and Positive Bias Temperature Instability (PBTI) become severer with shorter channel length and use of high-k gate dielectrics. Meanwhile, the access transistor in SRAM suffers alternating HCA and PBTI when Read '0' is followed by Write '0'. Characterization and modelling Interacted HCA-PBTI Degradation (IHPD) have become a crucially challenging task in industry [7]. Previous research [8-11] predicted device lifetime at operation Vdd of HCA (**Fig.1**) or PBTI (**Fig.2**) separately, based on the accelerated-voltage method (HCA under Vg=Vd and PBTI under Vg are used in this paper), where unique power-law time and voltage exponents can be observed, respectively. However, this is not the case if PBTI stress is followed by HCA, or HCA stress is followed by PBTI (**Fig.3a&4a**), where the degradation does not follow a unique power law. Simply adding degradations of HCA and PBTI together have been proven invalid [7]. We proposed a unified Cyclic Anti-neutralization Model (CAM) framework [12] for HCA and PBTI, but their interaction has not been investigated so far.

In this paper we will firstly investigate the property of different defects under separate HCA and PBTI stress, and then their interaction. For the first time we show that three different types of defects, i.e., Pre-existing Cyclic Electron Trap (PCET), Generated Cyclic Electron Trap (GCET), and Anti-Neutralized Defect (AND), play different roles in IHPD. PCET is the pre-existing defect responsible for the repeatable charging/ discharging in IHPD. GCET is generated by HCA stress but not by PBTI. It has deeper energy level than PCET. Both HCA and PBTI generate Anti-Neutralized Defect (AND), which cannot be discharged once generated. Each type of defect has different charging/discharging kinetics under HCA and PBTI, leading to the complex degradation kinetics as shown in **Fig.3&4**.

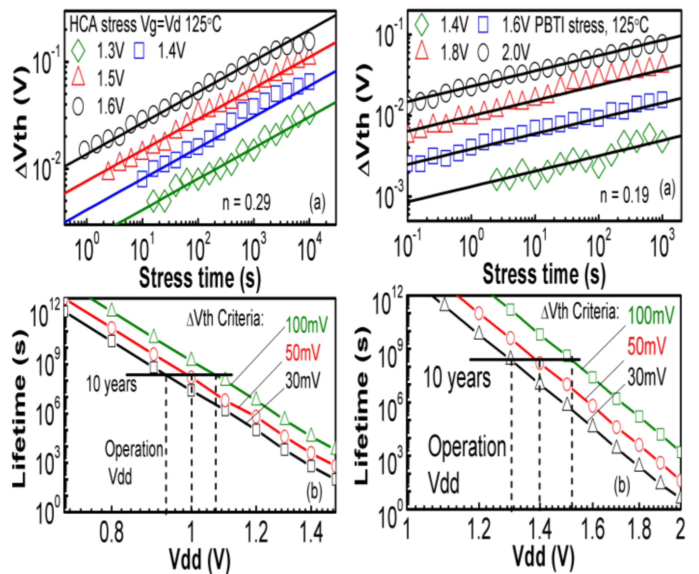


Fig. 1 Conventional power-law method for HCA lifetime prediction. (a) Vth degradation at accelerated Vg=Vd. (b) Vdd extrapolation for 10 years lifetime based on different ΔVth criteria.

Fig. 2 Conventional power-law method for PBTI lifetime prediction. (a) Vth degradation at accelerated Vg. (b) Vdd extrapolation for 10 years lifetime based on different ΔVth criteria.

Devices and Experiments

Devices used in this work were fabricated by an industrial 28nm CMOS technology, with metal gate and high-k dielectrics. Devices with two channel lengths, 36nm and 225nm, are used, both have a width of 900nm. All tests were carried out at 125°C.

Interaction between HCA and PBTI

To further investigate the impact of different stress sequences in **Fig.3a&4a**, i.e., HCA-PBTI-HCA or PBTI-HCA-PBTI, the 2nd stress is removed in the figures so that the 1st and 3rd stress can be compared. **Fig.3b** shows that in a short device, HCA (3rd stress, '■') follows the original HCA kinetics (1st stress, '□'), but the PBTI (3rd stress, '●') does not follow the original PBTI kinetics (1st stress, '○'). On the contrary, in a long device (**Fig.4b**), PBTI (3rd stress, '●') follows the original PBTI kinetics (1st stress, '○'), but the HCA (3rd stress, '■') does not. This clearly demonstrates the interaction existing between HCA and PBTI, i.e. insertion of HCA changes the kinetics of PBTI in short channel device, but insertion of PBTI in long channel device changes the kinetics of HCA instead. Consequently, degradation cannot be modelled by independent HCA and PBTI degradation mechanisms and kinetics without considering their interaction.

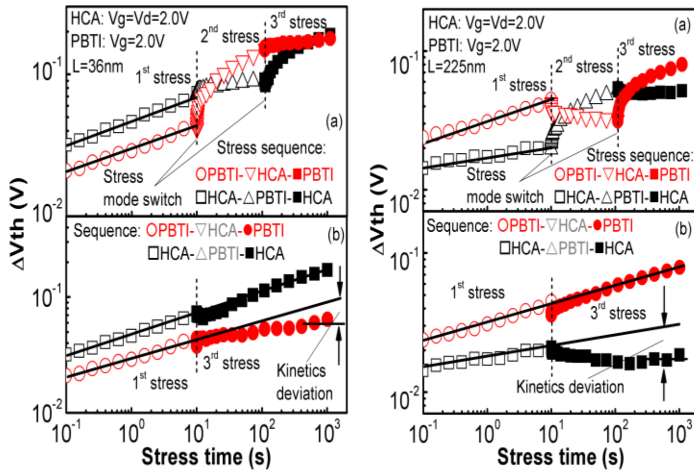


Fig. 3 (a) Alternating HCA-PBTI in short-channel device. Sequence: HCA-PBTI-HCA and PBTI-HCA-PBTI. (b) The 2nd stress are removed, and both ΔVth and stress time of the 3rd stress are reset to that at end of the 1st stress.

Fig. 4 Similar to Fig.3 except for the long device channel length. Conventional prediction is not valid for both channel lengths.

Lifetime Prediction for IHPD

By taking into account the interaction of HCA and PBTI in CAM framework, we can accurately model the IHPD for both short (**Fig.5**) and long channel (**Fig.6**) devices. The methodology is to decompose the overall interacted degradation into three different categories by individual type of defects: PCET, GCET and AND. Excellent agreement between test data and modelling results can be seen in **Fig.5a&6a**. Interacted degradation (**Fig.5b&6b**) and operation Vdd for 10 years (**Fig.5c&6c**) can be predicted by restoring the power-law for generated defects, GCET and AND. As expected, short channel device has shorter lifetime and lower operation voltage than long channel due to enhanced HCA. Prediction by simple HCA+PBTI leads to large errors of more than one decade (**Fig.5b&6b**). This methodology will be explained in detail as follows.

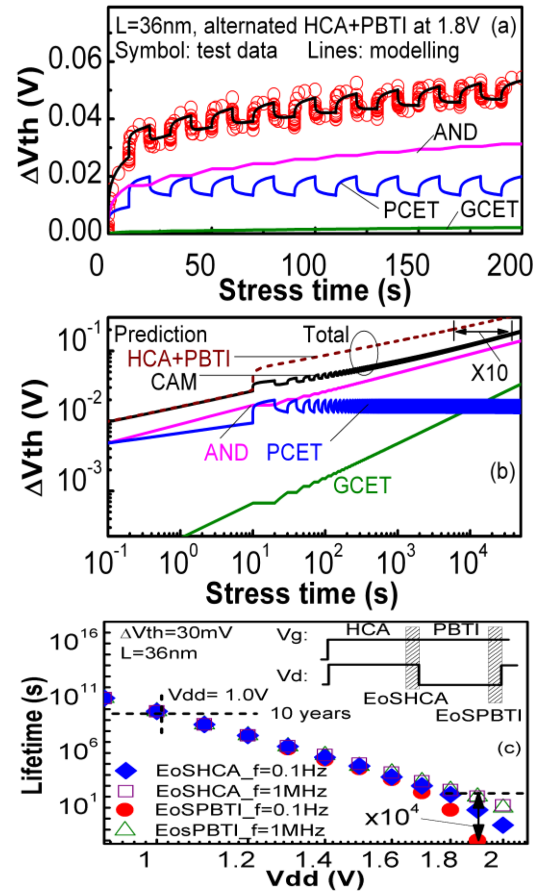
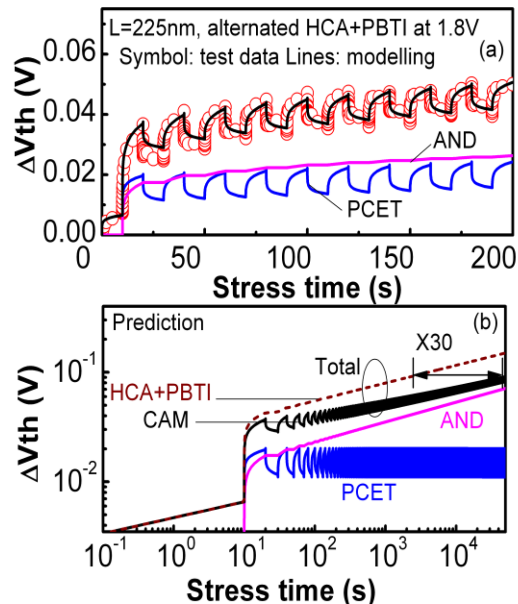


Fig. 5 Test results and modelling for short channel device at 1.8V (a) for IHPD. Lifetime prediction with ΔVth=100mV (b) and operation Vdd for 10 years (c) based on CAM framework.



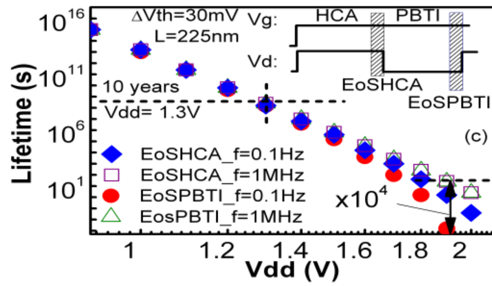


Fig. 6 Test results, modelling and prediction for long channel device. GCET is negligible since channel carrier become cold.

Modelling of Electron Traps (ETs)

Energy levels of PCET, GCET and AND are illustrated in **Fig.7a**. At flat band condition, they are located at 1.4, 1.6 and more than 1.8 eV below Ec of high-k (Ec_HK), respectively. This is supported by the measured ETs energy distributions (**Fig.8**) [12], where a lower HCA bias generates relative less GCETs. CETs (PCET & GCET) can be repeatedly charged/discharged at certain low ±Vg biases (albeit a more negative bias is needed for discharging GCET), but AND cannot be discharged once generated. **Fig.7b** shows the characterization method for each ET. The charging/generation kinetics of different ETs and their discharging property are still unknown and will be investigated. As an illustration, only short channel devices with L=36nm are used below.

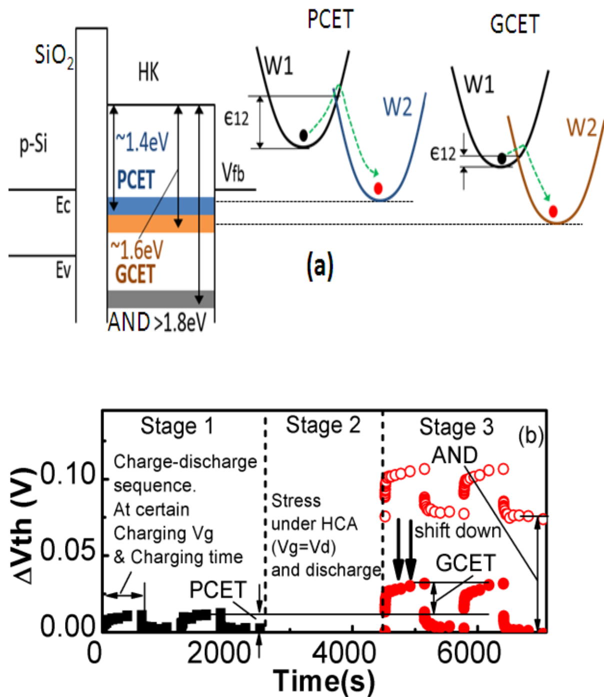


Fig. 7 (a) An illustration of ETs energy locations with regard to Ec_HK in CAM model. (b) Electrical method to characterize PCET, GCET and AND. The same Charge-discharge sequence are performed in Stages 1 and Stage 3 for charging/discharging CETs. Stage 2 is for heavy stress (data not shown here). When HCA is replaced by PBTI in Stage 2, GCET in Stage 3 is zero [12].

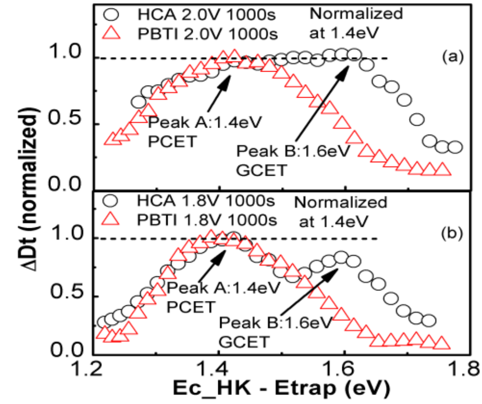


Fig. 8 Energy distributions for individual PBTI and HCA stress at 2.0V (a), and 1.8V (b).

A. *Pre-existing Cyclic Electron Trap - PCET*

Charging of PCET increases with charging time and voltage, and follows a power law (**Fig.9a&b&c**). The time exponent is extracted in **Fig.9b,** allowing the modelling of PCET's charging kinetics. Both PBTI and HCA stress do not increase the amount of PCET that can be charged at a lower charging voltage & time (**Fig.9d**), supporting its pre-existing nature. Only ~55% PCET is charged under HCA (Vg=Vd) condition when compared with PBTI (Vg only) condition (**Fig.10a**). Probably PCET in the pinch-off region is not charged since the weakened vertical electric field by Vd (**Fig.10b**).

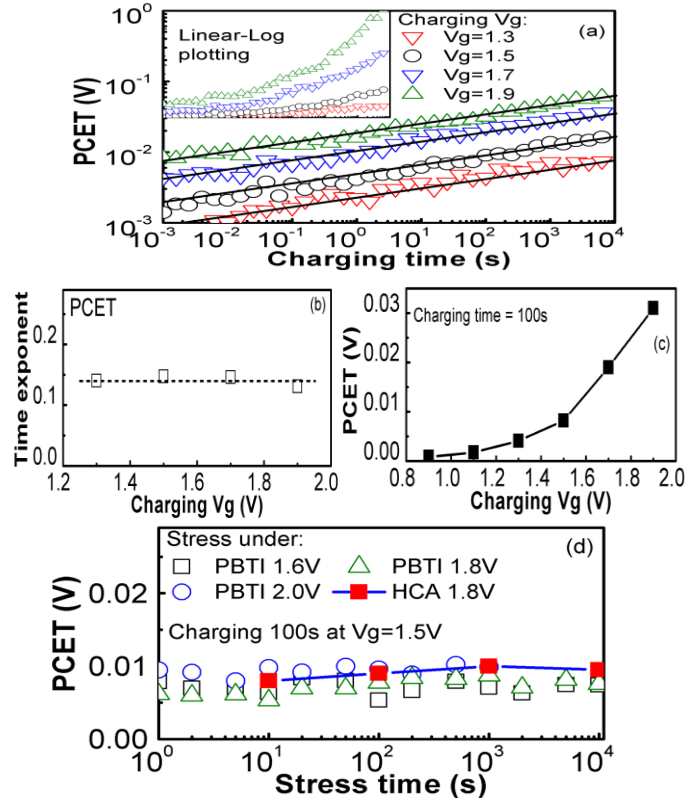


Fig. 9 Charging property of PCET. (a) PCET follows a power law with charging time. (b) Extracted time exponent. (c) PCET increases with charging Vg. (d) Stress (HCA or PBTI) doesn't increase the PCET charged at a fixed voltage and time, supporting that they are pre-existing in device as fabricated.

To model its dynamic kinetics (Fig.5&6), discharging property of PCET also needs to be obtained. Discharge can be carried out at either a negative Vg (Vg mode) or a positive Vd (Vd mode). Fig.11 shows the discharge of PCET at Vg mode is very fast and starts from 1µs already, but at Vd mode it starts from ~1ms. Discharge completes within 100s in both cases. We will only consider the Vd discharge mode because in circuits such as the access transistor in SRAM and current mirror [13, 14], a high bias is always kept on the drain during non-operation state.

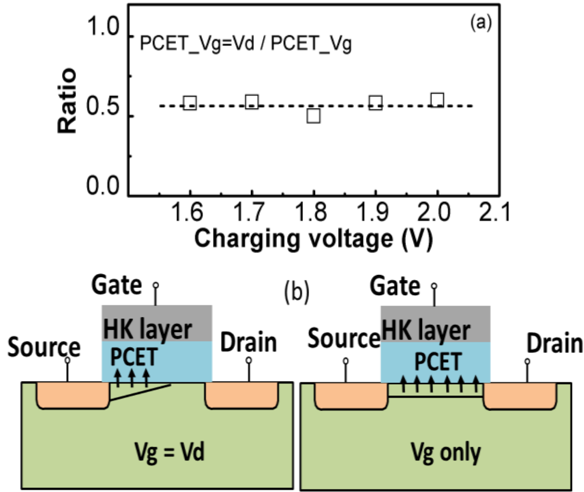


Fig. 10 (a) Ratio between PCETs charged under Vg=Vd condition and Vg-only condition. (b) Explanation.

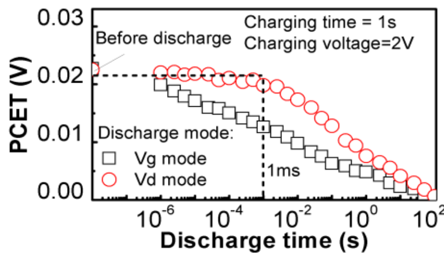


Fig. 11 PCET under different discharge modes: Vg mode (Vg=-2V, Vd=Vs=0) and Vd mode (Vd=2V, Vg=Vs=0).

Fig.12 shows the modelling procedure of PCET discharge. The discharged PCET (ΔPCET) follows the logarithmic kinetics against discharging time for both charging conditions, Vg-only (Fig.12a) and Vg=Vd (Fig.12b), and a unique kinetics is obtained after normalization (Fig.12c). The equation ΔPCET=A+B*Ln(t) can be used for discharging, therefore, where B is proportional to charging voltage.

B. Generated Cyclic Electron Trap – GCET

Unlike PCET, GCET can only be generated by HCA stress, not by PBTI [12]. Modelling by extrapolation requires constant time exponent 'n', but Fig.13a&c shows 'n' reducing for higher charging Vg. A constant 'n' (Fig. 13b&c), however, can be restored for GCET after removing the PCET, which is applicable at different HCA stress voltages (Fig.14).

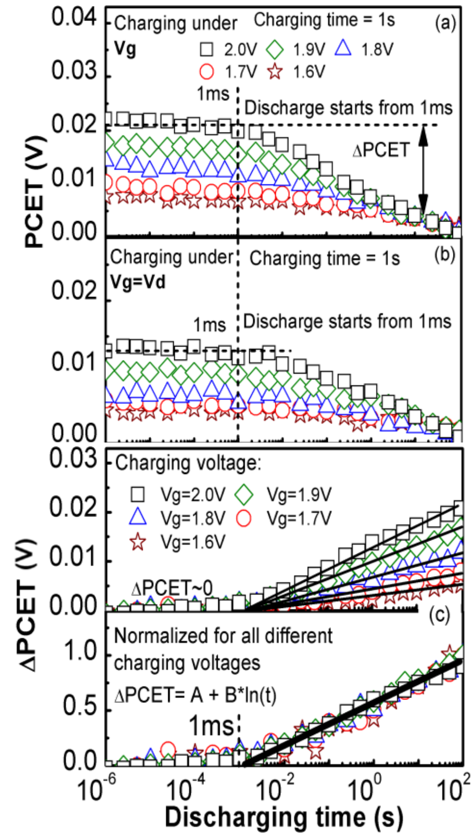


Fig. 12 Modelling for PCET discharging (Vd mode). PCET is charged for 1s under (a) Vg-only, and (b) under Vg=Vd conditions. (c) The discharged ΔPCET follows logarithmic law against discharging time and can be normalized to a unique kinetics.

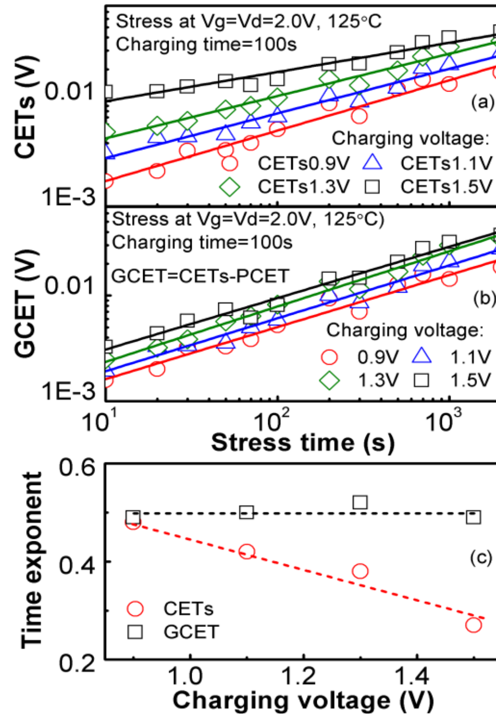


Fig. 13 Charging kinetics of CETs (a) consists of both PCET and GCET. (b) GCET-only, after removing PCET, follows a good power law. (c) Comparison of time exponents in (a) and (b).

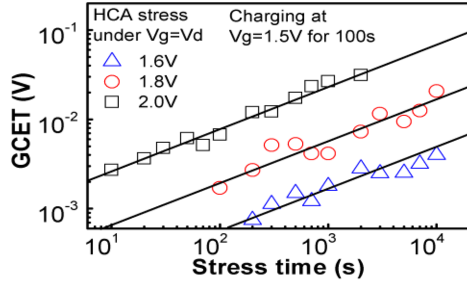


Fig. 14 GCET generation kinetics under different HCA stress voltages, measured at a fixed charging condition. The same time exponents are obtained.

The discharging kinetics under Vg mode ('□') and Vd mode ('○') after the HCA stress are compared in **Fig.15**, which is also compared with the PCET discharging kinetics at Vd mode ('—' in **Fig.15**) taken from **Fig.11**. The good agreement between '○' and '—' suggesting that only PCET is discharged at Vd mode after HCA stress, and the generated GCET can only be discharged at Vg mode. Since GCET is only generated by HCA, and cannot be discharged at Vd mode, it should not participate in the interaction during IHPD in the access transistor of SRAM, because in this particular application it will remain charged once generated.

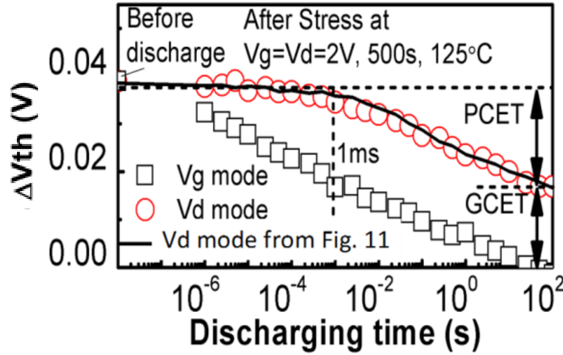


Fig. 15 Discharge of CETs under different modes. GCET doesn't discharge under Vd mode. The black solid line is taken from the Vd mode in Fig.11 but shifted accordingly. Device was heavily HCA stressed to generate GCET. Local Vth after stress and complete discharge is used as reference.

C. Anti-Neutralized Defect - AND

As shown in **Fig.7b**, AND cannot be discharged under either the Vg or Vd discharge mode, because of its deep energy levels at more than 1.8 eV below Ec_HK (**Fig.7a**). Its generation kinetics under HCA stress and PBTI stress are shown in **Fig.16a&b**, respectively. AND generation under HCA stress has a large time exponent than PBTI in short channel device (**Fig.16c**).

D. Combined ETs charging and discharging kinetics

Combining the charging/generation and discharging kinetics extracted for PCET, GCET and AND in above sections, we can successfully simulate the complex interaction between HCA and PBTI, as shown in **Fig.5&6**, and restore the power law for accurate lifetime prediction. The complex charging/ discharging behavior in **Figs.3-6** can be explained as follows:

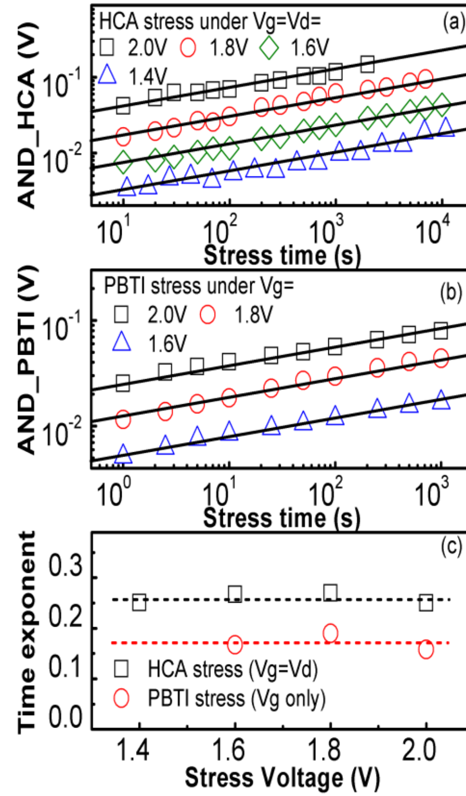


Fig. 16 AND generation under (a) HCA stress and (b) PBTI stress. AND does not discharge under Vg or Vd discharge modes due to its deep energy location. (c) HCA gives a large time exponent than PBTI since the use of short channel device.

1. In short channel device (**Fig.3**), HCA is more severe than PBTI at the same stress voltage [9,15], so that the generation of AND and GCET during HCA dominates, and 3rd HCA ('■') can largely follow 1st HCA ('□') after removing the 2nd PBTI. In contrast, 3rd PBTI ('●') cannot follow 1st PBTI ('○'), because the corresponding precursors are consumed by the heavier 2nd HCA stress.
2. In long channel device (**Fig.4**), carriers in channel become colder, as a result AND and GCET generation during HCA becomes negligible. This agrees with the observation in **Fig.4b** that 3rd PBTI ('●') follows 1st PBTI ('○') well after removing the 2nd HCA. In contrast, 3rd HCA ('■') cannot follow 1st HCA ('□'), because more PCET is charged (**Fig.10**) during 2nd PBTI, leading to the discharge in 3rd HCA ('■'), instead.
3. The charging-up/discharging-down cycles observed in **Fig.5&6** are caused by PCET only, as shown by the simulation results (blue lines), which does not increase at longer stress times, confirming its pre-existing nature.
4. At high frequency, End-of-Stress (EoS) HCA ('□') overlaps with EoS PBTI ('△') in both short (**Fig.5c**) and long (**Fig.6c**) channel devices. At low frequency, the slow discharging kinetics of PCET starting from 1ms (**Fig.11&12**) is enabled, so that there is a larger disagreement ('●'&'◆') at high Vdd, which becomes smaller at lower Vdd due to reduced PCET charging.

SRAM Operation Emulation

To examine the impact of above IHPD modelling in practical SRAM operation, a test pattern is implemented to emulate it for the access transistor. **Fig.17a** shows the simulated waveforms during alternating Read '0' and Write '0'. The access transistor suffers from alternating HCA and PBTI with the Vd discharge mode inserted in between. At high frequency (**Fig.17b**) End-of-Stress (EoS) HCA, End-of-Recovery (EoR) HCA, EoS PBTI and EoR PBTI overlap with each other with a unique time exponent 'n'. At lower frequency 'n' differs significantly (**Fig.17c**), caused by the PCET charging/discharging. This can be further confirmed in **Fig.18a** where constant PCET during stress is measured by EoSPBTI–EoRPBTI ('□'&'■') and EoSHCA–EoRHCA ('○'&'●'), and it reduces at higher frequency (**Fig.18b**). By conventional extrapolation, ΔVth projected to 10 years (**Fig.18c**) is underestimated at high IHPD voltage, however, overestimated at operation voltage because of the distorted 'n'.

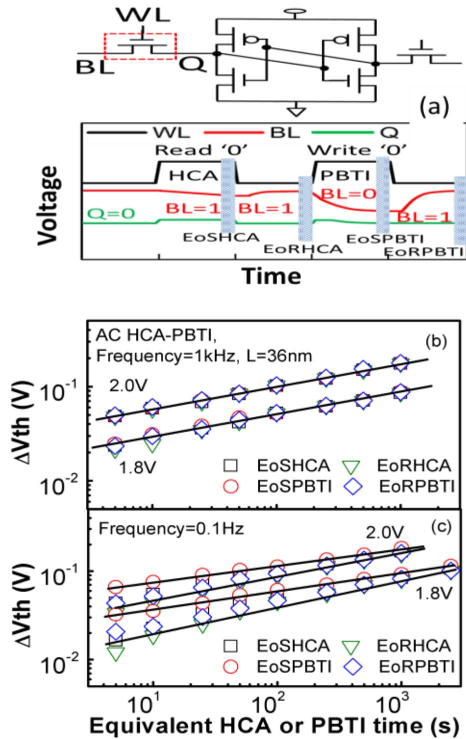
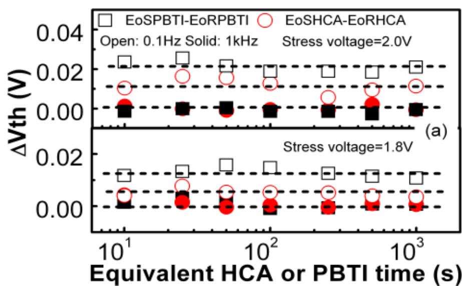


Fig. 17 SRAM access transistor suffers interacted HCA-PBTI stress during Read '0' and Write '0'. (a) Simulated waveform shows BL is always high during WL=0, suggesting a Vd discharge mode. Results for (b) high frequency and (c) low frequency by emulating the SRAM Read '0' and Write '0' test pattern in (a).



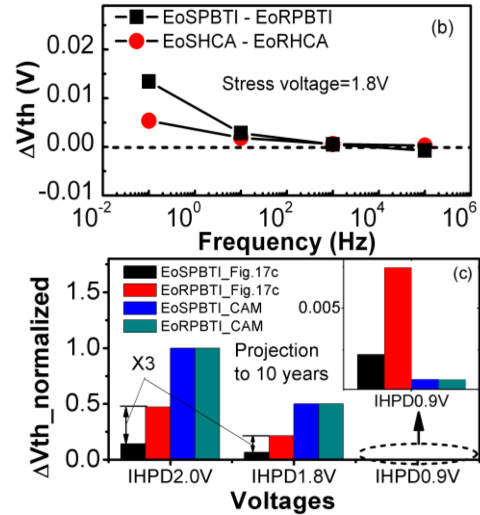


Fig. 18 EoSPBTI–EoRPBTI & EoSHCA-EoRHCA at (a) 2.0V and 1.8V are constant, confirming they are from PCET. (b) Its frequency dependency. PCET causes the 'n' variation in Fig.17c. (c) ΔVth prediction to 10 years by conventional extrapolation (data is from Fig. 17c) and CAM model.

Conclusion

Interacted HCA and PBTI degradation has been carefully examined in this work. For the first time, a comprehensive model has been developed based on our CAM framework, by taking into account the charging/discharging of three different types of defects during alternating HCA and PBTI stress. Good agreement has been achieved between test data and simulation results. Without considering the HCA/PBTI interaction, device lifetime can be underestimated by over one decade. The successful emulation under the SRAM operation pattern makes this work a useful tool for circuit designer to evaluate circuit reliability and operation margin.

Acknowledgement

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