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Experimental Testbed for PA Characterization and Pre-Distortion with Relaxed Sampling Rate Requirements

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Abstract — **This paper explores an interleaving approach to expand the effective sampling rate of analog-to-digital converters (ADCs) with application to power amplifier characterization and digital pre-distortion. By interleaving a known test signal, it is shown that a 250 MSPS ADC can be used to effectively sample at 2 GSPS, providing 1 GHz of observational bandwidth. A 200 MHz "stretched" LTE signal is then acquired using this technique, and digital pre-distortion is applied to an amplifier under test to prove the concept.**

Index Terms — **Analog-to-digital converters, characterization, digital pre-distortion, radio frequency, receivers, wideband.**

I. INTRODUCTION AND SUMMARY

This work presents a hardware implementation of an interleaving technique [1] used to digitally extend the effective sampling rate of an analog-to-digital converter (ADC). In normal operation, an ADC can only observe a bandwidth that is identical to the sampling speed; through this work we show that the effective sampling rate can be increased, and therefore the observational bandwidth of an ADC. To prove that the increased sampling rate is accurate, digital pre-distortion (DPD) is then applied to an amplifier under test.

Other research in this area includes subsampling techniques in the presence of periodic signals [2], as well as complex modulated signals [3], frequency stitching [4] and under-sampling restoration digital pre-distortion (USR-DPD) [5]. One of the disadvantages of these techniques is the increased signal processing required. The advantage of the interleaving approach in [1] is that it requires minimum signal processing, but it is a strictly offline method. However an offline method is perfectly suited for the laboratory testing of amplifiers.

A full description of the under sampling interleaving technique can be found in [1]. For normal characterization techniques a known test signal is sent through a device under test (DUT), the output is then sampled and compared to the original signal. In this way, any distortion to the signal is due to the nonlinearities of the DUT, which can then be corrected with DPD. With this interleaving technique, a synthetic test signal is created by cyclically shifting the known test signal by 1 sample and appending it to the previous waveform copy. This creates a test signal which has the same characteristics as the original test signal, and hence has virtually no impact on the DUT's behavior. The number of times the test signal is shifted is related to the desired increase to the observable bandwidth.

One of the technologies to be associated with 5G is mmWave and wider channel bandwidths of at least 200 MHz;

this will therefore require further work into acquisition techniques in order to be able to properly sample higher bandwidths at mmWave. With wider bandwidths, the traditional vector signal analysis (VSA) based approach to sampling and applying DPD becomes increasingly difficult. This is because of analog filtering and the sampling speed of current VSAs, which are not wide enough to capture the full signal bandwidth and enough sideband information for DPD to work. Traditionally 3 or 5 times the signal bandwidth is require for DPD to work. Another approach is to down mix an RF signal to a suitable intermediate frequency (IF), and then sample it with a high speed oscilloscope. The disadvantage here is that high speed oscilloscopes have a lower dynamic range due to having less bits in the ADCs. The advantage of the interleaving approach demonstrated in this paper is that cheaper and slower ADCs with a high number of bits can be used. This approach is therefore a cost effective way of providing a high bandwidth sampling technique with a very high dynamic range.

In the prototype designed in this paper, a 250 Mega-samples-per-second (MSPS) ADC is used to effectively sample at 2 GSPS. This is an 8 times increase. The original signal is shifted 8 times, creating a signal that is 8 times longer and is clocked at 2 GHz. The ADC samples at 250 MSPS, and catches every 8th sample. All the original test samples are captured, but they are now in the wrong order; the signal is then de-interleaved and the original test signal can be recovered.

The contributions of this paper can be summarized as:

- FPGA/ADC based approach, rather than using a VSA interleaving approach as demonstrated in [1]. In the setup proposed in this paper, the full sampling speed is used due to less analog filtering on the RF front end of the ADC board.
- An 8-fold increase in the effective sampling speed from 250 MSPS to 2 GSPS using a custom built setup. Previous work in interleaving only demonstrated in hardware a maximum 5-fold increase in sampling speed, constructing an effective sampling speed of 120 MSPS [1].
- Showing up to a 10-dB increase in dynamic range compared to standard oscilloscope based measurement setups for wideband signals.
- Theoretical based implementation of mmWave signal acquisition and power amplifier linearization.

II. EXPERIMENTAL SET UP

A. Hardware Used and Acquisition Method

A block diagram of the hardware set up can be seen in Fig. 1. The hardware used for this experimental PA characterization set-up prototype is as follows. The ADC was an Analog Devices AD9643 mounted on an evaluation board, which was connected to an Analog Devices HSC-ADC-EVALCZ evaluation board; this allowed the ADC to be controlled and data acquisition to be carried out via a connected computer. The ADC board was operated using the Analog Devices, Visual Analog and SPI software. A baseband IQ signal was created by stretching a 20 MHz LTE to 200 MHz, the IQ signal was then up-converted to 500 MHz carrier frequency in MATLAB. 500 MHz was chosen as a carrier frequency as it provided a better starting point to any further up conversion to higher frequencies, including mmWave. The ADC was also AC coupled, and therefore similar in architecture to a non-zero IF down converter. The ADC board had a maximum RF bandwidth of 800 MHz, which would usually mean a maximum channel bandwidth of 5 times less than this, so 160 MHz. It was decided that a 200 MHz test signal was to be used as the amplifier under test was only mildly non-linear, so an observation bandwidth of three times the main channel bandwidth would be sufficient.

The test signal was then interleaved to create the synthetic test signal with a clock frequency of 2 GHz. The signal was then uploaded to a Keysight M8190A Arbitrary Waveform Generator. This generator was effectively used as a high speed digital-to-analog converter (DAC). From here, the 500 MHz IF signal could then be further up converted to a higher RF if required. The RF signal was then fed through the DUT before being down converted to 500 MHz IF, and then split between a Rohde and Schwarz FSQ26 Signal Analyzer and the ADC board. After data acquisition from the ADC board the data was evaluated in MATLAB, as well as performing DPD. After applying DPD, the signal was uploaded to the signal generator so the DPD improvements could be observed on the signal analyzer. The work flow can be seen in Fig. 2.

In order to fully observe a signal over a span of 800 MHz, 1.6 GSPS would be required to satisfy the Nyquist limit [6]. In order to fully explore the interleaving technique, an effective sampling rate of 2 GSPS was desired, giving a Nyquist limit of 1 GHz. Despite this being higher than the required Nyquist limit to observe the test signal, 2 GSPS was chosen for two reasons. Firstly, the ADC operates at 250 MSPS; the effective sampling rate needs to be an integer multiple of the ADC sampling rate, so 1.6 GSPS would not be achievable. Secondly, 2 GSPS was more convenient for the up sampling of the original 20 MHz LTE signal. 2 GSPS also provided the required synchronization between the DAC of the signal generator and the ADC of the receiver, which is essential for the interleaving technique to work. The original signal was interleaved 8 times; with the 250 MSPS ADC this would give the required 2 GSPS effective sampling speed.
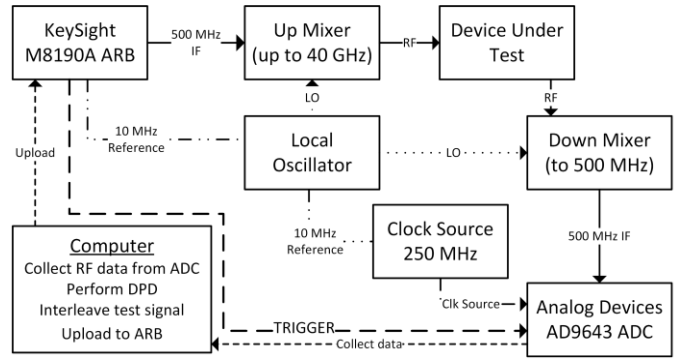

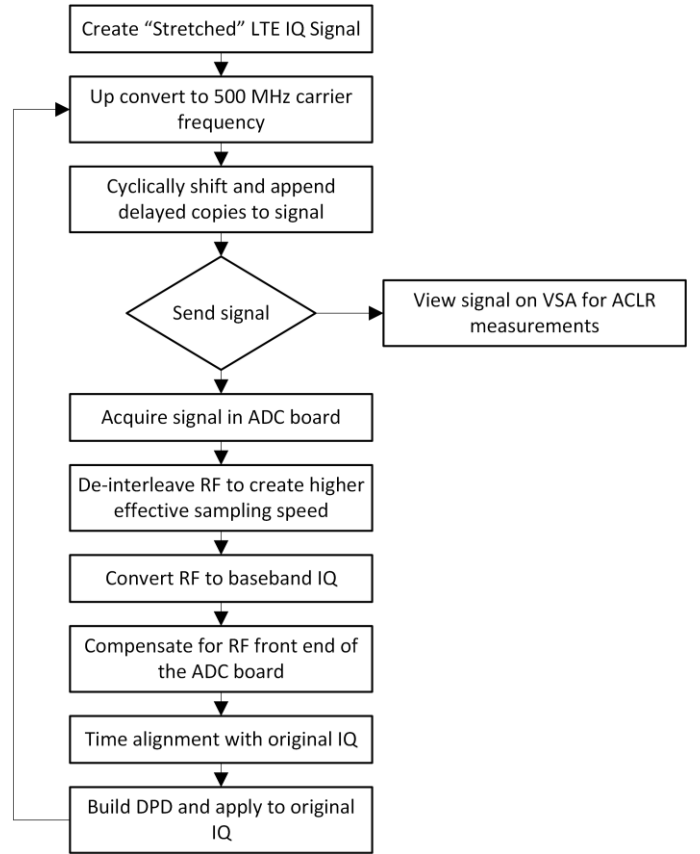Fig.1   Block diagram of the experimental test-bed set up.

Fig. 2   Work flow of the acquisition, interleaving and DPD method.

B. Preliminary Testing without a DUT

The IF signal at 500 MHz was fed directly into the ADC board. After the signal had been captured at 250 MSPS, it was then interleaved back to create an effective sampling speed of 2 GSPS. This interleaved RF was then passed through an 800 MHz low-pass filter (LPF) in MATLAB. This was because the effective RF bandwidth of the ADC board was 800 MHz.

Fig. 3 shows the full FFT of the signal as sampled by the ADC board before interleaving. The test signal is not fully observable and this would not be sufficient to be able to perform DPD to correct for any nonlinearities in a power

amplifier (PA). Fig. 4 shows the full FFT after interleaving, creating an effective sampling rate of 2 GSPS. As can be seen, the signal is now fully observable and correctly centered at 500 MHz. This now provides sufficient observational bandwidth for DPD to work, once the RF signal is converted back down to baseband IQ.

The IQ signal was calculated by demodulating from 500 MHz back down to baseband. This created an IQ signal that was compared to the original IQ signal for DPD synthesis. After the initial test run without a DUT, it was found, as expected, that the RF front-end of the ADC board exhibited a non-equal frequency response over its bandwidth. This could easily be compensated for by using a simple memory polynomial post-distortion technique, thus creating the coefficients to correct the ADC's RF front-end frequency response. This meant that when the DUT was being tested, the sampled IQ could be post distorted with the same coefficients to allow IQ comparison at baseband.

C. Comparing Interleaving Techniques with Traditional Acquisition Methods

The advantage of the interleaving technique is that it allows the use of slower ADCs with a higher dynamic range due to having more available bits. Fig. 5 shows a comparison of the interleaving approach and a more traditional approach with an oscilloscope. The data shown was captured using a Keysight MSO-S 804A at 2 GSPS. In both cases, the 500 MHz signal has been converted back to baseband IQ. The ADCs in this oscilloscope have a resolution of 10-bits, whereas the ADC board used for the interleaving has a resolution of 14-bits. Fig 5. shows that there is almost a 10 dB increase in the dynamic range by using the interleaving acquisition method.
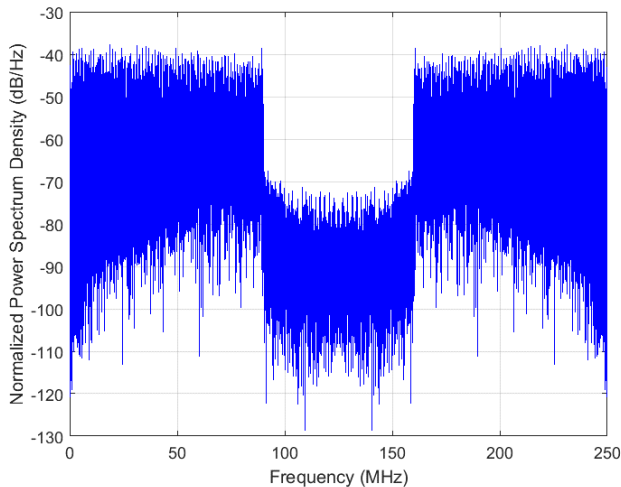

Fig. 3   FFT of the input signal at the ADC sampling rate of 250 MSPS. Due to the Nyquist limit, the actual observation window is only 125 MHz.
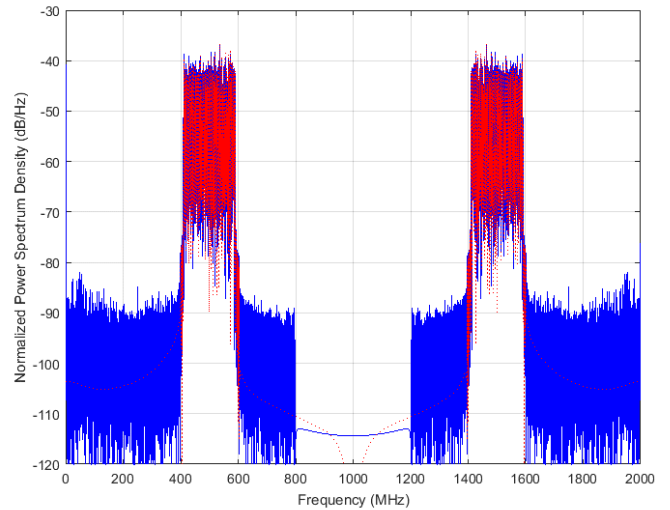

Fig. 4   FFT of the interleaved RF signal (blue) and the original RF signal (red). The effective sampling rate is now 2 GSPS giving an effective observational bandwidth of 1 GHz due to the Nyquist limit. The filtering after 800 MHz can clearly be seen.
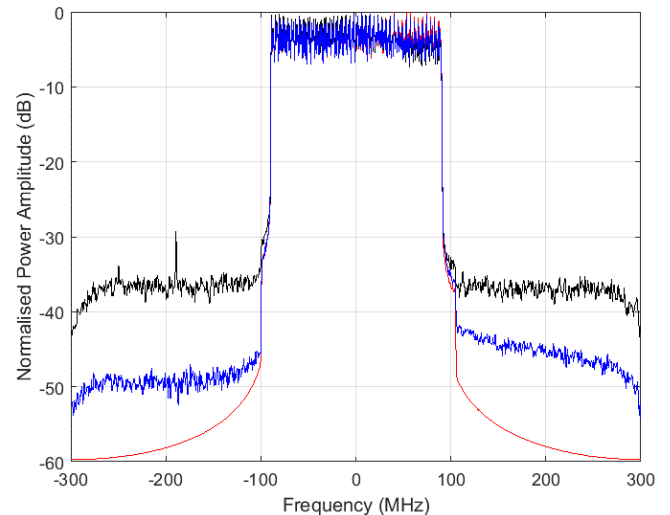

Fig. 5.   Comparison of acquisition techniques. The red plot is the original IQ signal as uploaded to the signal generator. The black plot is the oscilloscope acquisition method and the blue is the interleaving approach, including the post distortion to correct for the nonlinearities of the RF front end on the ADC board. Here, it can be seen that the dynamic range has been in-creased by almost 10 dB as a direct result of having more available bits in the ADC.

III. VALIDATION OF ACQUISITION METHOD FOR DPD

To fully test that the interleaved RF data is a correct representation of sampling at a higher sampling speed, an amplifier was used as a DUT. Under normal operation, one would require at least 3 times the signal bandwidth in order to observe enough side band information for DPD to work for a mildly non-linear DUT. If DPD could be applied using the interleaving technique to linearize an amplifier, this would

then prove that the interleaved data is an accurate representation of sampling at a higher data rate.

In order to fully test the validity of this sampling method, the 500 MHz IF would be up converted to a higher frequency for the DUT. The up and down mixers available at the time allowed this to be done at mmWave. A Miteq DB0440LW1 was used for the up conversion, this allowed a maximum frequency of 40 GHz. For the down conversion, a KeySight M9362AD01 PXIe Quad Downconverter: 10 MHz to 50 GHz was used. However, a suitable mmWave amplifier was unavailable at the time of doing these tests. In order to test the validity of the test set up, it was decided to up convert the signal to 7.5 GHz so an available DUT could be tested.

A Mini-Circuits ZVE-8G amplifier was used for this test. This is a wideband medium power amplifier, with a bandwidth of 2000-8000 MHz. The IF signal was first up converted to 7.5 GHz before being fed through the amplifier. The output was attenuated and then down converted to 500 MHz IF, before being split between the signal analyzer and the ADC board. Attenuators were used to protect the devices.

The same RF signal as discussed in section II was used and acquired using the ADC board and interleaving technique. A simple memory polynomial pre-distortion was applied to the acquired IQ signal, compared to the original IQ signal. The signal was then up-converted to 500 MHz carrier frequency as before and loaded into the signal generator. The resultant DPD signal as captured from the signal analyzer can be seen in Fig. 6; linearization has been achieved across 600 MHz of bandwidth. To achieve comparable nonlinearity compensation using commercial VSA systems, at least a 1.2 GSPS ADC would be required. This proves that the interleaving based PA characterization test bed proposed in this paper is capable of accurately capturing 2 GHz of bandwidth using only a 250 MSPS ADC.

IV. Conclusions

In this paper, a broadband testbed for PA characterization and digital pre-distortion was built. The sampling rate of the feedback path ADC was effectively increased using a digital domain interleaving technique. In the developed testbed, a 250 MSPS ADC was used to create an effective sampling speed of 2 GSPS. To assess the bandwidth extension of the characterization setup, a DUT was characterized using a 200 MHz test signal in order to build the corresponding DPD. It was shown that the proposed approach enabled the 250 MSPS ADC to linearize the PA over 600 MHz bandwidth, thus proving the broadband capabilities achieved using the concept of the considered interleaving technique.
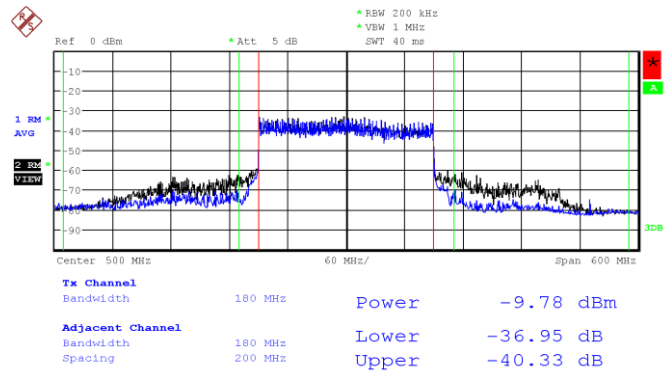

Fig. 6. DPD improvement of a wideband 200 MHz "stretched" LTE signal over 600 MHz captured using a 250 MSPS ADC and interleaving technique. The ACLR measurements settings (offset and integration bandwidth) used are scaled versions of the 20 MHz LTE signals standard.

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