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An E-mode p-channel GaN MOSHFET for a CMOS compatible PMIC

Ashwani Kumar, Member, IEEE, and Maria Merlyne De Souza, Member, IEEE

Abstract—The operation principle of a low power E-mode p-channel GaN MOSHFET is explained via TCAD simulations. The challenges of achieving negative threshold voltage with the scaling of gate length are addressed by adjusting the mole fraction of an AlGaN cap layer beneath the gate. An inverter consisting of the proposed p-channel GaN MOSHFET with a gate length of $0.25\ \mu m$ shows promise of a CMOS compatible Power Management IC in the MHz range.

Index Terms—2DHG, Enhancement mode, Gallium Nitride, p-channel MOSHFET, superjunction, inverter, switching speed.

I. Introduction

AMONG the various techniques for overcoming the trade-off between the on-resistance and breakdown voltage in a high power device in GaN, polarization superjunction (PSJ) technology [1], [2] is an attractive solution which can be considered as the equivalent of CoolMOS in silicon [3]. The presence of a polarization induced 2DHG above the 2DEG across the barrier layer forms a superjunction which helps prevent current collapse by suppressing the non-linear distribution of the electric field around the drain-side gate edge, [1], [2] thus improving the reliability.

The next challenge for GaN power devices is integration of the gate driver and power device, to reduce the parasitic loop inductance and facilitate high frequency switching in converters [4], [5]. Additionally, complementary logic with normally-off (E-mode) operation is preferred to reduce static power consumption, simplify circuitry and for fail-safe operation [6]. Therefore, a p-channel E-mode GaN MOSHFET is desirable.

The inherent use of the 2DHG in a PSJ heterostructure (GaN/AlGaN/GaN or GaN/AlInGaN/GaN) makes it a suitable platform for such integration. The operation of both p-channel and n-channel devices has been demonstrated on this platform [4], [7]. Achieving E-mode operation in GaN is challenging because the polarization induced 2DEG or 2DHG first needs to be depleted at zero gate voltage. In n-channel GaN HFETs or MOSHFETs, various techniques to implement E-mode behaviour are recessed gate [8]–[10], or ion implantation [11]–[13]: both methods can be employed on a PSJ platform. On the other hand, less attention has been paid to p-channel devices due to the low mobility of holes in GaN ($\sim 16\ cm^2/cm$ at room temperature [14]), which leads to poor on-current and switching speed. E-mode operation of p-channel HFETs has been attempted via recessed gate [5], [15], [16], an Al_2O_3 separated gate on a GaN/AlN heterostructure [17], or reducing the polarization charge in GaN/AlInGaN/GaN heterostructures by adjusting the Al or In mole fraction [18]. However, except for the recessed gate approach, the others have similar challenges associated with optimisation of the substrate layers for all other devices on the platform. These choices can lead to deterioration of the performance and reliability of the power devices by reduction in density of the 2DEG/2DHG respectively. Moreover, even with a recessed gate, we have earlier demonstrated a trade-off between the threshold voltage V_{th} and the on-current I_{ON} in the conventional p-channel MOSHFET that can be addressed by a thin AlGaN cap layer beneath the gate, to achieve better control [19]. In this work, the dependence of the electrical characteristics of a p-channel GaN MOSHFET on gate length is investigated on a platform that is fully compatible with a power device in PSJ technology. The substrate parameters are closely aligned to those reported in [5], [15]. Subsequently the switching speed of the inverter is evaluated.

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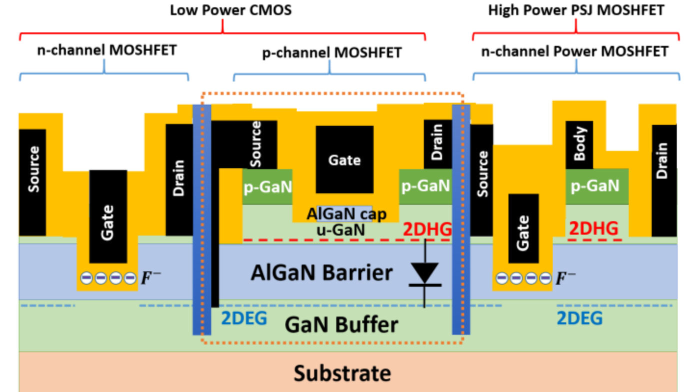

Fig. 1. Schematic of a common GaN/AlGaN/GaN platform consisting of low power CMOS and High Power PSJ MOSHFET. The 2DEG is connected to the ground. A combination of the 2DHG, AlGaN barrier, and 2DEG forms a diode that remains reverse biased.

II. Methodology And Settings

Fig. 1 highlights a schematic of an integration platform consisting of a low power CMOS device and a high power PSJ MOSHFET. In comparison to the work in [19], we consider a p-GaN/GaN/AlGaN/GaN heterostructure with layer specifications consisting of, from top to bottom, 30 nm Mg-doped p-GaN, 20 nm undoped GaN, $\sim 47-48\ nm$ AlGaN barrier with Al mole fraction of 23%, and a 1.5 μm GaN buffer on a substrate [20]. In comparison to the structure in [21], the 2DEG is connected to the ground. All simulations are

performed in Silvaco TCAD [22] using our model for the hole transport in p-channel GaN devices, calibrated against the experimental results of [15]. Accordingly, the maximum hole mobility is limited to $16\ cm^2/Vs$ [14] in a field dependent mobility model [23]. Additionally, a contact resistance ρ_c of $10^{-4}\ \Omega cm^2$ is used for source and drain contacts to p-GaN, which is an average contact resistance reported for p-GaN [24]. Charge and trap densities of $2.8 \times 10^{12} cm^{-2}$ and $2.5 \times 10^{12} cm^{-2}$ at oxide/GaN interface are found sufficient to match the experimental $I_{DS} - V_{GS}$ characteristics reported in [15].

III. Results And Discussions

E-mode operation in a conventional heterostructure without an AlGaN cap, may be examined by comparing the band diagrams at two different thicknesses of the oxide and channel layers (t_{ox} & t_{ch}) in Fig. 2 (a). Thinner oxide and GaN channel are required so that, sharp band bending in these layers can prevent the valence band at the GaN/AlGaN heterointerface from crossing the Fermi level, thus giving E-mode behaviour.

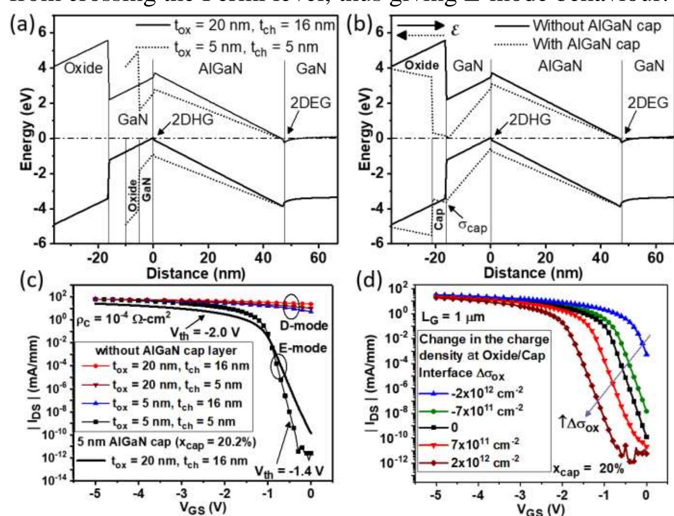

Fig. 2. (a) Comparison of the band diagram at two thicknesses of oxide and channel in a structure without an AlGaN cap, (b) Comparison of the band diagram with and without an AlGaN cap, (c) $I_{DS} - V_{GS}$ characteristics showing the dependence on thickness of the oxide and channel layers, with and without the AlGaN cap layer, (d) Impact of trap charge density at the interface of the oxide and AlGaN cap.

In contrast, inclusion of an AlGaN cap introduces a positive polarization charge at the heterointerface between the AlGaN cap and the GaN channel, σ_{cap}, which can be controlled by changing the Al mole fraction in the cap layer x_{cap}. A comparison of the band diagrams with and without the AlGaN cap in Fig. 2 (b), illustrates that a presence of the polarisation charge σ_{cap} increases band bending in the GaN channel, leading to elimination of the hole quantum well at the GaN/AlGaN interface. This consequently leads to E-mode operation for thicker layers of the channel and oxide in comparison to that in the conventional structure. It can also be noted in Fig. 2 (b) that the introduction of σ_{cap} alters the direction of the electric field in the oxide. This is of crucial benefit that reverses the behaviour of $|V_{th}|$ with respect to t_{ox} as opposed to that in the conventional device [19].

The transfer characteristics of devices in Fig. 2 (c) reveal that without the presence of the AlGaN cap, the thicknesses of the oxide and GaN channel layers (t_{ox} & t_{ch}) need to be reduced to $\sim 5\ nm$ to increase the $|V_{th}|$ to $|-1.4|\ V$. Such low values introduce considerable constraints on the manufacturability of the conventional structure. Owing to the trade-off between $|V_{th}|$ and $|I_{ON}|$, the maximum drain current $|I_{ON}|$, for the structure with AlGaN cap, at a higher $|V_{th}|$ of $|-2\ V|$ remains smaller ($25\ mA/mm$) than that of the structure without an AlGaN cap at a smaller $|V_{th}|$ of $|-1.4\ V|$ ($62\ mA/mm$). The trap charge at the interface of the oxide and AlGaN cap could vary due to processing or during device switching. Fig. 2 (d) compares the transfer characteristics with the change in the net trap density at the interface of the oxide/AlGaN cap σ_{ox}, showing that a large variation in σ_{ox} ($> 7 \times 10^{11} cm^{-2}$) can significantly affect the V_{th} and on-off current ratio of the device.

As shown in Fig. 1, a combination of the 2DHG, AlGaN barrier, and 2DEG acts as a p-n diode, where the AlGaN barrier of $47\ nm$ acts as a depletion region between the 2DEG and 2DHG. With negative voltage on the drain and gate, this diode remains reverse biased, and leakage current through the 2DEG in this condition has been experimentally shown to be $\sim 10\ nA/mm$ through the AlGaN barrier [25]. This agrees with negligible values in the simulations.

The behaviour of the threshold voltage with the Al mole fraction x_{cap}, in Fig. 3 (a), depicts a rise in $|V_{th}|$ with x_{cap}. At higher x_{cap}, the band bending in the GaN channel becomes more pronounced due to an increase in polarisation σ_{cap}, leading to a lowering of the valence band at the GaN channel/AlGaN barrier interface. A $|V_{th}|$ of $|-3.0\ V|$ is achievable for an x_{cap} of 23%.

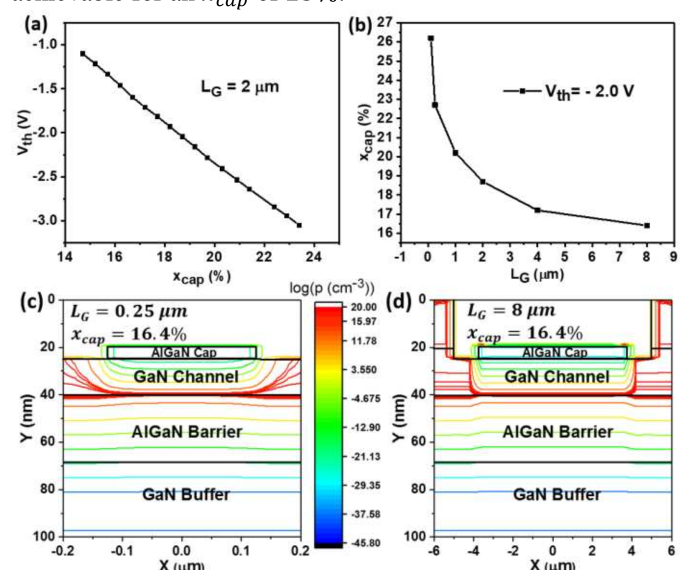

Fig. 3. (a) Threshold voltage V_{th} vs. Al mole fraction in the AlGaN cap layer x_{cap}. (b) x_{cap} vs. gate length L_G to maintain a fixed V_{th} of $-2\ V$. (c) and (d) (colour online) are contour plots of the hole density for the devices with gate lengths of 0.25 μm and 8 μm, respectively.

In comparison to silicon, the V_{th} of the current heterostructure is not just dependent upon the vertical thicknesses but also severely the gate length L_G. It is seen in Fig. 3 (b) that with reduction of L_G, a higher x_{cap} is required to maintain the $|V_{th}|$ at $|-2\ V|$. To understand this behaviour, the

contour plots of the device cross section under zero gate bias are presented in Figs. 3 (c) & 3 (d) for two different gate lengths ($0.25\ \mu m$ and $8\ \mu m$). The dependency between V_{th} and L_G arises from the fact that a 2DHG forms at the bottom interface of the GaN channel which is farther from the gate rather than at the top interface. Hence, even though holes in the vicinity of the top interface in the GaN channel are depleted irrespective of the gate length, as shown in Figs. 3 (c) & 3 (d), there is a finite penetration of holes under the gate at the bottom interface of the channel. It is observed from Figs. 3 (c) & 3 (d) that at smaller L_G, the relative penetration of holes at the bottom interface of the GaN channel under the AlGaN cap is higher, leading to a degradation in $|V_{th}|$. Hence, x_{cap} needs to be raised from $16.4\ \%$ to $26.2\ \%$ as the gate length is reduced from $8\ \mu m$ to $0.10\ \mu m$ to maintain V_{th} at a fixed value of $-2.0\ V$ (Fig. 3 (b)).

As shown in Fig. 4, utilising a smaller channel length not only increases the on-current but also leads to an improvement in on-off current ratio I_{ON}/I_{OFF} for devices with identical V_{th}. With smaller L_G, the length of the region depleted of 2DHG in the GaN channel also becomes smaller, leading to a reduction in the total sheet resistance between the drain and source. Therefore, $|I_{ON}|$ of the device improves at smaller L_G, achieving a maximum of $37\ mA/mm$ at L_G of $0.10\ \mu m$. The improvement in I_{ON}/I_{OFF} emerges from a higher x_{cap} at smaller L_G to maintain the threshold voltage. The rise in σ_{cap} with higher x_{cap} suppresses the relative penetration of holes under the gate thereby minimizing the leakage current. Hence, the ratio of I_{ON}/I_{OFF} shows an improvement from ~ 2 to ~ 12 orders of magnitude as L_G shrinks from $8\ \mu m$ to $0.25\ \mu m$. However, at the shorter gate length ($0.10\ \mu m$), a higher σ_{cap}, necessary to maintain the same V_{th} no longer suffices to suppress the relative penetration of holes under the gate. This increases the off-current of the device, resulting in a degradation in the on-off current ratio by an order of magnitude. Hence a gate length of $0.25\ \mu m$ can be considered optimal.

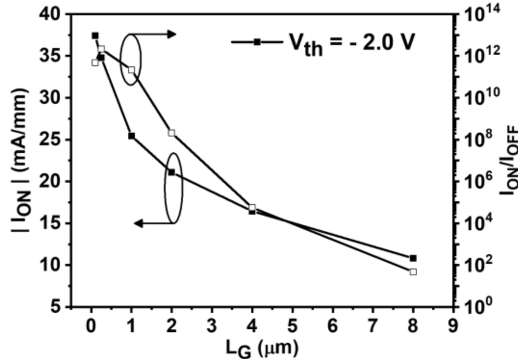

Fig. 4. Behaviour of the on-current $|I_{ON}|$ and I_{ON}/I_{OFF} with gate length L_G as x_{cap} is changed to keep a fixed threshold voltage V_{th} of $-2.0\ V$.

The circuit diagram for calculating the rise time and switching speed of an inverter, using mixed mode simulations is shown in Fig. 5 (a). The rise time for a load capacitor C_L is calculated as $t_{Rise} = \int_0^{0.9\times V_{DD}} dV \cdot C_L/I_{DS}$. The total load capacitance for a fan-out of 5 at the output is estimated as:

$$C_L \approx 5\left(1+\frac{W_n}{W_p}\right)C_{GS,max} + \left(1+\frac{W_n}{W_p}\right)C_{DS,max} \quad (1)$$

where $C_{GS,max}$ and $C_{DS,max}$ are the maximum values of the gate and drain capacitances for the p-channel GaN MOSHFET, and the factor $(1 + W_n/W_p)$ accounts for n- and p-channel devices with W_n and W_p widths. With W_n/W_p of $1/10$, the rise time t_{Rise} of devices, with and without the AlGaN cap, are extracted from the transient simulations of output voltage V_{OUT} with time in Fig. 5 (b) at a gate length of $0.25\ \mu m$. A 3 times higher t_{Rise} for the device without the AlGaN cap is the result of thinner oxide and channel layers, which leads to much higher $C_{GS,max}$, $2.0\ pF/mm$, compared to $0.3\ pF/mm$ for the device with AlGaN cap. $C_{DS,max}$ for the two devices remains $\sim 1.5\ pF/mm$, higher than $C_{GS,max}$ in the device with AlGaN cap, owing to the parasitic capacitance introduced by the underlying 2DEG, which is estimated to be $\sim 1.23\ pF/mm$, from the simulation of C_{DS} at different thickness of AlGaN barrier t_b (not shown). Assuming both p-channel and n-channel have similar rise and fall times at W_n/W_p of $1/10$, the switching speed f_{sw} of the inverter described as:

$$f_{sw} = (t_{Rise} + t_{Fall})^{-1} \approx (2 \cdot t_{Rise})^{-1} \quad (2)$$

yields a value of $\sim 625\ MHz$ for a C_L corresponding to a fanout of 5.

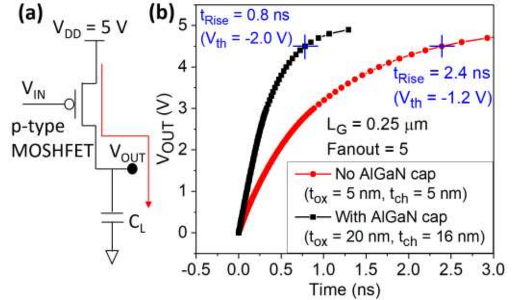

Fig. 5. (a) Circuit diagram for calculating the rise time, (b) Output voltage or variation of the load voltage in devices without and with AlGaN cap vs. time as the input voltage is switched from $5\ V$ to $0\ V$ at $t = 0$.

Compared to a t_{Rise} of $670\ ns$, reported by R. Chu et al. [5] for their fabricated p-channel device, a significantly smaller t_{Rise} is the result of much smaller on-resistance (R_{on}) and load capacitor of $143\ \Omega\cdot mm$ and $3.3\ pF/mm$ compared to their values of $1314\ \Omega\cdot mm$ and C_L estimated $\approx T_{Rise}/2.2R_{on} = 231\ pF/mm$, respectively from their work. Our smaller on-resistance is the result of higher on-current facilitated by lower access resistances and depletion beneath the channel, facilitated by the AlGaN cap. If their value of C_L of $231\ pF/mm$ were employed, the corresponding rise time is predicted to be $56\ ns$, an improvement of at least a factor of 10 in switching speed.

IV. Conclusion

A low voltage p-channel E-mode GaN MOSHFET for integration alongside a high power device on a common GaN/AlGaN/GaN platform is investigated. The E-mode operation is realised using a thin AlGaN cap layer between the GaN channel and gate dielectric that suppresses the penetration of holes beneath the channel. The technique not only improves the on-current but also suppresses the leakage current, leading to orders of magnitude improvement in on-off ratio at short gate lengths. The simulated inverter offers promise of CMOS integrated gate drivers for MHz switching of power conversion circuits in GaN.

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