Cyclic voltammetry peaks due to deep level traps in Si nanowire array electrodes

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Abstract When metal-assisted-chemical-etching (MACE) is used to increase the effective surface area of Si electrodes for electrochemical capacitors it is often found that the cyclic voltammetry characteristics contain anodic and cathodic peaks. We link these peaks to the charging-discharging dynamics of deep level traps within the nanowire system. The trap levels are associated with the use of Ag in the MACE process that can leave minute amounts of Ag residue within the nanowire system to interact with the H₂O layer surrounding the nanowires in a room temperature ionic liquid. The influence of the traps can be removed by shifting the Fermi level away from the trap levels via spin-on-doping. This results in lower capacitance values but improved charge-discharge cycling behaviour. Low frequency noise measurements proof the presence or absence of these deep level traps.

Index terms: silicon nanowires, deep level traps, electrochemistry, supercapacitor

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I. INTRODUCTION

Si nanowire arrays (NWAs) are investigated for use as electrodes in electrochemical energy storage devices such as supercapacitors [1] and batteries [2]. Electrodes in electrochemical storage devices are normally based on highly conductive materials with large surface area such as e.g. activated carbon [3]. The interest in Si-based electrodes is mainly driven by the ubiquitous character of Si and its well-established CMOS (complementary metaloxide-semiconductor) related fabrication technology that opens the field of monolithically integrated storage devices in consumer electronics. Large surface areas can be obtained by converting Si bulk into NWAs. These can be made in different ways such as, vapor-liquid-solid (VLS) growth [4], electrochemical etching [5], reactive ion etching (RIE) [6] and metal-assisted chemical etching (MACE) [7]. MACE offers a simple wet electrochemical method to create a NWA from Si bulk that avoids the use of vacuum equipment. In this work, Si NWAs are fabricated via MACE using Ag as catalyst. The NWs are coated with a thin SiO₂ layer in boiling nitric acid to improve their electrochemical robustness. They are used as the working electrode in the room temperature ionic liquid (RTIL) [Bmim][NTf₂].



Figure 1: SEM cross section of a Si NWA after 1 SOD (left) and 3 SOD steps (right). The difference in length is due to slight variations in etch conditions and the SOD oxidation and oxide removal process that removes the bundled top region of the NWA.

The electrochemistry at the semiconductor-electrolyte interface is different from that of a metal-electrolyte

interface in that both a bandgap as well as a space charge region exist in semiconductors that are absent in

metals [8]. In principle, the capacitance of the space charge region, C_{sc} is in series with that of the double layer in the electrolyte, C_{dl} . If C_{sc} is small in comparison to C_{dl} , it can dominate the capacitance of the system. Therefore, heavily doped Si NWAs are required to reduce the width of the space charge region. Another important feature of semiconductors is the presence of interface states at the surface of Si. These states introduce energy trap levels in the bandgap of the semiconductor at the interface with the electrolyte. The trap levels pin the Fermi level when the interface state density is high, such that the space charge region is electrically shielded from the applied voltage. In that case, the applied voltage drops mainly across the electrochemical double layer [9], allowing the structure to work as a double layer electrode. The high density of dangling bonds and surface defects in MACE-fabricated Si NWAs results in a high density of surface trap levels [10]. In addition to interface states, the material preparation process can introduce additional active trap centres. It has been reported that the metals used for MACE, such as Au or Ag [11, 12], can diffuse into the material and create metal-specific deep level trap centres. For our system, we have confirmed the presence of deep level traps in the Si NWA electrodes by low frequency noise measurements that proof the existence of a strong generation-recombination centre at low frequency (large time constant). The cyclic voltammetry measurements of the Si NWA-RTIL interface then shows anodic and cathodic peaks that are related to each other and are independent of the RTIL chosen. We associate these peaks with the charging and discharging of the Agrelated deep level traps in the Si NWs and a thin H₂O layer that surrounds the NWs in the array [13].

A possible method to remove the residual Ag and passivate the Si NW surfaces is rapid thermal oxidation (RTO) and oxide removal [10]. This method was applied and it reduced the amplitude of the peaks but did not remove them altogether. Another method is based on the knowledge that the electrical activity of the deep level traps depends on their energetic position in the bandgap with respect to the Fermi level. Increasing the doping of the Si NWA via e.g. spin-on-doping (SOD) [14] moves the Fermi level in the silicon below the band edge for degenerate doping densities. This hinders charge transfer between the deep level traps and the electrolyte. Accordingly, in those cases, low frequency noise measurements confirm the de-activation of the trap levels for any SOD type, B, Al, and Ga used.

II. EXPERIMENTAL

<100> p-type silicon samples, with resistivity ρ = 0.01-0.02 Ω cm (B doped, $N_A \sim 10^{18}$ cm⁻³) and 2 cm x 2 cm area, were used. The samples were cleaned in solvents followed by a piranha etch (3:1 H₂SO₄:H₂O₂) for 10 min. The back side is protected during the 2-step MACE process: the 1st step in 0.005 M AgNO₃ : 5 M HF for 2 min nucleates Ag nanoparticles (NPs) on the Si surface ; the 2nd step in 0.1 M H₂O₂ : 4.9 M HF for 60 min etches the NWs. The Ag NPs are removed in 1:1 concentrated HNO₃ : DI water for 3 min. Samples are thoroughly rinsed in DI water after each step. The range of diameters of the nanowires lie between 50 nm – 300 nm. The length and the density of the Si NWs are 15 - 20 μ m and ~10⁹ NWs·cm⁻², respectively. For boron SOD the native oxide is first removed in 5% diluted HF. SOD was spun at 2500 rpm for 40 s with an initial acceleration of 500 rpm·s⁻¹. Solvents are removed on a hotplate at 200 °C for 6 min and dopant activation was done by rapid thermal annealing at 800 °C for 1 min under O₂ atmosphere to avoid the growth of a boron rich layer [15]. The resulting glass layer is removed in diluted HF. The SEM crosssection of the Si NWA after 1 and 3 SOD steps is given in figure 1.

Heated, concentrated HNO₃ (10 min) was used to coat all Si NWAs with a thin (~2 nm) SiO₂ layer to protect the Si NWs from electrochemical reactions [1- Qiao]. The back side of the sample was metallised with a 100 nm Al layer after RIE (reactive ion etching) oxide removal in CHF₃ (25 sccm) - Ar (25 sccm) - O₂ (2 sccm) at 200 W for 5 min at 20 °C. The contacts were annealed at 200 °C for 1 min under Ar atmosphere.

A CH760C potentiostat was used for cyclic voltammetry (CV) with a three-electrode setup. The Si NWA is used as the working electrode, a Pt coil wire as the counter electrode and an Ag wire as the pseudo-reference electrode. All electrodes were thoroughly cleaned before use. Measurements are carried out in ionic liquid [Bmim][NTF2], dried at 80 °C under vacuum for 12 hours giving a Karl-Fischer titration water contents of 11 ppm. The electrochemical window of a Au/dried [Bmim][NTF₂] system is ~4.4V. The electrochemical cell used was custom built [16]. The electrochemical potential window (EW) was chosen to be in the voltage range for which I_{max} < 3 x I_{mw} , where I_{max} is the current at the edge of the voltage window and I_{mw} in the middle of the voltage window. For CV characteristics with current peaks, the operating potential window was constrained to voltages where $I_{max} \approx I_p$ with I_p the redox peak current.

The areal capacitance, C can be calculated from a CV plot using:

$$C = \frac{i}{dV/dt} \cdot \frac{1}{A} \tag{1}$$

where $i = \frac{i_a + i_p}{2}$ with $i_{a,p}$ the anodic and cathodic current, defined from the voltammogram at their minimum absolute value, dV/dt is the experiment's scan rate and A is the projected surface area. The working electrode surface area, is A = 1.327 cm². The effective surface area of the NWA, A_{eff} is estimated using the capacitance value of a Si bulk sample prepared without SOD and coated in 120 °C HNO₃ giving $C = 6 \ \mu$ F. The extracted capacitance value, using the same preparation technique on a Si NWA that does not exhibit peaks is $C = 1060 \ \mu$ F. Using these known values, the unknown NWA-structured surface area can be estimated. This gives an effective NWA surface area in contact with the liquid $A_{eff} = 234$ cm². The reported areal capacitances are calculated using A.

The 1/f noise spectral density due to voltage fluctuations, S_V from the load resistor, R_L connected in series with the NWA were obtained using a SR770 FFT spectrum analyzer in a frequency range from 1 mHz to 100 kHz at 300 K. Background noise was measured using the zerobias set-up and subtracted from the total device noise. Measurements used the custom built electrochemical cell

that was placed in a Faraday cage and the devices were biased with a battery at 1 V [17]. Contacts were made with a 3 mm diameter spring-loaded Au top probe onto the NWA and a Cu back plate. The spectral noise density of the short circuit current fluctuations, S_l , was calculated using the formula:

 $S_{I} = S_{V} \left[\frac{R_{L} + R_{D}}{R_{L} \times R_{D}} \right]^{2}$ where R_{D} is the NWA's differential resistance. (2)

III. RESULTS AND DISCUSSIONS

The cyclic voltammogram (CV) of the non-degenerately doped SiO₂-coated Si NWA in [Bmim][NTf₂] is shown in figure 2. The CV scans are given for increasing voltage windows, starting from –ve. The CV measurement shows an anodic (+ve) and cathodic peak (-ve). Initially no reduction peak is observed until the forward scan nears the potential for the oxidation peak (inner blue dashed line). Extending the forward scan voltage shows a strong increase of the reduction peak as the oxidation peak potential is reached (red full thick line). These observations demonstrate that the peaks are related.



Figure 2: Cyclic voltammograms of the non-degenerately doped SiO₂ coated Si NWA in [Bmim][NTf₂] for different potential scan ranges with scan speed, $v = 200 \text{ mV} \cdot \text{s}^{-1}$. Potentials are plotted versus the Ag pseudo reference electrode. All scans started at the same negative potential (-ve) but the voltage scan window is increased in the positive direction.

In order to exclude the RTIL as the origin of the peaks, CV measurements were carried out in different electrolytes, including an aqueous solution of NaClO₄·H₂O, LiClO₄ in propylene carbonate and the [Emim][HSO₄] ionic liquid. The results are given in figure 3. Indeed, common to all the CVs is the occurrence of a redox feature within the EW of the electrolyte medium. The peak position shifts due to the different reference potentials in the respective media. The presence of peaks in all four media confirms that their origin is not due to the electrolyte system, but instead related to the electrode itself and/or a common impurity in solution or on the surface.



Figure 3: Cyclic voltammograms of the non-degenerately doped SiO₂ coated Si NWAs – in 0.5 M NaClO₄.H₂O (red line), 0.5 M solution of LiClO₄ in propylene carbonate (PC) (blue line), and in [Emim][HSO₄] (green line) in comparison with in [Bmim][NTf₂] (black line) at v = 50 mV·s⁻¹.

The role of the electrode surface is investigated in further detail to establish whether other process parameters influence the peaks. Bulk Si samples with different SOD doping atoms (B, Ga and Al), coated in a thin SiO₂ layer using heated HNO₃ are used. No peaks are observed for these samples (figure 4), indicating that the peaks are unrelated to the SOD doping atom. In addition, CV measurements were carried out on bulk samples that underwent all MACE process steps, but without using AgNO₃. These samples have no NWs and did not show redox peaks (CV plots are similar to figure 4). These results exclude peaks related to contamination of the set-up or chemicals used. The remaining discriminating factor in MACE-etched NWAs is the use of Ag as a catalyst.



Figure 4: Cyclic voltammogram for SiO₂-coated bulk Si electrodes in [Bmim][NTf₂] at $v = 100 \text{ mV} \cdot \text{s}^{-1}$. Black line: untreated Si bulk, red line: B-SOD, blue line: Al-SOD and green line Ga-SOD.

In previous work, we found H_2O in the Si NWA, even under vacuum conditions [13]. It is thus possible that adsorbed H_2O layers play a part in the observed redox activity. Adsorbed water layers will be present on both bulk and NWA, but for bulk Si electrodes, the corresponding redox process does not occur or may be kinetically hindered. Redox peaks on bulk are unlikely to remain undetected, as the capacitive background current is significantly reduced compared to the Si NWA samples.

In [11], EDX on single NWs demonstrated that minute concentrations of Ag nanoparticles of less than 0.2% can remain on the NWs after the etch process, especially when bunching at the top of the nanowires hinders efficient Ag removal. In [12] the authors similarly reported

the presence of low concentrations of Ag that causes deep level trap states in the bandgap of Si with a concentration of the order to 10^{13} cm⁻³. We evaluate the presence of deep level traps by low frequency noise measurements. 1/f noise in Si/SiO₂ devices is generated by carrier trapping and de-trapping [18]. The 1/f shape of the noise spectral density is the result of the sum of Lorentzian power spectra, each associated to the lifetime of the different traps. For strong active deep level traps, the low frequency Lorentzian noise plateau becomes identifiable and defines the lifetime of the active trap level



Figure 5: Normalised current spectral noise density as a function of frequency (log-log plot) for the NWA showing peaks for a bias of 1 V. The dashed lines give the slope of the spectrum in different frequency ranges. The inset gives the normalised current spectral noise multiplied by the frequency. The position of the peak determines the lifetime of the characteristic trap level.

The low frequency noise measurements on Si NWAs (see figure 5) show very high amplitudes of normalized current spectral noise density, S_{l}/l^{2} due to the nearly continuous distribution of trap levels in the bandgap (interface states) [19] of the un-passivated NW surfaces. The 1/f noise spectrum of the Si NWA with redox peaks shows a clear deep level trap. Figure 5 shows a $f^{-\gamma}$ with $\gamma \approx 0.9$ behaviour at higher frequencies, representative of majority carrier number fluctuations [20]. At intermediate frequencies, $\gamma = 2$, indicative of a strong carrier generation-recombination (G-R) centre [21]. The inset highlights the position of the G-R centre, determined by the maximum value of $S_l \times f/l^2$ that defines the lifetime of the trap: $\tau \approx 5$ s. This result confirms the presence of a strong specific trapping centre in the Si NWA. A simple way to remove the surface traps is to remove the surface layer of the NWs. This can be done by oxidation and subsequent oxide removal. We have applied two methods: in the 1st method the Si NWA was oxidised 3 times using boiling HNO₃ at 90 °C for 10 min each and the resulting oxide was removed in a 5 min. 1 ml HF(50%): 10 ml DI water mixture after each oxidation

step. A 4th and last HNO₃ step was applied to obtain a thin SiO₂ surface layer. Based on the assumption that for 1 nm oxide 0.46 nm Si is consumed, this removes an estimated ~2.5 nm of Si. In the 2nd method, rapid thermal oxidation (RTO) [10, 22] was used twice at ~850 °C and the oxide was stripped after each step in the same way as the 1st method. The total thickness of removed Si is estimated at ~5 nm. A final HNO₃ steps coats the NWs with SiO₂. Figure 6 compares the CV plots of the three different electrodes. The oxide strip process reduces the absolute value of the current peaks and the overall current. Although less Si is removed in the 3x HNO₃ oxidation and strip process, the peak is reduced more. This might be caused by Ag diffusion further into the NWA for the higher temperature steps in the RTO. Additional oxidation and strip steps might ultimately remove the current peaks.

In a second approach, the influence of the G-R centre can also be removed by shifting the Fermi level away from the trap centre. This is achieved by changing the doping density in the Si NWA via SOD. In order to shift the Fermi level into the valence band (degenerate doping), the Si NWAs are doped using 3 SOD steps.



Figure 6: Cyclic voltammograms of three Si NWAs coated in SiO₂ measured in [Bmim][NTf₂] at v = 100 mV s⁻¹. The solid line is the reference, the dotted line is after 3 HNO₃ oxidations and oxide strips, the dashed line is after 2 RTO and oxide strips.

Three different doping atoms are used: B, Al and Ga. The CV and noise measurements are shown in figure 7. None of the CVs shows any significant redox activity in the relevant potential range and the G-R signal has also disappeared from the 1/f noise spectrum. Hence, there appears to be a correlation between the

activity of the trap states and the redox activity of the electrode/solution interface [23]. The electron transfer partner in solution cannot be the RTIL itself because electron transfer to or from the RTIL cation and anion, respectively, occurs outside the EW, while the observed redox activity is observed within the stability window of the RTIL. An alternative explanation involves adsorbed H₂O on or inside the Si NWA, potentially providing the required donor and acceptor levels. This is in line with our previous findings [13] and those in reference [24]. The latter propose equilibration of deep-level surface states with water, rather than with the semiconductor, via surface state mediated electron transfer. Figure 8 gives a schematic of an energy band diagram with Ag related traps in the Si bandgap, in contact with an H₂O layer. Common trap levels in Si, associated to Ag are at a position of ~0.56 eV under the conduction band edge (an acceptor state) and ~0.23 eV above the valence band edge (a donor state) [25]. The population of traps is determined by their position relative to the Fermi level and carrier generation-recombination processes [19]. The Fermi level in Si is pinned due to the large density of surface states [5]. Therefore, the external voltage will drop mainly across the electrolyte [4]. The space charge region drawn at equilibrium (figure 8a) is based on the results of thermoelectric measurements on Si NWAs that show that the surface of MACE etched p-Si NWs is depleted [26]. Degenerately doped Si (figure 8b) shows less surface depletion.



Figure 7: (a) Cyclic voltammograms of a 3x B (red line), 3x AI (blue line) and 3x Ga (green line) SOD Si NWA coated in SiO₂ measured in [Bmim][NTf₂] at $v = 100 \text{ mV} \cdot \text{s}^{-1}$. (b) Normalised current spectral noise density as a function of frequency for the 3x B-doped sample at V = 1V. The dashed line highlights the $\gamma = 1$ slope of the spectrum.

The energy band diagrams are based on the model proposed by N. Sato for adsorbed species [27] and are a qualitative schematic representation. When no SOD is applied, the Si NWA is non-degenerate and the Fermi level E_F , lies above the valence band edge E_v . In this case, the donor level d is filled. When a positive bias is applied to the electrolyte with respect to the Si NWA, the donor trap d releases its electrons into the electrolyte

electron acceptor level, A (figure 8a2). In the opposite bias direction (figure 8a3), the electrolyte transfers electrons back into the donor trap level d. This is consistent with figure 2 where the cathodic peak is only established when the anodic peak happens. The trap level d first needs to empty its electrons before the electron transfer from the electrolyte electron donor level D can occur. The position of the Fermi level is critical for these carrier exchanges to occur. If the Si is degenerately doped, as given in figure 8b, then the donor trap level is empty. Applying +ve (figure 8b2) overlaps the empty donor trap level d with the empty acceptor level A, no electron transfer occurs. For the opposite bias (figure 8b3), no transfer is possible as long as d and A overlap. The absence of anodic and cathodic peaks in n-type Si NWAs [1 – Qiao] is also consistent with this reasoning because the Fermi level is positioned well above the Ag trap centres for n-doped Si.

The presence of deep level traps in Si NWA electrodes for supercapacitors has an impact on the operation stability of the electrode. Although the capacitance value of the electrodes with traps is higher (see Table 1), its performance degrades faster with number of chargedischarge cycles as illustrated in figure 9.



Figure 8: Sketch of energy band diagrams [1], a) non-degenerate Si NWA and b) degenerate Si NWA. Numbers 1, 2, 3 give equilibrium, +ve and -ve bias, respectively. a (acceptor) and d (donor) are the Ag related trap levels. The Fermi level is pinned, thus the space charge region is independent of bias, ve. N_T refers to the density of traps, subscript 0 refers to a charge neutral donor trap filled with electrons, whilst + refers to an empty trap level.

The higher initial capacitance is due to the capacitive dynamics of the charge exchange via traps whilst the degradation upon cycling might be due to an additional leakage current channel formed by the redox active sites.

Table 1: Numerical performance values for B-doped Si NWAs as an electrode in [Bmim][NTf₂]. EW: electrochemical window, *I*_{mw} midway current, and C capacitance per projected area calculated from the CV plots.

Working electrode	EW (V)	<i>I_{mw}</i> (A)	$C (\mu F/cm^2)$
No SOD	2.8	9.75 x 10⁻⁵	799
3xSOD	3.1	6.40 x 10⁻⁵	254

The device without redox peaks exhibits only a 6.5% capacitance loss over 3000 cycles, with the last 1500 cycles demonstrating device stability. However, the device with redox peaks exhibits a higher loss of capacitance of 17.3%, reaching an approximately constant value over the last 1000 cycles only.

IV. CONCLUSIONS

We measured and analyzed the occurrence of redox peaks in the cyclic voltammogram of p-Si NWA-ionic liquid interfaces. These redox peaks are associated to direct charge exchange between deep level traps in the Si and the thin H₂O layer that surrounds the NWs in the ionic liquid. The occurrence of slow traps was proven by low frequency noise measurements that identified a strong generation-recombination center with a lifetime of ~5 s. The deep level traps can be associated with diffused Ag, used as a catalyst in the nanowire fabrication process. Although removal of the surface layer of the Si NWs via an oxidation and strip method decreases the peaks, increasing the doping density to a degenerate level in the NWs via e.g. spin-on-doping might be a more effective method to de-activate the traps. Doping moves the Fermi level below the donor trap center, making is inactive within the EW. Cyclic voltammetry and low frequency noise measurements confirm the de-activation of the trap level for increased doping. The relevance of the presence of traps in Si

NWA-electrolyte applications is its reduced operation stability resulting in a higher capacitance loss with charge-discharge cycling. In addition, MACE-fabricated NWAs have become increasingly popular in black silicon solar cell applications. High levels of surface states and possible deep level traps will have a destructive influence on carrier surface recombination. Our work shows that Si surface removal via oxidation and oxide strip steps need to be carried out multiple times and at low temperatures in order to remove these traps from the surface. Designing a PV structure with degenerate doping in the NWA structure might be a better option to de-activate the deep level traps.



Figure 9: Capacitance retention over 3000 cycles for the Si NWA without peaks (black) and with redox peaks (red). Retention % is labelled at the 3000th cycle.

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VI. REFERENCES

 F. Thissandier, A. Le, O. Crosnier, P. Gentile, G. Bidan, E. Hadji, T. Brousse, and S. Sadki, "Highly doped silicon nanowires based electrodes for microelectrochemical capacitor applications," *Electrochem. commun.* 25, pp. 109–111 (2012).
 F. Thissandier, L. Dupré, P. Gentile, T. Brousse, G. Bidan, D. Buttard, and S. Sadki, "Ultra-dense and highly doped SiNWs for micro-supercapacitors electrodes," *Electrochim. Acta* 117, pp. 159–163 (2014).
 L. Qiao, A. Shougee, T. Albrecht, and K. Fobelets,

"Oxide-coated silicon nanowire array capacitor electrodes in room temperature ionic liquid," *Electochim. Acta* 2, pp. 32–37 (2016).

[2] M. Ge, X. Fang, J. Rong and C. Zhou, "Review of porous silicon preparation and its application for lithium-ion battery anodes", *Nanotechnol.* 24(42), pp. 422001-422010 (2013).

X. Su, Q. Wu, J. Li, X. Xiao, A. Lott, W. Lu, B. W. Sheldon, and J. Wu, "Silicon-Based Nanomaterials for Lithium-Ion Batteries: A Review", Adv. Energy Mater. 4(1), pp. 1-23 (2014).

[3] W. Ma, S. Chen, S. Yang, W. Chen, W. Weng, and M. Zhu, "Bottom-Up Fabrication of Activated Carbon Fiber for All-Solid-State Supercapacitor with Excellent Electrochemical Performance", *ACS Appl. Mater. Interfaces* 8(23), pp 14622–14627 (2016).

- [4] Y. Wu and P. Yang, "Direct Observation of Vapor -Liquid - Solid Nanowire Growth" J. Am. Chem. Soc. 123, pp. 3165–3166, (2001).
- [5] P. Kleimann, J. Linnros, R. Juhasz, P. Kleimann, J. Linnros, and R. Juhasz, "Formation of threedimensional microstructures by electrochemical etching of silicon", *Appl. Phys. Lett.* 79, 1727 (2001).
- [6] E. H. Klaassen, K. Petersen, J. Logan, N. I. Maluf, J. Brown, C. Storment, W. Mcculley, and G. T. A. Kovacs, "Silicon fusion bonding and deep reactive ion etching: a new technology for microstructures," *Sens. Actuators A* 52 (1–3), pp. 132-139 (1996)
- [7] Z. Huang, N. Geyer, P. Werner, J. de Boor, and U. Gösele, "Metal-Assisted Chemical Etching of Silicon: A Review," *Adv. Mater.*, 23(2), pp. 285–308 (2011).
 C. Li, K. Fobelets, C. Liu, C. Xue, B. Cheng, and Q. Wang, "Ag-assisted lateral etching of Si nanowires and its application to nanowire transfer", *Appl. Phys. Lett.* 103, 183102 (2013).
- [8] K. Rajeshwar, "Fundamentals of Semiconductor Electrochemistry and Photoelectrochemistry", Encyclopedia of Electrochemistry, Chapter 1 Wiley-VCH Verlag GmbH & Co. KGaA (2007).
- [9] A. J. Bard, A. B. Bocarsly, F.-R. F. Fan, E. G. Walton, and M. S. Wrighton, "The Concept of Fermi Level Pinning at Semiconductor/Liquid Junctions. Consequences for Energy Conversion Efficiency and Selection of Useful Solution Redox Couples in Solar Devices", J. Am. Chem. Soc. 102(11), pp. 3671-3677 (1980).
- [10] B. Jaballah, B. Moumni, and B. Bessais, "Formation, rapid thermal oxidation and passivation of solar grade silicon nanowires for advanced photovoltaic applications", *Solar Energy* 86 (6), pp. 1955-1961 (2012)
- [11] G. Venturi, A. Castaldini, A. Schleusener, V. Sivakov and A. Cavallini, "Influence of surface pre-treatment on the electronic levels in silicon MaWCE nanowires", *Nanotechnology* 26, 195705 (6pp) (2015).
 G. Venturi, A. Castaldini, A. Schleusener, V. Sivakov and A. Cavallini, "Electronic levels in silicon MaWCE

and A. Cavallini, "Electronic levels in silicon MaWCE nanowires: evidence of a limited diffusion of Ag", *Nanotechnology* 26, 425702 (5pp) (2015).

- [12] W. McSweeney, O. Lotty, N.V.V. Mogili, C. Glynn, H. Geaney, D. Tanner, J.D. Holmes and C. O'Dwyer, "Doping controlled roughness and defined mesoporosity in chemically etched silicon nanowires with tunable conductivity", *J. Appl. Phys.* 114, 034309 (11pp) (2013).
- [13] K. Fobelets, C.B. Li, D. Coquillat, P. Arcade, and F. Teppe, "Fourier Transform Spectroscopy of metal-assisted electroless etched silicon nanowire arrays", *RSC Adv.*, 3, 4434-4439 (2013)
- [14] B. Xu and K. Fobelets, "Spin-on-doping for output power improvement of silicon nanowire array based thermoelectric power generators," *J. Appl. Phys.* 115 (21), p. 214306, (2014).
- [15] B. Xu, W. Khouri, and K. Fobelets, "Two-Sided Silicon Nanowire Array/Bulk Thermoelectric Power

Generator", *IEEE Electron Dev. Lett.* 35 (5), 596 – 598 (2014).

- [16] K. Fobelets, M. Meghani, and C. Li, "Influence of Minority Carrier Gas Donors on Low-Frequency Noise in Silicon Nanowires", *IEEE Trans. Nanotechnol.* 13 (6), pp. 1176-1180 (2014).
- [17] C. Li, E. Krali, K. Fobelets, B. Cheng, and Q. Wang, "Conductance modulation of Si nanowire arrays", *Appl. Phys. Lett.* 101, 222101 (2012).
- [18] M.J. Kirton & M.J. Uren, "Noise in solid-state microstructures: A new perspective on individual defects, interface states and low-frequency (1/*f*) noise", *Adv. Phys.* 38 (4), pp. 367-468 (2006).
 F. N. Hooge, "1/f noise sources", IEEE Trans. Electron Dev. 41(11), pp. 1926-1935 (1994).
 D. M. Fleetwood, "1/f Noise and Defects in Microelectronic Materials and Devices", IEEE Transactions on Nuclear Science 62(4), pp.1462-1486 (2015).
- [19] D. R. Frankl, "Electrical properties of semiconductor surfaces", International series of monographs on semiconductors", Vol. 7, Pergamon Press, London (1967)
- [20] F. N. Hooge, "1/f noise", Physica B+C 83 (1) pp 14-23 (1976).
- [21] M. J. Kirton, and M. J. Uren, "Noise in solid-state microstructures: a new perspective on individual defects, interface states and low-frequency (1/f) noise", Adv. Phys. 38 (4) pp. 367-468 (1989).

- [22] S. Krylyuk, A. V. Davydov, I. Levin, A. Motayed, and M. D. Vaudin, "Rapid thermal oxidation of silicon nanowires", *Appl. Phys. Lett.* 94, 063113 (2009).
- [23] L. Bertoluzzi, L. Badia-Bou, F. Fabregat-Santiago, S. Gimenez, and J. Bisquert, "Interpretation of Cyclic Voltammetry Measurements of Thin Semiconductor Films for Solar Fuel Applications", *J. Phys. Chem. Lett.* 4(8), pp. 1334-1339 (2013).
 E. Kuçur, W. Bücking, R. Giernoth, and T. Nann, "Determination of Defect States in Semiconductor Nanocrystals by Cyclic Voltammetry", *J. Phys. Chem. B*, 109 (43), pp 20355–20360 (2005).
- [24] A. Iqbal, Md. S. Hossain, and K. H. Bevan, "The role of relative rate constants in determining surface state phenomena at semiconductor-liquid interfaces", *Phys. Chem. Chem. Phys.* 18, pp 29466-24477 (2016).
- [25] S.M. Sze, "Physics of semiconductor devices", p.21, 2nd. Ed. J. Wiley and Sons Inc. (1981).
 J.W. Chen, and A.G. Milnes, "Energy levels in Silicon", Ann. Rev. Mater. Sci. 10, pp. 157-228 (1980)
- [26] E. Krali, C. Li, K. Fobelets, and Z.A.K. Durrani, "Seebeck coefficients in silicon nanowire arrays", B-30-0, 9th European Conference on Thermoelectrics, Thessaloniki, Greece B-30-0 (2011).
- [27] N. Sato, "Electrochemistry at Metal and Semiconductor Electrodes", p. 189 Elsevier B.V. (1998).