Low-cost frequency-agile filter bank-based multicarrier transceiver implementation

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Abstract

Future television white space (TVWS) transceivers require frequency agility and adherence to spectral masks. For the 320 MHz wide UHF range for TVWS in the UK, this paper discusses two variations of a design for wideband digital up- and down converters at are capable of sampling at radio frequency. The designs consist of a two stage digital conversion is presented, comprising of a polyphase filter that implicitly performs upsampling and decimation, as well as a filter bank-based multicarrier stage capable of resolving the 8MHz channels of the TVWS band. The up- and down-conversion of 40 such channels is shown to not significantly exceed the cost of converting a single channel. The required spectral mask and the reconstruction error of the overall system can be controlled by the filter design. We demonstrate that even the more costly of the two transceiver designs can be implemented on a Virtex-7 FPGA with sufficient word-length to satisfy the spectral masks.

1. Introduction

Through the switch-over from analogue to digital television (TV), benign wireless communications channels in the so-called TV white space (TVWS) spectrum have become locally available. This has triggered a number of applications such as rural broadband access [1,2], offering additionally infrastructure for smart grid [3] and potentially 5G services. The TVWS spectrum in the UK ranges from 470 to 790 MHz and comprises of 40 channels, each with 8 MHz bandwidth. Potential devices that utilised these channel for wireless TVWS transmission must be frequency agile in order to select and change channels depending on geographical location, and strictly adhere to spectral masks which are likely to be imposed by regulators for the protection of incumbent users [4].

With the availability of powerful analogue-to-digital (ADC) and digital-to-analogue conversion (DAC) devices capable of operating close to 3GHz with sufficient bit resolution [5–7], frequency agile and flexible software defined radio transceivers for future TWVS devices are becoming viable. The aim of this paper therefore is to design and implement capable of converting the entire 320 MHz TVWS range from and to RF, and to explore the design's computational complexity, spectral selectivity and latency.

Standard orthogonal frequency division multiplexing (OFDM) cannot meet the permitted interference levels outlined in Fig. 1, such that filter bank-based multicarrier (FBMC) modulation [12–14] are preferred here Interestingly, filter bank techniques pre-date OFDM [8–11] but are seeing a revival because to their superior spectral confinement and resulting advantages in terms of synchronisation when compared to OFDM [15–17].

Operating generally in the baseband, in FBMC transceivers a number of subchannels or multiple users are allocated to spectrally well-confined frequency bands. Popular FBMC architectures are based on discrete Fourier transform (DFT) modulated filter banks [8,15] and derivative version [18], but also include iterated halfband schemes such as in [11]. Many FBMC systems that are reported in the context of frequency agility and cognitive radio [19,20] are located in the baseband. In the context of software radio, several implementations of filter bank-based wideband receivers have recently been discussed [21–24]. High-speed implementations such as e.g. [23] are essentially performing just a DFT, while more flexible designs such as [21,22] that employ filter banks are not concerned with computational complexity or real-time implementation.

Initial work for the proposed two stage TVWS transceiver architecture has been discussed in [25,26], with a low-rate implementation in [27]. Expanding on the elaboration of the single design in [28], this paper compares this to a second design option — with different conversions in the two stages and hence different properties — and details additional implementation considerations. For the implementation on an FPGA, compared to [25] the number of subbands had to

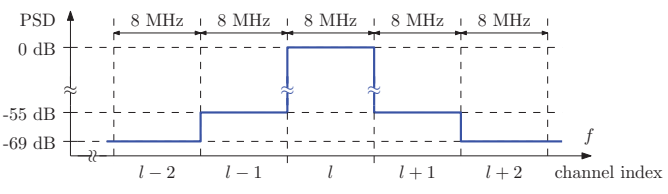

Figure 1. Spectral mask defining permissible power spectral density (PSD) levels in adjacent ($l \pm 1$) and next-adjacent ($l \pm 2$) TVWS channels [4].

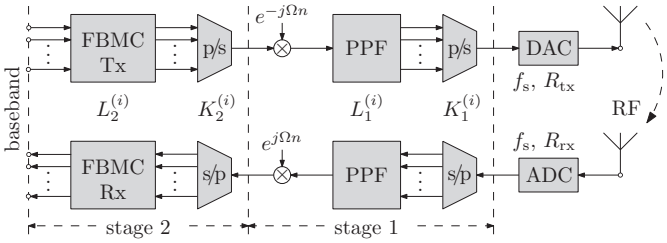

Figure 2. Proposed multi-stage TVWS filter bank with a polyphase filter (PPF) in stage 1 and an FBMC modulator in stage 2 implementing the transmitter (above) and the receiver (below).

be restricted to a power of two in [28], which here is also extended for the second design.

In this paper, Sec. 2 introduces the overall system, while Sec. 3 details some design aspects. Sec. 4 explores the multirate implementation and its impact on complexity and latency, with a demonstration of the designs in Sec. 5. The implementation on a Xilinx Virtex-7 device is reported in Sec. 6, with conclusions drawn in Sec. 7.

2. Proposed Transceiver Architecture

The proposed transceiver aims to concurrently demodulate all 40 channels covering the UK's TVWS spectrum from 470MHz to 790MHz. The upconverter in the transmitter has to fulfil the strict spectral mask shown in Fig. 1, which regulators are likely to impose [4]. While OFDM-based standards generally demonstrate too poor a frequency selection to satisfy this mask, FBMC systems can offer sufficient frequency selectivity.

An FBMC implementation is numerically most efficient with a single filter bank, as it requires fewer coefficients and therefore lower latency than an iterated filter bank with several stages and the overall response of interpolated FIR filters [29]. Interpolated FIR filter have bands of very high attenuation in their stopband range, and therefore a higher support and implementation cost compared to a direct, single filter design. However, targeting an FPGA implementation, there are restrictions on the sampling rate of such devices. Using a polyphase structure, data can be multiplexed and demultiplexed externally into a limited number of streams, with polyphase components running at a reduced rate on the FPGA. Hence, here a two-stage approach is pursued, leading to the proposed transceiver system as shown in Fig. 2.

The transmitter in the upper branch of Fig. 2 combines 40 TVWS baseband channels each of 8 MHz bandwidth in its stage 2 by means of an FBMC synthesis bank into a baseband signal that feeds into stage 1. A polyphase filter residing in stage 1, together with a position correcting term $e^{-j\Omega n}$, will translate the baseband signal to the UHF range of 470–790 MHz, running at a sampling rate f_s and having a word length R_tx. The real part of the analytic output is then passed to a DAC at radio frequency.

On the receiver side — the lower branch of Fig. 2 — the design is dual to the transmitter. The RF signal is sampled at f_s with word length R_rx as part of stage 1, where a complex-valued polyphase bandpass filter produces an analytic signal. The latter appropriately modulates a complex exponential of normalised angular frequency Ω such that the 40 channels of the TVWS spectrum sit at DC. In stage 2, an analysis filter bank implements the FBMC receiver and extracts the 40 TVWS baseband channels. Oversampled by a factor two, the FBMC outputs run at 16 MHz to ease subsequent tasks such as synchronisation, matched filtering, or further down-conversion within the individual 8 MHz channels.

3. Filter Bank Based Transceiver

This section provides details on the design of the proposed transceiver. Two different designs $i \in \{1, 2\}$ are proposed, performing a decimation/expansion by $K_1^{(i)}$ in stage 1, and operating $K_2^{(i)}$ channels with a decimation/expansion by $K_2^{(i)}/2$ in stage 2. The computational complexity of the proposed system will be analysed in Sec. 4., but a the power of two number of channels in the FBMC is favoured [28]. This differs from the non-power of two value of $K_2^{(i)}$ that had been used in our previous work [25], in order to enable the realisation on an FPGA as discussed later in Sec. 6..

3.1 Stage 1: Polyphase Filter

In stage 1 of the filter bank receiver, the UHF band from 470–790 MHz with a centre frequency $f_c = 630$MHz is extracted from the RF signal running at a rate $f_\mathrm{s} = 2.048$ GHz. The output of stage 1 is an analytic baseband signal with TVWS channels aligned from DC to 320MHz. This can be achieved by means of an analytic bandpass filter centred at f_c, with a suitable band limitation to permit decimation by a factor $K_1^{(i)}$. Fig. 3 sketches the required filter characteristic, whereby aliasing is permitted in the transition band, thus enabling a transition bandwidth $B_{\mathrm{T},1}^{(i)}$,

$$B_{\mathrm{T},1}^{(i)} = \frac{2.048\mathrm{GHz}}{K_1^{(i)}} - 320\mathrm{MHz} \quad . \tag{1}$$

To ensure that (1) is positive, the decimation ratio can take values $K_1^{(i)} \in [1, 4]$. Letting $K_1^{(2)} = 4$ leads to 512 MHz signals which can be realistically interfaced with an FPGA. Rather than filtering at RF followed by decimation, a polyphase approach demultiplexes the RF signal into $K_1^{(2)}$ polyphase components, each running at a reduced sampling rate, which are then passed into a polyphase network operating at frequency $f_\mathrm{s}/K_1^{(2)}$. The RF signal's polyphase decomposition was previously performed by hardware demultiplexers [25], but state-of-the-art ADCs such as [6] already offer an integrated demultiplexer, which serves the same purpose.

For $K_1^{(1)} < 4$ the resulting sampling rates of the polyphase components are too high to be directly interfaced with any state-of-the-art FPGA, unless oversampled polyphase structures are employed. To highlight the trade-off in selecting a lower decimation in stage 1, the case $K_1^{(1)} = 2$ will also be discussed. Fig. 3 outlines the resulting requirements for design of the polyphase filter $H_1^{(i)}(z)$.

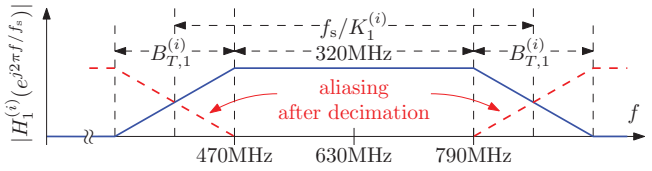

Figure 3. Stage 1 filter with passband width of 320MHz to capture UHF TVWS band; the transition bandwidth $B_{\mathrm{T},1}^{(i)}$ depends on the chosen decimation ratio $K_1^{(i)}$.

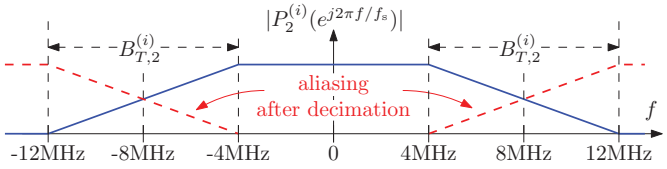

Figure 4. Stage 2 prototype filter with 8MHz passband width and decimation to 16 MHz sampling rate. All designs share the same absolute bandwidths but differ in their number of bands $K_2^{(i)}$.

In the receiver, the analytic output of stage 1 can be spectrally aligned with DC by correcting the lower frequency of 470MHz after aliasing through a modulation by $\Omega = 2\pi 470\mathrm{MHz}\cdot K_1^{(i)}/f_\mathrm{s}$. Alternatively, the incoming RF signal might first be demodulated to DC by a complex exponential, where a real-valued lowpass filter instead of the bandpass $H_1^{(i)}(e^{j\Omega})$ will extract the desired part of the spectrum. After lowpass filtering, a second modulation step could then re-align the decimated TVWS spectrum with DC. A misalignment in frequency would otherwise have to be addressed in stage 2 by applying appropriate frequency offsets to the FBMC that is to isolate the various 8 MHz TVWS channels.

The transmitter implementation is dual of the receiver, where state 1 applies a frequency shift by Ω followed by upsampling. Interpolation filtering can be performed with the bandpass $H_1^{(i)}(e^{j\Omega})$. Its widened transition bands do not matter due to the input signal to stage 1 fulfilling tight frequency mask characteristics. The real part of the analytic signal at the bandpass output can be fed to a DAC running at RF. The bandpass filter is again implemented as a polyphase structure, with a polyphase network sampled at $f_\mathrm{s}/K_1^{(i)}$. The latter operates on the FPGA, with the polyphase outputs interfaced to a hardware multiplexer [25], which is often already incorporated in state-of-the-art DACs [7].

3.2 Stage 2: Filter Bank-Based Multicarrier System

The two designs in stage 1 motivate different filter bank approaches in stage 2. Given the RF sampling rate of 2.048 GHz and a decimation ratio $K_1^{(i)}$ in stage 1, $K_2^{(i)} = \{128, 64\}$ 8 MHz bandwidth channels have to be extracted in stage 2, with the design combinations listed in Tab. 1. For each designs, only 40 of the $K_2^{(i)}$ channels are utilised. Due to the uniform ordering of these channels, a modulated filter bank represents efficient approach, whereby oversampling by a factor of 2 not only enables advanced baseband functionality but also relaxes constraints on the FBMC prototype $P_2^{(i)}(z)$ and therefore permits a cheaper prototype design as highlighted in Fig. 4 with a maximum possible transition bandwidth $B_{\mathrm{T},2}^{(i)}$. This design characteristic implies that the TVWS channel inputs to Tx stage 2 are perfectly bandlimited to 8 MHz.

The design is based on DFT modulated filter bank [30], where the analysis filter bank in the transmitter employs an inverse DFT and the synthesis bank in the receiver a DFT, thus aligning channels in ascending order from DC to 320 MHz.

4. Implementation Aspects

With a potential FPGA implementation in mind, Sec. 4.1 focuses on polyphase realisations, Sec. 4.2 on its computational complexity and Sec. 4.3 on word length considerations.

4.1 Polyphase Implementations

Stage 1 in the receiver necessitates a hardware demultiplexer to pass $K_1^{(i)}$ polyphase components of the digital RF signal into the FPGA for polyphase filtering. For stage 1 in the transmitter, the polyphase filter components are outputted from the FPGA, and need to be multiplexed in hardware to form the digital RF signal. As mentioned before, such hardware demultiplexers and multiplexers are often incorporated in state-of-the-art ADCs [6] and DACs [7].

The implementation in Sec. 3.1 employs a complex bandpass filter in polyphase realisation, combined with a frequency shift Ω. Based on a filter length $L_1^{(i)}$, a complexity of $C_1^{(i,a)} = 4L_1^{(i)}/K_1^{(i)} + 4$ real-valued multiply accumulates (MACs) arises. Alternatively, the stage 1 signal could be passed through real-valued lowpass filter. In combination with a modulation at both the input and output of stage 1, this leads to $C_1^{(i,b)} = 2L_1^{(i)}/(K_1^{(i)}) + 4K_1^{(i)} + 4$. The second implementation is only preferable if

$$C_1^{(i,a)} > C_1^{(i,b)} \quad \longleftrightarrow \quad L_1^{(i)} > 2(K_1^{(i)})^2 \quad , \qquad (2)$$

which is not satisfied for the selected values $K_1^{(i)} = \{2, 4\}$.

Different implementations are possible for stage 2, see e.g. [15]. Since circular buffers not useful for FPGA implementations, filter banks in polyphase implementation according to [31] are utilised, which require only a single tapped delay line, a set of multipliers, and the transform that is employed in the modulation of the filter bank. The latter, here uses a DFT implemented as a fast Fourier transform (FFT).

4.2 Computational Complexity and Latency

Recalling the complexity of the stage 1 filter considered in Sec. 4.1 and recognising that the polyphase filter bank requires $2L_2^{(i)} + 4K_2^{(i)} \log_2 K_2^{(i)}$ multiply accumulates (MACs) [31] at the lower rate of stage 2, the total complexity of a transmitter or receiver as depicted in Fig. 2 is

$$C^{(i)} = \left(L_1^{(i)} + \frac{L_2^{(i)}}{K_2^{(i)}} + 2\log_2 K_2^{(i)} + 1 \right) \frac{4f_\mathrm{s}}{K_1^{(i)}}, \qquad (3)$$

Table 1. Bandwidth reductions K_i for different receiver stages $i = 1, 2$ with associated increase in bit resolution ΔR_i, and other performance metrics. .

Design i		1	2
stage 1	$K_1^{(i)}$	2	4
	$\Delta R_1^{(i)}$ / bits	0.5	1
	$L_1^{(i)}$	12	44
stage 2	$K_2^{(i)}$	128	64
	$\Delta R_2^{(i)}$ / bits	3	2.5
	$L_2^{(i)}$	640	320
$C^{(i)}$ / GMAC/s		176.1	213.0
delay $\Delta^{(i)}$ / ns		83.7	40.5
reconstruction error / dB		62.9	63.1
adjacent channel leakage / dB		-65.3	-64.1
next-adj. channel leakage / dB		-71.4	-72.2

measured in real-valued MACs/s. In stage 2, the complexity of up- and downconversion of 40 channels by means of DFT-modulated filter bank is the same as for a single channel, plus the modulating transform i.e. a $K_2^{(i)}$-point DFT. The total complexity in (3) is likely to be dominated by the stage 1 filter with a length $L_1^{(i)}$, and is listed in Tab. 1 for the two different implementation options.

For linear phase prototype filters, the latency of either a filter bank transmitter or receiver is given by

$$\Delta^{(i)} = \frac{L_1^{(i)}}{2f_\mathrm{s}} + \frac{L_2^{(i)} K_1^{(i)}}{2f_\mathrm{s}} \quad . \tag{4}$$

This latency will be dominated by the lower rate stage 2 filter, with the overall transmitter or receiver delay for the two implementations indicated in Tab. 1.

4.3 Word Length Requirements

To satisfy the spectral mask in Fig. 1, the transmitter must possess a dynamic range of -69dB [4], requiring a minimum if 12 bits word length up to the DAC. The DAC characterised in [7] has a resolution of $R_\mathrm{tx} = 16$ bits. We therefore assume a 16 bit fixed point resolution for both the data and any coefficients in stage 1 and 2 filters in the transmitter, with a higher resolution for the accumulators and appropriate scaling prior to any rounding.

On the receiver side, the concatenation of filtering and decimation creates a gain in effective word-length, realising one extra bit of resolution for every oversampling by a factor of 4, because a bandwidth reduction also causes to a reduction in noise power without curtailing signal power. The gain in bits for the proposed filter bank transceiver is $\Delta R = \log_4 K = \frac{1}{2}\log_2 K$, where K is the reduction in bandwidth. In the process of reducing the bandwidth from 2.048 GHz to 8 MHz, $K = \frac{2.048\mathrm{GHz}}{8\mathrm{MHz}} = 256$ creates a gain in resolution by $\Delta R = 4$ bits.

The total gain of $\Delta R = 4$ bits is split across the two filter bank stages into $\Delta R = \Delta R_1^{(i)} + \Delta R_2^{(i)}$ as indicated in Tab. 1 for the two designs. Thus, the quantisation of filter coefficient in each stage has to be selected such that the greatest gain can be realised, demanding an extra resolution of at least 2 and 3 bits for stage 1 and 2 filters compared to their input signals,

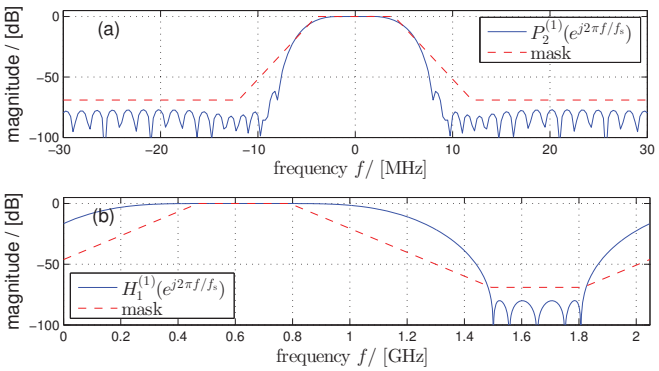

Figure 5. Magnitude responses of (a) stage 2 and (b) stage 1 prototype filters for design $i = 1$.

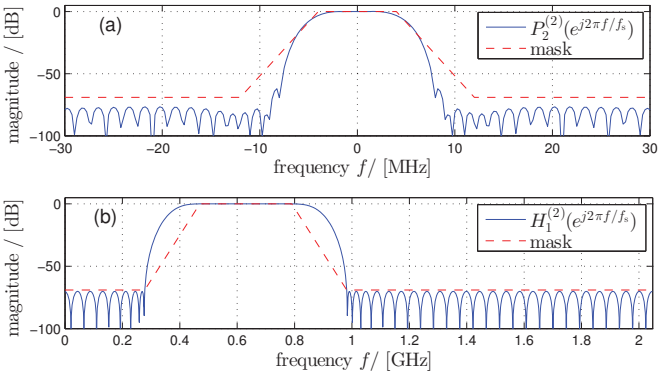

Figure 6. Magnitude responses of (a) stage 2 and (b) stage 1 prototype filters for design $i = 2$.

respectively. With the additional resolution of $\Delta R = 4$ bits, the targeted ADC [6] with $R_\mathrm{rx} = 12$ bits therefore provides a de-facto resolution of 16 bits for the down-converted 8 MHz TVWS channels if processing with appropriate word lengths is performed throughout the receiver chain.

5. Design, Simulations and Results

5.1 Filters and Power Spectral Densities

The prototype filters for stage 1 are constructed using a minimax design while stage 2 employs a root Nyquist approach [32,33], with magnitudes shown in Fig. 5 for design $i = 1$ and in Fig. 6 for design $= 2$. Responses can be seen to satisfy the stopband edges and adjacent channel attenuation of -69dB imposed by the spectral mask in Fig. 1 [4]. Satisfying this mask has been accomplished by adjusting the prototype filter lengths to the values listed in Tab. 1. Note that while e.g. design $i = 2$ using $K_1^{(2)} = 4$ and $K_2^{(2)} = 64$ has a simpler stage 1 as discussed in Sec. 3.1 and lower latency according to Tab. 1, its implementation cost is higher than design $i = 1$.

The PSDs of simulated Tx signals after stages 1 and 2 are shown in Fig. 7 for design $i = 1$ and in Fig. 8 for design $i = 2$, whereby each TVWS channel is loaded with a baseband signal of 5.33 MHz bandwidth [25]. The stage 2 transmitter outputs contain the 320 MHz TVWS baseband across 40 of the $K_2^{(1)} = 128$ channels for design $i = 1$ in Fig. 7(a) and of the $K_2^{(2)} = 64$ channels for design $i = 2$ in Fig. 8(a). Figs. 7(b) and 8(b) show

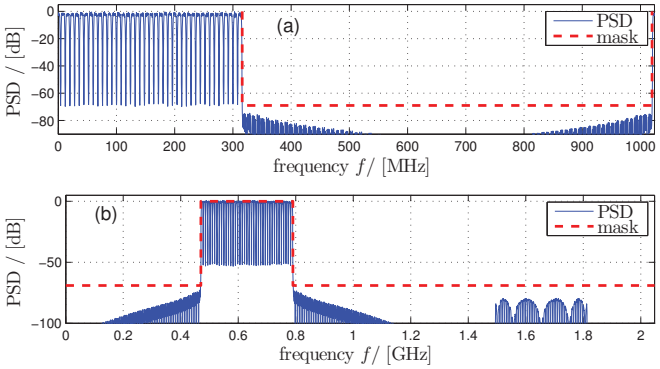

Figure 7. PSDs of transmit signal after (a) stage 2 and (b) stage 1. dashed lines for design $i = 1$.

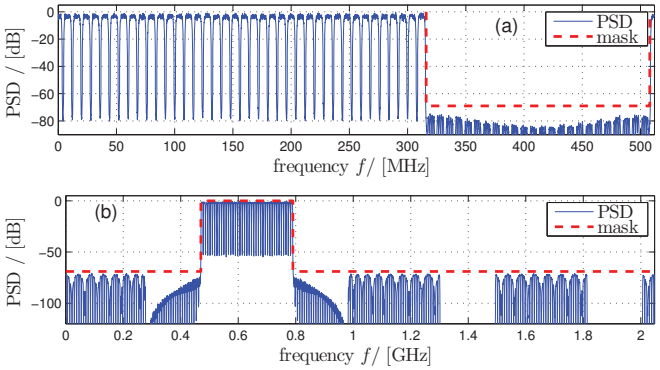

Figure 8. PSDs of transmit signal after (a) stage 2 and (b) stage 1. dashed lines for design $i = 2$.

the PSD of the stage 1 outputs of both designs, occupying the TVWS band 470–790 MHz with the spectral mask satisfied.

5.2 Reconstruction Error and Adjacent Band Leakage

Ideally the overall filter bank transceiver system should be transparent when transmitter and receiver are operated back-to-back as shown in Fig. 2. Testing to overall system, the reconstruction error between a transmitted and received 5.33 MHz channel, as well as the leakage level into adjacent channels, are provided in Tab. 1. The measured mean square error between input and output is equivalent to the reconstruction error of the filter bank, and therefore linked to the prototype filter design [32]. Due to the selection of the filter lengths $L_j^{(i)}$ for the jth stage in the ith design to satisfy with the overall desired spectral mask, all implementations meet the imposed requirement of at least -55dB for adjacent and -69dB for next-adjacent channels [4].

6. FPGA Realisation

Although fixed-point simulation results are reported below for both designs, the FPGA implementation as focused on realising to more costly design 2 on an FPGA.

Given the complexity analysis in Sec. 4.2, the design $i = 2$ with its more straightforward stage 1 but higher computational complexity has been implemented on a Virtex-7 XC7VX550T using the Xilinx ISE 14.6 software suite. For the transmitter,

Table 2. Transceiver hardware resource utilisation on a Virtex7-XC7VX550T FPGA device..

logic utilisation	number used	available	percentage used
LUTs	83566	346400	24%
FFs	63108	692800	9%
slices	26297	86600	30%
DSP48E1 units	1748	2880	60%

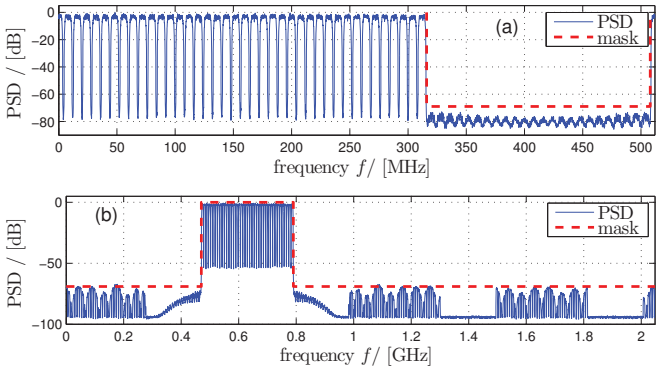

Figure 9. PSDs of transmit signal after (a) stage 2 and (b) stage 1. dashed lines for design $i = 2$.

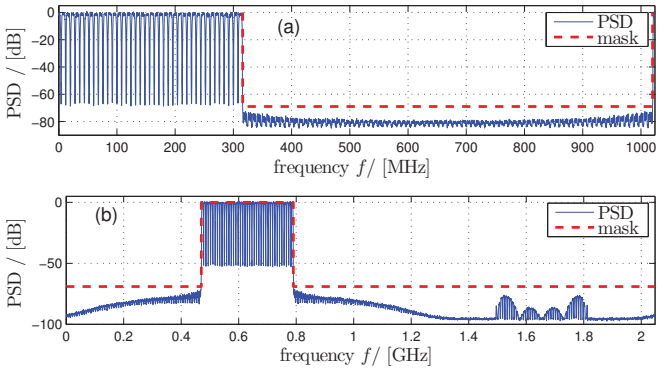

Figure 10. PSDs after (a) stage 2 and (b) stage 1 obtained by a bit-true and cycle accurate simulation with 16 bit word length for design $i = 1$.

the word-length is maintained at 16 bits throughout all stages to the output. In the receiver, a 12 bit signal is acquired from the ADC and thereafter allowed to grow by the appropriate gain in resolution up to 13 bits at the output of stage 1, and 16 bits at the output of stage 2, as summarised in Sec. 4.3. A complex exponential with 16 bit word length performs the frequency shifts in both Tx and Rx.

To safeguard that the timing requirements are met with stage 1 running at 512MHz, post-place and route timing analysis was performed. The analysis reported a minimum clocking period of 1.606ns, giving a maximum operating frequency of 622MHz. Table. 2 lists the hardware resources used by the design in terms of look up tables (LUTs), Flip-Flops (FFs), DSP48E1s, and slices [28].

Fig. 9 shows the PSDs obtained with a bit-true and cycle accurate simulation of design $i = 2$ in Simulink, with the system complying with the spectral mask. For design $i = 1$ the input rate of 1024 MHz is too high to be interfaced directly with state-of-the-art FPGAs, and more elaborate polyphase realisation would be required to implement this. Regardless, bit true simulation results (although not obtained in real time) are provided in Fig. 10, fulfilling the spectral mask.

7. Conclusion

This paper has discussed a frequency-agile two-stage filter bank transceiver design that can convert all 40 8 MHz wide channels in the TVWS band covering the frequency range from 470–790 MHz. The system satisfies regulatory requirements w.r.t. the spectral mask as well as hardware limitations on the sampling rate and the FPGA devices. Two different design have been demonstrated with different trade-offs between complexity, maximum sampling rate of polyphase components, and latency, and the ability to utilise extra word length afforded by oversampling. An FPGA implementation of the more complex design on a Virtex-7 device has been presented.

Acknowledgement

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