Practical Computation of di/dt for High-Speed Protection of DC Microgrids

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***Abstract*—DC microgrids have the potential to radically disrupt the distribution system market due to the benefits offered in easing the integration and control of distributed renewable energy resources and energy storage systems. However, the non-zero-crossing fault current profiles associated with short-circuited DC systems present a major challenge for protection. Isolation of faulted networks prior to the peak-current discharge of DC-side capacitors may address this challenge if rapid fault detection speeds (shorter than $2ms$) can be achieved. Accordingly, novel methods of utilising the rate-of-change-of-current (di/dt) have been proposed in the literature to realize new, high-speed distance protection strategies. This paper proposes two practical methods for optimizing the numerical computation of di/dt of fault current transients and evaluates the performance of each within a MATLAB/Simulink model of a DC microgrid with artificially injected measurement noise.**

Keywords—DC microgrids, Power system measurements, Digital signal processing, Power system protection.

I. Introduction

Within the last decade, significant research and development effort has been placed in integrating renewable energy resources such as photovoltaics and wind turbines into smartgrid and microgrid power distribution systems [1]. Given the naturally intermittent nature of these resources, integration of energy storage systems in conjunction with hierarchical energy management and flexible control strategies have enabled the challenge of balancing local energy generation and consumption to be resolved [2]. These modern distribution systems can enable a more environmentally-friendly source of power generation to be realised whilst ensuring a more secure regional power network [4].

Concurrently, there has been significant growth in converter interfaced loads consuming DC power within both the domestic and industrial sector, driven by the fundamental advancements in highly efficient and flexible power electronic conversion technologies [5]. Examples include DC supplied data-centres [6], electric vehicle charging stations, consumer electronics, and building and street LED lighting systems [7]. Accordingly, a radical shift to DC power distribution is now being considered for smartgrid and microgrid applications owing to the complimentary benefits offered in simplifying the control and integration of such subsystems, reducing the number of power electronic conversion stages, and improving the end-to-end efficiency of the overall distribution system [8]. Similar transformational shifts to DC power distribution are also being considered for aircraft and shipboard electrical power systems [9-14].

However, comprehensive power quality, protection and safety standards for large-scale DC microgrids have yet to be established. In particular, there still exists many challenges in designing a secure and resilient DC system that can withstand the substantial peak-current profiles associated with rail-to-rail or rail-to-ground short circuit faults. In addition, the dynamics of DC fault currents are significantly more transient than faults within conventional AC distribution systems, and so are more challenging to protect [15]. Furthermore, the non-zero-crossing fault current profiles associated with short-circuited DC systems present a major challenge for protection. Isolation prior to the peak-current discharge of DC-side capacitors may address this challenge if ultra-fast ($< 2ms$) [15] and reliable fault detection can be achieved. One such promising method that can meet these demanding fault detection requirements is threshold triggered rate-of-change-of-current (ROCOC), or di/dt-based trip-mechanisms [17]. Indeed, the accurate measurement of di/dt may be exploited in many novel high-speed overcurrent and distance protection strategies for DC microgrids [17]. However, computationally deriving di/dt using non-ideal and noisy current measurement signals is a practical challenge that needs to be addressed prior to implementing such protection functions.

Accordingly, this paper proposes two methods for optimising the numerical computation of di/dt of fault current transients and evaluates the quality of the derived ROCOC measurement for each using a simulated model of a DC microgrid with artificially injected measurement noise. The first method is an approach to derive the optimised selection of sampling frequency for a current measurement signal whilst minimising noise pickup. The second method is the application of a tuned finite impulse response (FIR) filter to condition the signal prior to discrete di/dt computation. Practical application of these signal conditioning methods are then discussed for di/dt-based fault detection algorithms for future high-speed DC protection devices.

II. Current Behavior of DC Short-circuit Fault

The peak current magnitude of a short-circuit fault within a DC microgrid, owing to the rapid discharge of DC-side filter capacitors, can cause significant damage to any component

through which fault current is carried. In particular, reverse diodes associated with constituent solid-state switch devices within power electronic (PE) converter interfaces, such as IGBTs and power MOSFETs, may be exposed to high currents that are significantly greater than their rated.

A. DC Short-circuit Fault Current

The equivalent circuit shown in Fig. 1 illustrates the contributing stages of a DC short-circuit fault. Irrespective of the current contribution from the AC side, the initial fault current behaviour can be divided into 2 stages [15]. Stage 1 is the natural response of the equivalent RLC circuit as the filter capacitor discharges, and Stage 2 is the circulation of fault current through the freewheeling diodes. The transition from Stage 1 to Stage 2 occurs when the capacitor voltage decreases to zero.

1) Stage 1. Capacitor Discharge:

Fletcher in [19] derives the RLC current and voltage response as

$$i_L(t) \approx \frac{v_{C_F}}{L\omega_d} e^{-\alpha t} sin(\omega_d t) \tag{1}$$

$$v_{C_F}(t) \approx \frac{v_{C_F}(0)}{\omega_d} e^{-\alpha t} \left[\omega_d cos(\omega_d t) + \alpha sin(\omega_d t)\right] \tag{2}$$

where α is the damping factor (or Neper frequency) defined as $\alpha = R/2L$, $\omega_d = \sqrt{(\omega_0^2 - \alpha^2)}$ is the damped resonant frequency, $\omega_0 = 1/\sqrt{(LC_F)}$ is the resonant radian frequency, $v_{C_F}(0)$ is the initial voltage across the capacitor C_F, L and R are the total inductance and resistance in the fault current loop. The rate of change of current is also derived as

$$\frac{di_L(t)}{dt} \approx \frac{v_{C_F}(0)}{L} e^{-\alpha t} \left[cos(\omega_d t) - \frac{\alpha}{\omega_d} sin(\omega_d t)\right] \tag{3}$$

The following features can be observed from the above equations:

- The capacitor voltage is proportional to i_L, v_{C_F}, and di_L/dt, qualifying the use of a scaled low-voltage system in short-circuit experiments.
- Higher fault resistance and lower cable inductance cause greater fault current attenuation.
- The natural frequency only depends on the filter capacitance and cable inductance.
- With the same natural frequency, a higher fault resistance causes a lower damping frequency.
- When the fault resistance is high enough, i.e. $\alpha > \omega_0$, the fault current will transition from underdamped to overdamped. Stage 2 only occurs in the case of underdamped conditions.

2) Stage 2. Diode Freewheeling:

As the filter capacitor voltage collapses to zero, the fault path loop will transition to flowing through the freewheeling diodes within the converter instead of the filter capacitor after the peak current point. However, the peak fault current during this stage is normally far greater than the rating of diodes resulting in permanent damage to the devices. Therefore, the protection needs to trip in advance of this stage. Fig. 2 shows the current and voltage response during these two stages.

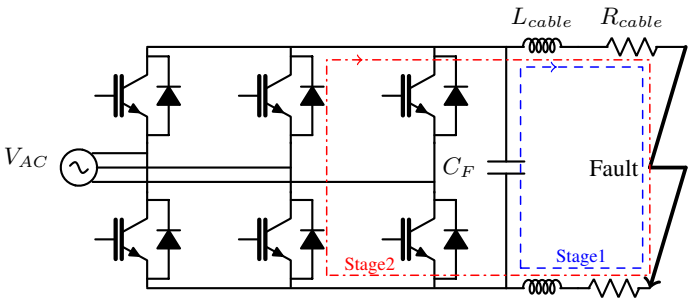

Fig. 1: The equivalent circuit of a converter with a pole-to-pole fault [16].

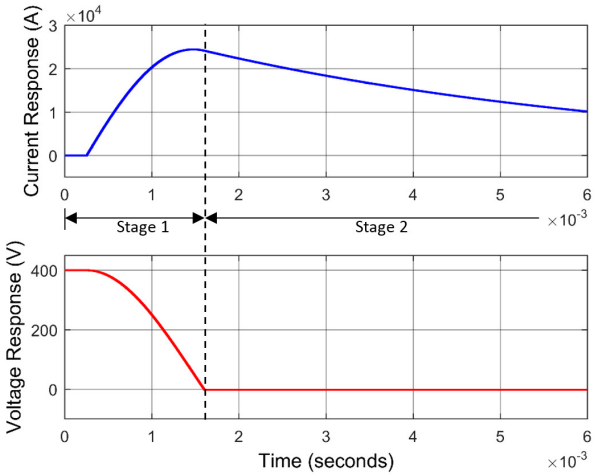

Fig. 2: Typical current and voltage characteristics of a DC short-circuit fault [15].

B. Derivation of DC Short-circuit Fault Transient (ROCOC)

A model of the system shown Fig. 1 was constructed in MATLAB/Simulink using a set of practical network parameters obtained from reference [refHigh-speed Differential], as described in Table I. The VSC regulates the DC-side voltage to $400V$, whilst $125A$ is continuously supplied to a representative load connected to the microgrid. A short-circuit fault is applied after 0.25 millisecond of simulation time at an equivalent distance of 35m from the filter capacitor. The resultant fault current waveform can be described using (1) and is plotted in Fig. 3. Fig. 3 also shows the fault current transient with white noise satisfying $X \sim \mathcal{N}(0, 20^2)$ augmented on to the measurement of this transient. As evident from this figure, the noise does not heavily distort the waveform.

Assuming the current transient waveform is sampled using an analogue to digital converter (ADC), a numerical derivation of di/dt can be obtained, where

$$\frac{di(t)}{dt} = \frac{i(t) - i(t - \Delta T)}{\Delta T} \tag{4}$$

However, this numerical method of determining di/dt may result in a severely noisy signal that masks the real di/dt. This is evident in Fig. 4 whereby di/dt of the fault current transient shown in Fig. 3 is derived for both waveforms (with and without noise) using equation (4) with an assumed ADC

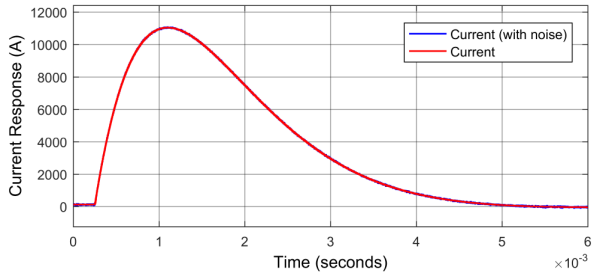

Fig. 3: Fault current response.

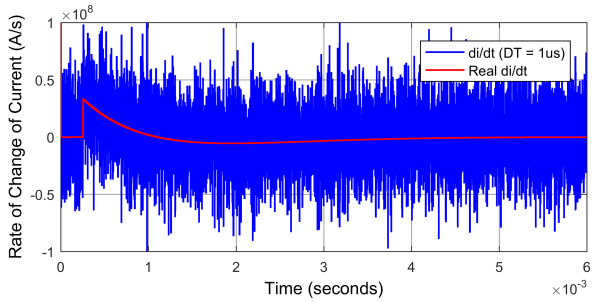

Fig. 4: A failure of di/dt computation with injected noise.

sampling frequency of 1MHz. Given that ΔT is $1\mu s$, the rate-of-change of the noisy current waveform amplifies the existence of noise, resulting in a failed computation of di/dt.

TABLE I: DC MICROGRID NETWORK PARAMETERS

$v_{C_F}(0)$	$i_L(0)$	R/m	L/m	C_F	$C_{F_{ESR}}$	d_f
$400V$	$125A$	$0.64m\Omega$	$0.34\mu H$	$56mF$	$2m\Omega$	$35m$

III. METHOD OF OBTAINING RATE OF CHANGE OF CURRENT

In order to resolve the challenge associated with obtaining an accurate di/dt measurement using noisy current data, this section presents two approaches and compares them by analyzing their advantages and drawbacks.

A. Optimized Sampling Frequency (OSF) Selection

The first approach aims to constrain the effect of noise by enlarging the time step of numerical computation. If the computational time step is defined as M times the sampling period ΔT, the computation equation can be represented as

$$\frac{di_n}{dt} = \frac{i[n] - i[n-M]}{M \times \Delta T} \tag{5}$$

To test the sensitivity of this approach $M\Delta T$ was selected to be $25\mu s$, $100\mu s$ and $400\mu s$ respectively. As shown in Fig. 5, the di/dt computation result suppresses the effect of noise as a function of the increasing time steps. However, it is evident that larger time steps decrease the accuracy of the initial di/dt computation both in terms of attenuating the peak value and

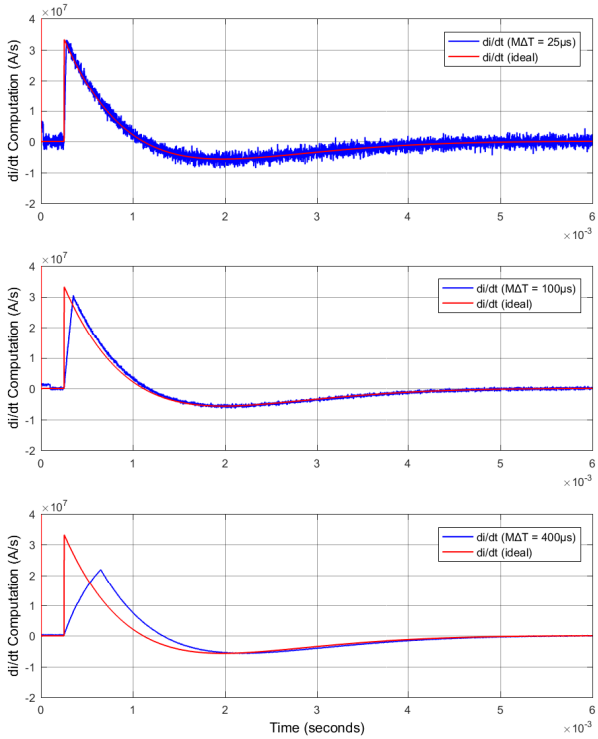

Fig. 5: di/dt computation results with different sampling frequencies.

delaying the peak time of di/dt computation, in comparison to the ideal case. This introduces a discussion about optimizing time step setting.

Assuming a white noise distribution of $X[n] \sim \mathcal{N}(0, \sigma^2)$, the time step may be selected so that the worst error of di/dt computation of two successive samples is constrained within $\pm\varepsilon$ with a probability of 98%. Since the two successive samples are independent, the difference satisfies $x[n] - x[n-1] \sim \mathcal{N}(0, 2\sigma^2)$. Looking up the standard Normal Table,

$$P(-2.33(\sqrt{2}\sigma) < x[n] - x[n-1] < 2.33(\sqrt{2}\sigma)) = 0.98 \tag{6}$$

Assuming the limits are set to

$$-\varepsilon < \frac{x[n] - x[n-1]}{M \times \Delta T} < \varepsilon \tag{7}$$

The 98% confidence error function of the di/dt computation to the time step can be derived, where

$$\varepsilon = \frac{2.3262\sqrt{2}\sigma}{M \times \Delta T} \tag{8}$$

For example, when setting $M\Delta T = 25\mu s$, the limitation of 98% di/dt computations on the pure white noise signal is calculated as $\pm\varepsilon = \pm 2.636 \times 10^6$ as shown in Fig. 6. The result verifies the assumption that 5858 out of 6000 samples (97.63%) are within the designed limits. In this scenario, the real peak of di/dt can be calculated to be $3.36 \times 10^7 A/s$ using (3). Assuming ε is within $\pm 10\%$ of ideal di/dt signal, i.e. 3.36×10^6, in terms of (8), the $M\Delta T = 25\mu s$ term should be set greater than $19.6\mu s$.

This method enables careful selection of the time step to realize an effective di/dt computation of a noisy current

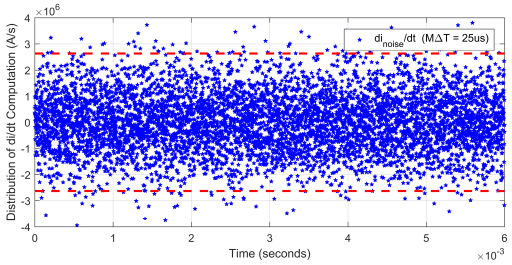

Fig. 6: di/dt computation errors when $M\Delta t = 25\mu s$.

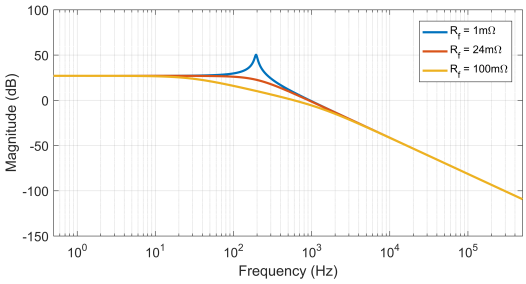

Fig. 7: Spectrum of short-circuit faults with different fault resistances.

measurement signal. Furthermore, this method may be easily embedded into hardware such as microcontrollers and FPGAs. The primary drawback associated with this method is that the peak of di/dt may be attenuated and the delay to peak may decrease the sensitivity of any protection system that utilizes di/dt for fault detection. Accordingly, this method may be better suited for processing low-noise current signal.

B. Finite Impulse Response (FIR) Filter

The second method to accommodate for a fault current transient measurement with added noise applies the use of a FIR filter prior to ROCOC computation. This method is being considered as a DC short circuit fault has a limited bandwidth due to network characteristics, and so high frequency components of noise may be filtered out. Applying a Fourier transform on (1), the frequency distribution of a fault current signal is derived as

$$I(\omega) \approx \frac{v_{c_F}(0)}{L} \cdot \frac{1}{\omega_d^2 + (\alpha + j\omega)^2} \tag{9}$$

Applying the cable inductance and filter capacitance parameters in Table I, the spectrum diagram of fault current can be illustrated, as shown in Fig. 7. Whether the fault causes an overdamped or underdamped transient, the main frequency content is within a low band. As the frequency exceeds $10kHz$, the profiles are overlapped indicating that the intensity is independent to the fault resistance. The cut-off frequency should designed such that

$$f_c \gg f_0 = \frac{1}{2\pi\sqrt{LC_F}} \tag{10}$$

While designing a low-pass filter the cut-off frequency, in accordance with (10), should be located at the overlapping

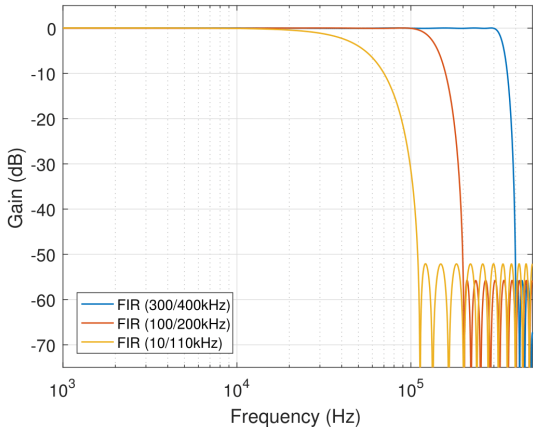

Fig. 8: Frequency responses of FIR low-pass filters.

segment so that the original fault current signal is not distorted due to the application of the filter. In this case, the filter parameters in Table II are used. The impulse response of these FIR filters is illustrated in Fig. 8.

Fig. 9 shows the results of applying these FIR filters, verifying the effectiveness of computing di/dt.The result shows the method is effective, however the following aspects need to be taken into consideration when designing such filters:

TABLE II: PARAMETERS OF FILTER DESIGN

Type	$f_{sampling}$	f_{pass}	f_{stop}	N_{order}
FIR	$1MHz$	$300kHz$	$400kHz$	24
FIR	$1MHz$	$100kHz$	$200kHz$	24
FIR	$1MHz$	$10kHz$	$110kHz$	24

- The selected cut-off frequency is recommended to be approximately two orders of magnitude greater than the natural frequency.
- The buffer band of the filter must not be too narrow, normally wider than 5% of the sampling frequency. This is because narrow buffer bands require more FIR numerators, resulting in longer delay to output signal.

C. Evaluation

According to Fig. 5 and Fig. 9, both approaches are capable of effectively depressing the errors in di/dt computation. The first method optimises the computing step time in terms of the variance of the noise signal so that the di/dt computation error can be limited within a specific range. The second method applies a low-pass FIR filter with a designed cut-off frequency to remove high frequency noise content from the current signal to improve the quality of the di/dt computation. The first method is simpler in design and can quantify the error level, but excessive requirements may attenuate the peak di/dt signal and decrease the accuracy of when the maximum ROCOC occurs. Accordingly, it is more suitable for coping with low-power noise. The second method employs an FIR filter that cannot quantify the error level, but does not decrease or severely delay the di/dt peak. This method is therefore

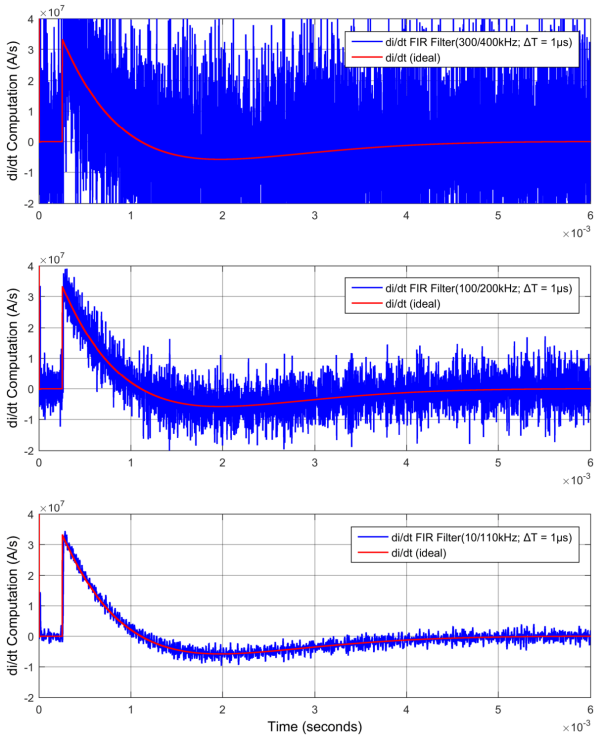

Fig. 9: Result of di/dt computations with low-pass FIR filters.

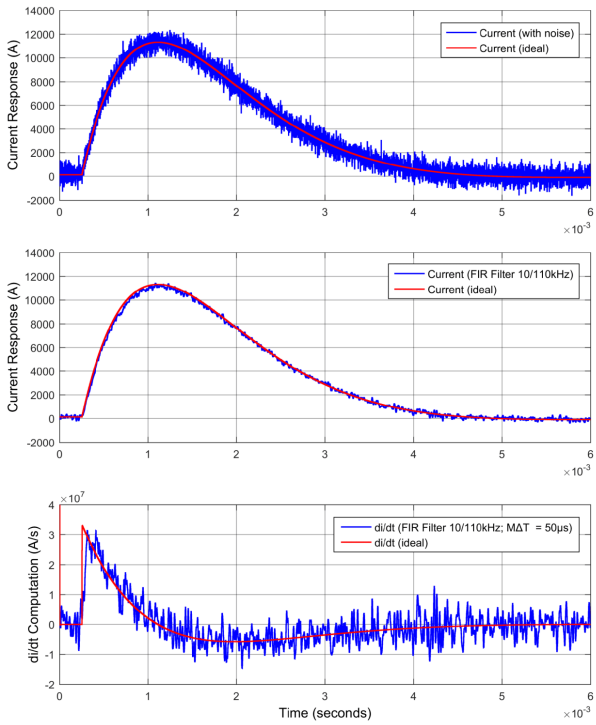

Fig. 10: di/dt computation for lower SNR signal with combination of the 2 methods. (a) Original current signal. (b) Current signal after FIR filter. (c) di/dt computation with filter and longer time step.

feasible for processing current transient signals with high-power noise. Taking the advantages of both methods, better performance can be obtained by combining them together. In practical applications, since the signal-noise-ratio (SNR) may be as low as that shown in Fig. 10 (a) whose $\sigma \sim 500$, neither of the methods may be effective. In this case, a low-pass filter may be applied first to constrain the high-frequency noise, as shown in Fig. 10 (b). Then, optimal selection of the computational time step may be applied. Fig. 10 (c) demonstrates the resulting di/dt waveform when applying a combination of these methods. Although the peak time is delayed by $50\mu s$ in comparison to the ideal case, the peak point is similar to that of the ideal case. This result is not realizable by using either method individually.

Regardless of the results obtained using the OSF method, the filter method, or the combination of both, the di/dt computation may be suitable to recognize the peak point of di/dt. However, none of these methods result in a di/dt signal produced from a current measurement that contains noise that is ideal in nature. Accordingly, DC protection relays that utilize di/dt should be designed to make tripping decisions based on several successive samples rather than one single sample to allow for suppression of noise and error samples.

IV. Discussion on the Impact on Fault Detection Speeds

A. High-speed Overcurrent Protection

This section will compare the fault detection speeds using current threshold-based overcurrent protection (CBOCP) and instantaneous di/dt-based overcurrent protection (DBOCP). Employing the same network parameters used in the previous case study, the fault current response and ideal di/dt response of different fault resistances are plotted as Fig. 11.

Given that the cable resistance is $24m\Omega$, Fig. 11 shows the short circuit responses of $24m\Omega, 124m\Omega, 224m\Omega$. Fig. 11 (a) shows that the $24m\Omega$ fault peak current magnitude is $11320A$ and occurs at $861\mu s$ after fault application; the $124m\Omega$ peak fault current magnitude is $3138A$ and occurs at $423\mu s$ after fault application; and the $224m\Omega$ fault peak current magnitude is $1842A$ and occurs at $300\mu s$ after fault application. In 11 (b), the peak point of di/dt appears at the initial moment of fault application and has a very close magnitude irrespective of fault resistance. This relationship has been proven by Fletcher in [19]. The CBOCP method is delayed while detecting faults, and it has the risk of missing a high resistance fault if the threshold is set too high. On the other hand, the DBOCP method enables the fault to be detected at initial moment that the fault occurs whilst avoiding the risk of missing a high-resistance fault. However, the period that faults are seen is shorter than the CBOCP method which requires reliable current measurement devices with sufficiently high sampling rates to avoid missing the high di/dt period. Table III compares the fault detection times with different threshold settings from simulation results. From these results, it is evident that the CBOCP method can detect faults within tens of microsecond, and misses the high resistance fault with high threshold setting. Although the release time of the CBOCP method is sufficiently long such that it decreases the risk of missing the fault in the relay, the slower detection creates the potential to trip at high current levels, which raises the probability of damaging internal converter solid-state switch

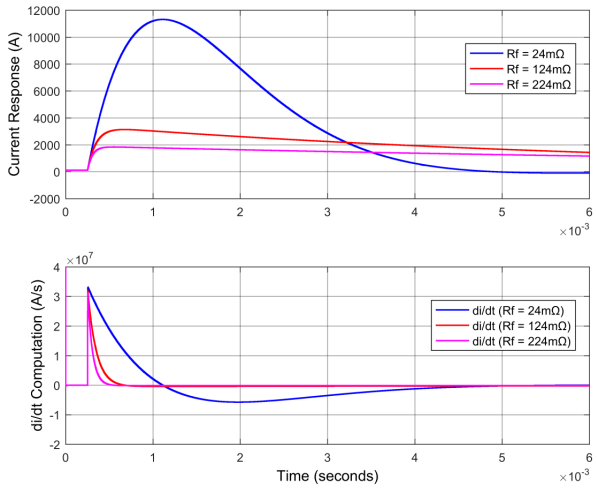

Fig. 11: Fault responses. (a) Current profiles. (b) di/dt profiles.

devices. Conversely, DBOCP is capable of detecting the fault rapidly and consistently ($1ms$). In addition, the number of samples before release is still enough to achieve reliable fault detection with high-fidelity measurement.

However, this method has some limitations in distinguishing between a sudden load change and a fault condition. Considering a pure resistive load change, the value of di/dt at the moment of a load change or a fault is [19]:

$$\frac{di_L(0^+)}{dt} \approx \frac{v_{C_F}(0^-) - i(0^-)R(0^+)}{L(0^+)} \tag{11}$$

where $R(0^+)$ represents the total post-fault series resistance in the current path. According to (11), for a short circuit fault, the term iR is negligible, and accordingly any faults inside the protection zone can be detected rapidly from the moment of application. However, for both sudden load changes and high impedance faults, the term $i(0)R(0)$ may not be dismissible. For example, consider a capacitive load such as a dual-active-bridge converter. The connection of the capacitor at the load side of the converter could temporarily collapse the network voltage. The current profile in this case is initially very similar to that of a fault complicating the distinction between normal and fault transient events. It may be possible to fine tune the di/dt threshold to distinguish between the majority of cases but soft start functions associated with the capacitive converter loads may also be required to prevent fault-like load transients on the network.

TABLE III: COMPARISON OF FAULT DETECTION TIME

Method	Threshold Setting	Resistance of Fault ($m\Omega$)	Detection Time (μs)	Release Time (μs)
CBOCP	$500A$	24	12	3860
		124	13	12750
		224	14	15750
	$2000A$	24	61	3030
		124	89	3553
		224	missed	missed
DBOCP	$1 \times 10^7 A/s$	24	1	465
		124	1	112
		224	1	65
	$2 \times 10^7 A/s$	24	1	227
		124	1	49
		224	1	27

B. High-speed Distance Protection

Fletcher [17] proposed a patent for DC distance protection based on initial di/dt computation. Substituting $t = 0$ into (3), the relationship between di/dt and the total cable inductance in the fault path can be derived as:

$$L \approx \frac{v_{C_F}(0)}{di_L(0)/dt} \tag{12}$$

Since the cable distance is proportional to the distance from the fault to the filter capacitor, this equation can be used to estimate the fault location. For example, in this case study, from Fig. 11 (b), the $di_L(0)/dt = 3.32 \times 10^7 A/s$. Accordingly, the cable inductance is calculated as $12\mu H$, which is very close to the actual value of $11.9\mu H$. However, one limitation of this method is that the type of fault resistance cannot be estimated. Meghwani [18] has recently improved the method in order to compute the total fault resistance with the use of a 2nd order derivative of fault current. In this manner, taking the derivative of (3) gives,

$$\begin{aligned}\frac{d^2 i_L}{dt^2} \approx & -\frac{v_{C_F}(0)}{L} 2\alpha e^{-\alpha t} cos(\omega_d t) \\ & + \frac{v_{C_F}(0)}{L}\left(\omega_d + \frac{\alpha^2}{\omega_d}\right) e^{-\alpha t} sin(\omega_d t)\end{aligned} \tag{13}$$

Substituting $t = 0$,

$$\frac{d^2 i_L}{dt^2} \approx -\frac{v_{C_F}(0)R}{L^2} \tag{14}$$

$$R \approx -\frac{d^2 i_L(0)/dt^2}{v_{C_F}(0)} \cdot L^2 \tag{15}$$

According to (15), the fault resistance can be obtained at one sample after the peak of di/dt, as shown in Fig. 12 (b) and (c). For example, for the lowest resistance case, the calculated fault resistances using (15) are $24.71m\Omega$ and $24.62m\Omega$, both of which are quite close to the actual $24m\Omega$. However, there exists significant error while calculating the higher fault resistances. As shown in Table IV, the estimation of higher values of R_f is accurate when there is no prefault current. However, when prefault load current exists, the estimations of fault resistance contain significant error. As such, in practice, this method can only be used to accurately estimate the resistance of short circuit faults and identify the nature of high resistance faults. Additionally, it will be challenging for the measurement instrumentation to realise the higher sampling rate necessary accurately capture the fault current d^2i/dt^2. Further research on the estimation of R_f is required for a complete assessment of the effectiveness of this approach in practical DC microgrid protection applications.

TABLE IV: R_f ESTIMATION USING d^2i/dt^2

Actual R_f	d^2i/dt^2 (no prefault load) ($\times 10^{11} A^2/s^2$)	Estimated R_f ($m\Omega$)	d^2i/dt^2 (prefault load) ($\times 10^{11} A^2/s^2$)	Estimated R_f ($m\Omega$)
$24m\Omega$	-0.6865	24.714	-0.6840	24.624
$124m\Omega$	-3.4070	122.652	-4.7740	171.864
$224m\Omega$	-5.9930	215.748	-8.5530	307.908

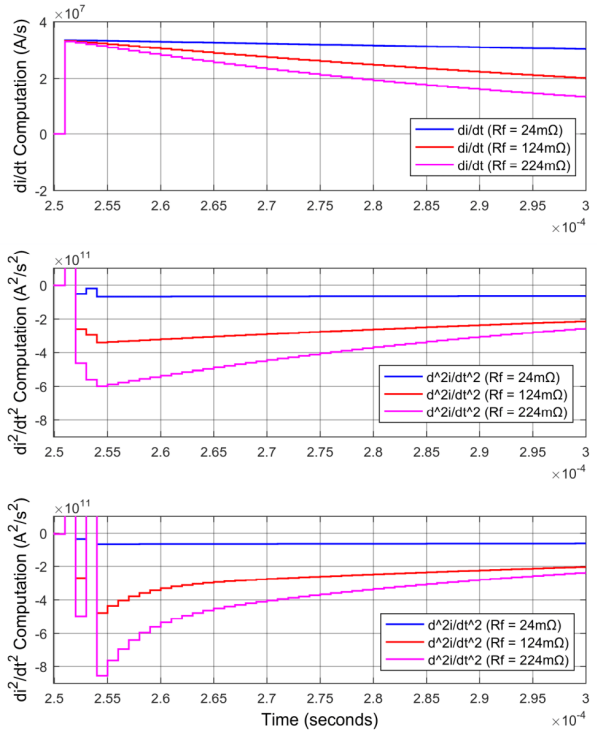

Fig. 12: Fault responses under various prefault loading conditions. (a) di/dt profiles. (b) d^2i/dt^2 without prefault load. (c) d^2i/dt^2 with prefault load.

V. Conclusion

This paper proposed two methods for optimizing di/dt computation of short circuit faults within DC networks by optimizing the sampling frequency and designing an FIR filter in terms of the noise level and the fault current frequency respectively. Both approaches were verified through simulation case studies. The accurate computation of initial di/dt has the potential to make a significant contribution to the network protection of DC microgrids, including through novel high-speed overcurrent and high-speed distance protection schemes. This paper has evaluated both applications with results which show that di/dt based overcurrent protection (DBOCP) is technically faster than the traditional current threshold based overcurrent protection (CBOCP) and maintains sensitivity to high-resistance faults. The di/dt based distance protection method has also be shown to accurately estimate the electrical distance to the fault, and distinguish between short and resistance fault conditions.

Planned further research by the authors in this area includes undertaking real time experiments with a scaled voltage test rig in order to evaluate the practical limits of the performance of the OSF method, the FIR filter method and their combination for the computation of di/dt. This in turn will facilitate the evaluation of the speed and fault distance estimation aspects of di/dt based overcurrent methods.

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