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Research Article

Design of Pixellated CMOS Photon Detector for Secondary Electron Detection in the Scanning Electron Microscope

Joon Huang Chuah[1,2] and David Holburn[1]

[1] *Electrical Engineering Division, Department of Engineering, University of Cambridge, 9 JJ Thomson Avenue, Cambridge CB3 0FA, UK*
[2] *Department of Electrical Engineering, Faculty of Engineering, University of Malaya, 50603 Kuala Lumpur, Malaysia*

Correspondence should be addressed to Joon Huang Chuah, jhc53@cam.ac.uk

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This paper presents a novel method of detecting secondary electrons generated in the scanning electron microscope (SEM). The method suggests that the photomultiplier tube (PMT), traditionally used in the Everhart-Thornley (ET) detector, is to be replaced with a configurable multipixel solid-state photon detector offering the advantages of smaller dimension, lower supply voltage and power requirements, and potentially cheaper product cost. The design of the proposed detector has been implemented using a standard 0.35 μm CMOS technology with optical enhancement. This microchip comprises main circuit constituents of an array of photodiodes connecting to respective noise-optimised transimpedance amplifiers (TIAs), a selector-combiner (SC) circuit, and a postamplifier (PA). The design possesses the capability of detecting photons with low input optical power in the range of 1 nW with 100 μm $\times$ 100 μm sized photodiodes and achieves a total amplification of 180 dBΩ at the output.

1. Introduction

The Everhart-Thornley (ET) detector has been widely used as the secondary electron detector for the scanning electron microscope (SEM) for the past half a century [1]. The detector consists mainly of collector, scintillator, light pipe, photomultiplier tube (PMT), and preamplifier. Being a vital component of the ET detector, PMT is responsible for sensing the arrival of photons, converting them to electrons, and multiplying the number of electrons which essentially produce an amplified output current. Its dominance of use is due chiefly to its ability to provide an excellent sensitivity solution.

The rapid advancement of semiconductor technologies in recent years has manifested in many applications in various fields. Solid-state method essentially allows the integration of large operating components into a small microchip. Complementary metal-oxide-semiconductor (CMOS) processes, which are silicon based, have become the most popular among all technologies thanks to its ability to provide low-cost solutions and highly integrated design. Certain CMOS processes do attract special attention owing to their ability to include both optical devices and electrical circuits into a monolithic microchip. This form of integration is very popular in the optical communications world, both wired and wireless, in the past decade [2–5]. Apart from communications, it also finds a number of implementations in optical storage systems [6]. In the optical sensory sectors, numerous applications such as camera sensory devices, optical microsensors particularly used in medical monitoring, and remote controls have benefited greatly from the capability of the latest CMOS processes to fabricate optoelectronic integrated circuit (OEIC) [7]. With these successful implementations, it is hoped that some aspects of the existing ET detector could be enhanced by capitalising on the available semiconductor technologies.

The invention of single-photon accuracy detectors using avalanche photodiode (APD) operating in Geiger mode, commonly known as single-photon avalanche diode (SPAD), has drawn a lot of interest recently [8–10]. These photon detectors, usually constructed in arrays, produce very encouraging results and are suitable for use in many low

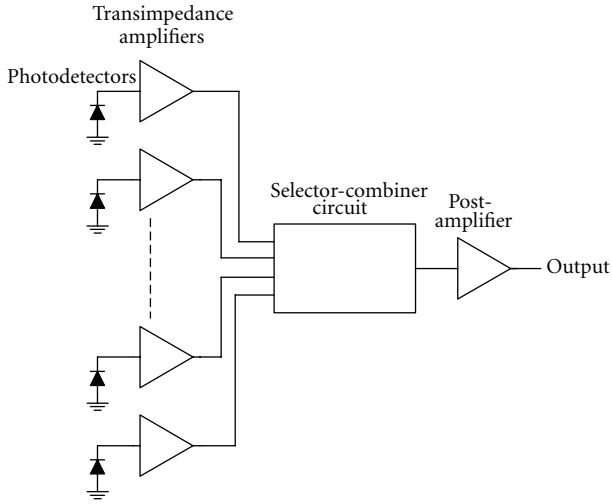

Figure 1: Block diagram of multipixel photon detector.

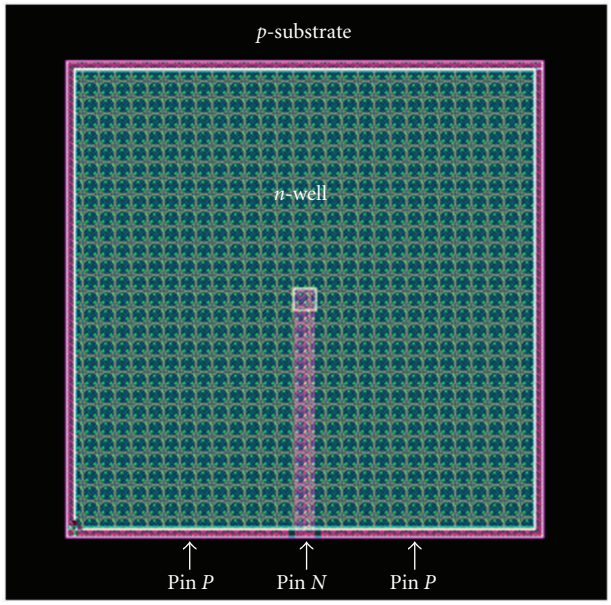

Figure 2: Construction of n-well p-substrate photodiode.

luminescence applications [11–15]. However, the downside is that they could be easily saturated even by a small DC signal. To remedy this problem, an external attenuator is usually used to reduce the number of photons approaching the detectors, and this solution is not an integrated one [16]. In certain designs, in order to increase the dynamic range while maintaining the die size remains, a detector with higher number of pixels is necessary. This would reduce the fill factor, thus resulting in fewer photons being detected. Apart from single-photon avalanche detectors, charge-coupled device (CCD) is not suitable for our application due to the requirement of instantaneous photo detection at the video bandwidth.

In this research, we attempt to produce a pixellated silicon-based detector for the use of secondary electron

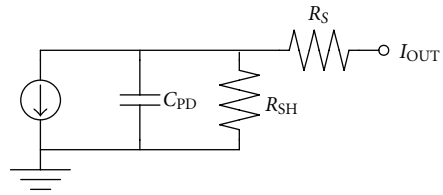

Figure 3: Equivalent circuit of photodiode.

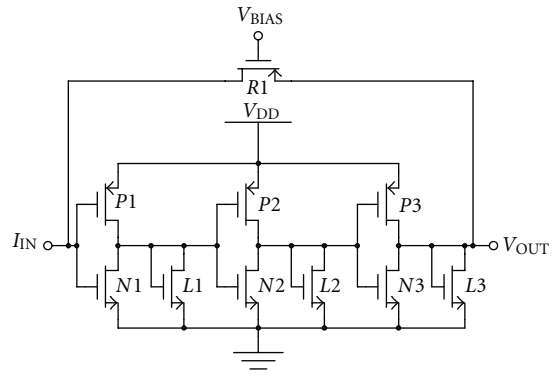

Figure 4: Circuit diagram of transimpedance amplifier.

detection in the SEM. It essentially substitutes some constituent components of the ET detectors with a monolithic solution. Additionally, this design is configurable, thus providing flexibility to control the circuit for improved performance of the detector. The proposed microchip offers the potential advantages of better compactness, higher cost effectiveness, higher bandwidth, and lower voltage and power requirements and better integration. Furthermore, implementation of circuits in a CMOS technology also results in a future opportunity of integrating mixed-signal and digital subblocks, for example, analogue-to-digital converter (ADC) and digital signal processor (DSP) for complex manipulation of information. The design of the photon detector has been realised in a 0.35 μm CMOS technology offered by Austriamicrosystems.

2. Multipixel CMOS Photon Detectors Architecture and Circuit Design

The top-level design of the integrated circuit consists of an array of photodiodes, an array of low-noise transimpedance amplifier (TIA), a selector-combiner circuit (SC), and a post-amplifier (PA), as shown in Figure 1. In this version of design, nine photodiodes and nine TIAs are constructed mainly for experimental measurement and evaluation purposes. This optoelectronic microchip aims to detect optical signal of 1 nW or lower. The photons detected by the photodiode are converted to a current signal with a photosensitivity figure of 0.33 A/W at 850 nm. The TIA is then used to change the current signal to voltage signal with a gain of 120 dBΩ. Voltage signals from TIAs of interest are selected to be added by the SC. The summed signal is subsequently amplified by the PA to a range that could be easily detected and processed.

The pixellated feature of the detector is an important part of the entire design as it provides a few distinct benefits. Firstly, it improves the bandwidth of the detector as the capacitance of an individual photodiode seen by a TIA is much smaller compared to that of a larger photodiode. Secondly, it allows the selection and combination of signals detected by certain photodiodes. This helps in producing a better average signal-to-noise ratio (SNR) as photons travelling from the light pipe to the detector are very often not spatially distributed.

2.1. Photodetector. Photodetector is the first component of the entire detector circuitry to receive the incoming signal. It essentially converts the optical signal to the electrical signal for subsequent processing. There are three options that photodiodes can be constructed in this 0.35 μm fabrication process, namely, n-diff and p-substrate diode (ND), p-diff and n-well diode (PD), and n-well and p-substrate diode (NWD). In our design, the NWD type of photodiode has been created because it provides the best responsivity among all the possible photodiode constructions. This photodiode is able to achieve a responsivity value of 0.33 A/W for the detection of photons with a wavelength of 850 nm. This process technology also comes with an additional inorganic antireflective coating (ARC) layer that greatly improves the transmission of photons towards the photodiode. Figure 2 illustrates the layout of the photodiode. It is surrounded by P pin while N pin is located at bottom middle. Its equivalent circuit is shown in Figure 3. The photodiode occupies a dimension of 100 μm $\times$ 100 μm, and, with this size, it produces a photodiode capacitance, C_{PD}, of 0.8 pF and a dark current of 4.5 fA at room temperature. By using (1) [17], where T is temperature, A_j is the junction area, and J_s is the saturation current density, the shunt resistance, R_{SH}, is found to be 925 GΩ. By measuring the metal length and counting the number of contacts used in the photodiode layout, the series resistance R_S is estimated to be 7.5 Ω:

$$R_{SH} = \left.\frac{\partial V}{\partial I}\right|_{V=0} = \frac{kT}{qJ_sA_j}. \quad (1)$$

2.2. Transimpedance Amplifier. TIA is used to convert current signal to voltage signal with a large transimpedance gain. As shown in Figure 4, the TIA incorporated in this detector has three stages of amplification, each of which consists of a push-pull CMOS inverting amplifier and an NMOS diode-connected load. A feedback resistor, $R1$, implemented using a PMOS transistor, is used to control both the gain and the bandwidth of the TIA. A PMOS transistor is chosen mainly because it generates less noise compared to an NMOS transistor. Equation (2) is applied to determine the resistance of $R1$, R. In this design, V_{GS} is set to 1.35 V to produce a feedback resistance of 2.25 MΩ. An extra advantage of this circuit topology is that voltage biases at the input and output are automatically set without any additional biasing circuitry:

$$R = \frac{L}{K_pW(V_{GS} - V_T - V_{DS})}, \quad (2)$$

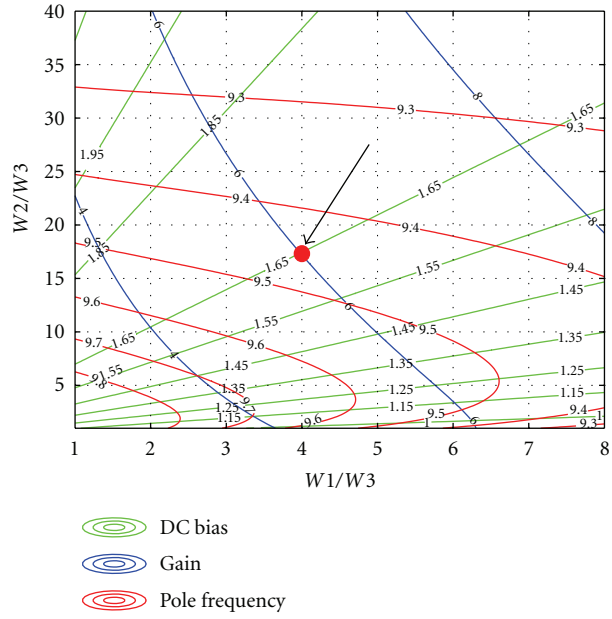

Figure 5: Nomograph for noise optimisation.

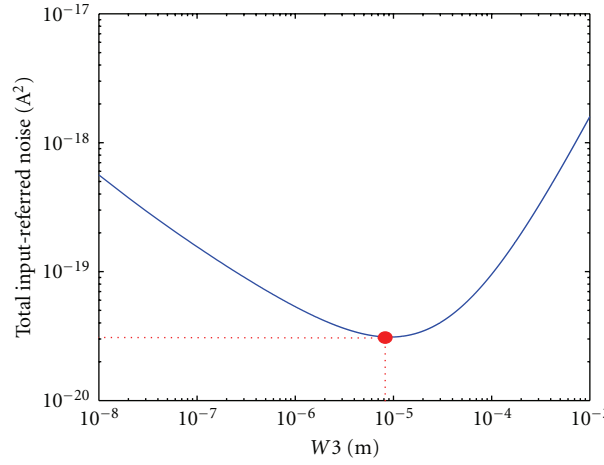

Figure 6: Determining the width of load transistor for the lowest noise.

where L is the channel length, W is the channel width, K_p is the transconductance parameter, and V_T is the threshold voltage.

To determine the size of transistors of the TIA, a graphical technique known as nomograph has been used [18]. For simplicity, a single stage of amplification is designed individually and the other stages are duplicates of the single stage. As shown in Figure 5, a nomograph is generated to assist the selection of suitable ratios of $W1/W3$ and $W2/W3$ that satisfy the DC bias, pole frequency, and voltage gain requirements. In this design, a DC bias of 1.65 V is chosen. A logarithm of pole frequency greater than 7.18 (obtained from $\log(4.3 \times BW)$) is necessary to ensure circuit stability. A voltage gain of 6.0 is chosen as a satisfactory compromise. A larger voltage gain could provide lower, hence better, input and output impedances; however it requires a larger die area

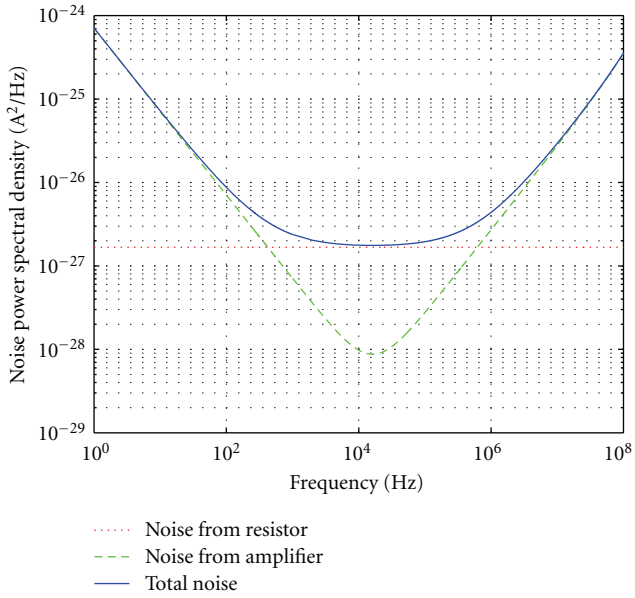

Figure 7: Noise power spectral density.

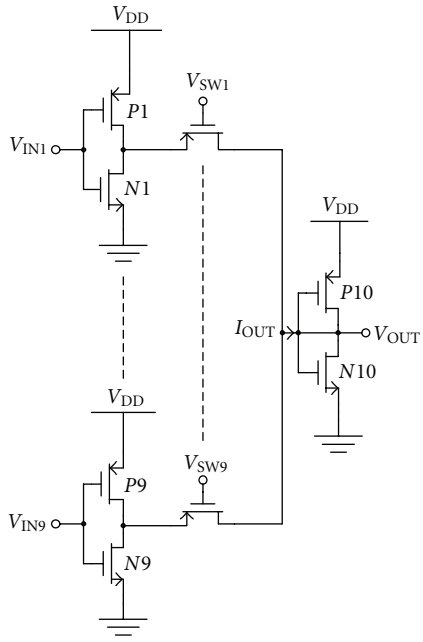

Figure 8: Circuit diagram of selector-combiner circuit.

and higher power consumption and causes poorer stability. By using these values on the nomograph, approximate ratios of $W1/W3$ and $W2/W3$ were determined to be 4.0 and 16.0.

In this TIA design, the first stage of amplifier must provide sufficiently large gain in order to render noise contributions from transistors of the subsequent stages insignificant. This widely used approach also simplifies the noise calculation. Equation (3) is used to compute the input-referred noise contributed by the first stage of amplifier and the feedback resistor [18]:

$$i_{\text{eq,in}}^2 = \frac{4kT}{R_f} + \frac{8kT}{3g_m}\left(1+\frac{1}{A1}\right)(2\pi C_{\text{in}})^2 f^2 + \frac{8kT}{3g_m}\left(1+\frac{1}{A1}\right)\frac{1}{R_f^2} + \frac{\left(K_{fn}+K_{fp}\right)I_{dsp}}{g_m^2 C_{ox} L_{effn}^2}(2\pi C_{\text{in}})^2 f + \frac{\left(K_{fn}+K_{fp}\right)I_{dsp}}{g_m^2 C_{ox} L_{effn}^2 f}\frac{1}{R_f^2}. \tag{3}$$

Total input-referred noise is then transformed as follows:

$$i_{\text{eqTOT,in}}^2 = \left\{\frac{4\pi q V_t C_{\text{in}} B}{A} + \frac{8qV_t}{3g_m}\left(1+\frac{1}{A1}\right)\frac{(\pi C_{\text{in}}B)^2}{A^2}\right\} I_2 B + \frac{8qV_t}{3g_m}\left(1+\frac{1}{A1}\right)(2\pi C_{\text{in}})^2 I_3 B^3 + \frac{\left(K_{fn}+K_{fp}\right)I_{dsp}}{g_m^2 C_{ox} L_{effn}^2}(2\pi C_{\text{in}})^2 I_{f2} B^2 + \frac{\left(K_{fn}+K_{fp}\right)I_{dsp}}{g_m^2 C_{ox} L_{effn}^2}\frac{(\pi C_{\text{in}}B)^2}{A^2} I_{f1}, \tag{4}$$

where q is the electron charge, V_t is the thermal voltage, C_{in} is the input capacitance, B is the bit rate, and K_{fn} and K_{fp} are the flicker coefficients of the NMOS and PMOS transistors, respectively. $A1$ is voltage for a single stage while A is the total voltage gain for three stages. It is noteworthy that B equals two times of the target bandwidth and g_m is the addition of the transconductance of transistors $P1$ and $N1$. I_2, I_3, I_{f1}, and I_{f2} can be conveniently substituted with 0.4026, 0.0361, 11.038, and 0.0983, respectively, all of which are obtained from Personick integrals and flicker noise integrals [19].

To optimise the noise performance of the design, the width of the NMOS load transistor, $W3$, may be varied. This essentially changes I_{dsp}, C_{in}, and g_m, thus $i_{\text{eqTOT,in}}^2$. It is important to bear in mind that C_{in} must take into account the capacitive contribution of C_{pd}. In this design, the target bandwidth used is 3.5 MHz. As shown in Figure 6, $W3$ for the lowest total input-referred noise can be easily obtained from the graph. For ease of calculation and layout drawing, the optimal $W3$ is rounded up to 8 μm and the resultant total input-referred noise is estimated at 3.13×10^{-20} A^2. With this value for $W3$, the noise power spectral density with respect to frequency is plotted in Figure 7. The graph reveals that the feedback resistor is the dominant noise contributor for frequency ranging between 400 Hz and 0.5 MHz.

2.3. Selector-Combiner Circuit. Selector-combiner circuit provides a flexibility of choosing signal of interest from particular pixels to be added up and sent to the output. Figure 8 depicts a 9-input SC circuit. V_{IN1} to V_{IN9} are the signal input pins while V_{SW1} to V_{SW9} are their corresponding control pins. PMOS transistors instead of NMOS transistors

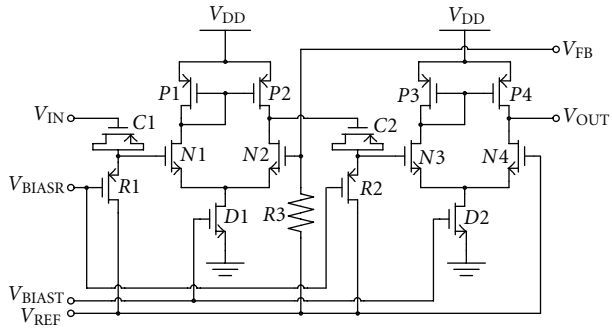

Figure 9: Circuit diagram of postamplifier.

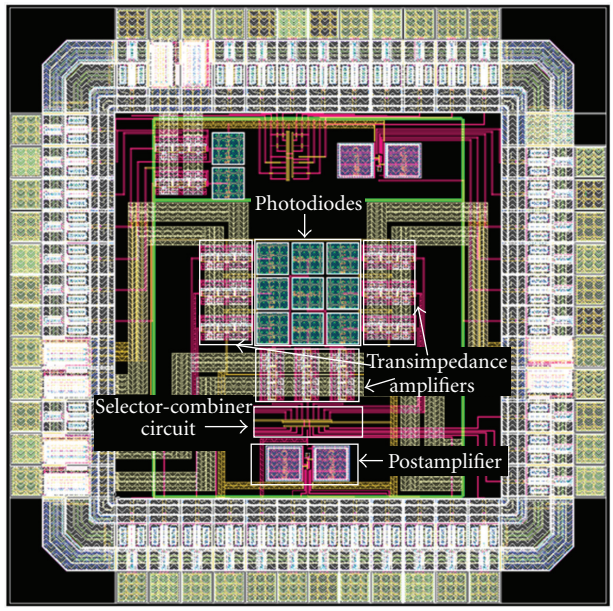

Figure 10: Microchip layout showing all subblocks.

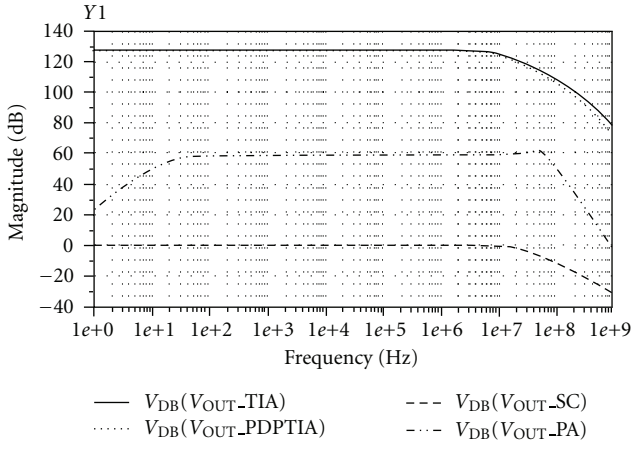

Figure 11: Frequency response for detector subblocks.

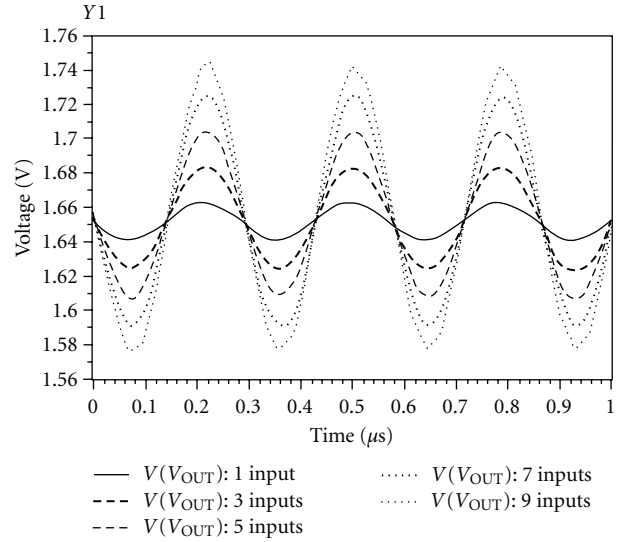

Figure 12: Simulation results for summing of signals in SC circuit.

are used as switches because they produce relatively lower noise. The signal-adding part of this circuit essentially performs a voltage-to-current conversion followed by a current-to-voltage conversion [20]. The W/L ratios of PMOS and NMOS transistors are adjusted so that (5) is fulfilled. Equations (6)–(8) prove that the summation of signals of this circuit is linearly operated and simulation result has then shown that this remains true for the output voltage ranging between 1.0 V and 2.15 V. A major advantage of using this technique compared to an op amp to add up signals is that fewer transistors are used, thus less chip area:

$$\beta = \beta_N = \beta_p, \tag{5}$$

$$I_{OUT} = -4\sum_{i=1}^{n} V_{INi}(V_{DD} - V_T)\beta, \tag{6}$$

$$V_{OUT} = \frac{I_{OUT}}{4\beta(V_{DD} - V_T)}, \tag{7}$$

$$V_{OUT} = \sum_{i=1}^{n} V_{INi}, \tag{8}$$

where β is the transconductance gain factor, V_{DD} is the supply voltage, and V_T is the threshold voltage.

2.4. Postamplifier. Postamplifier is necessary in this microchip to amplify the weak signal from SC circuit to be sufficiently large for good detection at the output. As illustrated in Figure 9, the PA in the detector comprises two stages of differential amplifier, both of which produce an open-loop voltage gain of approximately 44 dB individually. The maximum total voltage gain of this postamplifier is thus 88 dB. During the maximum voltage gain, the circuit, however, produces the lowest bandwidth. To improve bandwidth, voltage gain can be traded. Moreover, voltage gain of this circuit is adjustable to prevent saturation of signal, and it is

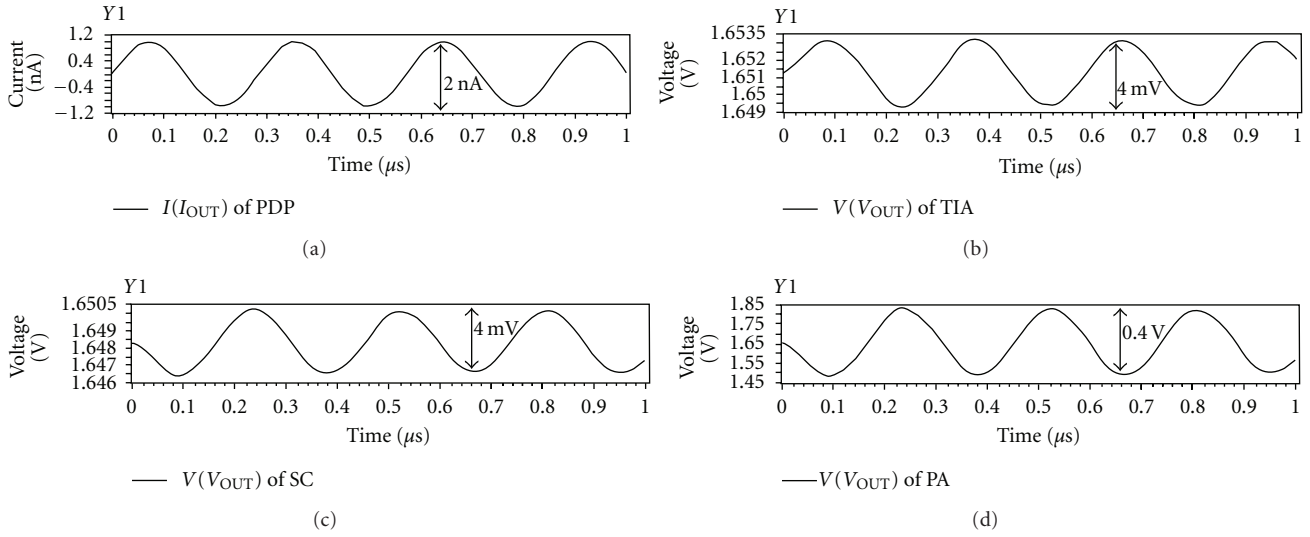

Figure 13: Transient analysis at different output points.

common to limit the output signal to 1 Vppk to be sent to an interface board in the processing machine.

Signal from the SC circuit is AC-coupled to the PA by using a RC filter that is, in our design, implemented with two PMOS transistors, with $C1$ acting as a capacitor while $R1$ as a resistor. Gate terminal of $C1$ is connected to the signal input meanwhile the source, drain, and bulk of $C1$ are bundled and connected to the input of the first stage differential amplifier. The size of $C1$ is made sufficiently large, 100 μm $\times$ 100 μm, producing a capacitance of 46 pF. The bulk of this transistor has a parasitic capacitance of 1.8 pF with p-substrate (connected to ground); thus the bandwidth of the circuit has been negatively affected. The semiconductor process does offer the capability of creating polysilicon-insulator-polysilicon (PIP) capacitor; however, none has been created in this circuit. The main reason is that, to achieve the same capacitance value, the lateral dimension of the PIP capacitor has to be 5.8 larger than that of the capacitor created using a PMOS transistor. Furthermore, the parasitic capacitance connecting to p-substrate is as large as 7.9 pF, and this would greatly affect the circuit bandwidth. The W/L ratio of $R1$ is set to a very small value in order to produce a high resistance. V_{BIASR} is used to adjust the resistance of $R1$ and thus the cut-off frequency of the filter. The overall gain of the PA is controlled by the ratio of the resistance of $R4$ to the resistance of $R3$. $R3$ is built-in on the microchip and implemented using n-diffusion. $R4$ is an external discrete component, and its terminals are to be connected between V_{FB} and V_{OUT}.

3. Results and Discussions

Figure 10 presents the layout of the entire microchip. The dimension of this integrated circuit is 1960 μm $\times$ 1960 μm. Nine pixels of NWD photodiode are located in the middle of the chip while their corresponding TIA is critically placed very close to them, as can be seen on the left, bottom, and right of the photodiode array. The SC circuit is placed between the TIAs and the PA. The PA is placed next to the IO cells at the bottom end of the chip as it possesses many interface signals. The chip will be packaged using QFN48; 8 pins for power/ground, 39 for signals, and 1 to connect to the cavity of the package.

Several simulations were carried out to ensure that the circuits work per design specifications. Figure 11 shows the frequency response for the subblocks of the photon detector. From this graph, the -3 dB bandwidth (and gain) of the TIA individually, the TIA connected to the photodiode, the SC, and the PA are found to be 10.72 MHz (126 dB), 8.91 MHz (126 dB), 27.44 MHz (-0.39 dB), and 71.22 MHz (59.18 dB), respectively. It is worth noting that the result of TIA connected to PD is slightly worse compared to that of the TIA alone due to the photodiode capacitance seen by the input of the TIA. Figure 12 exhibits the simulations results of summing signals from different inputs of the SC circuit. Each input is supplied with a 20 mVppk sine wave. The signals are combined without much distortion when the switches are turned on incrementally from V_{SW1} to V_{SW9}. Figure 13 shows the transient analysis at different output points of the microchip. The first waveform, swinging with a peak-to-peak voltage of 2 nA, represents the signal produced by the photodiode. The second waveform is the output signal from the TIA which has been amplified to about 4 mVppk. Almost identical to the second waveform, the next waveform is the output from the SC circuit producing ignorable loss. The last waveform shows that the signal has been boosted to a range that could be easily measured. The overall transimpedance gain produced by the microchip is approximately 180 dBΩ.

The design is currently being fabricated in a 0.35 μm CMOS Opto process by Austriamicrosystems (C35B4O1). Apart from an additional ARC layer for enhancing photosensitivity, this 4-metal-layer technology has an EPI substrate with the thickness of 14 μm which substantially improves the performance of cut-off frequency and dark current. Important optical and electrical measurements will be acquired when the microchip is delivered from the foundry.

4. Conclusion

A design of multipixel photon detectors using an optically enhanced CMOS technology has been presented. Simulation results show that each photodiode of this optoelectronic microchip can detect signals with optical power as low as 1 nW. Total transimpedance amplification of the entire circuit is over 180 dBΩ, and the detector gain is adjustable in the TIAs and the PA. The 3 dB cut-off frequency of the entire circuit is above 3.5 MHz meeting the minimum requirement for video applications. This novel configurable solid-state solution could be used for the secondary electron detection in the SEM providing the benefits of smaller dimension, lower supply voltage and power requirements, and potentially lower product cost.

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