# All-GaN Integrated Cascode Heterojunction Field Effect Transistors

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*Abstract*—All-GaN integrated cascode heterojunction field effect transistors were designed and fabricated for power switching applications. A threshold voltage of +2 V was achieved using a fluorine treatment and a metal-insulator-semiconductor gate structure on the enhancement mode part. The cascode device exhibited an output current of 300 mA/mm by matching the current drivability of both enhancement and depletion mode parts. The optimisation was achieved by shifting the threshold voltage of the depletion mode section to a more negative value with the addition of a dielectric layer under the gate. The switching performance of the cascode was compared to the equivalent GaN enhancement-mode-only device by measuring the hard switching speed at 200 V under an inductive load in a double pulse tester. For the first time, we demonstrate the switching speed advantage of the cascode over equivalent GaN enhancement-mode-only devices, due to the reduced Miller-effect and the unique switching mechanisms. These observations suggest that practical power switches at high power and high switching frequency will benefit as part of an integrated cascode configuration.

*Index Terms*—Power electronics, Semiconductor devices, Semiconductor switches, SPICE, Semiconductor heterojunctions.[1]

## I. INTRODUCTION

Cascode devices of GaN heterojunction field effect transistors (HFETs) plus Si MOSFETs have recently attracted much attention and are now commercially available [1-8]. The typical layout consists of a series connection of a high voltage depletion-mode (D-mode) GaN device and a low voltage enhancement-mode (E-mode) Si device as shown in Fig. 1. The GaN plus Si hybrid cascode device not only enables normally-off operation, but the cascode structure also offers the advantage of mitigation of the Miller effect, leading to an improved switching speed and reduced switching losses [8-9]. This makes cascode devices strong candidates for high power and high frequency switching applications. However, a few issues have been reported that may negate the speed advantage in the GaN plus Si hybrid cascode devices [10-13]. Firstly, the connections between the Si MOSFET and GaN devices result in increased parasitic inductance, which can cause excessive 'ringing' effects at fast switching speed thus limiting high frequency operation [12-13]. This brings challenges to the packaging design as reported by several studies on the effect of improved packages for the hybrid cascode devices [12-15]. In addition, due to the mismatch in intrinsic capacitances between the Si and GaN devices and the body diode in the Si MOSFET, the Si device can be driven into avalanche mode causing additional switching energy loss [10]. Moreover, the mismatched capacitances together with the parasitic inductance may cause large oscillations during turn-off under high current operation [11]. Adding an external capacitor between the drain and gate of the Si device was proposed in [10] and [11] to match the capacitance in the hybrid cascode device and prevent avalanche in the Si device, at the expense of additional parasitic inductance and careful designs in the device packaging are required.

In this study, we proposed an all-GaN integrated cascode device by replacing the Si MOSFET with a low voltage GaN E-mode device, so that the issues above can be addressed and the switching speed can be improved. The avalanche in the low voltage device during turn-off can be avoided due to the lack of body diode in the GaN E-mode device. In additional, the parasitic inductance can be minimized by monolithic integration, reducing the oscillation during turn-off operation [11] as well as leading to improved parallel operation [16]. Only a few studies on the integrated cascode structure have been reported and are limited to RF applications [17] and [18]. Additionally, there has been no analysis of the interrelationships between the E and D-mode devices, which is required to enable full optimization of the cascode design for switching applications. In this paper, we describe the design and fabrication of all-GaN integrated cascode devices for switching applications and present an analysis of the optimization requirements.

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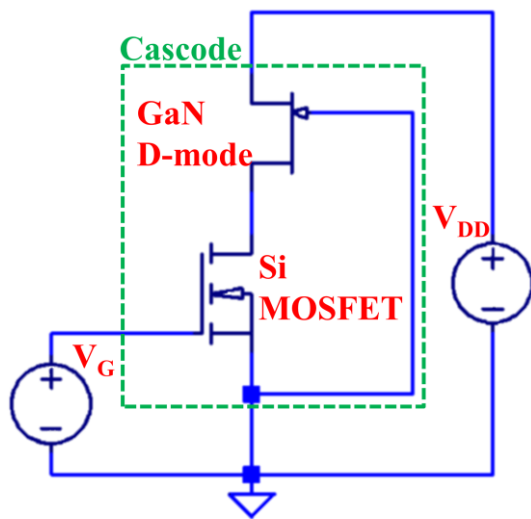
Fig. 1.  Circuit diagram of GaN + Si MOSFET cascode configuration.

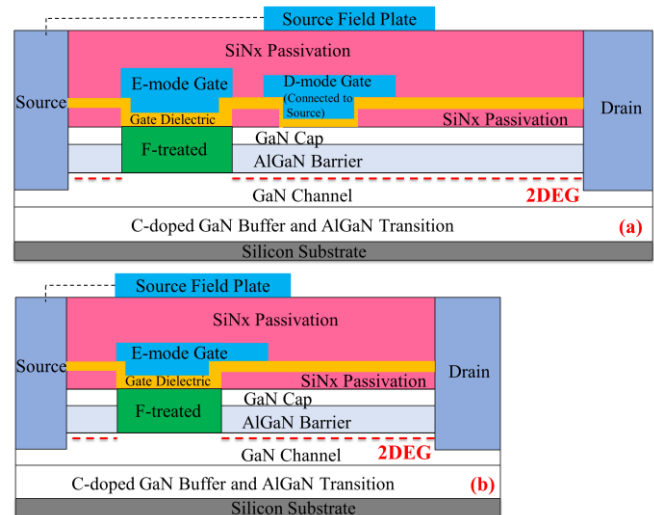1.5 μm D-mode gate length and 5 μm gap between D-mode and E-mode gates), respectively.



Fig. 2.  Device structure of (a) an all-GaN integrated cascode device and (b) an E-mode-only device with source field plate.
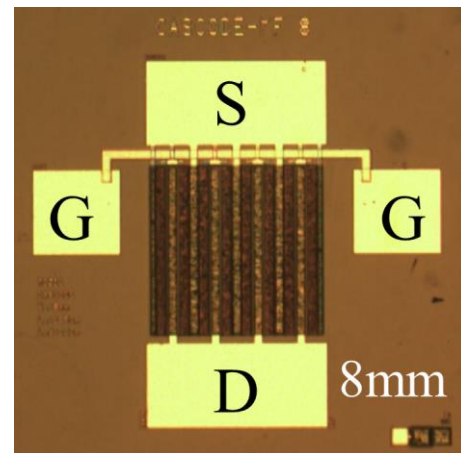
## II. DC CHARACTERISTICS

### A. Device fabrication

Fig. 2 shows the structures of an all-GaN integrated cascode device and a GaN E-mode-only device. The GaN/AlGaN/GaN heterojunction structure was grown on a 6-inch Si substrate using metal-organic chemical vapour deposition. All-GaN monolithically integrated cascode devices were fabricated using a standard GaN HFET fabrication process. Firstly, mesa isolation was performed by inductively coupled plasma etching to define the device area. An ohmic metal stack (Ti/Al/Ni/Au) was deposited and annealed at 830 ℃ to form the source and drain contacts. A typical contact resistance of 0.7 Ω·mm was obtained from transmission line model measurements. Devices were passivated with 70 nm $SiN_x$ using plasma enhanced chemical vapour deposition (PECVD) and a 1.5 μm gate window was opened by etching through the $SiN_x$ layer using reactive ion etching (RIE) for both the E-mode and D-mode gate. A $CHF_3$ plasma-treatment in an RIE system was performed on the E-mode gate window to implant fluorine and shift the threshold voltage, $V_{th}$, from negative to positive [19]. A nominally 20 nm thick $SiN_x$ layer was deposited using PECVD prior to the T-shaped Ni/Au gate metal formation step to form a metal-insulator-semiconductor (MIS) gate structure in the E-mode section. Both a Schottky gate and an MIS gate for the D-mode part of the cascode structure were studied and will be discussed further in Section II-C. A gate-connect field plate (GFP) was formed on the gate of the D-mode part in the cascode configuration. Finally, devices were passivated with 300 nm of PECVD $SiN_x$ before the formation of the source-connected field plate (SFP), and Ti/Au bond pads were deposited after via opening in this $SiN_x$. Devices with gate widths, $W_g$, of 100 μm and 8 mm were fabricated. Fig. 3 shows the optical image of a 8 mm integrated cascode device. For comparision, GaN D-mode-only and E-mode-only devices were also fabricated at the same time. All devices have a gate length of 1.5 μm, GFP extension ($L_{GFP}$) of 1 μm and SFP ($L_{SFP}$) extension of 2 μm. The source-drain separation ($L_{SD}$) of the E-mode-only and the cascode devices are 16 μm and 22.5 μm (additional



Fig. 3.  Monolithically integrated AlGaN/GaN HFET cascode configuration with gate width of 8 mm.

### B. DC characteristics

Fig. 4(a) shows the gate transfer characteristics of 100 μm gate width E-mode-only and cascode devices. Both E-mode-only and cascode devices have a positive $V_{th}$ of +2 V. It is noted that these devices may suffer from switching issues [20] due to relatively low $V_{th}$ under high dv/dt operations and reliability issues due to the instability of the fluorine treatment [21-22] and MIS gate [23-25] techniques. Other E-mode technologies such as MOSFETs [26] and p-AlGaN gate [27] or other E-mode technologies which address these concerns can be applied to realize the integrated cascode configuration.

Fig. 4(b) shows the I-V characteristic of the cascode device. An on-resistance ($R_{on}$) of 27 Ω·mm (6 m Ω·cm² normalized to the active area between source and drain contacts and gate width) is measured from the cascode device, which is higher than other reported lateral single [26 and 28] and vertical devices [29-32]. The higher $R_{on}$ is a

result of larger device area to accommodate both D-mode and E-mode parts. An output current of 200 mA/mm at $V_{DS} = 10$ V and $V_{GS} = +10$ V was measured from the cascode device. The D-mode-only device with a Schottky gate as shown in Fig. 4(a) has a $V_{th}$ of -5.5 V and an output current around 575 mA/mm at $V_{DS} = 10$ V and $V_{GS} = +2$ V, while the E-mode-only device has the same $V_{th}$ as the cascode but a higher output current close to 300 mA/mm. Since both the E-mode and D-mode parts have the same $W_g$, the output current of the cascode structure is limited by the section with the lower current drivability, which is the E-mode part in this case. However, a lower output current in the cascode device compared to its equivalent E-mode-only device is observed and this indicates that some optimization of the design is required to achieve the maximum output current in the cascode device.
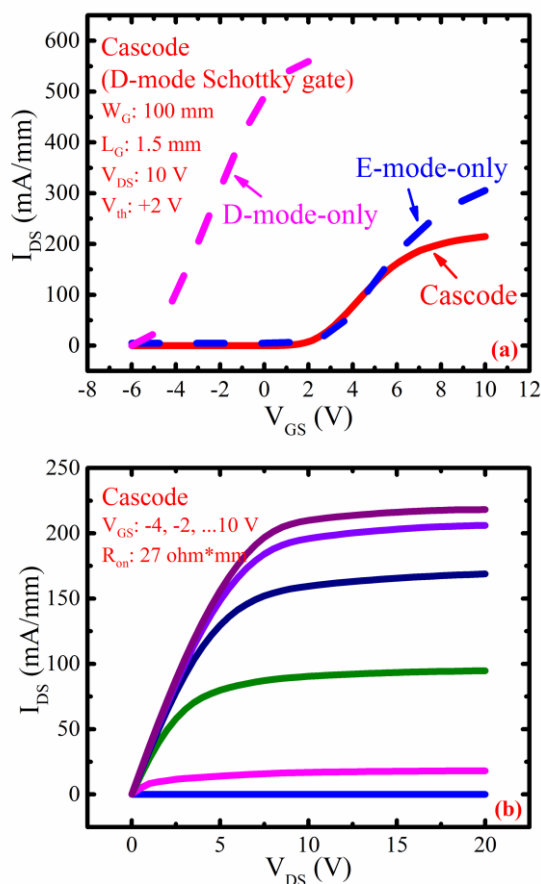


Fig. 4.    (a) Gate transfer characteristics of an all-GaN integrated cascode device together with an equivalent E-mode-only device and a D-mode-only device (b) I-V characteristic of a 100 μm gate width cascode device.

To facilitate the full understanding of how the cascode configuration works, particularly the voltage transients from off-state to on-state between the E-mode and D-mode, a cascode device with an additional ohmic pad between the D-mode gate and the E-mode gate was fabricated, as shown in the inset of Fig. 5. This layout does not change the I-V characteristics and allows the potential between the D-mode gate and the E-mode drain ($V_{M\_DC}$) to be monitored. Fig. 5 illustrates the measured $V_{M\_DC}$ as a function of the E-mode

gate bias, $V_{GS}$. During the off-state ($V_{GS}<V_{th\_cascode}$), $V_{M\_DC(off)}$ is equal to 5.3 V, which is the magnitude of the D-mode threshold voltage ($V_{th\_D}$), and the channel under the D-mode gate metal is fully depleted. When $V_{GS}$ increases to the on-state ($V_{GS}>V_{th\_cascode}$), $V_{M\_DC}$ drops and the channel under both D-mode and E-mode gates begin to conduct. At the on-state ($V_{GS} = +8$ V), $V_{M\_DC(on)}$ or $V_{DS\_E-mode(on)}$ is equal to 2.8 V, which is below the 'knee' voltage of the E-mode part. As a result, the output current of the cascode device is limited by the drain-source voltage $V_{DS\_E-mode(on)}$ of the E-mode part and hence needs to be at the 'knee' voltage of the E-mode part to guarantee the maximum current drivability of the cascode configuration.
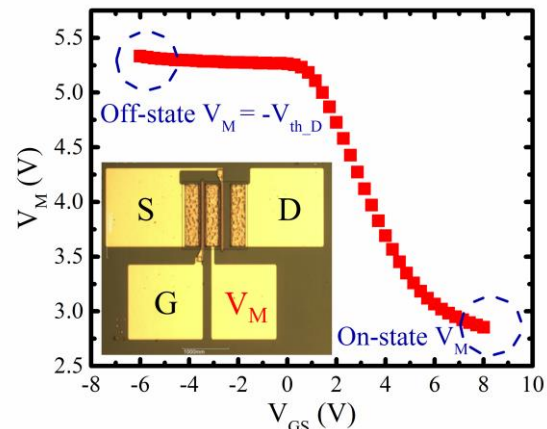


Fig. 5.  The middle point voltage ($V_M$) measured as a function of gate bias using a cascode device with an extra pad between the E-mode gate and the D-mode gate. The on-state value of $V_M$ determines the conducting state of both D-mode and E-mode parts in the cascode device.

To optimize the output current of the cascode device, we equate the current through the D-mode and E-mode parts by engineering $V_{th\_D}$ and hence control $V_{M\_DC(on)}$ to ensure both parts are biased at the desired $V_{DS}$ during the on-state. From Fig. 6, $V_{M\_DC(on)}$ depends on the D-mode $V_{th}$ and how much $V_{M\_DC}$ drops when the gate bias increases. Therefore, by increasing the D-mode $V_{th}$ (to be more negative), $V_{M\_DC(on)}$ or $V_{DS\_E-mode(on)}$ will also increase until it reaches the E-mode 'knee' voltage. However, a more negative $V_{th\_D}$ also increases $V_{M\_DC(off)}$ and hence increases the total energy stored at the middle node of the cascode during switching, which may increase the switching loss and limit the switching frequency. Therefore, it is vital to optimize the D-mode $V_{th}$ to match the output current of both E-mode and D-mode sections for maximum overall current.
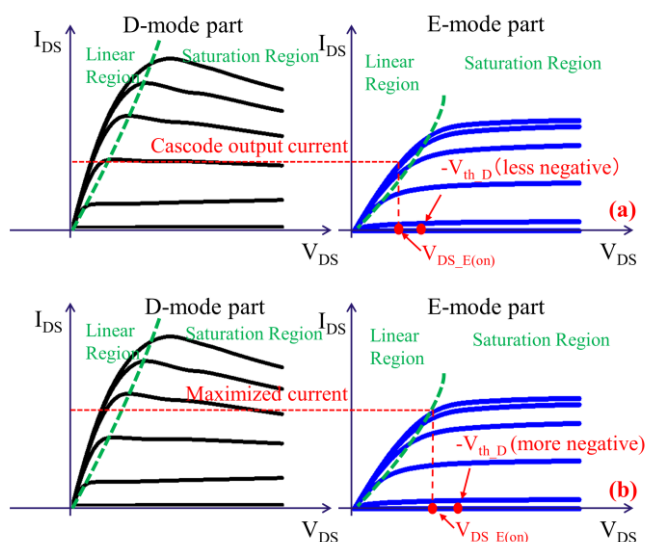
Fig. 6. (a) A less negative $V_{th\_D}$ yields a smaller $V_{DS\_E(on)}$ and cascode output current (b) A more negative $V_{th\_D}$ pushes $V_{DS\_E(on)}$ to the $V_{knee\_E}$ and improve the cascode output current to its maximum value.

### C. Output current optimization

An LTSPICE simulation of the all-GaN cascode based on a Si JFET model was conducted to obtain the optimum D-mode $V_{th}$ for the maximum overall current. Fig. 7(a) shows the schematic diagram of the simulation circuit. The device parameters used in the simulation were extracted experimentally as shown in Table I. Capacitive elements were not considered for the DC simulations.
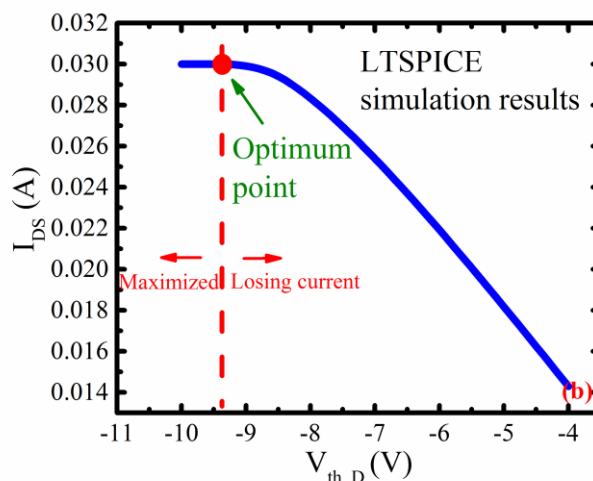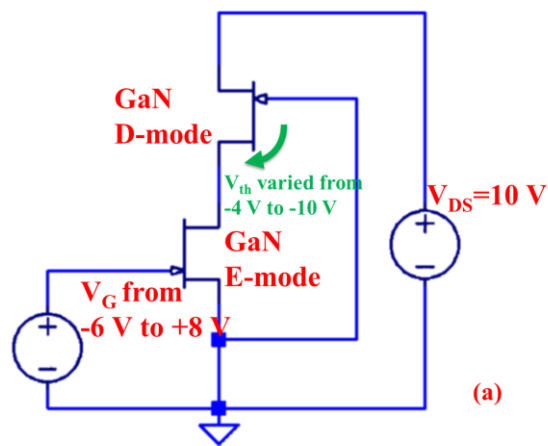


Fig. 7. (a) Simulation circuit used to study the influence of the D-mode $V_{th}$ on the output current of the cascode device. (b) Simulation results of drain current indicating an optimum D-mode $V_{th}$ that leads to the maximum output current.

TABLE I
SUMMARY OF DEVICE PARAMETERS USED IN LTSPICE FOR $V_{TH}$ ENGINEERING

|  | D-mode part | E-mode part |
|---|---|---|
| Gate width ($W_g$) | 100 µm | 100 µm |
| Trans-conductance ($g_m$) | 150 mS/mm | 75 mS/mm |
| On-resistance ($R_{on}$) | 13 Ω mm | 14 Ω mm |
| Threshold voltage ($V_{th}$) | -4 V to -10 V | +2 V |

Fig. 7(b) shows the simulated output current of a cascode device with varying $V_{th}$ of the D-mode part. The output current increases with increasing (negative) D-mode $V_{th}$ as a result of increasing $V_{DS\_E-mode(on)}$ as discussed above. The simulated current reaches its maximum value at a $V_{th}$ of -9.2 V. At this point, $V_{DS\_E-mode(on)}$ reaches the 'knee' voltage of the E-mode part (5.9 V) and hence no further improvement in the drain current is observed up to -10 V.

In order to verify the simulated results, two cascode structures were fabricated: one with a Schottky gate structure for the D-mode part and the other one with a nominally 10 nm PECVD SiN$_x$ MIS gate to shift $V_{th}$ more negative. Fig. 8 compares $V_{th}$ of GaN D-mode-only devices with a MIS gate and Schottky gate. $V_{th}$ of the D-mode devices is shifted from -5.5 V to -8.5 V with the MIS gate. The output current of the cascode configuration, as shown in the gate transfer characteristics, has been successfully improved from 150 to 300 mA/mm for the device with a D-mode MIS gate which is at similar level as the GaN E-mode-only device at $V_{GS}$ =10 V.

This shows an excellent agreement with the simulated results and highlights the importance of matching both D-mode and E-mode to provide the maximum output current in the cascode devices.
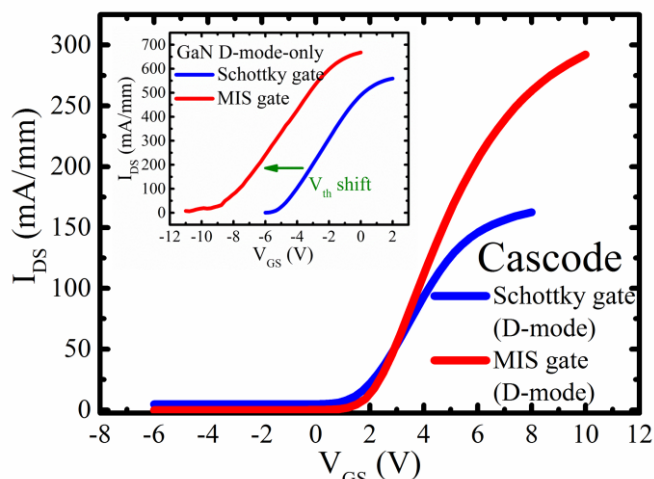


Fig. 8. Cascode output characteristics showing an improved current from the optimised cascode structure resulting from an increase in the threshold voltage of the D-mode section (inset).

## III. SWITCHING PERFORMANCE

### A. Experimental

The hard switching performance was compared between an 8 mm gate width multi-finger gate all-GaN integrated cascode device and an 8 mm gate width GaN E-mode-only device using a double pulse tester (DPT). Fig. 9 shows the circuit diagram of the measurement setup of the DPT for the devices. A 0.5 mH inductive load was used to deliver a 0.4 A load current. A commercial gate driver supplying a voltage from -4 V to +6 V was used to switch on the device. A high gate resistor (100 Ω) was used for both $R_{G\_on}$ and $R_{G\_off}$ to limit the gate drive current and hence slow the switching speed to better enable the switching comparisons. The load current to peak gate current ratio was around 10:1. Schottky diodes were used in both gate and load loops to minimise the reverse recovery time. The devices were wire bonded to a printed circuit board for the measurement and is shown highlighted in the box in Fig. 10. In total two pulses were applied to the gate of both devices. The first pulse was to build up the load current and the turn-off time was measured at the end of the first pulse. The turn-on transient was recorded at the beginning to the second pulse. The drain current was sensed by a 400 MHz bandwidth current viewing resistor T&M SDN-414-01. The gate voltage, drain current and drain voltage were monitored and recorded by a LeCroy WaveSurfer oscilloscope.
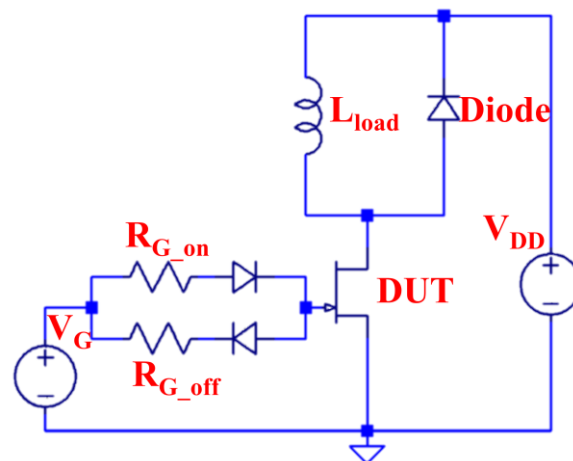


Fig. 9. Circuit diagram of Double Pulse Tester for switching speed measurement.
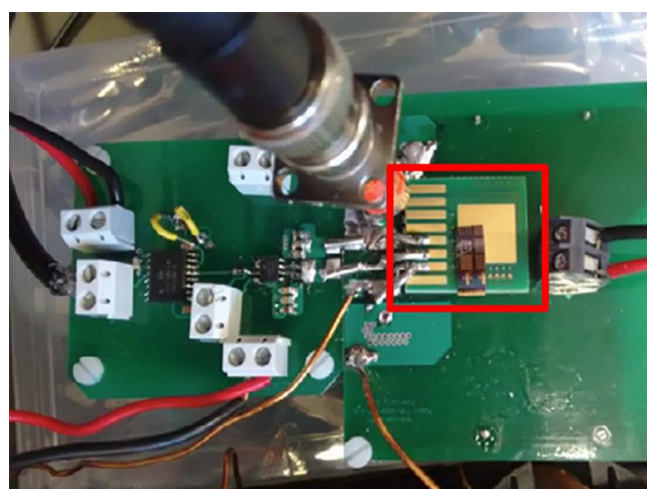


Fig. 10. An optical image of the DPT measurement setup.

The switching speed of both cascode and GaN E-mode-only devices were measured at 200 V drain bias. Typical switching sequences of the cascode configuration has been detailed in [9], therefore, in this study, we will simplify the explanation of the switching waveforms and extract the voltage and current rise (fall) time for comparison. During turn-on from $t_0 - t_1$, as shown in Fig. 11 (a), the current in the cascode ($I_{DS}$) rises up to the load current value after $V_{GS}$ of both the E-mode and D-mode parts reach the value that can provide the load current. After that, the voltage of cascode ($V_{DS}$) drops to the on-state voltage during $t_1 - t_2$. The overshoot of the current during the interval of $t_1 - t_2$ is due to the discharge of the parallel capacitance in the load loop. During the turn-off from $t_0 - t_2$, as shown in Fig. 11 (b), $V_{DS}$ rises up first to 200 V after the $V_{GS}$ falls below $V_{th}$. In the interval of $t_0 - t_1$, $I_{DS}$ steps down from the load current due to the charging of the parasitic parallel capacitance in the load loop [8-9]. The ringing effect during $t_0 - t_2$ is caused by the parasitic inductance in the circuit. The E-mode-only device shows an increased ringing amplitude compared to the cascode which could be caused by differences in the wire bonding geometry detail. However, this should have little influence on the comparison. $V_{DS}$ reaches 200 V at $t_2$, where $I_{DS}$ starts to drop and the turn-off transition ends at $t_3$.

Results of switching speed and energy loss for both

devices are summarized in Table II. The rise/fall times of $V_{DS}$ and $I_{DS}$ are extracted from 10% of their peak values to 90%. The energy loss is calculated by the integration of the $I\,V$ product during the switching transition period. The all GaN integrated cascode device exhibits a faster switching speed compared to the E-mode-only device, resulting in approximately 35% and 21% less in the turn-off and turn-on switching energy losses, respectively.

gate is located on (for Schottky gate) or close to the semiconductor (for MIS gate) in the cascode, the channel under the D-mode gate will be fully depleted before the region between the D-mode and E-mode gates as the off-state drain bias increases. Once the channel under the D-mode gate is depleted ($V_{th}$ for the Schottky and the MIS gate is 5 V and 9 V, respectively), the region between the D-mode and E-mode gates is effectively shielded from the drain bias and the
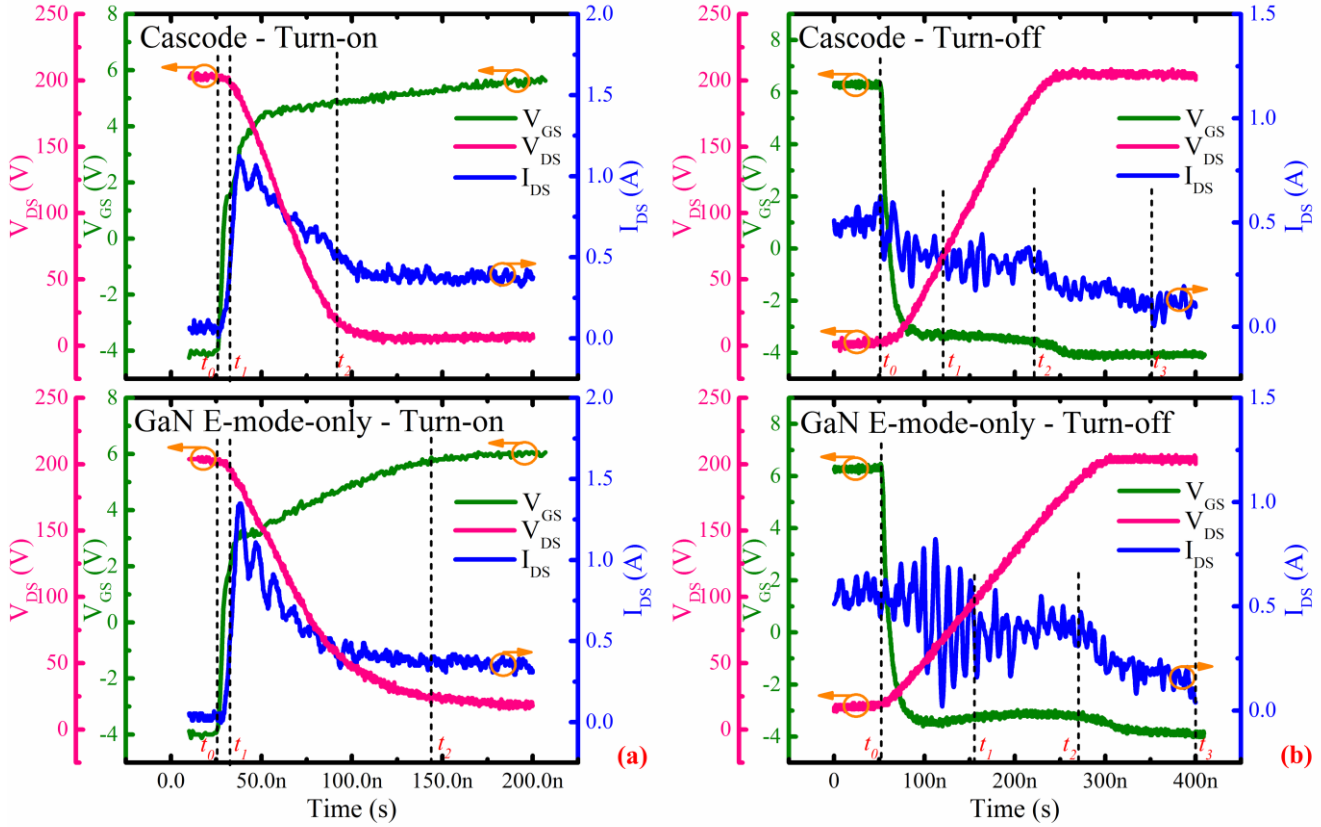


Fig. 11. 200V (a) turn-on and (b) turn-off switching waveforms for 8 mm cascode and 8 mm GaN E-mode-only devices.

TABLE II
SUMMARY OF SWITCHING RESULTS AT 200 V FOR THE ALL GaN INTEGRATED CASCODE CONFIGURATION AND GaN E-MODE-ONLY DEVICE

| | | Cascode | GaN E-mode-only |
|---|---|---|---|
| Turn-on | Current rise time ($t_{r\_I}$) | 5 ns | 5 ns |
| | Voltage fall time ($t_{f\_V}$) | 51 ns | 104 ns |
| | Turn-on energy loss ($E_{on}$) | 5.55 μJ | 7.02 μJ |
| Turn-off | Current fall time ($t_{f\_I}$) | 110 ns | 110 ns |
| | Voltage rise time ($t_{r\_V}$) | 134 ns | 200 ns |
| | Turn-off energy loss ($E_{off}$) | 9.39 μJ | 14.41 μJ |

## B. Discussion

Inspection of Fig. 2(b) reveals the possibility of the SFP acting as a gate to form a D-mode device in a cascode-like configuration. However, the fundamental operational difference between the integrated cascode configuration and the E-mode-only device is the presence of 2DEG in the region between D-mode and E-mode gates during the off-state in the cascode. A TCAD simulation based on the structures of our cascode and E-mode-only devices was carried out, as shown in Fig. 12 (a) and (b). As the D-mode

2DEG is retained as observed in the TCAD simulation in Fig. 12(c) and (e). This leads to reduction in the Miller effect as the Miller capacitance becomes the gate-drain capacitance of the E-mode part ($C_{GD-E}$) and is only subject to a relatively low voltage (which is equal to the D-mode gate $V_{th}$) and not the full drain bias during switching. On the other hand, the GaN E-mode-only device does not exhibit such behaviour as the depletion region extends continuously from the gate towards the drain as shown in Fig. 12(d) and (f) at high drain voltage. As a result, $C_{GD}$ is subject to the high drain voltage during the switching processes. The SFP, on the other hand, will result in a reduction in the effective $C_{GD}$ as it enhances the depletion region extension toward the drain compared to the device without SFP. Note that the value of the intrinsic capacitance ($C_{GD}$) in the E-mode-only device can be several times smaller than $C_{GD-E}$ in the cascode device due to a smaller E-mode gate to E-mode drain spacing in the latter. However, because the voltage at the drain of the E-mode part is much lower compared to the drain voltage, especially for high voltage applications, the cascode device still retains a benefit in the switching speed. The conduction band diagram under the E-mode and D-mode gate in the cascode device can be found in Fig. 12 (g) and (h), respectively.
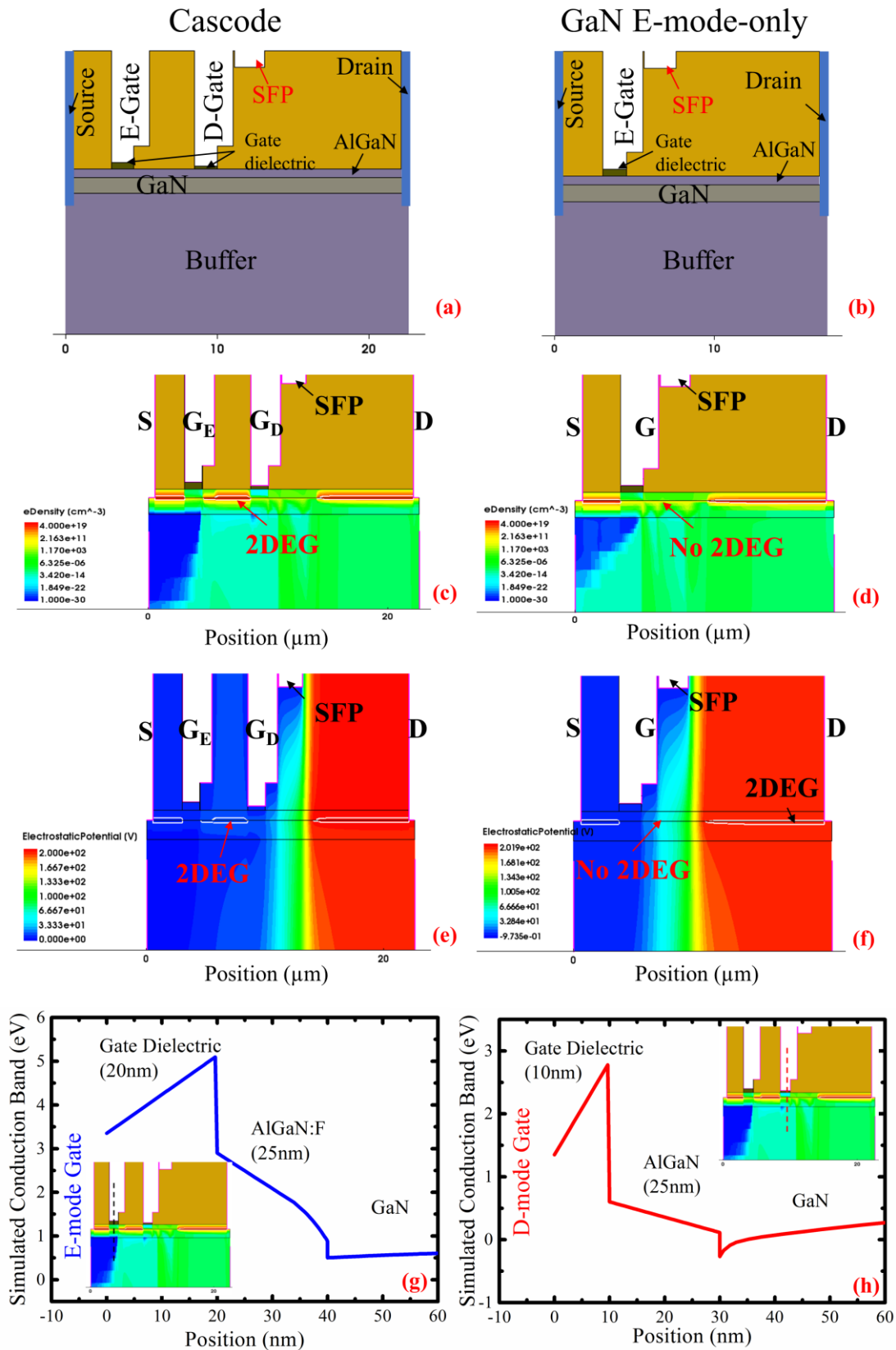
Fig. 12. Device structures of (a) cascode and (b) E-mode-only used in TCAD simulation. TCAD simulation of electron density for (a) integrated cascode device and (b) single GaN E-mode device during off-state at $V_{DS}$ = 200 V and $V_{GS\_E-mode}$ = 0 V. TCAD simulation of electrostatic potential for (c) integrated cascode device and (d) single GaN E-mode device during off-state at $V_{DS}$ = 200 V and $V_{GS\_E-mode}$ = 0 V. The integrated cascode device is with $L_{SD}$ =22.5 μm, $L_{GD}$ =12 μm, $L_{GFP}$ =1 μm and $L_{SFP}$ =2 μm. The single GaN E-mode device is with $L_{SD}$ =16 μm, $L_{GD}$ =12 μm, $L_{GFP}$ =1 μm and $L_{SFP}$ =2 μm. Conduction band diagram under (e) E-mode and (f) D-mode gate in the cascode device at $V_{DS}$ = 0 V and $V_{GS\_E-mode}$ = 0 V. A uniform fluorine concentration with sheet density of 1.2x10$^{13}$ cm$^{-2}$ in the AlGaN barrier under E-mode MIS gate was used in the simulation.
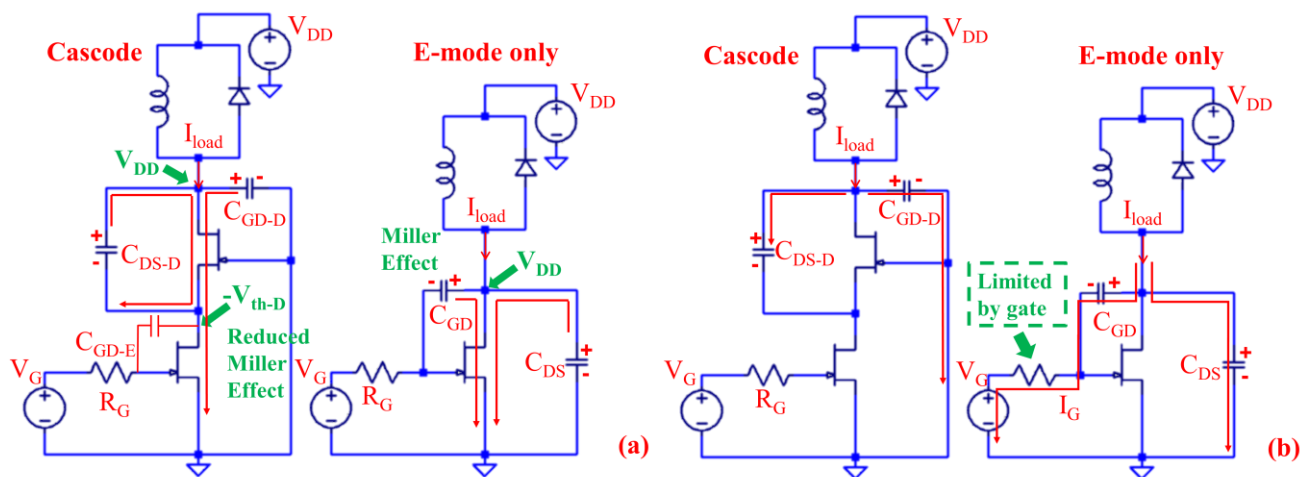
Fig. 13. The charging and discharging paths of the output capacitance in the cascode device and GaN E-mode-only device with SFP during (a) turn-on process and (b) turn-off process.

Up to this point we have discussed the differences between the cascode and E-mode-only devices in terms of how they function. We will now consider the fundamental charging mechanisms of each, leading to the observed differences in the switching speeds. During turn-on, because the effective Miller capacitance is shifted to $C_{GD-E}$ at the middle point, the majority of the energy stored in the output capacitance of the cascode device is dissipated with no Miller-effect. In addition, the energy stored in $C_{DS-D}$ is discharged through the D-mode channel only, as shown in Fig. 13(a). Therefore, the fact that our D-mode device has a higher trans-conductance ($g_m$) and current drivability, which enables a larger discharging current within the D-mode channel, also contributes to the faster turn-on speed for the cascode device. During turn-off, the output capacitance of the cascode device is charged up to the high voltage by the full load current which is normally higher than the current in the gate loop, while the charging process of the output capacitance is limited by the current at the gate node in the E-mode-only device as illustrated in Fig. 13(b). This larger charging current is the main reason for the cascode device to be more advantageous in turn-off compared to turn-on, as observed in our experimental and [1], [4] and [8]. The turn-off advantage strongly depends on the load current to peak gate current ratio [8]. With a good gate driver and small gate resistor to provide sufficient gate current, the switching performance of the E-mode-only device is expected to be comparable to that of cascode device [8]. However, in this case the cascode device would still benefit from a lower di/dt in the gate loop to achieve the same switching speed. In addition, the availability of gate drivers with current capability close to the load current is limited in high current applications.

These observations show that, for practical high frequency and high power switches, the cascode device will have lower switching losses compared to the equivalent E-mode-only device. The price to pay for this advantage is a slightly more complex structure and a higher specific on-resistance.

## IV.  CONCLUSION

The all-GaN integrated cascode configuration is an excellent candidate for high frequency high power applications due to the reduced Miller effect and reduced parasitics. Devices were fabricated with a positive $V_{th}$ of +2 V and output current of 300 mA/mm. Careful optimization of the D-mode device threshold voltage is required to achieve maximum cascode current drivability, which equals the output current of its E-mode part. The fundamental operational difference between an integrated cascode device and GaN E-mode-only device is discussed using TCAD simulation. This shows that the presence of the 2DEG in the region between D-mode and E-mode gates during the off-state is the key to enable the device cascode switching behaviour. All-GaN integrated cascode devices show relatively faster switching speed and 35% (21%) less in turn-off (turn-on) switching energy loss under 200 V hard switching measurement compared with GaN E-mode-only device with SFP. The advantage originates from the reduced effective Miller-capacitance and the unique switching mechanisms in the cascode device. Compared with the GaN E-mode-only device, the cascode can achieve a given switching frequency but with less current requirement in the gate driving circuit. As power increases, a greater benefit will accrue from switches incorporating a cascode structure.

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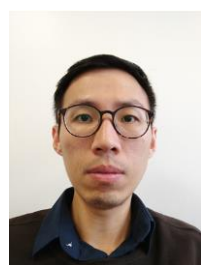
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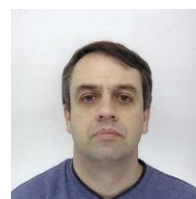
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