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## GENERALIZING ROOT VARIABLE CHOICE IN WAVE DIGITAL FILTERS WITH GROUPED NONLINEARITIES

Kurt James Werner

The Sonic Arts Research Centre (SARC)  
School of Arts, English and Languages  
Queen’s University Belfast, UK  
k.werner@qub.ac.uk

Michael Jørgen Olsen

Center for Computer Research  
in Music and Acoustics (CCRMA)  
Stanford University, CA, USA  
mjolsen@ccrma.stanford.edu

Maximilian Rest

E-RM Erfindungsbüro  
Berlin, Germany  
m.rest@e-rm.de

Julian D. Parker

Native Instruments GmbH  
Berlin, Germany  
julian.parker@  
native-instruments.de

### ABSTRACT

Previous grouped-nonlinearity formulations for Wave Digital Filter (WDF) modeling of nonlinear audio circuits assumed that nonlinear (NL) devices with memoryless voltage–current characteristics were modeled as voltage-controlled current sources (VCCSs). These formulations cannot accommodate nonlinear devices whose equations cannot be written as NL VCCSs, and they cannot accommodate circuits with cutsets composed entirely of current sources (including NL VCCSs). In this paper we generalize independent and dependent variable choice at the root of WDF trees to accommodate both these cases, and review two graph theorems for avoiding forbidden cutsets and loops in general.

### 1. INTRODUCTION

Along with State Space Modeling [1–4] and Port Hamiltonian Systems [5–8], the *Wave Digital Filter* (WDF) [9–15] formalism is a major approach to Virtual Analog modeling of audio circuits. In short, the Wave Digital Filter approach reframes an electrical circuit into a tree-like structure that separates electrical elements from their topological connections, represents each electrical element and topological connection mathematically with explicit input–output relationships in the (typically voltage or power) wave domain, discretizes reactive elements (most commonly using the trapezoidal rule), and resolves delay-free loops in the resulting structure by tuning the port resistance parameter of the wave variable definition at each port in the circuit. For circuits built entirely out of series and parallel connections, this approach is entirely modular. Good numerical behavior and incremental passivity can normally be inherited from passivity of the reference circuit and the use of wave variables [16]. The original WDF formalism could accommodate a single nonlinear electrical element at the root of the WDF tree [17]; since typical audio circuits rather contain multiple nonlinear devices, handling multiple nonlinearities is currently a main subject of WDF research. Three recent approaches to handling multiple nonlinearities involve the resolution of fictitious delays in non-tree-like structures using techniques from multidimensional signal processing with convergence guaranteed in some cases by the contractive properties of passive circuit elements [18–21], “dynamic adaptation” of one-port nonlinearities which are not at the root [22], or global iterative solution over a WDF structure [23].

In this paper, we’ll deal with another recent thread in WDF research starting with [24] that is focused on solving the scattering matrices of complicated “ $\mathcal{R}$ -type” adaptors [11] and the application of the topological insights of [25] (decomposition of a circuit graph into an SPQR tree) to generalized formulations for circuits involving multiple nonlinearities [12, 13]. This approach groups all

nonadaptable elements (most importantly nonlinearities) together at the root of a WDF tree<sup>1</sup> and interfaces that multiport root element to standard WDF subtrees using an  $\mathcal{R}$ -type adaptor. Representing the mathematical relationships in this structure directly causes a number of delay-free loops in the signal flow graph, which may be resolved by a variety of methods.

Findings from this thread have enabled WDF simulation of circuits with complicated non-series/parallel topologies that may involve absorbed multiport linear elements [11] as well as multiple non-adaptable linear circuit elements [15] or nonlinear elements [12] grouped together at the root of a tree structure. These include audio circuits that were previously out of scope for WDF modeling: guitar tone stacks, active tone control circuits [11], the Hammond organ vibrato/chorus [15], circuits using operational amplifiers (modeled as ideal or using macromodels) [14] or operational transconductance amplifiers [27], Sallen–Key filters [28, 29], guitar distortion stages [12], transistor [13] and triode [30] amplifiers, the Fender 5F6-A preamp stage [31], the Korg MS-50 Filter [32], relaxation oscillators [33], and the bass drum circuit from the Roland TR-808 Rhythm Composer [34].

However, two classes of circuits which may appear to be handled by those techniques on a topological level actually fail for reasons related to the choice of independent and dependent variables in the constituent equations of the circuits’ nonlinear devices. The first class of circuits involves nonlinear devices whose constituent equations are inherently written in a way that is incompatible with the previous WDF formulation [12]. The second class of circuits involves forbidden topological combinations of nonlinear devices with a certain mathematical description and ideal sources. Specifically these are circuits involving:

1. cutsets on the circuit graph composed entirely of nonlinearities with current as the dependent variable and ideal independent or controlled current sources; or
2. loops on the circuit graph composed entirely of nonlinearities with voltage as the dependent variable and ideal independent or controlled voltage sources.

These restrictions also apply in the context of State Space and Port Hamiltonian System modeling. In the State Space context, it is acknowledged that any node with only nonlinearities attached creates an inconsistent system if they are treated as controlled current sources, motivating the development of the Generalized State Space approach [4]. This is a special case of the restriction that a circuit may not contain any cutsets composed entirely of devices with current as the dependent variable. In the Port Hamiltonian System context, “implicit” formulations which in practice corre-

<sup>1</sup> Similar to [26], although allowing root topologies other than parallel.

spond to series combinations of voltage-controlled (controlled current) components or parallel combinations of current-controlled (controlled voltage) components require extensions to the standard approach [6]. These appear to be two special cases of the cutset and loop restrictions respectively. It is possible that the broader topological restrictions may not be widely recognized in audio circuit modeling since the most common problematic arrangement of diodes—series combinations of diodes and anti-parallel combinations of diodes in series—can be reasonably and intuitively modeled as a single one-port device in many circumstances [35].

In this paper, we extend a WDF formalism involving grouped nonlinearities at the root of an SPQR tree [11–13] to accommodate a wider variety of independent–dependent variable descriptions of nonlinear elements, enabling simulation of the two problematic classes of circuits mentioned above. For the first class of circuits, we exploit the proposed generalization to accommodate whatever pair of independent–dependent variables is required for each nonlinearity. For the second class of circuits, we explain the meaning of the forbidden topological connections and variable choices in terms of graph and network theory, give principles for choosing proper independent–dependent variable pairs, and show how to implement these principles using the proposed generalization. In this way, the class of problematic circuits which have been accommodated in the State Space and Port Hamiltonian context may be accommodated in the Wave Digital Filter context as well.

The rest of the paper is structured as follows. §2 outlines the proposed generalization to the WDF approach. §3 explains the first problematic class of circuits and how they can be accommodated using the proposed generalization. §4 explains the second problematic class of circuits and how they can be accommodated using the proposed generalization. To support a general search for problematic cutsets and loops, §5 reviews two graph theorems.

## 2. WDFS WITH GROUPED NONLINEARITIES

In this section we review the method of grouped nonlinearities in WDFs, simultaneously extending it to handle nonlinearities and nonadaptable linear circuit elements expressed with a wide variety of independent and dependent variables.

### 2.1. Overview

The method of grouped nonlinearities in WDFs is outlined diagrammatically in Fig. 1. In this formulation there are five conceptual relationships to consider:

- All nonlinearities of the circuit grouped together into a nonlinear multiport element at the root of a tree structure (labeled “nonlinearities”). The behavior of the group of nonlinearities is expressed mathematically by  $\mathbf{y}_c = \mathbf{f}(\mathbf{x}_c)$ , where  $\mathbf{x}_c$  is a vector of independent network port variables and  $\mathbf{y}_c$  is a vector of dependent network port variables.
- A change of variables  $\mathbf{x}_c$  and  $\mathbf{y}_c$  to the vectors of incident and reflected voltage waves  $\mathbf{a}_c$  and  $\mathbf{b}_c$  (labeled “change of variables”), the subscript  $c$  denoting “converter.”<sup>2</sup> This change of variables is expressed mathematically by the matrix  $\mathbf{C}$  with partitions  $\mathbf{C}_{11}$ ,  $\mathbf{C}_{12}$ ,  $\mathbf{C}_{21}$ , and  $\mathbf{C}_{22}$ .
- A compatibility relationship between  $\mathbf{a}_c$  and  $\mathbf{b}_c$  and “internal” port wave variables  $\mathbf{a}_i$  and  $\mathbf{b}_i$ , simply enforcing port

<sup>2</sup>This relates to earlier approaches to interfacing State Space and WDF systems [36].

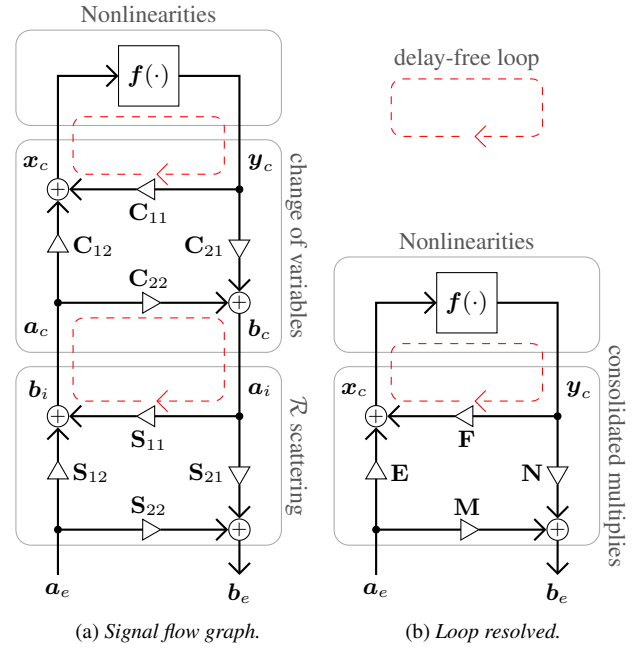


Figure 1: Proposed method signal flow graphs.  $\mathbf{a}_e$  is supplied by and  $\mathbf{b}_e$  delivered to classical WDF subtrees below.

connection criteria between the scattering matrix below and the multiport nonlinear element  $\mathbf{y}_c = \mathbf{f}(\mathbf{x}_c)$ . This is expressed mathematically by  $\mathbf{a}_c = \mathbf{b}_i$  and  $\mathbf{a}_i = \mathbf{b}_c$ .

- Scattering between  $\mathbf{a}_i$  and  $\mathbf{b}_i$  and “external” port wave variables  $\mathbf{a}_e$  and  $\mathbf{b}_e$ . This is expressed mathematically by the scattering matrix  $\mathbf{S}$  with partitions  $\mathbf{S}_{11}$ ,  $\mathbf{S}_{12}$ ,  $\mathbf{S}_{21}$ , and  $\mathbf{S}_{22}$ . Because the circuit topology described by this scattering is usually a complicated  $\mathcal{R}$ -type topology [25], this is labeled “ $\mathcal{R}$  scattering.”
- The rest of the WDF structure which is fed reflected waves  $\mathbf{b}_e$  by the root topology and provides incident waves  $\mathbf{a}_e$ . The rest of the structure has the form of a standard WDF “connection tree” [11, 37] and is not shown in the diagram.

These relationships are shown as a vector signal flow graph in Fig. 1a, where delay-free loops are represented by red dashed arrows. The root is described by the system of equations

$$\begin{aligned} \text{Nonlinearities} & \quad \left\{ \begin{aligned} \mathbf{y}_c &= \mathbf{f}(\mathbf{x}_c) \end{aligned} \right. & (1) \\ \text{change of variables} & \quad \left\{ \begin{aligned} \mathbf{x}_c &= \mathbf{C}_{11}\mathbf{y}_c + \mathbf{C}_{12}\mathbf{a}_c \\ \mathbf{b}_c &= \mathbf{C}_{21}\mathbf{y}_c + \mathbf{C}_{22}\mathbf{a}_c \end{aligned} \right. & (2) \\ \text{compatibility} & \quad \left\{ \begin{aligned} \mathbf{a}_c &= \mathbf{b}_i \\ \mathbf{a}_i &= \mathbf{b}_c \end{aligned} \right. & (4) \\ \text{scattering} & \quad \left\{ \begin{aligned} \mathbf{b}_i &= \mathbf{S}_{11}\mathbf{a}_i + \mathbf{S}_{12}\mathbf{a}_e \\ \mathbf{b}_e &= \mathbf{S}_{21}\mathbf{a}_i + \mathbf{S}_{22}\mathbf{a}_e \end{aligned} \right. & (6) \end{aligned}$$

Some of the delay-free loops can be resolved using matrix algebra [11], yielding a consolidated version of (1)–(7)

$$\begin{aligned} \mathbf{y}_c &= \mathbf{f}(\mathbf{x}_c) & (8) \\ \mathbf{x}_c &= \mathbf{E}\mathbf{a}_e + \mathbf{F}\mathbf{y}_c & (9) \\ \mathbf{b}_e &= \mathbf{M}\mathbf{a}_e + \mathbf{N}\mathbf{y}_c & (10) \end{aligned}$$

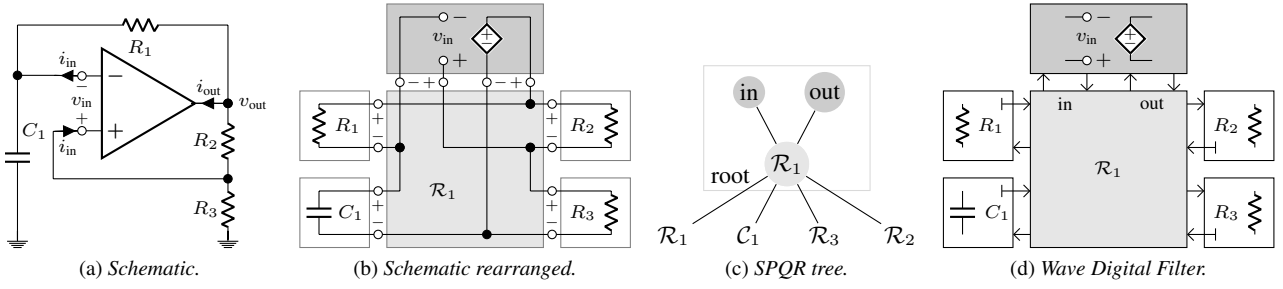


Figure 2: Relaxation oscillator schematic and derivation of Wave Digital Filter structure.

with

$$\begin{aligned} \mathbf{E} &= \mathbf{C}_{12}(\mathbf{I} + \mathbf{S}_{11}\mathbf{H}\mathbf{C}_{22})\mathbf{S}_{12}, & \mathbf{F} &= \mathbf{C}_{12}\mathbf{S}_{11}\mathbf{H}\mathbf{C}_{21} + \mathbf{C}_{11} \\ \mathbf{M} &= \mathbf{S}_{21}\mathbf{H}\mathbf{C}_{22}\mathbf{S}_{12} + \mathbf{S}_{22}, & \mathbf{N} &= \mathbf{S}_{21}\mathbf{H}\mathbf{C}_{21} \end{aligned}$$

where  $\mathbf{I}$  is the identity matrix and  $\mathbf{H} = (\mathbf{I} - \mathbf{C}_{22}\mathbf{S}_{11})^{-1}$ . This system of equations is shown as a vector signal flow graph in Fig. 1b; notice that one delay-free loop through  $\mathbf{F}$  and  $\mathbf{f}(\cdot)$  still remains. This delay-free loop can be resolved, e.g., by Newton–Raphson iteration [13], table lookup / the K method [12, 38], custom nonlinear solvers [33], or a final matrix inversion in the case that all nonadaptable elements are linear [15].

## 2.2. Populating $\mathbf{S}$

To use the method just outlined, matrices  $\mathbf{S}$  and  $\mathbf{C}$  must be populated.  $\mathbf{S}$  can be found using the techniques of [11], which applies Modified Nodal Analysis [39] to the  $\mathcal{R}$ -type topology where instantaneous Thévenin equivalents represent the incident wave at each port, combining with the WDF wave definition to solve for  $\mathbf{S}$ . If the  $\mathcal{R}$ -type adaptor contains no absorbed non-reciprocal elements, the method of [40] may be used to solve for  $\mathbf{S}$ .

## 2.3. New Considerations for $\mathbf{C}$

In previous work, the nonadaptable root elements were usually modeled in the Kirchhoff domain by  $i = \mathbf{f}(v)$ .<sup>3</sup> This aligns with standard models for common electrical elements like diodes (Shockley model), BJT transistors (Ebers–Moll model), and triodes. So, the derivation of the  $\mathbf{C}$  matrix assumed these Kirchhoff variables were to be converted to the wave variables  $a_c$  and  $b_c$ .

In this work, we generalize that approach so that each entry in the vector of independent ( $x_c$ ) and dependent ( $y_c$ ) root variables may be a voltage, current, or wave variable. These may be “mixed and matched” in two senses. First, it is not required that each nonlinear element have the same independent nor dependent variables. Second, it is possible to have, e.g., a Kirchhoff variable as an independent variable and a wave variable as a dependent variable (provided this still represents a single-valued function). It should be obvious that the independent and dependent variables at any port may not be linear combinations of one another.

In general, the relationship between the incident wave  $a_n$  and reflected wave  $b_n$  at a port  $n$  and two other variables which may

 Table 1:  $t_{11,n}$ ,  $t_{12,n}$ ,  $t_{21,n}$ ,  $t_{22,n}$  for different dependent and independent variables at a port  $n$ .

	independent variable		dependent variable		
$x_n$	$t_{11,n}$	$t_{12,n}$	$y_n$	$t_{21,n}$	$t_{22,n}$
$v_n$	1/2	1/2	$i_n$	1/(2R <sub>n</sub> )	-1/(2R <sub>n</sub> )
$i_n$	1/(2R <sub>n</sub> )	-1/(2R <sub>n</sub> )	$v_n$	1/2	1/2
$a_n$	1	0	$b_n$	0	1

be linear combinations of  $a_n$  and  $b_n$  is expressed by

$$\begin{bmatrix} x_n \\ y_n \end{bmatrix} = \begin{bmatrix} t_{11,n} & t_{12,n} \\ t_{21,n} & t_{22,n} \end{bmatrix} \begin{bmatrix} a_n \\ b_n \end{bmatrix}. \quad (11)$$

Solving for  $x_n$  and  $b_n$  yields an equation in the form of  $\mathbf{C}$

$$\begin{bmatrix} x_n \\ b_n \end{bmatrix} = \begin{bmatrix} c_{11,n} & c_{12,n} \\ c_{21,n} & c_{22,n} \end{bmatrix} \begin{bmatrix} y_n \\ a_n \end{bmatrix}, \quad (12)$$

where

$$\begin{bmatrix} c_{11,n} & c_{12,n} \\ c_{21,n} & c_{22,n} \end{bmatrix} = \begin{bmatrix} t_{12,n} & t_{11,n}t_{22,n} - t_{12,n}t_{21,n} \\ \frac{t_{22,n}}{1} & -\frac{t_{21,n}}{t_{22,n}} \end{bmatrix}. \quad (13)$$

The matrix partitions  $\mathbf{C}_{11}$ ,  $\mathbf{C}_{12}$ ,  $\mathbf{C}_{21}$ ,  $\mathbf{C}_{22}$  of  $\mathbf{C}$  are typically diagonal, with “stamps” along the diagonals determined by the independent and dependent variables of each nonlinearity. For a root topology with  $N$  nonlinearities they take the form

$$\mathbf{C}_{11} = \text{diag}(c_{11,1}, c_{11,2}, \dots, c_{11,N}) \quad (14)$$

$$\mathbf{C}_{12} = \text{diag}(c_{12,1}, c_{12,2}, \dots, c_{12,N}) \quad (15)$$

$$\mathbf{C}_{21} = \text{diag}(c_{21,1}, c_{21,2}, \dots, c_{21,N}) \quad (16)$$

$$\mathbf{C}_{22} = \text{diag}(c_{22,1}, c_{22,2}, \dots, c_{22,N}), \quad (17)$$

with entries given in terms of  $x_n, y_n$  for each port  $n$  by (13).

Values for  $t_{11}$ ,  $t_{12}$ ,  $t_{21}$ ,  $t_{22}$  entries that accommodate voltage, current, and incident and reflected waves are given in Tab. 1.

## 2.4. New Considerations for $\mathbf{f}(\cdot)$

The  $\mathbf{E}$ ,  $\mathbf{M}$ , and  $\mathbf{N}$  matrix multiplies in Fig. 1b can be computed with no special considerations. However, the  $\mathbf{F}$  matrix multiply and evaluation of the  $\mathbf{f}(\cdot)$  vector nonlinear function evaluation form a delay-free loop, or implicit relationship. These can be combined into a zero-finding function

$$\mathbf{x}_c = \mathbf{E}\mathbf{a}_e + \mathbf{F}\mathbf{f}(\mathbf{x}_c) \rightarrow \mathbf{h}(\mathbf{x}_c) = \mathbf{E}\mathbf{a}_e + \mathbf{F}\mathbf{f}(\mathbf{x}_c) - \mathbf{x}_c. \quad (18)$$

<sup>3</sup>In [15], they were modeled in the wave domain as  $\mathbf{b} = \mathbf{f}(\mathbf{a})$ .

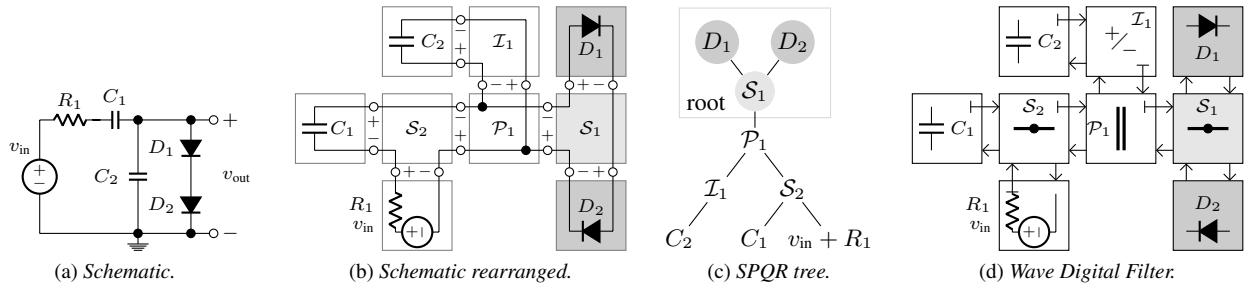


Figure 3: Series clipper schematic and derivation of Wave Digital Filter structure.

 Table 2: Determinant of  $(\mathbf{I} - \mathbf{C}_{22}\mathbf{S}_{11})$  for different variable choices for series clipper (Fig. 3).  $\Gamma = R_1 + R_2 + R_3$ .

		port 2 variables: $x_2 \rightarrow y_2$						
		$v_2 \rightarrow i_2$	$v_2 \rightarrow b_2$	$i_2 \rightarrow v_2$	$i_2 \rightarrow b_2$	$a_2 \rightarrow v_2$	$a_2 \rightarrow i_2$	$a_2 \rightarrow b_2$
port 1 variables: $x_1 \rightarrow y_1$	$v_1 \rightarrow i_1$	0	$2R_1/\Gamma$	$4R_1/\Gamma$	$2R_1/\Gamma$	$4R_1/\Gamma$	0	$2R_1/\Gamma$
	$v_1 \rightarrow b_1$	$2R_2/\Gamma$	1	$2(R_1 + R_3)/\Gamma$	1	$2(R_1 + R_3)/\Gamma$	$2R_2/\Gamma$	1
	$i_1 \rightarrow v_1$	$4R_2/\Gamma$	$2(R_2 + R_3)/\Gamma$	$4R_3/\Gamma$	$2(R_2 + R_3)/\Gamma$	$4R_3/\Gamma$	$4R_2/\Gamma$	$2(R_2 + R_3)/\Gamma$
	$i_1 \rightarrow b_1$	$2R_2/\Gamma$	1	$2(R_1 + R_3)/\Gamma$	1	$2(R_1 + R_3)/\Gamma$	$2R_2/\Gamma$	1
	$a_1 \rightarrow v_1$	$4R_2/\Gamma$	$2(R_2 + R_3)/\Gamma$	$4R_3/\Gamma$	$2(R_2 + R_3)/\Gamma$	$4R_3/\Gamma$	$4R_2/\Gamma$	$2(R_2 + R_3)/\Gamma$
	$a_1 \rightarrow i_1$	0	$2R_1/\Gamma$	$4R_1/\Gamma$	$2R_1/\Gamma$	$4R_1/\Gamma$	0	$2R_1/\Gamma$
	$a_1 \rightarrow b_1$	$2R_2/\Gamma$	1	$2(R_1 + R_3)/\Gamma$	1	$2(R_1 + R_3)/\Gamma$	$2R_2/\Gamma$	1

$\mathbf{h}(\mathbf{x}_c) = \mathbf{0}$  is solved (i.e., finding a suitable  $\mathbf{x}_c$ ) using Newton–Raphson iteration [13] by first providing an initial guess  $\mathbf{x}_c^{(0)}$  and iterating according to

$$\mathbf{x}_c^{(k+1)} = \mathbf{x}_c^{(k)} - \mathbf{J}(\mathbf{x}_c^{(k)})^{-1} \mathbf{f}(\mathbf{x}_c^{(k)}) \quad (19)$$

where index  $k$  is the iteration count and  $\mathbf{J}(\cdot)$  is the Jacobian operator. A typical initial guess at time step  $n$  is  $\mathbf{x}_c^{(0)}(n) = \mathbf{x}_c(n-1)$ ; an alternative is given in [13].

Given a set of incident waves  $\mathbf{a}_e$  on the root, (18) can be solved using Newton–Raphson iteration [13] to yield  $\mathbf{x}_c$ .  $\mathbf{y}_c = \mathbf{f}(\mathbf{x}_c)$  is evaluated to find  $\mathbf{y}_c$ , and  $\mathbf{y}_c$  and  $\mathbf{a}_e$  are finally used to find  $\mathbf{b}_e$ .

In the new generalized framework, elements of the vectors of independent root variables  $\mathbf{x}_c$  and dependent root variables  $\mathbf{y}_c$  may be voltages, currents, or any linear combination. Earlier we discussed the implications of that for forming  $\mathbf{C}$ . Of course, this also affects the definition of  $\mathbf{f}(\cdot)$ .

### 3. FIRST CLASS OF PROBLEMATIC CIRCUITS

The first class of circuits that require the generalization presented in this paper are those circuits whose constituent equations are written in a way that cannot be rewritten in the form  $\mathbf{i}_c = \mathbf{f}(\mathbf{v}_c)$ . These include, e.g., clipping operational amplifier models, clipping operational transconductance amplifier models, analog multipliers, logic gate models, and one-ports with non-functional  $v$ - $i$  curves, e.g. “s-type” nonlinear one-ports [41].

#### 3.1. Example of First Class

As an example, we consider the family of clipping operational amplifiers (op amp) models. Op amps are two-port devices character-

ized by four network variables:  $v_{in}$ ,  $i_{in}$ ,  $v_{out}$ , and  $i_{out}$ . In some circuits, op amps may exhibit non-ideal voltage clipping behavior, which may be modeled with a  $\tanh(\cdot)$ -based function [4]. In some circuits op amps are configured to act as voltage comparators, which may be modeled with a  $\text{sgn}(\cdot)$ -based function. As nonlinear two-ports, op amps are modeled by

$$\begin{bmatrix} v_{out} \\ i_{in} \end{bmatrix} = \begin{bmatrix} f_1(i_{out}, v_{in}) \\ f_2(i_{out}, v_{in}) \end{bmatrix} = \mathbf{f} \left( \begin{bmatrix} i_{out} \\ v_{in} \end{bmatrix} \right). \quad (20)$$

Typically we have  $f_2(i_{out}, v_{in}) = 0$ , but  $f_1(i_{out}, v_{in})$  can take a number of forms, e.g.

$$\text{clipper: } v_{out} = V_{\max} \tanh(Av_{in}) \quad (21)$$

$$\text{comparator: } v_{out} = V_{\max} \text{sgn}(v_{in}), \quad (22)$$

where  $A$  is the op amp’s gain in the clipper model (100000 is typical) and  $V_{\max}$  is the op amp saturation voltage in each model.

An example taken from [33] of an audio circuit using an op amp configured as a comparator is a relaxation oscillator, shown in Fig. 2a. This circuit is rearranged as shown in Fig. 2b, yielding the WDF structure in Fig. 2d. The two ports of the nonlinearity are labeled “in” and “out.” The input variables  $\mathbf{x}_c$  and output variables  $\mathbf{y}_c$  are defined as in (20). To accommodate this set of independent and dependent variables which are necessary for the op amp models just discussed we derive

$$\begin{aligned} t_{11,\text{out}} &= \frac{1}{2R_{\text{out}}}, & t_{12,\text{out}} &= \frac{-1}{2R_{\text{out}}}, & t_{21,\text{out}} &= \frac{1}{2}, & t_{22,\text{out}} &= \frac{1}{2} \\ t_{11,\text{in}} &= \frac{1}{2}, & t_{12,\text{in}} &= \frac{1}{2}, & t_{21,\text{in}} &= \frac{1}{2R_{\text{in}}}, & t_{22,\text{in}} &= \frac{-1}{2R_{\text{in}}} \end{aligned}$$

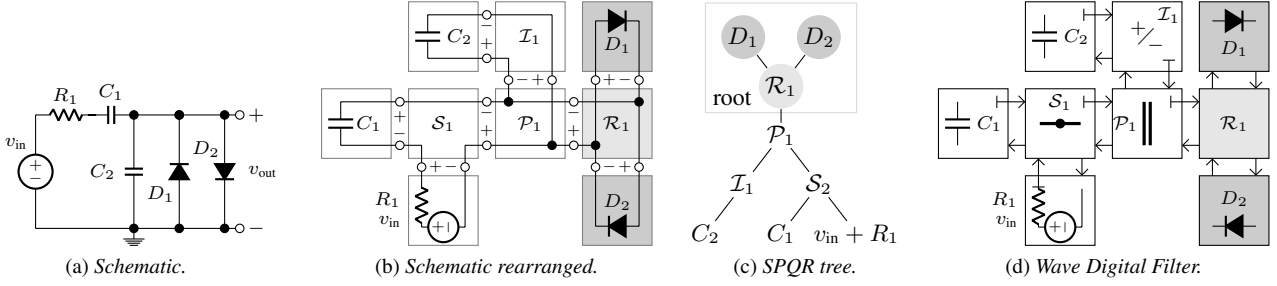


Figure 4: Parallel clipper schematic and Derivation of Wave Digital Filter structure.

 Table 3: Determinant of  $(\mathbf{I} - \mathbf{C}_{22}\mathbf{S}_{11})$  for different variable choices for parallel clipper (Fig. 4).  $\Delta = G_1 + G_2 + G_3$  and  $G_x = 1/R_x$ .

		port 2 variables: $x_2 \rightarrow y_2$						
		$v_2 \rightarrow i_2$	$v_2 \rightarrow b_2$	$i_2 \rightarrow v_2$	$i_2 \rightarrow b_2$	$a_2 \rightarrow v_2$	$a_2 \rightarrow i_2$	$a_2 \rightarrow b_2$
port 1 variables: $x_1 \rightarrow y_1$	$v_1 \rightarrow i_1$	$4G_3/\Delta$	$2(G_2 + G_3)/\Delta$	$4G_2/\Delta$	$2(G_2 + G_3)/\Delta$	$4G_2/\Delta$	$4G_3/\Delta$	$2(G_2 + G_3)/\Delta$
	$v_1 \rightarrow b_1$	$2(G_1 + G_3)/\Delta$	1	$2G_2/\Delta$	1	$2G_2/\Delta$	$2(G_1 + G_3)/\Delta$	1
	$i_1 \rightarrow v_1$	$4G_1/\Delta$	$2G_1/\Delta$	0	$2G_1/\Delta$	0	$4G_1/\Delta$	$2G_1/\Delta$
	$i_1 \rightarrow b_1$	$2(G_1 + G_3)/\Delta$	1	$2G_2/\Delta$	1	$2G_2/\Delta$	$2(G_1 + G_3)/\Delta$	1
	$a_1 \rightarrow v_1$	$4G_1/\Delta$	$2G_1/\Delta$	0	$2G_1/\Delta$	0	$4G_1/\Delta$	$2G_1/\Delta$
	$a_1 \rightarrow i_1$	$4G_3/\Delta$	$2(G_2 + G_3)/\Delta$	$4G_2/\Delta$	$2(G_2 + G_3)/\Delta$	$4G_2/\Delta$	$4G_3/\Delta$	$2(G_2 + G_3)/\Delta$
	$a_1 \rightarrow b_1$	$2(G_1 + G_3)/\Delta$	1	$2G_2/\Delta$	1	$2G_2/\Delta$	$2(G_1 + G_3)/\Delta$	1

using the stamps from Tab. 1 and procedure from §2.3. Using (13) this yields the appropriate  $\mathbf{C}$  matrix

$$\mathbf{C} = \begin{bmatrix} \mathbf{C}_{11} & \mathbf{C}_{12} \\ \mathbf{C}_{21} & \mathbf{C}_{22} \end{bmatrix} = \begin{bmatrix} -R_{\text{in}} & 0 & 1 & 0 \\ 0 & -1/R_{\text{out}} & 0 & 1/R_{\text{out}} \\ -2R_{\text{in}} & 0 & 1 & 0 \\ 0 & 2 & 0 & -1 \end{bmatrix}.$$

This choice of  $\mathbf{C}$  in the proposed general framework enables the simulation of the relaxation oscillator.<sup>4</sup>

#### 4. SECOND CLASS OF PROBLEMATIC CIRCUITS

A second class of circuits that require the generalization presented in this paper are circuits that include cutsets composed entirely of nonlinearities (and current sources). In circuit theory, it is forbidden to have any cutset in a circuit graph composed entirely of current sources [41]. The presence of a cutset of current sources in a circuit creates the potential for a violation of Kirchhoff’s current law: the sum of currents entering a node must equal the sum of currents leaving that node. A dual restriction is that no loop in a circuit graph may be composed entirely of voltage sources [41]. The presence of a loop of all voltage sources creates the potential for a violation of Kirchhoff’s voltage law: the sum of voltages around any loop in the circuit must equal zero. This is a circuit theoretic argument but it is also expressed in the mathematics of the root topology. In the case of violating either the loop or the cutset criteria, it appears that in the WDF context the consequence is that the matrix  $(\mathbf{I} - \mathbf{C}_{22}\mathbf{S}_{11})$  which needs to be inverted is made singular. Examples will be given in the next section.

<sup>4</sup>Anti-aliasing and multi-rate methods can be used to improve the simulation of the relaxation oscillator; these are described in Olsen *et al.* [33].

To fix this class of circuit, start with the standard choice of independent and dependent network variables for each nonlinearity. Identify each loop and cutset in the circuit by hand or using the graph theorems discussed in §5. If any problematic cutsets or loops exist, choose new dependent variables for some of the nonlinearities that make up that cutset or loop to avoid the issue.

#### 4.1. Examples of Second Class

To discuss these issues, we consider three circuits: the “series diode clipper” shown in Fig. 3a, the “parallel diode clipper” shown in Fig. 4a, and the “series–parallel diode clipper” shown in Fig. 5.

Consider the series diode clipper and its WDF structure derivation shown in Fig. 3. Notice that inside the root topology  $\mathcal{S}_1$  in Fig. 3b, we have a node with only diodes connected to it. If the diodes were written in the form  $i = f(v)$ , a current-source-only cutset is created. A remedy for this circuit would be to write either or both of the diodes in the form  $v = f(i)$ , or more broadly in any form that does not have current as the dependent variable. In Tab. 2, the determinant of matrix  $(\mathbf{I} - \mathbf{C}_{22}\mathbf{S}_{11})$  is shown for the 49 different possible choices of  $x_n$  and  $y_n$  at port 1 (diode  $D_1$ ) and port 2 (diode  $D_2$ ). Notice that for the combinations that are forbidden according to circuit theory (both diodes with current as the dependent variable), the matrix which needs to be inverted becomes singular (its determinant is 0)—hence the circuit cannot be simulated using those variables.

It is not always a valid solution to choose voltage as the dependent variable. Consider the parallel diode clipper and its WDF structure derivation shown in Fig. 4. Notice that inside the root topology  $\mathcal{R}_1$  in Fig. 4b there is a loop composed only of diodes. If the diodes were both written in the form  $v = f(i)$ , a voltage-source-only loop is created,  $(\mathbf{I} - \mathbf{C}_{22}\mathbf{S}_{11})$  becomes singular, and

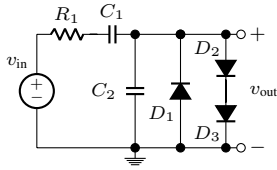


Figure 5: Series-parallel clipper schematic.

the circuit cannot be simulated. For this circuit, it suffices that one or both diodes is written in the form  $i = f(v)$ , or more broadly in any form that does not have voltage as the dependent variable. In Tab. 3, the determinant of matrix  $(\mathbf{I} - \mathbf{C}_{22}\mathbf{S}_{11})$  is shown for the 49 different possible choices of  $\mathbf{x}_n$  and  $\mathbf{y}_n$  at port 1 (diode  $D_1$ ) and port 2 (diode  $D_2$ ). Notice that for the combinations that are forbidden according to circuit theory (both diodes with voltage as the dependent variable), the matrix which needs to be inverted becomes singular (its determinant is 0)—hence the circuit cannot be simulated using those variables.

Sometimes it is necessary to choose different variables for each nonlinearity. For example, consider the series-parallel diode clipper shown in Fig. 5. Writing all three diodes in the form  $i = f(v)$  creates a current-source-only cutset but writing all three diodes in the form  $v = f(i)$  creates a voltage-source-only loop: both forbidden cases causing a singular matrix. Here the solution is that at least one diode is written with current as the dependent variable to avoid the loop, and that at least one of  $D_2, D_3$  is written with voltage as the dependent variable to avoid the cutset.

## 5. ENUMERATING LOOPS AND CUTSETS ON GRAPHS

In the previous section we discussed circuits whose cutsets and loops were easily identifiable at a glance. Unfortunately in general circuits may be very complex and involve too many loops and cutsets to enumerate at a glance. To handle problematic circuits in general it is necessary to examine all loops and cutsets in the circuit graph and choose the dependent variables of the nonlinearities to avoid current-source-only cutsets and voltage-source-only loops. Here we review dual graph theorems for enumerating loops and cutsets in a graph (an alternative to identifying them by visual inspection as in the previous section) and demonstrate their application to two circuits discussed in §4.

### 5.1. Find All Loops in a Circuit

Here we review a theorem for enumerating the set of all loops in an electrical circuit and give example applications of the theorem for the parallel diode clipper.

The theorem is stated as follows [42, p. 50]:

1. Let the circuit be represented by a nonoriented, connected graph  $\mathcal{G}$  with  $v$  vertices and  $e$  edges, where each vertex represents a node in the circuit and each edge represents a one-port electrical element in the circuit.
2. Choose a tree  $\mathcal{T}$  on  $\mathcal{G}$ . Form a set of fundamental loops with respect to  $\mathcal{T}$  by reinstating each edge of the cotree  $\mathcal{T}'$  one at a time to create fundamental loops each involving one edge and a tree path formed by some or all of the branches of  $\mathcal{T}$ . The fundamental loops are represented mathematically by a matrix  $\mathbf{B}_f$  where each of the  $e - v + 1$  fundamental loops is a row, and the  $e$  edges of  $\mathcal{G}$  are the columns.

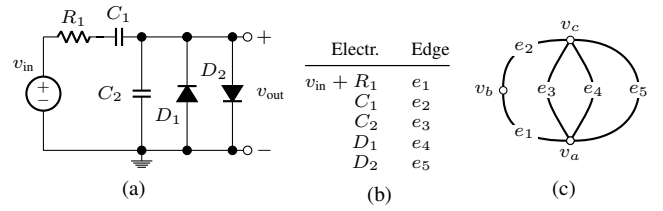


Figure 6: Parallel clipper (a) Schematic, (b) Mapping from circuit elements to graph edges, and (c) Graph.

3. Form an intermediate matrix  $\mathbf{B}_1$  by adding to  $\mathbf{B}_f$  all the possible ring sums among the rows of  $\mathbf{B}_f$ . The ring sum of two sets  $S_1$  and  $S_2$  is the set  $S_1 \oplus S_2$  that has edges in  $S_1$  or  $S_2$  but not both [42, p. 14].
4. Eliminate redundant rows in  $\mathbf{B}_1$ , i.e. rows that appear more than once, to form  $\mathbf{B}_a$ , the loop matrix encoding all valid loops on  $\mathcal{G}$ . Redundant rows represent edge-disjoint unions of loops [42, p. 44].

Now, an example on the parallel diode clipper will illustrate the application of this theorem.

#### 5.1.1. Parallel Diode Clipper Loops

Consider the parallel diode clipper whose schematic is shown in Fig. 6a. Using the mapping between electrical component and graph edges shown in Fig. 6b, a graph  $\mathcal{G}$  of the parallel clipper is formed in Fig. 6c.  $\mathcal{G}$  has 3 nodes  $\{v_a, v_b, v_c\}$  and 5 edges  $\{e_1, e_2, e_3, e_4, e_5\}$ , i.e.,  $v = 3$  and  $e = 5$ .

To enumerate all loops on  $\mathcal{G}$  we choose a tree  $\mathcal{T} = \{e_2, e_3\}$  and corresponding co-tree  $\mathcal{T}' : \{e_1, e_4, e_5\}$ . Combining each edge  $c \in \mathcal{T}'$  with other edges chosen from  $\mathcal{T}$  yields  $e - v + 1 = 3$  fundamental loops  $\{c_{e_1}, c_{e_4}, c_{e_5}\}$  encoded in a matrix  $\mathbf{B}_f$

$$\mathbf{B}_f = \begin{matrix} c_{e_1} \\ c_{e_4} \\ c_{e_5} \end{matrix} \begin{bmatrix} 1 & 1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 1 & 0 \\ 0 & 0 & 1 & 0 & 1 \end{bmatrix} \begin{matrix} c_1 \\ c_2 \\ c_3 \end{matrix}.$$

We take all possible ring sums among the rows of  $\mathbf{B}_f$  to find the intermediate matrix

$$\mathbf{B}_1 = \begin{matrix} c_{e_1} \\ c_{e_4} \\ c_{e_5} \\ c_{e_1} \oplus c_{e_4} \\ c_{e_1} \oplus c_{e_5} \\ c_{e_4} \oplus c_{e_5} \\ c_{e_1} \oplus c_{e_4} \oplus c_{e_5} \end{matrix} \begin{bmatrix} 1 & 1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 1 & 0 \\ 0 & 0 & 1 & 0 & 1 \\ 1 & 1 & 0 & 1 & 0 \\ 1 & 1 & 0 & 0 & 1 \\ 0 & 0 & 0 & 1 & 1 \\ \color{red}{-1} & \color{red}{-1} & \color{red}{-1} & \color{red}{-1} & \color{red}{-1} \end{bmatrix} \begin{matrix} c_1 \\ c_2 \\ c_3 \\ c_4 \\ c_5 \\ c_6 \\ \text{redundant} \end{matrix}.$$

The last ring sum represents an invalid loop, so it is discarded in forming  $\mathbf{B}_a$ . The final loop matrix  $\mathbf{B}_a$  and graphical representation of the six loops  $\{c_1, c_2, c_3, c_4, c_5, c_6\}$  is given by



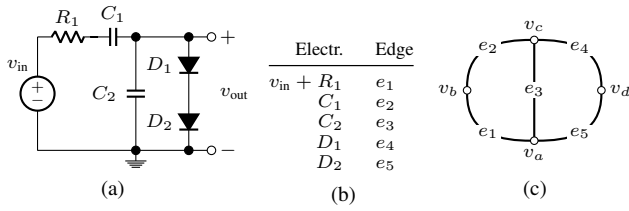
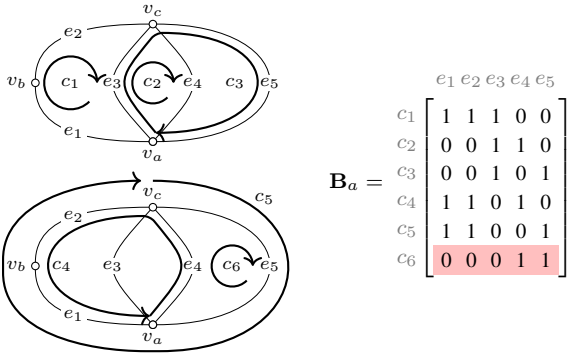


Figure 7: Series clipper (a) Schematic, (b) Mapping from circuit elements to graph edges, and (c) Graph.



The last loop  $c_6 = \{e_4, e_5\}$  would be composed entirely of voltage sources if diodes  $D_1$  and  $D_2$  (edges  $e_4$  and  $e_5$ ) are both modeled in the form  $v = f(i)$ , as we saw earlier in §4.

## 5.2. Find All Cutsets in a Circuit

Here we review a theorem for enumerating the set of all cutsets in an electrical circuit and give an example application of the theorem to a circuit discussed in §4: the series diode clipper.

The theorem is stated as follows [42, p. 58]:

1. Let the circuit be represented by a nonoriented, connected graph  $\mathcal{G}$  with  $v$  vertices and  $e$  edges.
2. Choose a tree  $\mathcal{T}$  on  $\mathcal{G}$ . Form a set of fundamental cutsets with respect to  $\mathcal{T}$  by removing each edge of the cotree  $\mathcal{T}'$  one at a time to create fundamental cutsets each involving one tree edge and some or all of the edges of  $\mathcal{T}'$ . The fundamental cutsets are represented mathematically by a matrix  $\mathbf{Q}_f$  where each of the  $v - 1$  fundamental cutsets is a row, and the  $e$  edges of  $\mathcal{G}$  are the columns.
3. Form an intermediate matrix  $\mathbf{Q}_1$  by adding to  $\mathbf{Q}_f$  all of the possible ring sums among the rows of  $\mathbf{Q}_f$ .
4. Eliminate redundant rows in  $\mathbf{Q}_1$  to form  $\mathbf{Q}_a$ , the *cutset matrix* encoding all valid cutsets on  $\mathcal{G}$ .

Now, an examples on the series diode clipper will illustrate the application of this theorem.

### 5.2.1. Series Diode Clipper Cutsets

Consider the series diode clipper whose schematic is shown in Fig. 7a. Using the mapping between electrical component and graph edges shown in Fig. 7b, a graph  $\mathcal{G}$  of the parallel clipper is formed in Fig. 7c.  $\mathcal{G}$  has 4 nodes  $\{v_a, v_b, v_c, v_d\}$  and 5 edges  $\{e_1, e_2, e_3, e_4, e_5\}$ , i.e.,  $v = 4$  and  $e = 5$ .

To enumerate all cutsets on  $\mathcal{G}$  we choose a tree  $\mathcal{T} = \{e_2, e_3, e_4\}$  and corresponding cotree  $\mathcal{T}' = \{e_1, e_5\}$ . Removing each edge  $k \in \mathcal{T}$  with other edges chosen from  $\mathcal{T}'$  yields  $v - 1 = 3$  fundamental cutsets  $\{k_{e_2}, k_{e_3}, k_{e_4}\}$  encoded in a matrix  $\mathbf{Q}_f$

$$\mathbf{Q}_f = \begin{matrix} & e_1 & e_2 & e_3 & e_4 & e_5 \\ \begin{matrix} k_{e_2} \\ k_{e_3} \\ k_{e_4} \end{matrix} & \begin{bmatrix} 1 & 1 & 0 & 0 & 0 \\ 1 & 0 & 1 & 0 & 1 \\ 0 & 0 & 0 & 1 & 1 \end{bmatrix} \end{matrix} \cdot \begin{matrix} k_1 \\ k_2 \\ k_3 \end{matrix}$$

We take all possible ring sums among the rows of  $\mathbf{Q}_f$  to find the intermediate matrix  $\mathbf{Q}_1$

$$\mathbf{Q}_1 = \begin{matrix} & e_1 & e_2 & e_3 & e_4 & e_5 \\ \begin{matrix} k_{e_2} \\ k_{e_3} \\ k_{e_4} \\ k_{e_2} \oplus k_{e_3} \\ k_{e_2} \oplus k_{e_4} \\ k_{e_3} \oplus k_{e_4} \\ k_{e_2} \oplus k_{e_3} \oplus k_{e_4} \end{matrix} & \begin{bmatrix} 1 & 1 & 0 & 0 & 0 \\ 1 & 0 & 1 & 0 & 1 \\ 0 & 0 & 0 & 1 & 1 \\ 0 & 1 & 1 & 0 & 1 \\ 1 & 1 & 0 & 1 & 1 \\ 1 & 0 & 1 & 1 & 0 \\ 0 & 1 & 1 & 1 & 0 \end{bmatrix} \end{matrix} \cdot \begin{matrix} k_1 \\ k_2 \\ k_3 \\ k_4 \\ k_5 \\ k_6 \\ k_7 \end{matrix}$$

There are no redundancies in  $\mathbf{Q}_1$ , so the final cutset matrix  $\mathbf{Q}_a$  and seven cutsets  $\{k_1, k_2, k_3, k_4, k_5, k_6, k_7\}$  are given by

$$\mathbf{Q}_a = \begin{matrix} & e_1 & e_2 & e_3 & e_4 & e_5 \\ \begin{matrix} k_1 \\ k_2 \\ k_3 \\ k_4 \\ k_5 \\ k_6 \\ k_7 \end{matrix} & \begin{bmatrix} 1 & 1 & 0 & 0 & 0 \\ 1 & 0 & 1 & 0 & 1 \\ 0 & 0 & 0 & 1 & 1 \\ 0 & 1 & 1 & 0 & 1 \\ 1 & 1 & 0 & 1 & 1 \\ 1 & 0 & 1 & 1 & 0 \\ 0 & 1 & 1 & 1 & 0 \end{bmatrix} \end{matrix}$$

The third cutset  $k_3 = \{e_4, e_5\}$  would be composed entirely of current sources if diodes  $D_1, D_2$  (edges  $e_4, e_5$ ) are both modeled in the form  $i = f(v)$ , i.e., the standard Shockley ideal diode law.

## 6. CONCLUSION

This paper extended the class of circuits that can be modeled using Wave Digital Filters with grouped nonlinearities at the root of a tree [11–15] by generalizing independent/dependent variable choice for nonlinearities. This accommodates nonlinear devices (e.g. clipping op amps) which require flexibility in variable choice as well as circuits with loops composed entirely of nonlinearities (and ideal voltage sources) or cutsets composed entirely of nonlinearities (and ideal current sources).

When possible, choosing reflected waves as the dependent variable for nonlinearities will avoid problematic loops and cutsets. A circuit theory interpretation of this is that voltage waves “look like” resistive voltage sources (Thévenin source) or equivalently resistive current sources (Norton sources) [11]. A Thévenin source will never contribute to a voltage-source-only loop since any loop involving the source will also involve its resistance, and a Norton source will never contribute to a current-source-only cutset since any cutset involving it will also involve its resistance.

Future work should explore the potential for root variable choice to have computational benefits. If there are any computational or



other benefits of flexibility in dependent variable choice for nonlinearities, the insights of this paper could be used in the other WDF formulations [18–23] which currently use wave variables only but also currently should not produce problematic cutsets or loops.

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