Development of novel low noise Switch-mode power supply designs for high fidelity audio power amplifiers

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Abstract

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Today, linear power supplies are widely used to provide the supply voltage rail to an audio amplifier and are considered bulky, inefficient and expensive due to the presence of various components. In particular, the typical requirements of linear designs call for physically large mains transformers, energy storage/filtering inductors and capacitors. This imposes a practical limit to the reduction of weight in audio power systems. In order to overcome these problems, Switch-mode Power Supplies (SMPS) incorporate high speed switching transistors that allow for much smaller power conversion and energy storage components to be employed. In addition the low power dissipation of the transistors in the saturated and off states results in higher efficiency, improved voltage regulation and excellent power factor ratings.

The primary aim of this research was to develop and characterize a novel low noise switch mode power supply for an audio power amplifier. In this thesis, I proposed a novel balancing technique to optimize the design of SMPS that elevate the performance of converter and help to enhance the efficiency of power supply through high speed switching transistors. In fact, the proposed scheme mitigates the noise considerably in various converter topologies through different mechanisms. To validate the proposed idea, the technique is applied to different converters e.g; PFC boost converter, flyback converter and full-bridge converter. The performance of audio amplifier is evaluated using designed SMPS to compare with existing linear power supply. On the basis of experimental results, the decision has been made that the proposed balanced SMPS solution is as good as linear solution. Due to novelty and universality of balancing technique, it can provide a new path for researchers in this field to utilize the SMPS in all other audio devices by further enhancing its efficiency and reducing system noise.

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List of Abbreviations and Acronyms

SMPS	Switch-mode power supply
LPS	Linear power supply
CM	Common mode
DM	Differential mode
MOSFETs	Metal-oxide semiconductor field-effect transistors
IGBTs	Insulated-gate bipolar transistors
THD	Total harmonic distortion
THD+N	Total harmonic distortion plus noise
EMI	Electromagnetic Interference
EMC	Electromagnetic Compatibility
EPC	Equivalent parallel capacitance
ESL	Equivalent series inductance
ESR	Equivalent series resistance
AEF	Active Electromagnetic filter
NP	Number of primary windings
NS	Number of secondary windings
PFC	Power factor correction
DCM	Discontinuous conduction mode
DCM	Continuous conduction mode
CRM	Critical conduction mode
LISN	Line impedance stabalization network
PWM	Pulse width modulation
RCF	Random carrier frequency
RPWM	Random pulse width modulation
EPC	Equivalent parallel capacitance
EPR	Equivalent parallel resistance

ZVS	Zero voltage switching
ZCS	Zero current switching
ZVZC	Zero voltage zero current switching
FFT	Fast fourier transform
SRC	Series resonant converter
PRC	Parallel resonant converter
SPRC	Series parallel resonant converter
PCB	Printed circuit board

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In the end, I would like to extend my gratitude to all those who helped and supported me towards the successful completion of this research project.

1 CHAPTER 1 INTRODUCTION

This thesis details a research project to develop novel low noise switch mode power supply designs for high fidelity audio power amplifiers.

1.1 Overview

The audio power amplifier is an electronic device which is used to amplify the audio signal in an audio system. The quality of an audio system is measured by the accuracy of reproduction of an audio signal. There are various methods to quantify the fidelity of audio systems based on the several measures such as frequency response, total harmonic distortion and noise (THD+N) (Self 2009). The frequency response measures the linearity (reproduction of audio signal without distortion) of an amplifier. It should be flat in the frequency range of human hearing (20Hz-20kHz) for a high end audio system. On the other hand, the THD is also an important factor to quantify the audio system because it measures the performance of an audio system which depends on accuracy of the reproduced audio signal. The THD+N should be less than the 0.1% for a high fidelity audio system (Duncan 1996).

The high fidelity performance of an audio system is limited as a result of the noise generated by the power supply which interfers with and distorts the audio signal. Currently, the linear type of power supply achieves the lowest harmonic distortion in an audio output stage. However, it is bulky, inefficient and expensive due to the necessity of various components. In particular, a relatively large power transformer is utilized in these power supplies to meet the large variation in load current resulting from typically large dynamic variations in sound level. Furthermore, these power supplies operate at the power line frequency of 50/60Hz which requires other components such as energy storage/filtering inductors and smoothing capacitors which are physically large at these operating frequencies. This imposes a practical limit on the achievable reduction of weight in audio power systems and the large components are costly. In order to overcome these limitations, Switch-mode Power Supplies (SMPS) which are able to operate at higher operational frequencies have been introduced as the power source in many types of electronic system. SMPS incorporate high speed switching transistors that allow for much smaller power conversion and energy storage components to be employed. In addition the low power dissipation of the transistors in the saturated and off states results in higher efficiency, improved voltage regulation and excellent power

factor ratings. However, due to the higher switching frequency used in SMPS, the rate of change of voltage (dv/dt) and current (di/dt) across the switching power transistors causes significant Electromagnetic interference (EMI) emission (Nagrial and Hellany 1999). Consequently unless extensive shielding is used, which is usually impractical in commercial products, the EMI noise interfers with the audio signal leading to distortion and a reduction in fidelity. Therefore, at the present time there exists a clear need for novel techniques to reduce the affect of EMI noise generated by a SMPS. Thus the principal aim of this research project is to investigate techniques for the design of low noise switch mode power supplies for audio power amplification.

1.2 Aims and Objectives

The primary aim of this research project is to investigate techniques for the design of low noise switch mode power supplies for audio power amplification. Whilst the use of SMPS in audio amplification is not novel in itself, the contribution will arise from design optimisation to achieve the lowest possible harmonic distortion (less than 0.1%) in the audio output stage (Duncan 1996). This will allow the Switch Mode Power Supplies to be used in the highest-fidelity audio systems such as those produced by the company collaborating with this research - Naim Audio.

It is important to emphasise that EMI noise reduction in SMPS for an audio amplifier cannot simply be achieved through additional filtering. The reason is that the normal amplitude transients that occur in music audio signals result in variations in load impedance which usually makes filter design too complicated and/or impractical. Therefore improved SMPS designs must provide alternative solutions to the noise production problem.

The principal research aim gives rise to a number of key research objectives:

- Propose a novel technique of internal EMI filter to cope with converter to mitigate noise internally.
- Review and analyse current research in the field.
- Develop a detailed understanding of the relevant background theory and knowledge of the international Electromagnetic Interference (EMI) regulatory requirements.

- Develop knowledge and skills in the methodical design and experimental evaluation of SMPS for audio power applications with emphasis on EMI noise reduction techniques.
- Understand how to translate SMPS designs into optimal printed circuit board layouts so as to minimise radiated, conducted and parasitically coupled noise.
- Understand and use appropriate experimental techniques to evaluate and characterise SMPS prototype designs.
- To critically review the project, draw key conclusions and identify limitations and scope for future work.

1.3 Outline of this thesis

This chapter introduces of the research project and states the aims and objectives of proposed investigation.

Chapter 2 Discusses the theoretical background relating to SMPS design, implementation and characterisation.

Chapter 3 Presents a comprehensive literature review of research topics relevant to this project.

Chapter 4 Describes the methodology used to develop the novel low noise SMPS designs and performance evaluation through simulation and bench characterisation.

Chapter 5 Presents the experimental results obtained from the performance evaluation of the new designs.

Chapter 6 A discussion of the results, conclusions and suggestions for the future research work.

References and appendices are presented at the end of this thesis.

2 CHAPTER 2 THEORETICAL BACKGROUND

2.1 Introduction

The basic block diagram of a SMPS is shown in figure 1. The initial stage is input rectification and filtering. Input voltage is typically rectified by a diode rectifier and then followed by a bulk storage capacitor. The fast power semiconductor switching devices such as power MOSFETs or BJTs are used to produce the high frequency square wave signal. This signal is then fed to the primary side of a high frequency transformer to isolate the source and load. In addition a suitable voltage magnitude can be obtained at the secondary side of transformer corresponding to the transformer turns ratio. This voltage is then rectified and filtered to obtain the output dc voltage. To obtain the regulated output voltage, the feedback circuit is designed to control the switching devices (Whittington et al. 1997).

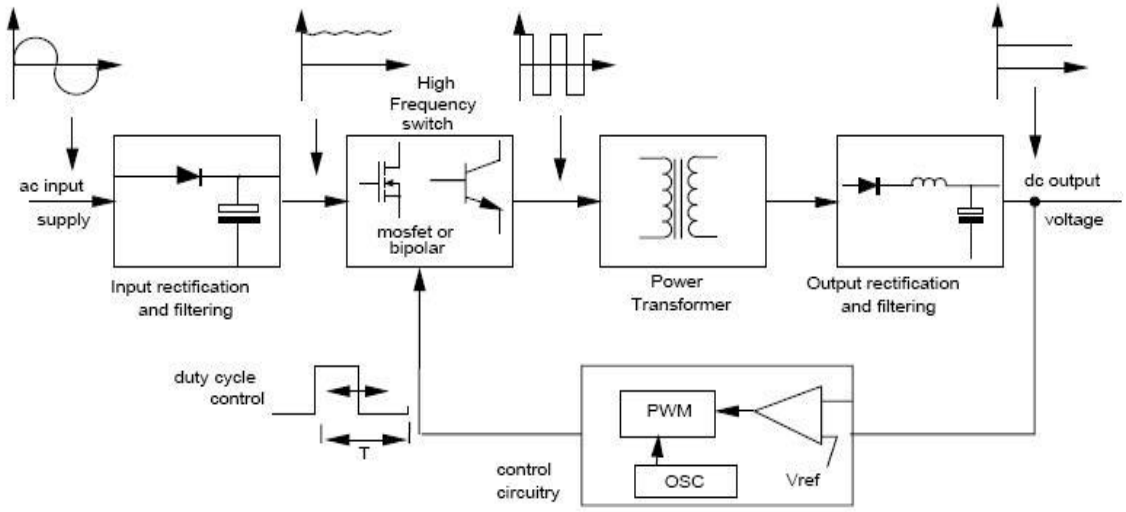


Figure 1 : Block Diagram of Switch mode Power Supply (Whittington et al. 1997)

There exist several topologies of SMPS each developed to fulfill the power supply requirements in various applications. In this chapter these different SMPS topologies are evaluated in order to identify the most suitable generic design for the current research project.

Topologies of SMPS can be classified into two major categories on the basis of isolation:

2.2 Non-Isolated SMPS

Which is typically further classified into two sub-types

2.2.1 Step-down (Buck) regulator

In this type of converter, the average output voltage is lower than the input voltage. (Mohan 2011). The basic topology of this converter is shown in figure 2.

In this topology the input voltage is switched at high frequency by placing the switch Q1 in series with the input voltage. During the steady state operation of the circuit, the operation can be divided into two timing intervals the ON time and the OFF time. During the ON time interval, the diode D1 is reverse biased and the circuit acts as a low pass LC filter. Also the input voltage is supplying the energy to the output through the inductor. The inductor is charged during this time interval. While, during the OFF time interval, the diode D1 is forward biased and the inductor acts as source to supply the power to the load RL through the diode.

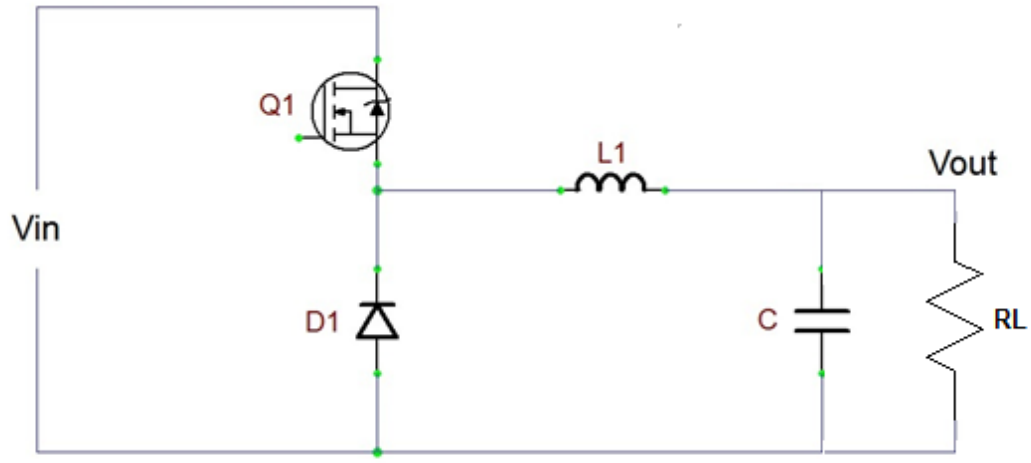


Figure 2: Step-down Converter

The equation to find the output voltage is given as

$$V_{OUT} = d \, . \, V_{IN} \quad (1)$$

$$d = \frac{T_{ON}}{T_S} \quad (2)$$

d = duty cycle, T_{ON}= ON Period, T_S = Switching Period

Majid et al. (2012) analyzed the EMI noise of the buck converter and concluded that the size of EMI filter can be greatly reduced in the case of higher switching frequencies (range of MHz).

2.2.2 Step-up(Boost) converter

In this type of converter, the average output voltage is typically higher than the input voltage (Mohan et al. 2007). The basic topology of this converter is shown in figure 3.

In this topology the input voltage is switched at high frequency by placing the switch in parallel with the input voltage. During the steady state operation, the circuit can be divided into two timing intervals the ON time and OFF time. During the ON time interval, the diode D1 is reverse biased and the supply voltage provides the power to the inductor. The inductor is charged during this time interval. While, during the OFF time interval, the diode D1 is forward biased and both (input voltage and inductor) supply the voltage to the output.

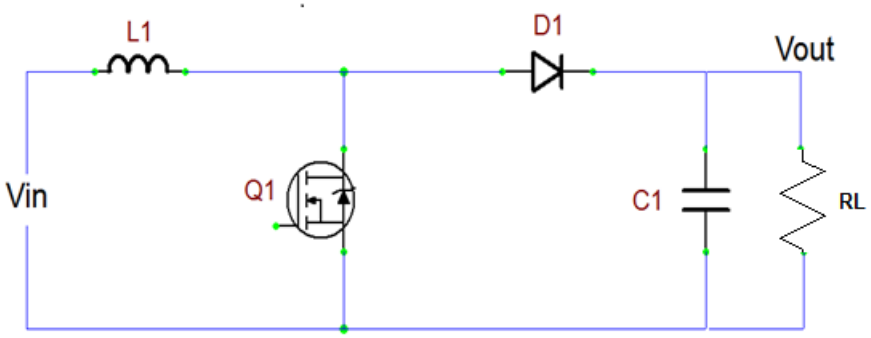


Figure 3: Step-up Converter

The equation to find the output voltage is given as

$$V_{OUT} = \frac{V_{IN}}{(1-d)} \quad (3)$$

$$d = \frac{T_{ON}}{T_S} \quad (4)$$

Wang et al. (2007) analysed the EMI performance of the boost converter model. They proposed the general balance technique to minimize the common-mode noise. In this technique, two methods were introduced:

Reduction of CM noise due to the abrupt change of MOSFET source voltage

In this method, the boost inductor is split into two parts to balance the parasitic capacitance of source/drain with the ground. As a result, the CM (common mode) noise is relatively reduced compared to the unbalanced converter (Wang et al. (2007).

Reduction of CM noise due to output capacitor voltage

There are two possible methods to reduce the CM noise due to output capacitor voltage.

Reduce the parasitic capacitance between the load and ground

Reduce the ESL (Equivalent series inductor) and ESR (Equivalent series resistor) of output capacitors.

2.3 Isolated Converters

The isolated converter can be classified into two types the asymmetrical and symmetrical converters as shown in figure 4. This classification is based on their magnetic cycle swing in the B-H plot as shown in figure 5. Asymmetrical converters are those in which the magnetic operating point of the transformer remains in the same quadrant. The other converters are known as symmetrical.

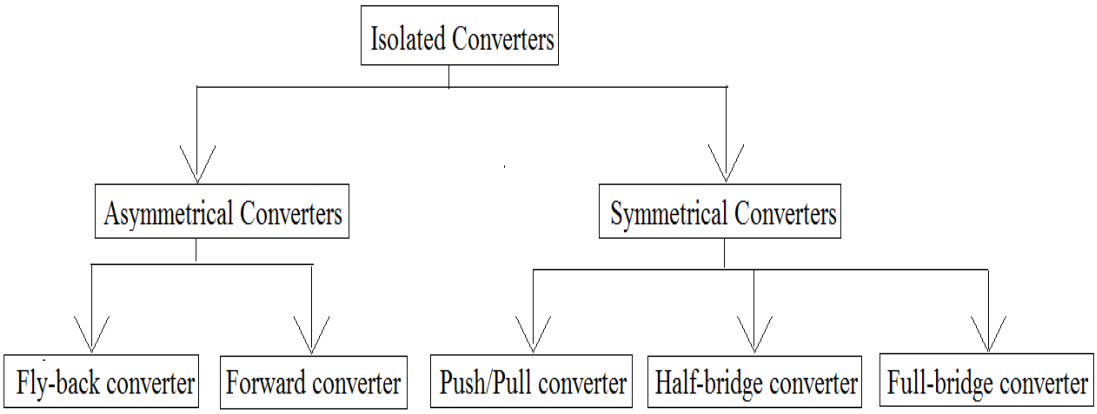


Figure 4: Isolated Converters

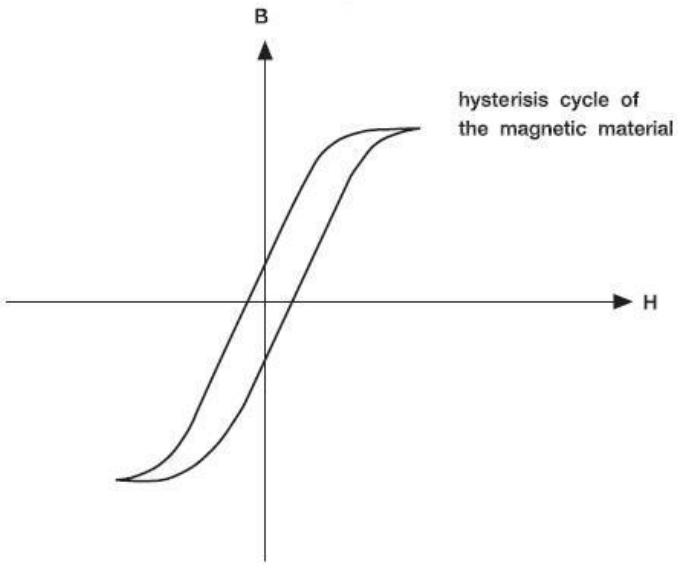


Figure 5: B-H plot of magnetic (Sullivan 1995)

2.3.1 Asymmetrical Converters

2.3.1.1 Fly-back converter

In a fly-back converter, the transformer is used for isolation to isolate the output voltage and the input voltage source. The basic topology of this converter is shown in figure 6.

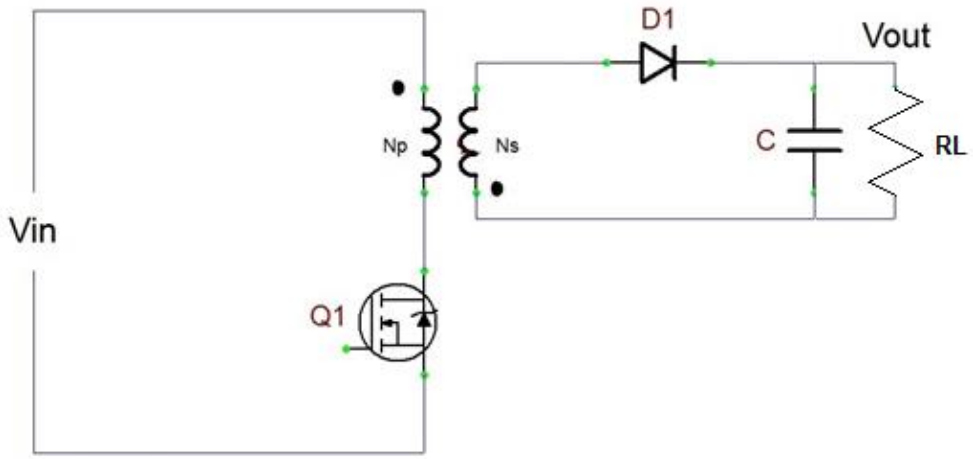


Figure 6: flyback converter

When the switch Q1 is ON, the transformer stores the energy in the primary Lp inductance and the energy stored in transformer is transferred to the secondary output when the switch is OFF.

The equation to find the output voltage is given by

$$V_{OUT} = \frac{V_{IN}.d}{n.\ (1-d)} \quad (5)$$

$$d = \frac{T_{ON}}{T_S} \quad (6)$$

$$n = Np / Ns \quad (7)$$

Np= Number of primary windings

Ns= Number of secondary windings

Yang et.al (2013) analysed the transformer of an isolated converter to try and reduce the common mode EMI noise. They identified the advantages and disadvantages of different methods of transformer shielding for mitigating of common mode EMI noise. They further proposed that the balance concept based on double shielding can be used to minimize common mode EMI. It was proved experimentally that this technique significantly reduced EMI noise compared to other shielding techniques (Yang et.al 2013).

2.3.1.2 Forward converter

In a forward converter, the transformer is used to isolate the output voltage and the input voltage source. The basic topology of this converter is shown in figure 7.

When the switch is in the ON state, the input source energy transfers directly to the load RL through the diode D1 and inductor. Whilst, when the switch is OFF, the inductor provides the energy to the load through the diode D2.

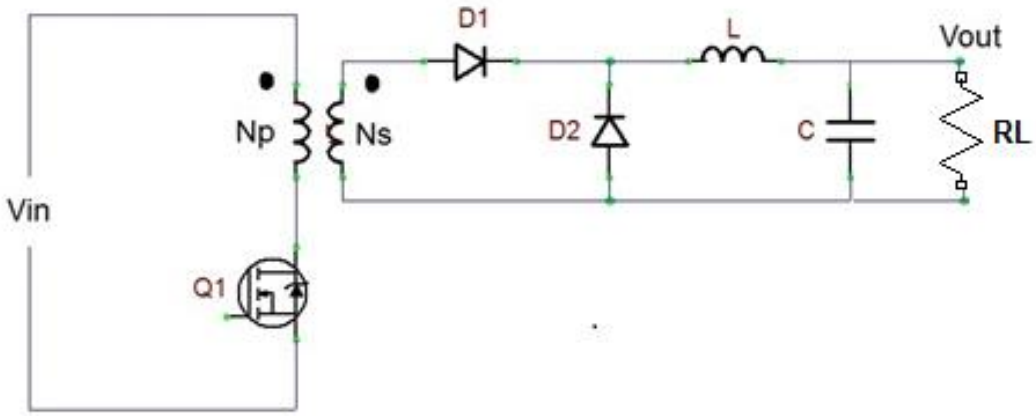


Figure 7: forward converter

The equation to find the output voltage is given as

$$V_{OUT} = \frac{V_{IN} \cdot d}{n} \quad (8)$$

$$d = \frac{T_{ON}}{T_S} \quad (9)$$

$$n = Np / Ns \quad (10)$$

Np = Number of primary turns

Ns = Number of secondary turns

Yazdani et. al (2015) examined the mitigation technique of conducted EMI noise in the forward converter and modified the forward converter to achieve a symmetric forward converter. They demonstrated that greater attenuation of EMI noise could be achieved at a higher operational frequency in the symmetrical converter as compared to a conventional converter. They also showed that using a coupled inductor in the symmetric converter helps to minimize the output voltage noise.

2.3.2 Symmetrical Converters

In these types of converters, an even number of switches are always used to exploit the transformer's magnetic circuit in a better way as compared to asymmetrical converters.

The advantage of using the even number of switches is to run the transformer core with equal and opposite flux.

2.3.2.1 Push/Pull converter

In a Push/Pull converter, the transformer is used for isolation to isolate the output voltage and the input voltage source. Moreover, dot notation is commonly used in transformer schematic. The dot node of transformer have same instantanous polarity (both dot end are in phase). The basic topology of this converter is shown in figure 8.

The input voltage is switched across the primary side of the transformer by switching the two switches Q1 and Q2 alternately for an equal time (Pressman et al. 2009). As a result, a pulsating voltage is produced across the primary winding of the transformer. The transformer is used for isolation and also to step down the primary voltage to the required output level.

During the ON interval (TON) of switch Q1, a positive voltage is applied across the dot end of transformer and the non-dot end is negative. As a result, the upper diode D6 acts as conducting (forward-biased) and lower diode D5 is not-conductive (reverse-biased). The forward biased diode D6 provides the path to transfer the energy from the transformer secondary side to the output load and inductor. The switch Q1 is turned OFF at the end of the TON period and the next interval is the TOFF period. During the OFF time interval, Q1 and Q2 are OFF and this time is called a ‘dead time’. This dead time is necessary in order to avoid simultaneously conduction of both switches. During this dead time, the leakage energy stored in the transformer primary is dissipated through the body diode of the switch and the diode D5 also becomes forward-biased on the secondary side of the transformer. The diodes D5 and D6 are both conducting during the dead-time providing a path for the inductor current. The inductor current is split into two parts and passes through the secondary transformer windings (NS1 and NS2). Thus the voltage applied to the transformer’s secondary windings is equal and opposite. Consequently, the practical voltage across the secondary is zero and a constant flux density is produced across the transformer core. In the similar way, the Q2 switch works for the next half period of switching frequency.

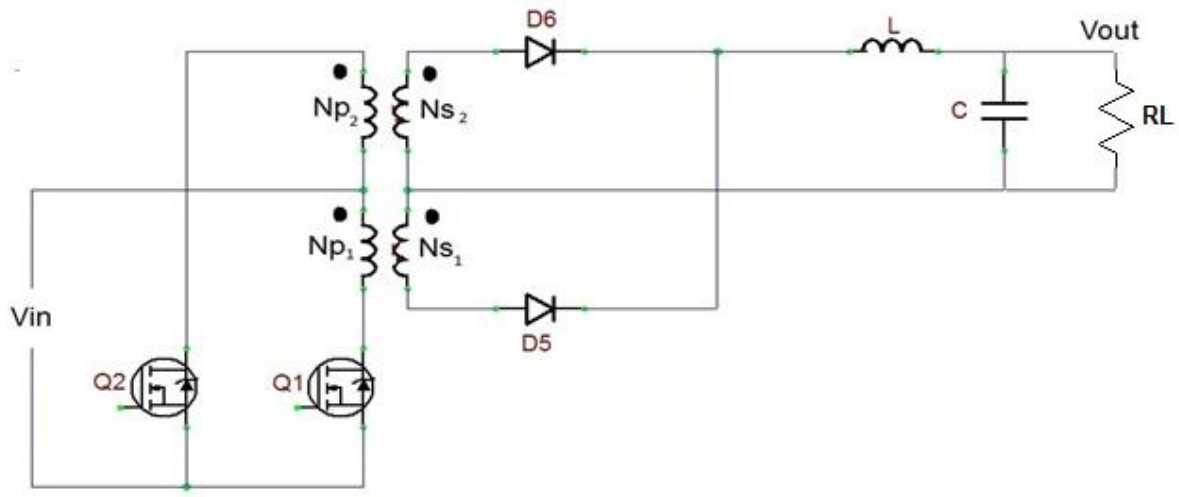


Figure 8: Push-pull converter

The equation to find the output voltage is given as

$$V_{OUT} = \frac{V_{IN} \cdot 2 \cdot d}{n} \quad (11)$$

$$d = \frac{T_{ON}}{T_S} \quad (12)$$

$$n = Np / Ns \quad (13)$$

Np = Number of primary turns

Ns = Number of secondary turns

2.3.2.2 Half-bridge converter

In a Half-bridge converter, the transformer is used for isolation to isolate the output voltage (Vout) and the input voltage source (Vin). The basic topology of this converter is shown in figure 9.

As shown in the figure 9, one leg of bridge is constructed by transistors Q1 and Q2, while the other leg of a bridge is formed by capacitor C3 and C4 (Maniktala 2012). As a result this configuration is called half-bridge converter.

The input voltage is switched across the primary of the transformer by switching the two switches Q1 and Q2 alternately for equal times. In a result, a pulsating voltage

is produced across the primary of transformer. The transformer is used for isolation and also to step down the primary voltage to the required output level.

During steady state operation, the capacitors C3 and C4 used in half bridge converters are equal and charge to equal voltages of half the input voltage. During the time period TON, the upper switch Q1 is ON, which results in the transformer's primary side (dot end) becoming positive and the other end of the primary connected to the intersection of capacitors (C3 and C4). Therefore the voltage across the transformer's primary side winding is the half of VIN during TON period. The transformer's primary side (dot end) is connected to the V_{IN} positive and the other end is at half the potential of V_{IN}. On the secondary side of transformer, the diode D3 becomes forward biased and diode D4 becomes reverse biased. The diode D3 provides the path to transfer the transformer secondary energy NS1 to the load through the inductor. As a result, the voltage across the inductor L is equal to the difference of secondary voltage and output voltage. The switch Q1 is turned OFF at the end of the TON period and the next interval is TOFF period. During the OFF time interval, Q1 and Q2 are OFF and this time is called a dead time. This dead time is necessary in order to avoid simultaneous conduction of both switches (Q1 and Q2).

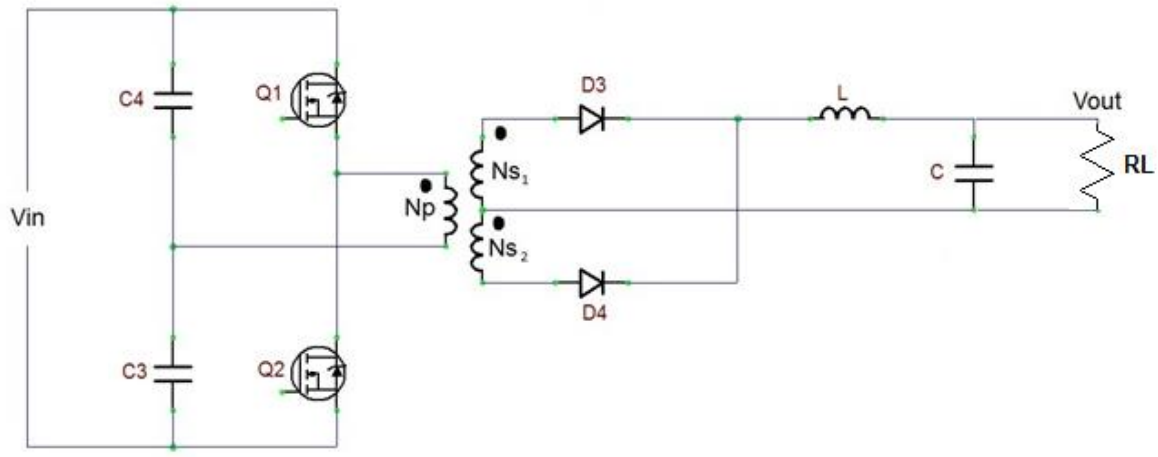


Figure 9: half-bridge converter

During the OFF time interval TOFF, the leakage energy stored in the transformer primary is dissipated through the body diode of the switch Q2 and the diode D4 also becomes forward-biased on the secondary side of transformer. The diodes D3 and D4 are both conducting during dead-time and provide a path for the inductor current. The inductor current is split into two parts and passes through the secondary transformer

windings (NS1 and NS2). Thus the voltage applied to the transformer secondary windings is equal and opposite. Consequently, the voltage across the secondary is zero and constant flux density is produced across the transformer core. On the other hand, the voltage across the inductor L is equal to the output voltage in the reverse direction. Therefore, the inductor current decreases linearly during this time.

For the next half cycle of time period, the switch Q2 turns ON, which results in the transformer primary's side (dot end) connects to negative potential of input voltage and the other end of transformer primary connects to the intersection of capacitors (C3 and C4). Therefore the voltage across the transformer primary is half of VIN in the reverse direction during the TON period. Q2 turns OFF after the TON period and next interval is TOFF. During the OFF time interval, Q1 and Q2 are OFF to avoid the simultaneously conduction of both switches. In similar way, the next cycle repeats to turn ON and OFF switches Q1 and Q2 alternately for the half of cycle.

The equation to find the output voltage is given as

$$V_{OUT} = \frac{V_{IN} .d}{n} \quad (14)$$

$$d = \frac{T_{ON}}{T_S} \quad (15)$$

$$n = Np / Ns \quad (16)$$

2.3.2.3 Full-bridge converter

In a Full-bridge converter, the transformer is used for isolation to isolate the output voltage and the input voltage source. The basic topology of this converter is shown in figure 10.

As shown in figure 10, the switches Q1 and Q4 form one leg of the bridge and switches Q3 and Q2 formed the other leg (Billings and Morey 2010). The common leg of both transistors Q1 and Q4 is connected to transformer's primary dot end and Q2 and Q3 is connected to the other end. As a result, the applied voltage across primary is pulsating AC voltage. The transformer function is to provide the isolation between input and output voltages as well as step down the pulsating voltage up to the required output level.

During the ON time interval, the switches Q1 Q2 turn ON, which results in the primary (dot end) to connect the positive potential of V_{IN} and the other end to the

negative of V_{IN}. On the secondary side of transformer, D3 becomes forward-biased and the diode D4 becomes reverse biased. Also the diode D3 provides a path to transfer the transformer secondary energy NS1 to the load through the inductor. As a result, voltage across the inductor L is equal to the difference of secondary voltage and output voltage.

The switches Q1 Q2 become turned OFF at the end of TON period and the next interval is TOFF period. During the TOFF period, all four switches (Q1 Q2 and Q3 Q4) are OFF and this time is called a dead time. This dead time is necessary in order to avoid simultaneously conduction of both the switches.

During the OFF interval of switches (Q1 Q2), the leakage energy stored in the transformer primary is dissipated through the body diode of switch pair Q3 Q4 and the diode D4 also become forward-biased on the secondary side of transformer. The diodes D3 and D4 are both conducting during dead-time and provide a path to the inductor current. The inductor current is split into two parts and passes through the secondary transformer windings (NS1 and NS2). Thus the voltage applied to the transformer secondary windings is equal and opposite. Consequently, the practical voltage across the secondary side is zero and constant flux density is produced across the transformer core. On the other hand, the voltage across the inductor L is equal to the output voltage in the reverse direction. Therefore, inductor current decreases linearly during this time.

For the next half time interval, switches Q3 Q4 turn ON, which results in the primary (dot end) to connect the negative potential of V_{IN} and the other end to the positive of V_{IN}. On the secondary side of transformer, D4 becomes forward-biased and the diode D3 becomes reverse biased. Also the diode D4 provides a path to transfer the transformer secondary energy NS2 to the load through the inductor. As a result, the voltage across the inductor L is equal to the difference of secondary voltage and output voltage. The switches Q3 Q4 become turned OFF at the end of TON period. In a similar way, the next cycle repeats to turn ON and OFF switches Q1 Q2 and Q3 Q4.

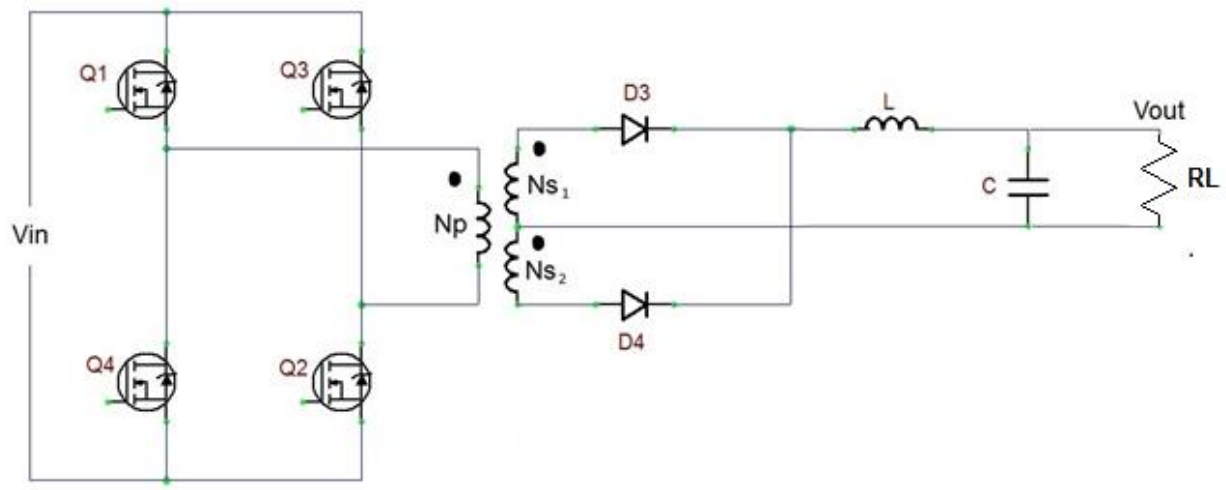


Figure 10:Full-bridge converter

The equation to find the output voltage is given as

$$V_{OUT} = \frac{2.\ V_{IN}\ .\ d}{n} \tag{17}$$

$$d = \frac{T_{ON}}{T_S} \tag{18}$$

$$n = Np / Ns \tag{19}$$

2.4 Power factor correction

In the initial stage of SMPS, the input circuit typically consists of a full-wave rectifier followed by a bulk capacitor as shown in figure 11. The peak voltage of input (Vin) sine wave is maintained by a bulk capacitor until the following peak appears to recharge it as shown in figure 12. During the peaks of input voltage waveform (shown in blue colour) , the current (shown in green colour) is drawn from the input and this current must possess sufficient energy to withstand the load until the following peak (as shown in figure 12). As a result, the power factor of a power supply is reduced and harmonic content becomes high. The regulatory bodies set a standard defined by EN61000-3-2 to impose the restriction on line current harmonic pollution. Therefore, it has become a standard practice to modify the power supply using a power factor correction (PFC) circuit.

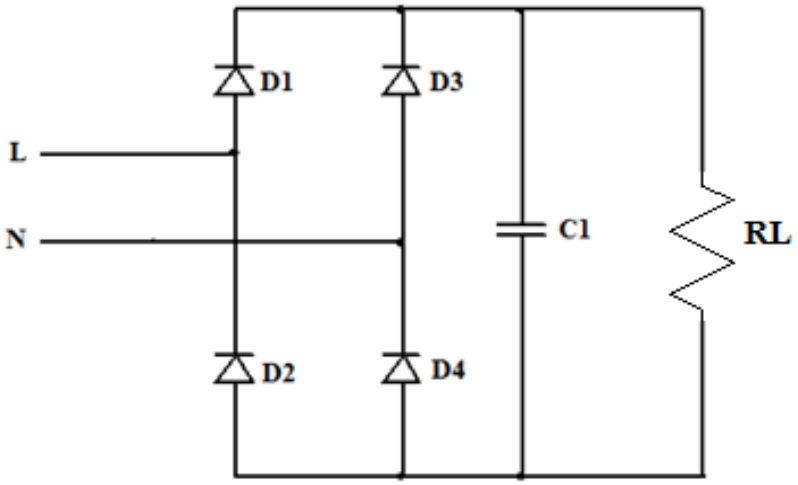


Figure 11: Full-wave rectifier

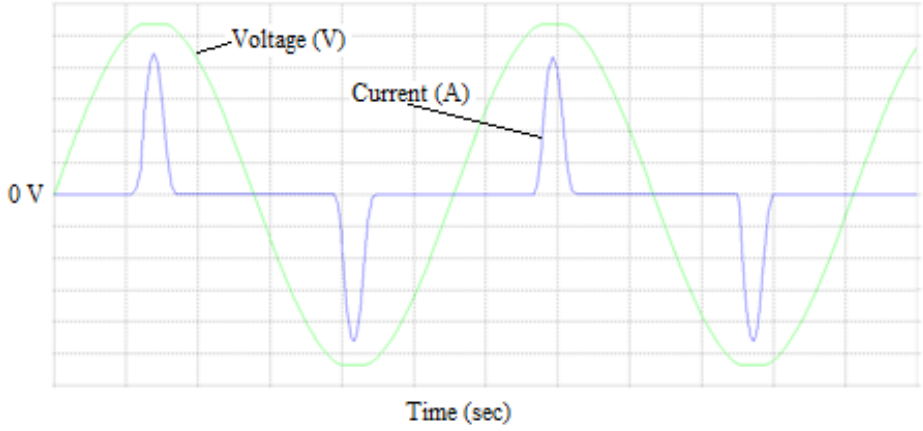


Figure 12: Waveform of full-wave rectifier

The primary aim of a PFC circuit is to decrease the harmonic elements of mains current. PFC circuits can be categorized as active and passive circuits. This classification depends on components used in the circuit. In active PFC circuits, inductors and active switching devices are normally used and the output voltage is regulated for line variations. On the other hand, only passive components are used in passive PFC and output voltage has line variations as it is not regulated.

2.4.1 Passive PFC Converter

In passive PFC circuits, the passive components with Diode Bridge are used to improve the power factor correction. There are many possible schemes to implement passive PFC circuits such as Passive PFC with Inductor on the DC Side or the AC Side (figure 13). The advantages of passive PFC circuits are simple design, no high frequency EMI noise and reliability (Garcia et al. 2003). However, there is a practical limitation of these filters due to bulky size of passive components, absence of voltage regulation and line frequency noise (Suzuki et al. 1997).

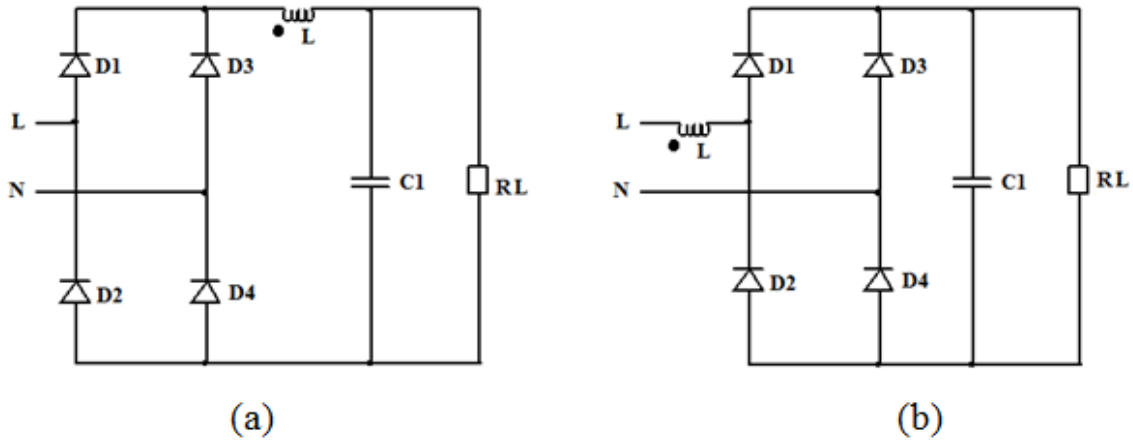


Figure 13: (a) Passive PFC with Inductor on the DC Side (b) Passive PFC with Inductor on the AC Side PFC

2.4.2 Active PFC Converter

The active PFC can be implemented by incorporating buck, boost or a buck-boost converter between the input filtering capacitor and diode bridge rectifier. It is operated by a control method in which switches are precisely controlled to shape the input current to follow input voltage. The switching frequencies of these circuits are much higher as compared to line frequency and the output voltage is also regulated to minimize the output ripple voltage. The output voltage is regulated in all types of active PFC circuit by setting it lower or higher depending on converter type used. In a buck converter, the output voltage is set to a lower value than the maximum amplitude of input voltage. While in a boost converter, the output voltage is set to a higher value as

compared to maximum value of input voltage. The output voltage can be set to a lower or a higher value in case of a buck-boost converter.

These converters can be classified further into three types based on inductor current continuity and discontinuity. This classification includes continuous conduction mode (CCM) , discontinuous conduction mode (DCM) and critical conduction mode (CRM) (Chen and Chen 2015). In CCM, the current through the inductor during one switching cycle can never reach zero. While in DCM, the current through the inductor reaches zero for some time during each switching cycle interval. However, in critical mode, the conduction is in between continuous and discontinuous mode.

2.4.2.1 Buck Converter based Active PFC

In this topology, the input voltage is stepped down to the output voltage and the output voltage is regulated as shown in figure 14. It works only if the input voltage is higher as compared to the set regulated output voltage. During a time interval of t1 to t2, there is no input current flowing in a circuit as shown in figure 15. That causes distortion of the line input current near the zero crossing point of the input voltage. The input current is also discontinuous due to the high switching frequency switch that interrupts the line current in every switching period. As a result, the high frequency components accompanied in a line current would increase overall EMI noise in a circuit.

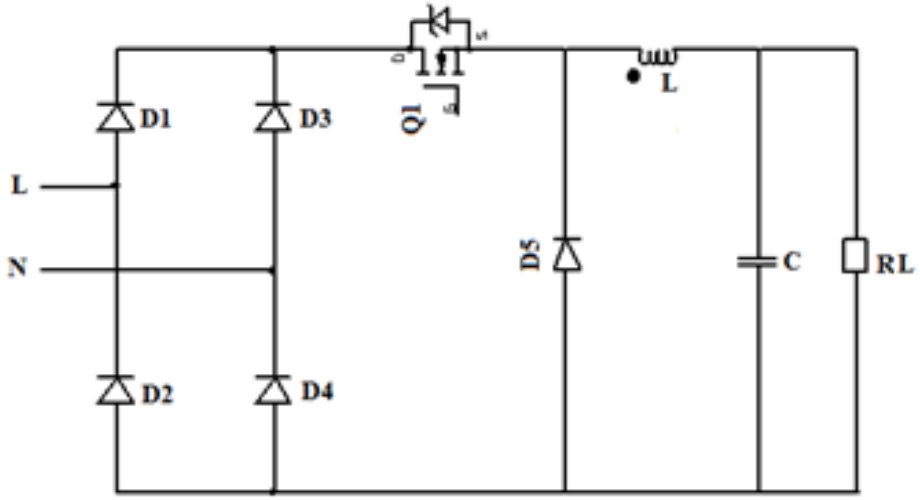


Figure 14:Buck PFC Converter

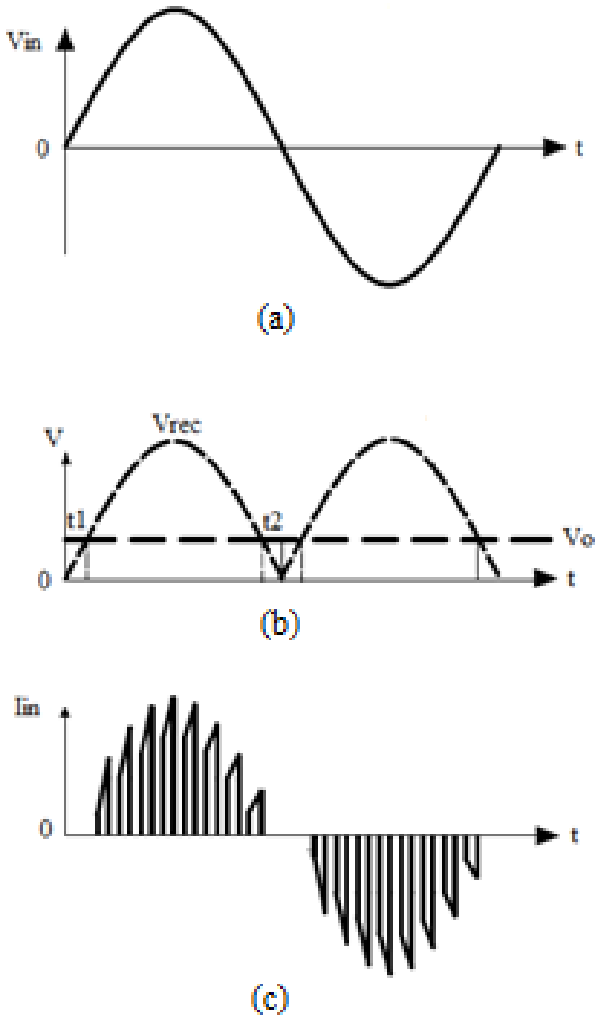


Figure 15:Waveforms of Buck PFC Converter

2.4.2.2 Boost Converter based Active PFC

The boost converter topology is most common for PFC circuits. It operates in three modes - continuous conduction mode (CCM), discontinuous conduction mode (DCM) and transition mode control. The transition mode control is also known as critical conduction mode (CRM) which works at the limit between CCM and DCM by controlling the switching frequency with a controller. CCM boost converter and its related waveforms are shown in figure 16 and figure 17 (Lai and Chen 1993).

In this topology, the input voltage is step up and the output voltage is regulated through controlling the switching frequency of a converter. It operates throughout the line frequency cycle and also there is no crossover distortion for input current. As a result, the line current has no distortion near the zero crossing points of the input voltage. The input current follows the continuous conduction as an inductor is employed

in series with the input voltage and not disturbed by high frequency switching. Therefore, the input current is not affected with higher switching frequency components which results in lower EMI.

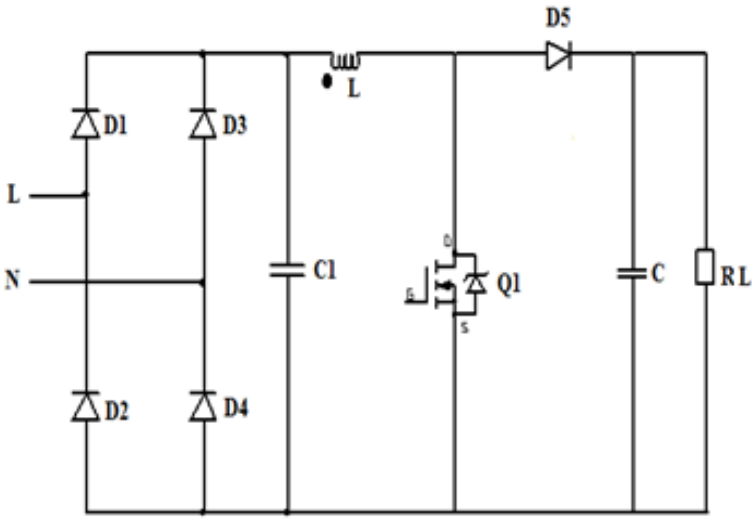


Figure 16:Boost PFC converter (Lai and Chen 1993)

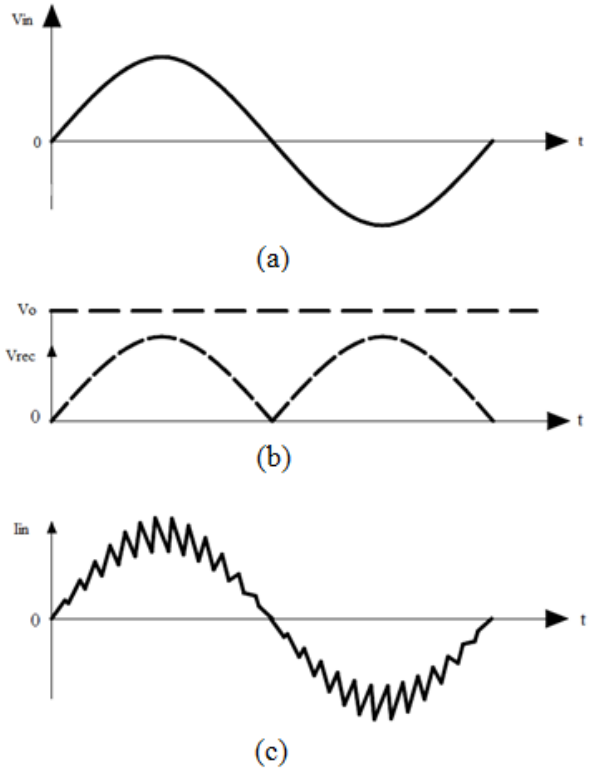


Figure 17:Waveforms of Boost PFC converter (Lai and Chen 1993)

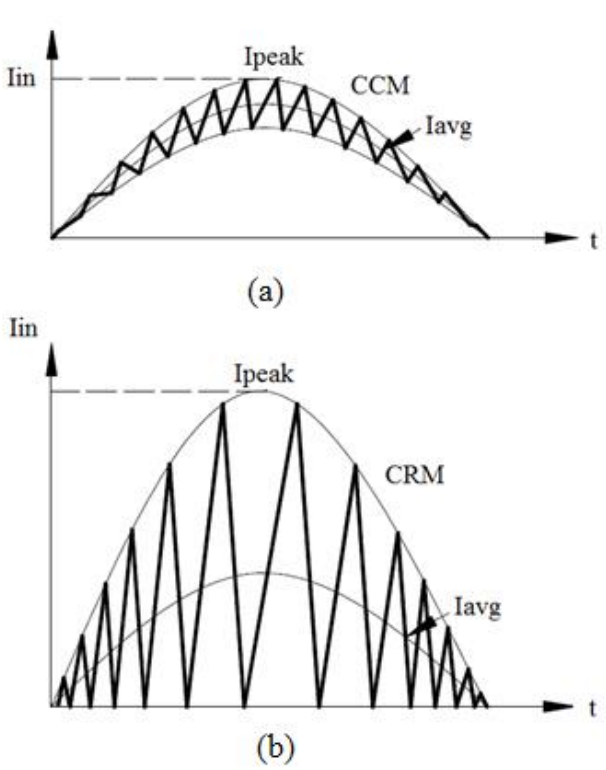


Figure 18: Waveforms of CCM and CRM Boost PFC converter (Lai and Chen 1993)

In a boost PFC converter, the inductor current can be either in continuous or discontinuous mode depending on the type of controller technique used as shown in figure 18. In comparison to CCM or CRM techniques, the DCM converter operates with fixed switching frequency and has inductor current in discontinuous mode. It also introduces large peak currents due to discontinuous mode over every cycle of switching period. Moreover, it generates larger EMI noise due to high frequency components incorporated within it. Therefore, it is not used commonly for PFC circuit. In CRM mode converter, a hysteresis control of variable frequency with zero current boundary is normally used. This controller has stable input current control and also reduces the losses of reverse recovery rectifier. In this mode, the ON-time remains constant while the OFF-time is changing according to set of input and output voltage regulation required. As a result, when input voltage is lowest, the switching frequency is highest and vice versa.

The generation of conducted EMI noise in boost converter operating in DCM and CCM have been presented in the literature (Ji et al. 2015). In order to reduce the overall size of a converter, the integration of boost inductor and EMI filter have been proposed

and evaluated (Deng et al. 2014). The reported results showed the effectiveness of integration experimentally.

2.4.2.3 Buck-Boost Converter based Active PFC

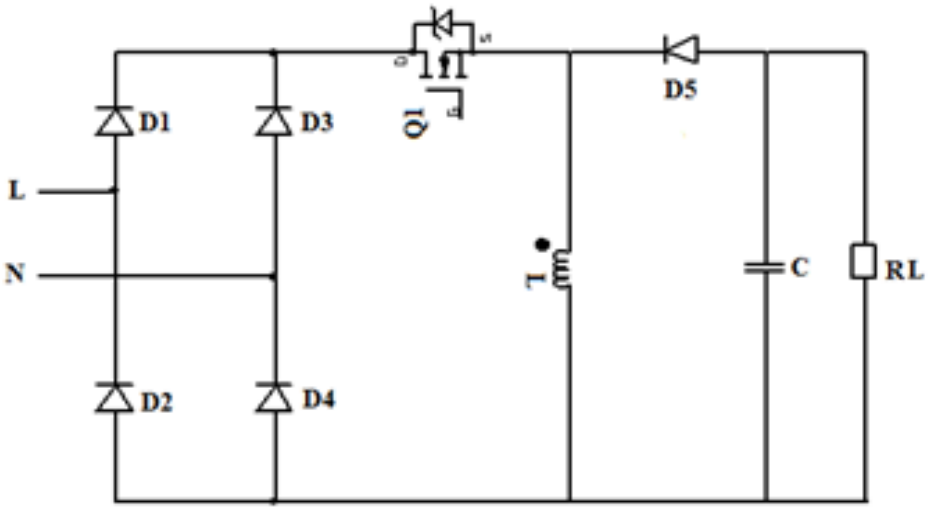


Figure 19:Buck-boost PFC converter

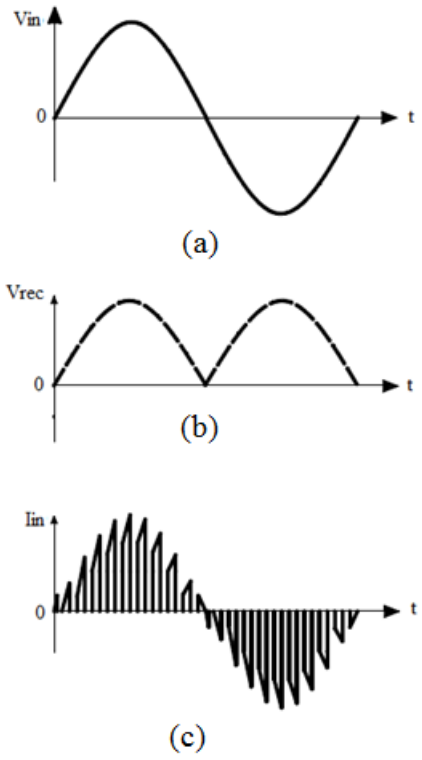


Figure 20:buck-boost PFC converter

In buck-boost converter (figure 19 and figure 20), the input voltage can be step up or step down according to the required output voltage. There is no crossover distortion for input current as the converter operates throughout the line frequency cycle as shown in figure 19. As a result, no distortion in line current near zero voltage crossing points occurs. Also input current has discontinuity due to switching component switches in every cycle. Furthermore, a high-frequency component is added in the input current path of the converter that generates additional EMI noise.

2.5 Power supply requirement for audio amplifier

The power requirement of an audio amplifier is as follows:

Dual rail supply voltage (V)	=	$\pm$ 48 V
Max. Current (I)	=	6A
Max. Power (P)	=	1152W

The detailed specification of power supply is as follows

INPUT:

AC input voltage range	90VAC to 270VAC
AC input frequency	50Hz to 60Hz

OUTPUT:

Normal DC output voltage	$\pm$48 V
Tolerance DC Voltage	$\pm$ 2%
Maximum load current	6A
Maximum Output power	1152W

2.6 Summary

The converter topologies can also be classified on the basis of the needed power requirements. Non-isolated converters are unsuitable for high voltage and high power application because of the lack of isolation between the input and output voltage. These converters have very limited use producing only a single output over a limited output range. Conversely, these constraints can be removed by addition of transformers as in isolated converters. In the isolated converter, the fly-back and forward converter are

practicable up to 150 watts of output power level. The limitations (output power) of these converters are due to factors, such as, utilization of the magnetic (transformer) core and maximum voltage stress across the switch during the OFF time interval. On the other hand, push-pull topology is not suitable for high input voltage application (190VAC-230VAC) due to high voltage stress across the switch (2×Vin) and 50% utilization of the transformer primary windings. The magnetic core is not utilized completely in this type of converter because full input voltage applied across the transformer winding is in one direction when any one switch is conducting. These reasons make it better suited for low-voltage applications and power ratings up to 500W. The half-bridge converter is particularly suited for high voltage application as the maximum voltage stress of either switch is equal to the input voltage and fully utilizes the transformer primary windings. In this converter, the primary voltage of the transformer is equal to half of the input voltage VIN when either switch is ON which made this converter more suitable for power levels up to 500W. Moreover, the full-bridge converter is particularly suited for high input voltage applications for reasons, such as, maximum voltage stress of either switch is equal to the input voltage and utilization of the high frequency transformer is complete. In this converter, the primary voltage of transformer is equal to the input voltage VIN during either switch is ON which made this converter more suitable for power levels exceeding 500W.

The PFC topology can be selected on the basis of minimum EMI noise generated within a converter. The passive PFC are not suitable due to bulky size of passive components, absence of voltage regulation, expensive components and line frequency noise. On the other hand, these constraints can be removed by an active PFC converter. In the active buck and buck-boost PFC converter, input current has discontinuity due to switching component switches in every cycle of switching period. As a result, the high frequency components accompanied within a converter. This reason made it unsuitable for low noise SMPS. Therefore, PFC boost converter is particularly suited for lower EMI noise converter application.

3 CHAPTER 3 LITERATURE REVIEW

3.1 Introduction

An essential requirement for electrical and electronic equipment is for the power supply to provide a reliable and regulated output to the load. The main issues that influence the design phase of a power supply are the power performance requirement, weight, reliability and cost (Brown 1994). These issues have in the most part been resolved with the development of high voltage power transistors, which have made it possible to replace the linear power supply with a high switching frequency switch-mode power supply (SMPS). The fast power semiconductor switching devices such as power MOSFETs or IGBTs are mostly used in SMPS and the switching frequency extends from tens to hundred of kilohertz. Due to the higher switching frequency used in SMPS, the change of dv/dt and di/dt across the power switches causes significant Electromagnetic interference (EMI) emission (Christopoulos 1992; Nagrial and Hellany1999). It is therefore generally necessary to limit the EMI emission and compliance with EMC standards. A number of research papers (Chung et al. 1998;Shoyama et al. 2003; Wang et al. 2013; Bera et al. 1999; Britto et. al 2012; Cochrane et al. 2003; Omata et al., 2014; Xie et al. 2015; Zhou et al. 2016 ; Tamate et al. 2010; Hamill and Krein 1999; Wang et al. 1997) have been published to discuss the mitigation techniques of Electromagnetic Interference (EMI). In this chapter, a review has been made on several EMI mitigation techniques proposed in the literature for SMPS.

There are several questions to assess in this chapter are as follows

- Why it is important to minimise the EMI in SMPS for audio systems?
- What techniques are available to reduce EMI in SMPS?
- What are the most appropriate techniques to mitigate EMI for audio systems?
- Are potential solutions constrained by the need for compliance with EMI regulatory requirements?

3.2 Electromagnetic Interference (EMI)

Electromagnetic interference is defined as an electromagnetic disturbance that degrades or limits the performance of electronic and electrical equipment (Paul 2006). The major source of EMI emission in SMPS is due to the high switching frequency of power MOSFETs or IGBTs. There are two types of switching techniques used in SMPS to control the switches: hard switching and soft switching. In hard switching techniques, the change of high dv/dt and di/dt is the major cause of high switching losses as well as high EMI noise. Conversely, soft switching techniques minimize the switching losses due to the switch turn ON at zero voltage and the switch turn OFF at zero current with the help of resonant techniques. Several papers have been published to discuss the soft switching technique that results in substantial minimization of switching losses (Lin 2016; Yazdani and Rahmani 2014; Abbasi et al. 2014; Hua and Lee 1991; Lee and Moon 2013).

Brown (1994) classified the noise into two categories (i) radiated noise which can be coupled between components through the surrounding air and (ii) conducted noise which propagates through interconnecting wires and PCB tracks. The major source of radiated noise in SMPS is due to current flow through the conductor at high frequencies. According to Ampere's law, an alternating current flowing through the conductor will generate an electromagnetic field around it and this law defines the generation of radiated noise in a SMPS. The control section for the power switches is also a source of radiated noise but is insignificant by comparison to the main converter section (Bausiere et al. 1993). On the other hand, the radiated emission from the converter side has enough energy to affect the proper functioning of the control section (Hellany and Nagrial 2001). Billings (1989) proposed that proper PCB track layout and wiring practices could improve the performance of SMPS by minimizing the propagation of radiated noise.

Conducted EMI noise is further divided into two sub-categories (i) common mode interference (CM) and (ii) differential mode interference (DM). The generation and coupling mechanisms are different for both sub-types of interference. The common mode interference is typically caused by parasitic couplings (such as inductive and capacitive) occurring within the SMPS (Switch-mode Power Supply) and it flows through the ground wire and returns back via phase and neutral lines. The differential mode interference is mainly due to the switching action of the transistor and flows through the neutral line and returns back via phase line. Several articles have attempted

to explain the generation of EMI noise in different types of converter (Gonzalez et al. 2003). The generation of EMI (Electromagnetic Interference) noise in the Step-up converter has been discussed by (Zhang et al. 1997; Wang et al. 2003; Crebier et al. 1999; Pengju et al. 2012; Ji et al. 2015). On the other hand, Nave (1991) and Mitchell (1999) deal with buck converters, Ninomiya et al. (1987) and (Paramesh and von Jouanne 2001; Makda and Nymand 2014) deal with the forward converter, and (Ninomiya and Harada 1980; Karvonen and Thiringer 2011; Longtao et al. 2012; Patel 2008) deal with offline flyback converters.

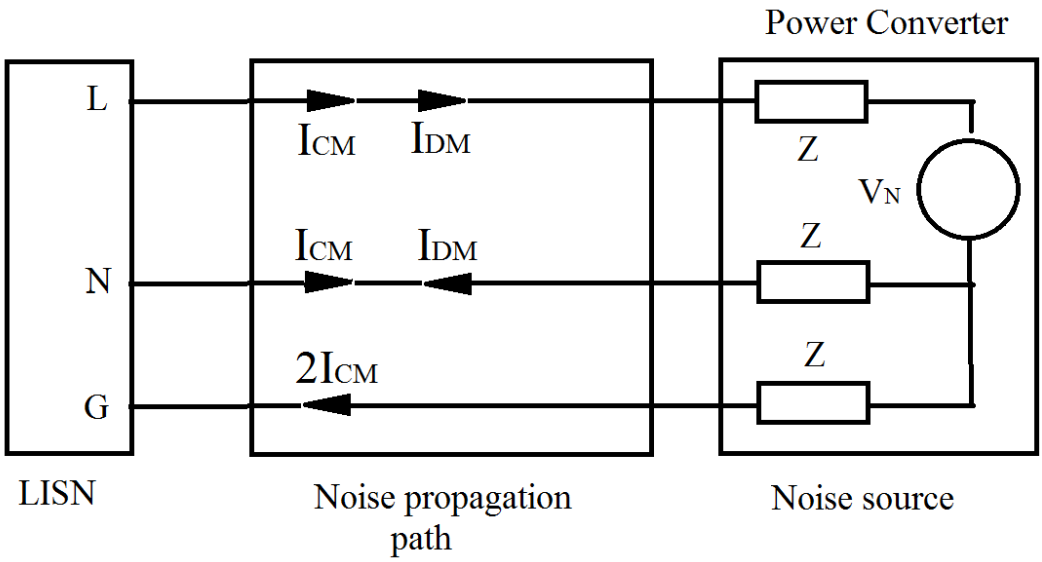


Figure 21: Noise source and propagation path for converter

The EMI noise measurement, sources and propagation coupling paths are shown in figure 21. It also uses a LISN (Line Impedance stabilization network) used for measurement of EMI noise using a spectrum analyser (De Beer et al. 2013). There are two ways to mitigate EMI noise in a converter either reduction at its source or along the propagation path. Various mechanisms are available to reduce the noise at source source. However, the simplest approach is to reduce the noise along the conduction path by incorporating an EMI filter. EMI noise reduction techniques are generally classified either as noise source mitigation scheme or noise propagation mitigation scheme. The noise source mitigation scheme can be subdivided into different schemes as discussed in next section. The noise propagation scheme can be also further sub-divided on the basis of methods used to mitigate it through a separate circuit located at the front-end of a converter or incorporated with in a converter. The former is known as external EMI

filter. While the later one is called as an internal EMI filter. The external EMI filter can be subdivided into active, passive and hybrid EMI filter. The internal EMI filter can be designed in a way that noise can circulate within a converter.

3.3 EMI Noise source mitigation

There are several benefits of employed noise source mitigation scheme within a converter such as reducing size, cost and better performance of SMPS. It minimizes noise interference between controller and noise sensitive components that helps to avoid malfunction of a converter. The various methods to mitigate noise at source point of a converter are as follows proper circuit design, appropriate PCB layout, selecting appropriate components, selecting switching frequency, switching control techniques, switching transition modification and interleaving converter.

3.3.1 Proper circuit design

The EMI noise generation can be controlled and minimized by an appropriate circuit design. It is therefore necessary to determine the mechanism of noise generation in a circuit. The main source of CM noise generation is occurrence of parasitic capacitance due to the switching components heat-sink being attached to ground (Sinclair et al. 1993). However, the connection of a heat-sink with low noise node can mitigate EMI noise significantly as illustrated in figure 22. However, the heat-sink usually needs to be connected to ground to fulfil safety requirements. To solve this issue, Knurek (1988) proposed a novel method by introducing a shielding layer between insulators of a heat-sink. The heat-sink is attached to ground and the shielding layer is connected to a quiet node (neutral line). The thermal performance of the heat-sink will be reduced due to the shielding layer used in this scheme. In some other cases, the noise produced by voltage switching can be reduced by relocating component in a circuit. The modified forward converter with rearrangement of its component is shown in figure 23. In the modified converter, the output filter inductor is moved to the negative rail of the output voltage that provides the transition of voltage (dv/dt) across diode equal to zero. In a similar way, the MOSFET can be rearranged to the upper position of primary side that provides constant voltage potential across the drain of MOSFET. This requires an additional component and complexity in a circuit to design the high-side driver for the MOSFET. Other researchers (Sinclair et al. 1993) have proposed methods to minimize current flowing in the parasitic capacitance by employing a heat-sink connected to ground

through an additional resistor. This scheme leads to dissipation of the current in an additional resistor and as a consequence minimized CM noise flow to ground.

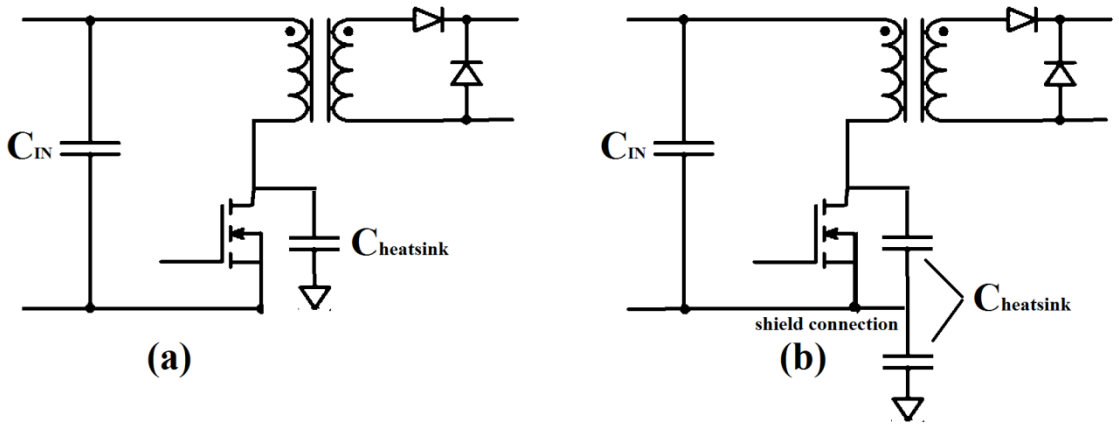


Figure 22: Forward converter (a) connection of heat-sink with ground (b) connection of heat-sink with quite node (Sinclair et al. 1993)

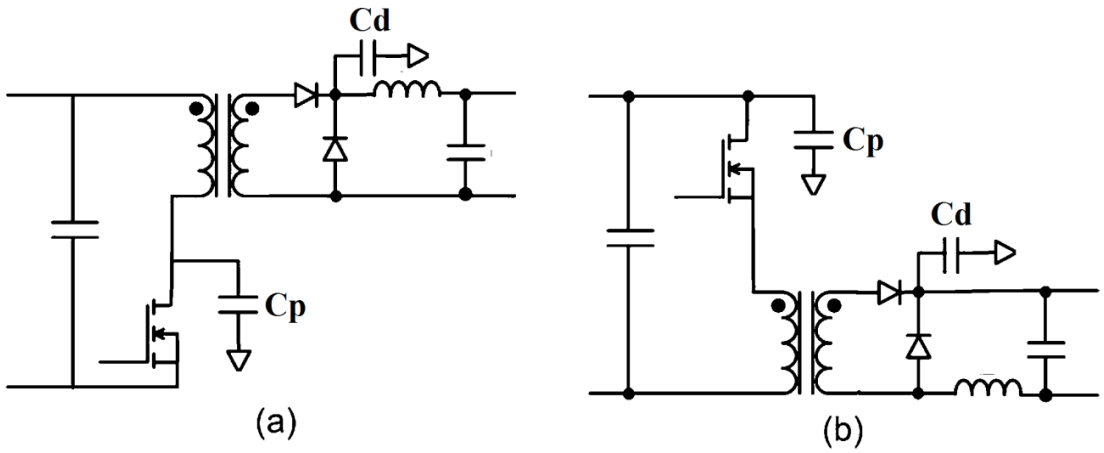


Figure 23: Forward converter (a) conventional method (b) modified with rearrangement of its components (Knurek 1988)

3.3.2 Appropriate PCB Layout

A number of research articles have been reported which discuss the EMI noise issues related to circuit layout and design schemes (Bhargava et al. 2011; Wu and Tse 1996; Fluke 1991; Pahlevaninezhad et al. 2014). They have proposed keeping leads of component as small as possible to minimize parasitic inductances of PCB. The lower parasitic inductance of a PCB will not only help to reduce ringing of voltage across switching devices but also results in lowering the amplitude of EMI noise. They discussed the effect of PCB layout on EMI noise in a converter. They suggested placing

of control circuit far away from noise source components would help to keep a distance between noise source (switching devices) and noise sensitive parts (control section) for prevention of disturbances within a converter. They also discussed issues related to sharing common ground in different parts of circuit. The noise generated due to one circuit may be coupled to other part of circuit through a common ground connection. The single-point grounding connections have been proposed to avoid noise coupling in different circuit modules of a converter. Also proper PCB design can help to reduce the filter size for mitigation of noise up to desired level (to meet EMI standard). Zhaoming et al. (2000) proposed different tools for PCB layout to minimize EMI generation in a circuit.

3.3.3 Selecting appropriate components

As previously mentioned the major source for CM noise generation is the occurrence of parasitic capacitance between switching components and ground. These parasitic capacitances arise due to the ground coupled heat-sink attached to the switching devices. Knurek (1988) compared different types of insulators used for heat-sinking. He concluded that aluminium oxide insulators have six times less dielectric constant as compared to commonly used silicon rubber insulators. Also, he experimentally proven that conducted EMI noise can be improved up to 10dBuV in the case of aluminium oxide insulator. Diode reverse recovery current also affects the EMI noise performance of a converter. EMI noise can be reduced by incorporating a diode with reduced recovery current. The performance of different types of diode with minimum reverse recovery current has been evaluated in boost converter (Spiazzi et al. 2003). The experimental results proved that using a SiC (silicon carbide) diode can help to reduce high frequency EMI noise. A similar method has been proposed by Shekhawat et al. (2002). They demonstrated that introducing a soft recovery diode in a PFC boost converter reduces noise significantly in the high frequency range.

3.3.4 Selecting switching frequency

EMI noise also depends on the operating switching frequency of a converter. A converter operating at lower switching frequency has the advantage of reduced EMI noise. However the overall size of the converter increases due to the typical bulky passive components needed for lower frequency operation. Rossetto et al. (2000)

suggested that a switching frequency of 70kHz provides the first two harmonics below the lower limit of frequency range for conducted EMI scan. As a result, the passive EMI filter size can be reduced significantly. A PFC boost converter with low switching frequency of 100 Hz was reported to minimize conducted EMI noise (Rossetto et al. 2000). In addition, a first-order filter was used to meet the requirement of EMI noise standards.

3.3.5 Switching techniques

Switching techniques play an important role on the behaviour of EMI noise. The main purpose of the switching technique is to control the flow of power and regulated output voltage. The most common technique used to control the switching MOSFET in a converter is called Pulse Width modulation (PWM). Normally a constant switching frequency is used with varied pulse width (duty cycle) to regulate the output voltage. However, the use of constant frequency increases the generation of spikes and associated harmonics. Therefore, a widely used scheme known as the spread spectrum technique has been implemented in SMPS to distribute spread EMI noise over a range of frequencies (Fardoun and Ismail 2009; Gonzalez et al.2007). These techniques use a variable switching frequency over the operational bandwidth to spread the noise. Comparison of fixed frequency (30-KHz) and variable switching frequency (30~166 kHz) has been evaluated in research paper by (Albach 1986). They concluded that conducted EMI noise of 18dBuV has been improved by implementing frequency modulation. A similar approach of frequency modulation has been proposed by Lin and Chen (1994) and Lin (1992). Furthermore, the EMI spectrum has been improved by approximately 10 dBuV using a frequency modulation method in a quasi-resonant dc-dc converter (Vilathgamuwa et al. 1999). They also proposed a method of frequency modulation to modulate switching frequency around an average value set by a control loop. Rossetto et al. (2000), presented a PFC boost converter with modulation of switching frequency at 100 Hz. In this approach the switching frequency of the modulation is set to a minimum value when the value of input current is highest. This scheme was shown to reduce EMI noise and to minimize switching losses. A comparison of different modulation techniques such as triangular, sinusoidal and exponential schemes with low and high switching frequencies has been implemented and presented by Balcells et al. (2005). They concluded that to accomplish a wide spread of the EMI noise spectrum, a greater deviation is required for low switching

frequencies compared to high switching frequencies. However, it was determined that periodic modulation techniques have potential to control more precisely the spread of EMI noise in a desired range of frequency bands when compared non-periodic modulation techniques. The noise at required frequencies can also be minimized with periodic modulation techniques.

A comparison of EMI performance for different control schemes was presented by Mahdavi et al. (1996). These schemes are synchronous and asynchronous PWM, hysteresis control with fixed and varying band, and constant time-on methods. They concluded that the performance of fixed band hysteresis control is superior to other schemes. However, the selection of control parameters has not been discussed with respect of effectiveness of reduction of EMI noise. The chaotic operations of SMPS are also used to spread the EMI noise emission over the range of frequencies. There are two different methods to implement chaotic behaviour in a converter. (i) a separate chaos generator is implemented into the PWM control technique (Mukherjee et al. 2005; Aruna and Premalatha 2011). (ii) the chaotic operation with in a power converter is designed (Li et al. 2008; Banerjee et al. 2002; Li et al. 2009). Furthermore, the chaos is implemented in Integrated circuit (IC) of PWM control based converter (Mukherjee et al. 2008). Different frequency modulation schemes have been proposed in the literature to minimize EMI noise known as the frequency hopping scheme (Stone and Chambers 1995), sigma delta modulation (Paramesh and Jouanne 2001), bi-frequency scheme (Zhang et al. 1994), and multi-step optimal converter (Quevedo and Goodwin 2004). These schemes have been implemented and experimentally proved that the level of conducted EMI noise is improved by up to 10 dBuV.

A novel method of frequency modulation has been analysed and proposed in the literature known as random carrier-frequency (RCF) (Tse et al. 2000). In this scheme, the duty cycle is kept constant while the switching frequency is varied randomly. The comparison of standard and RCF modulation method is also presented with respect of spreading the EMI spectrum (Lin and Chen 1994). It has been proved experimentally that RCF modulation is more effective in spreading the noise over a spectrum of EMI frequency. Mihalic and Kos (2006) proposed another scheme to spread the EMI noise over range of frequencies known as Random PWM (RPWM). In this scheme, the frequency of the switching device is maintained constant while the pulse width is varied randomly but the average of pulse width is set to the desired duty cycle required for regulation of output voltage. It has also been proved that the noise spectrum at lower

frequency range remains constant in the RPWM technique (Nave 1989). This would result into the limitation of effectiveness in this scheme that it is only suitable for high-frequency noise improvement.

3.3.6 Switching transition modifications

Voltage and current transition (dv/dt & di/dt) is a major cause of EMI noise generation in SMPS. EMI noise can be minimized by optimising the waveforms of the voltage across and/or current through switching devices. There are different techniques applied to shape the waveform of switching devices, such as, gate-drive modification, snubber, clamp circuits and soft-switching techniques.

3.3.7 Gate-drive modification

The slope of dv/dt and di/dt has an effect on conducted EMI noise. Lower transition rates of voltage and current waveforms result in minimizing EMI noise. However, this scheme only reduces high frequency noise content and low frequency noise content remains unchanged (Nave 1989). A simple approach has been implemented to decrease the slope of transition by increasing gate resistance of a switching MOSFET (Rashid 2007; Rossetto et al. 2000). As a result, the switching losses would be increased in this scheme. Another method of controlling the voltage and current slopes separately for switching devices has been implemented to limit EMI noise (Consoli et al. 1996).

3.3.8 Snubbers

Snubbers are commonly used to dampen the oscillation of voltage spikes across switching devices. It also helps to soften the switching transition. This can be considered as a form of low-pass filter as it eliminates the high frequency content of the switching period (Whittington et al. 1997). However, it increases power losses in a circuit and reduces the efficiency of converter. Therefore, these snubber circuits are not suitable for higher power converters due to increased complexity, cost and size. Low power dissipation snubbers with additional components have been proposed in the literature (Jinno et al. 2009). On the other hand, conduction losses and conducted EMI noise increases due to an additional component (Fujiwara and Nomura 1999). Snubbers can be implemented with active and passive components leading to classification of

active and passive circuits. There are additional voltage and current stresses present in lossless passive snubber circuits. In forward converters, the lossless active snubber has been improved by an addition of an inductor, capacitor and diodes (Jinno et al. 2009). Also the forward converter, a novel scheme has been introduced known as the regenerative snubber. In this technique, a regenerative circuit is used to reset transformer windings with the help of snubber circuits as shown in figure 24 (Abramovitz et al. 2010). There are also other benefits of these lossless snubbers such as reduced voltage spikes of dv/dt, achieving Zero Voltage Switching (ZVS) for switching devices and transferring recovered energy back to the source and load. In addition, more components are required to design regenerative snubbers and extra windings produce voltage spikes across the diodes.

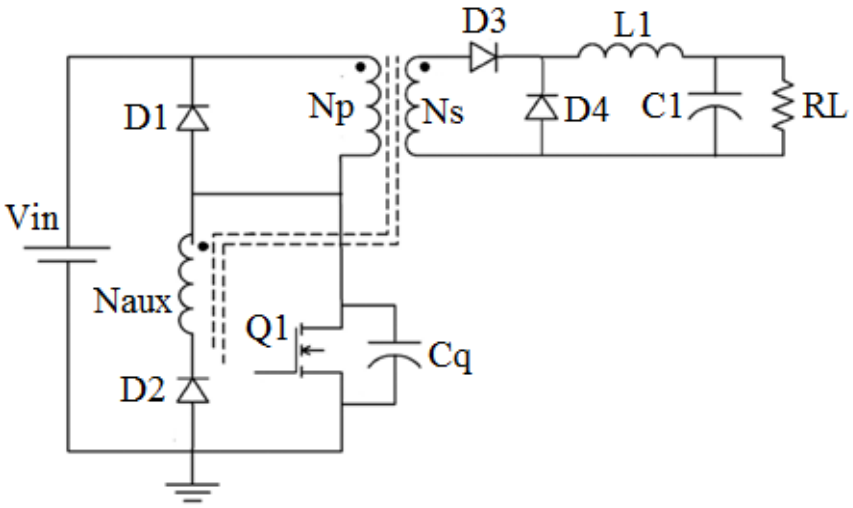


Figure 24: A typical energy regenerative snubber (Abramovitz et al. 2010)

3.3.9 Clamp circuits

Active clamp circuits are also used for mitigation of voltage ringing across switching devices (Lee et al. 2006; Mao et al. 2005). Mao et al. (2005), describe a half-bridge converter employing an active clamp snubber circuit. However, in a conventional half-bridge converter, the MOSFET body diode reverse recovery current produces an EMI noise at higher frequencies due to oscillations at turn OFF time. The proposed active-clamp in figure 25 makes stops diode conduction which reduces conducted EMI noise.

Moreover, the leakage inductance of the transformer's stored energy is transferred to the snubber capacitor during off-time, which eliminates ringing.

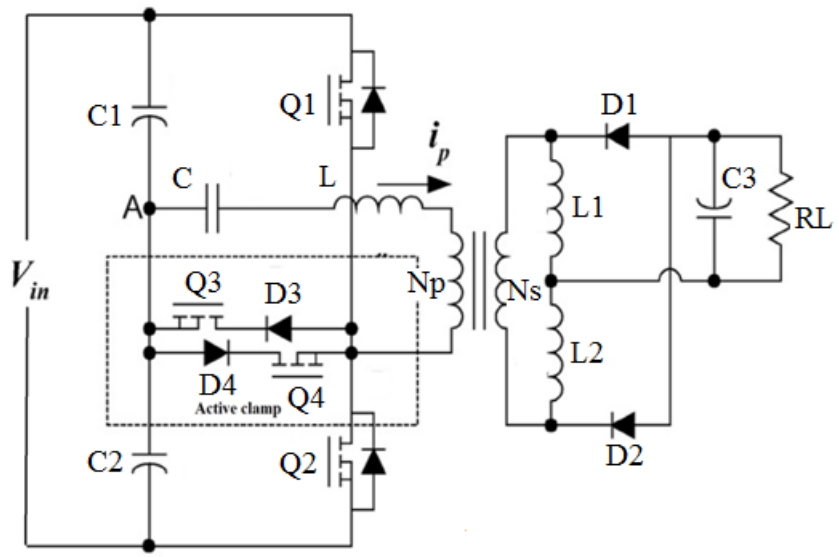


Figure 25: Active clamp for half bridge converter (Mao et al. 2005)

3.3.10 Soft-switching technique

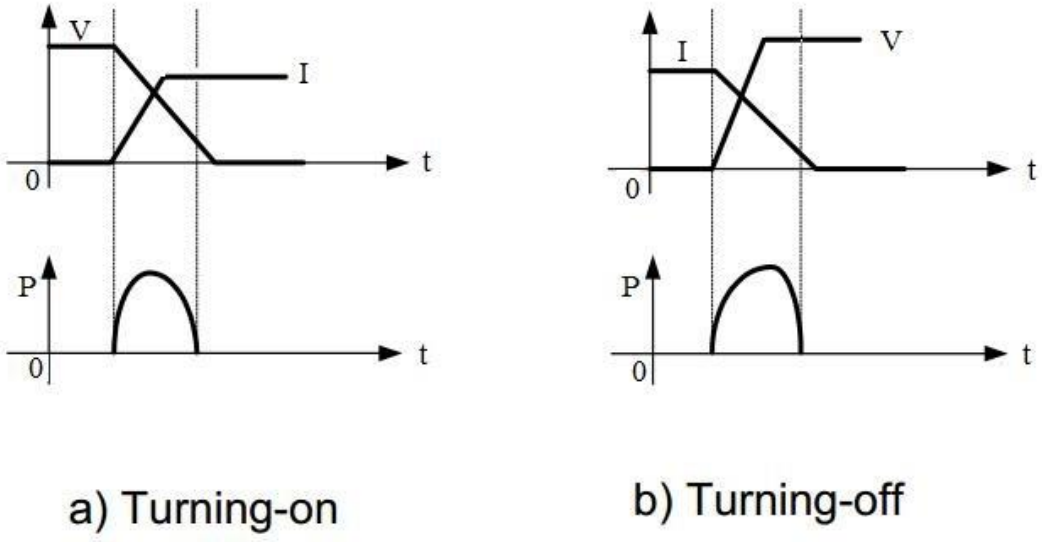


Figure 26: Hard Switching waveforms

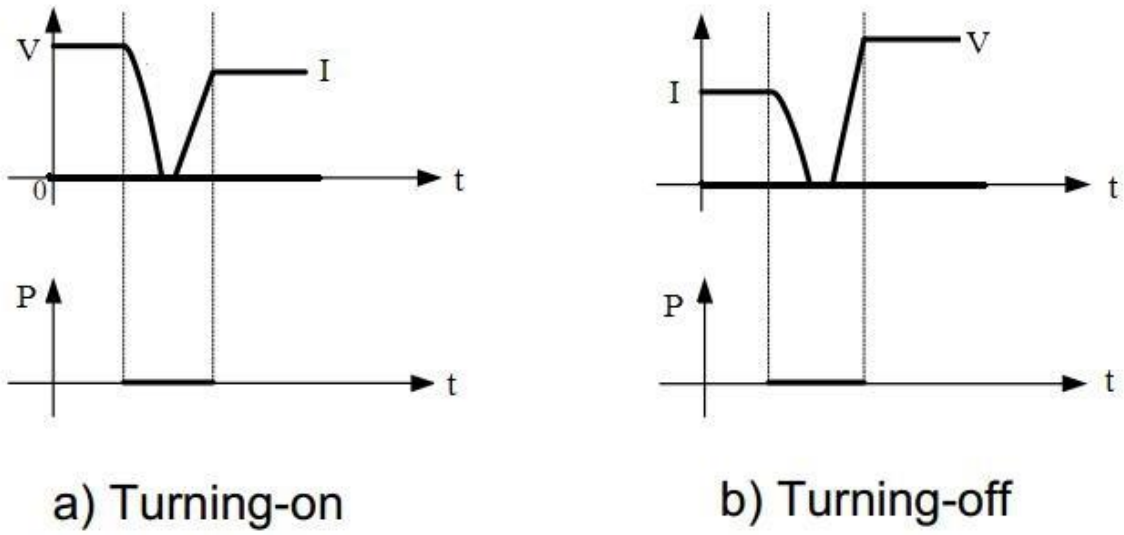


Figure 27: Soft Switching waveforms

There are two types of switching techniques used in SMPS to control the switches: hard switching and soft switching. In hard switching techniques (as shown in figure 26), the change of high dv/dt and di/dt is the major cause of high switching losses as well as high EMI noise. Conversely, soft switching techniques minimize the switching losses due to the switch turn ON at zero voltage and the switch turn OFF at zero current with the help of resonant techniques (as shown in figure 27).

Soft-switching techniques can also reduce dv/dt and di/dt in order to reduce EMI noise (Chung et al. 1998; Yoshida et al.2003; Yazdani and Farzanehfard 2012; Zhaoming et al. 2000). A review of different soft switching techniques have been presented in the literature (Ching and Chan 2008). The comparisons of soft and hard switching techniques have also been presented in Chung et al. (1998). These switching techniques have been applied to buck, boost and flyback converters experimentally and the results have demonstrated significant reduction of EMI noise. Berg and Ferreira (1998) showed experimentally that EMI noise can be improved by up to 10 dBuV for the case of the PFC boost converter. However, Zhang et al. (1996) argues that the noise spectrum of soft switching PFC does not show the same level of improvement as the hard switching PFC for the same power rating. This is attributed to extra noise arising from the auxiliary switch used in the soft switching technique. Furthermore, the layout of the auxiliary component can also affect conducted EMI noise in the soft-switched converter. Caldeira et al. (1993) present a comparison of conducted EMI noise in hard

and soft-switching converter designs. They conclude that properly considered snubbers for hard-switched converters can improve the spectrum of EMI noise to a level similar to that of the resonant converter. An optimization process for the quasi-resonant converter has been proposed and analysed by Joshi and Agarwal (1997). This optimization process improves the spectrum of conducted EMI noise by damping the voltage and current spikes.

3.3.11 Interleaving

Interleaving is another method to reduce EMI noise in SMPS (Zhang et al. 2013; Spano et al. 2014) which is best suited for high power converters. In this approach, parallel switching devices are connected in a way that the switching frequency remains constant and switching times are sequenced by phase shifting (Smolenski et al. 2014). In Wang et al. (2007) and Yang et al. (2010), the interleaved converter have been proposed and analysed. They proved experimentally that line ripple current can be minimized and conducted EMI noise reduced in the interleaved converter. The approach also helps to reduce the size of the magnetic component needed for filtering (Zumel et al. 2009; Barbosa 2002). It also reduces the ripple measured at the output capacitor, reduces component stress, and increases converter reliability (Jang and Jovanovic 2007; Sudhakarababu and Veerachary 2005). The overall costs of these converters does not increase considerably as they require lower rating current devices due to sharing of current in the interleaved components (Veerachary et al. 2003). The main drawbacks of these converters are larger size and extra components required in the design.

3.4 Techniques to reduce EMI Noise propagation

Conducted EMI noise mitigation applied along propagation paths can be divided into internal and external noise reduction techniques. The EMI filter section can also be subdivided into ‘internal EMI filter’ and ‘external EMI filter’ as discussed in the following section.

3.4.1 Internal EMI filter

The EMI noise in a SMPS can be minimized through use of an internal EMI filter with the help of providing noise current circulation paths within the converter itself. Several techniques have been proposed in the literature to circulate the noise current internally.

These can be classified into parasitic cancellation, compensation circuits and the balanced approach.

3.4.1.1 Parasitic cancellation

Parasitic components play an important role in providing a conduction path for CM noise within a converter. Thus the cancellation of parasitic elements would help to significantly reduce EMI noise in a SMPS. The main cause of parasitic elements is the presence of non-ideal behaviour of passive and active components in different frequency bands. An additional circuit is added to introduce a negative capacitance for cancellation of parasitic capacitance (Wang and Lee 2007). As a result, EMI noise is reduced significantly enhancing converter performance. Knurek (1988) also presented a method to reduce EMI emission by controlling the parasitic capacitance (primarily the heat sink and transformer winding capacitance) in SMPS. He presented several methods to control the parasitic capacitance associated with the heat sink, including use of a shielded insulator for the heat sink, moving the output filter choke to the negative lead and by addition of a snubber circuit. He showed experimentally that a significant reduction of EMI is possible through control of parasitic capacitance. Mee and Teune (2002) concluded that there are several methods to improve the EMC performance of SMPS, such as, minimizing loop areas in the layout, reducing the parasitic inductance and capacitance, and that input and output filters must have the low Equivalent Series Resistance (ESR). Other researchers have also proposed techniques to mitigate EMI noise through parasitic cancellation (Wang and Lee 2010; Wang et al. 2010; Fu et al. 2013).

3.4.1.2 Compensation circuits

Compensation methods are also an effective way to mitigate EMI noise within a converter. These are usually used to mitigate CM noise by minimizing earth leakage current (Ogasawara and Akagi 1996; Julian et al. 1996). Normally, an additional circuit is added to generate a compensation voltage of equal magnitude and out of phase with the original noise. These schemes can be divided into two categories passive and active techniques. Passive compensation techniques are easier to design and also cheaper as compared to active cancellation schemes. On the other hand, active solutions are more flexible to implement. Ogasawara and Akagi (1996), Xin et al. (1999) and Xin et al. (2000) proposed passive compensation schemes for minimizing current due to earth

leakage. Active compensation networks have been proposed for mitigation of CM noise in different converters (Ogasawara et al. 1989; Zhang et al. 2007). In Zhang et al. (2007), digital active cancellation can be implemented by DSP to sense CM noise and mitigate it through generating compensation noise. These active schemes are effective in mitigating EMI noise for switching frequencies up to 10 MHz.

Buck converter have been analysed with this technique and the simulation results shown that ripple current is substantially reduced in these converters (Kolar et al. 1997).

3.4.1.3 Balance Approach

Balance technique is the combination of parasitic cancellation and compensation network to confine CM noise within a converter. In this approach, the concept is to balance the impedances of noise source for mitigation of CM noise. This scheme proposes a simple and compact converter design as there is no need of external filter for noise reduction. A novel technique known as balanced switching conversion has been proposed in the literature to reduce the common mode conducted EMI noise (Shoyama et al. 2003; Wang and Lee 2007). The main reason for common mode EMI noise in a conventional unbalanced converter is to rapidly change the drain voltage which affects the current flow through parasitic capacitance between drain/collector of an active switch and the converter ground rail. In order to solve this problem, Shoyama et al. (2003) modified the conventional converter as shown in figure 28.

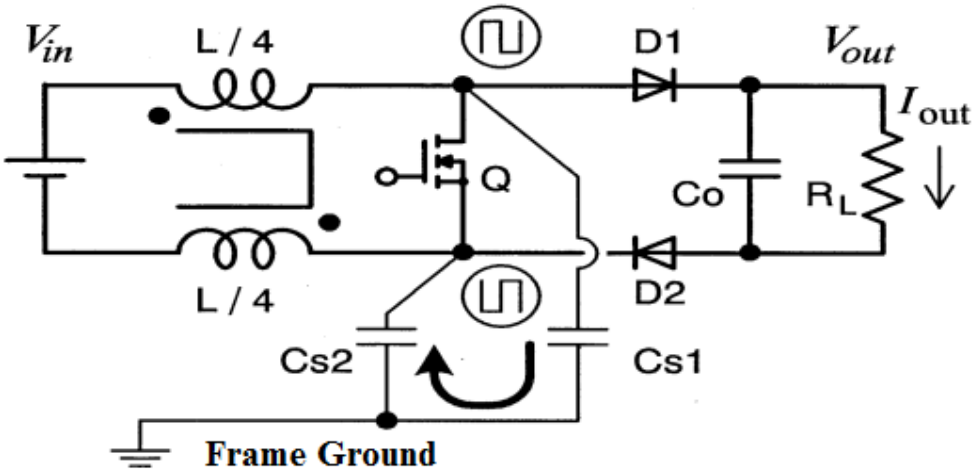


Figure 28: Balanced Boost Converter (Shoyama et al. 2003)

In the balanced converter, the winding of an inductor is divided equally into two parts, as a result the drain and source voltages of MOSFET change complementarily. Also

CM current is confined within the converter and CM noise is considerably reduced overall. Wang et al. (2007) have analysed the EMI performance of the boost converter model. They proposed the general balance technique to minimize the common-mode noise. In this technique, two methods were introduced:

Reduction of CM noise due to the abrupt change of MOSFET source voltage:

In this method, the boost inductor is split into two parts to balance the parasitic capacitance of source/drain with the ground. As a result, the CM noise is relatively reduced compared to the unbalanced converter.

Reduction of CM noise due to output capacitor voltage:

There are two possible methods to mitigate the CM noise due to output capacitor voltage.

- Reduce the parasitic capacitance between the load and ground
- Reduce the ESL (Equivalent series inductor) and ESR (Equivalent series resistor) of output capacitors.

Several other techniques have been proposed in the literature to reduce EMI noise internally and to enhance the efficiency of SMPS (Knurek 1988; Mee and Teune 2002; Bera et al. 1999).

3.4.2 External EMI filter

The principle approach to reduce the noise is to incorporate EMI low pass filters. The EMI filters are classified as passive, active or hybrid types depending on the technique employed. Passive filters use only passive components and are normally bulky. On the other hand, active filters use active electronic circuits and are normally not bulky as compared to passive filters (Hamza and Mei 2013). Often passive and active filters are combined to form hybrid EMI filters (Biela et al. 2009; Ali et al. 2012). Both types are discussed in the following sections.

3.4.2.1 Passive EMI filter

Passive EMI filter is commonly used for mitigation of EMI noise in SMPS. A number of research articles have been proposed technique for designing EMI filter (Raggl et al. 2010; Hsieh et al. 2008; Kotny et al. 2014; Makda and Nymand 2014). Conversely, the

design of such a filter is challenging in power electronics because the noise sources and load impedances are not constant for this filter (Nave 1991). The filter topology commonly used as a passive filter is shown in figure 29.

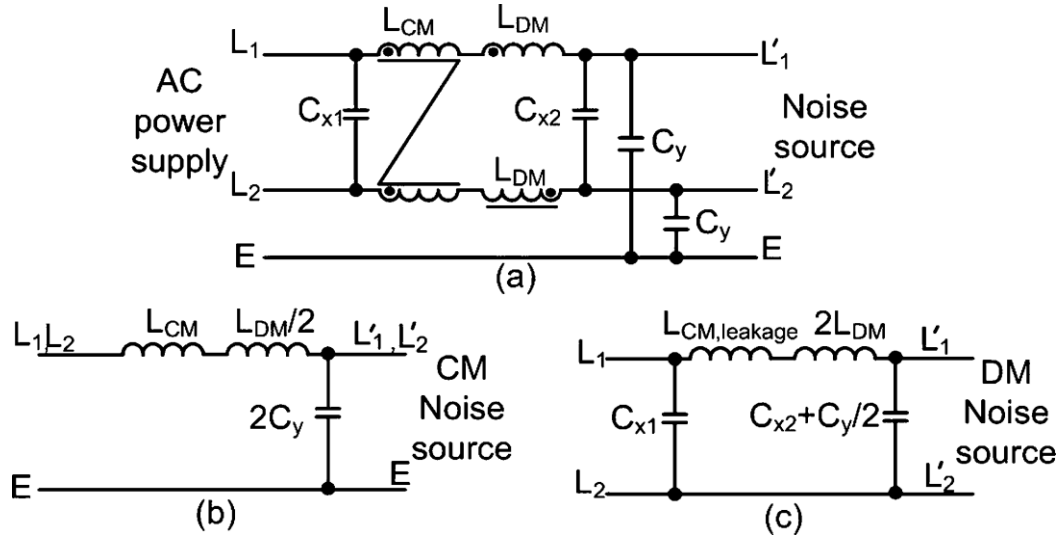


Figure 29: (a) EMI Passive filter (b) Common-mode filter (c) Differential-mode filter (Nave 1991)

It is noticed from figure 29 that some elements of the filter affect common mode (CM) or differential mode (DM) noise only and some affect both CM and DM noise. A common mode choke (Lc) affects CM noise only but the leakage inductance Lm between the two windings affects the DM noise. The X-capacitors affect only DM noise. While the Y-capacitor suppresses both the DM noise and CM noise, practically the large value of X-capacitor minimizes the effect of Y-capacitor on DM noise. Similarly, Ld suppresses both CM noise and DM noise, practically the large value of Lc minimizes the effect of Ld on CM noise.

Typically, these filters act as a low pass filter. In order to design a suitable passive filter, it is important to discern between DM noise and CM noise (Adirci et al. 2005). Guo et al. (2002) , Musznicki et al. 2008 and Caponet et al. (2001) have demonstrated a noise separator to isolate DM noise and CM noise. They proved that in order to design an effective EMI filter it is important to minimize the dominant component of the conducted noise. The next step is to measure the impedances of noise source for both DM and CM noises.

There are several methods discussed in the literature to measure the impedances of noise source for common-mode and differential-mode noise, such as, the resonance method, the insertion loss method and the two probe method. In the resonance method,

the input of the SMPS has been terminated with the opposite reactive component compared to noise source reactance (Nave 1991). The right choice of the values of the component is found empirically. In this method, the parasitic effects of reactive components become significant due to the circuit operating at high frequency and the circuit topology to measure the noise source impedance is not valid. On the other hand, the insertion loss method also requires some prior conditions to be fulfilled in order to measure the noise source impedance (Zhang et al. 2000). These conditions (depending on the value of inserted component) are that the inserted component impedance must be significantly smaller or larger than the noise source impedance. A novel method known as the two probe approach to measure the noise source impedance of SMPS has been developed in order to overcome the problem faced by previous (See and Deng 2004; Tarateeraseth et al. 2010). In this method (two probe method), noise source impedance can be measured by using a signal generator, spectrum analyser, some coupling capacitors, injecting current probe and receiving current probe. First the impedances of noise source are measured then the filter component parameters can be designed according to impedance-mismatch criteria (Nave 1991). To further improve the performance of the EMI filter, Ye et al. (2004) suggested maximum and minimum values of impedances required in the design of a passsive EMI filter. They designed an EMI filter for SMPS and also presented the experimental results to demonstrate that this method is an effective and simple way to design an EMI filter.

Passive EMI filters have components, such as, capacitors and inductors. These are not ideal components and the performances of these components depend on self-parasitic and parasitic coupling between components. Equivalent series inductance (ESL) for capacitors and equivalent parallel capacitance (EPC) for inductors are a very important factor for their performances. The performances of passive EMI filters have been affected by parasitic components at high frequencies. Neugebauer and Perreault (2006) have proposed a novel method (using an extra transformer and a capacitor) to cancel the effect of parasitic capacitance of the filter inductor at high frequency and to improve high frequency performance. Wang (2005) and Wang et al. (2006) proposed a method to cancel the effect of equivalent series resistance (ESR) and equivalent series inductance (ESL) of the capacitors. They arranged the capacitors in a network with extra inductors and resistors. As a result, the network acts as a filter in which the capacitor behaves without parasitic equivalent series resistance (ESR) and equivalent series inductance (ESL) improving the filter performance. Leakage inductance of

coupled inductors has also been used to cancel the effect of equivalent series inductance (ESL) of a capacitor in a filter (Pierquet et al. 2006). Conversely, Wang et al. (2008) integrated different parasitic cancellation techniques into one EMI filter to suppress the effect of components parasitics on EMI filter performance. They proved experimentally that the performance of both DM noise and CM noise filters were improved by integrating the parasitic cancellation technique.

The wide ranging variation in source and load impedances also affects the performance of an EMI filter and these filters are essentially non-dissipative. Several methods have been proposed to design the filter which can dissipate the unwanted signal (Ozenbaugh and Pullen 2011; Broyd´e 1988). But these filters have high power losses and are expensive compared to a non-dissipative filter (passive EMI filter).

3.4.2.2 Active EMI Filter

Active filters use active electronic components and are a possible alternative to bulky passive filters. AEF can be classified into two types, depending on the detection of disturbances at the source and/or at the receiver, such as, feed-back and feed-forward type. In feed-back AEF, the disturbance is sensed at the receiver and uses a control loop (feedback) to diminish the conducted EMI noise. On the other hand, feed-forward AEF, the disturbance is detected at the source and the noise is compensated by inserting an opposite polarity of equal amount of noise to reduce the noise level.

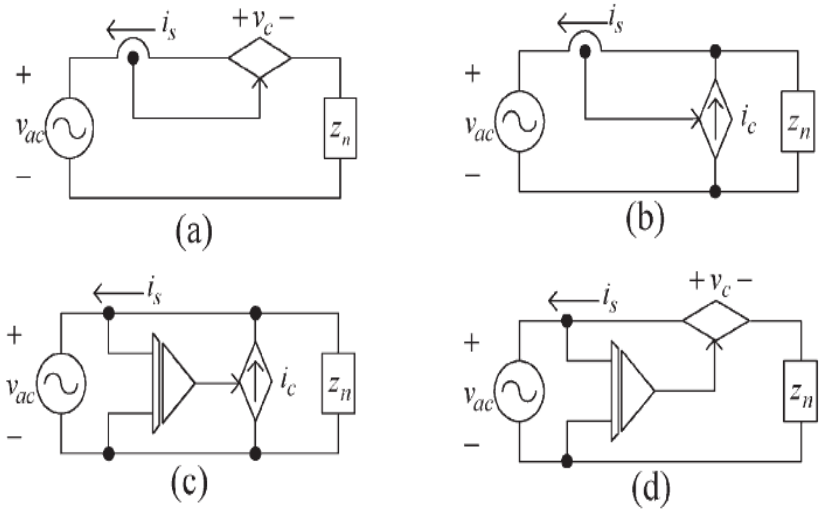


Figure 30: Feed-back Active EMI Filters. (a) Current-sense voltage compensation (b) Current-sense current compensation(c) Voltage-sense current compensation (d) Voltage-sense voltage compensation (LaWhite and Schlecht 1986; Poon et al. 2000)

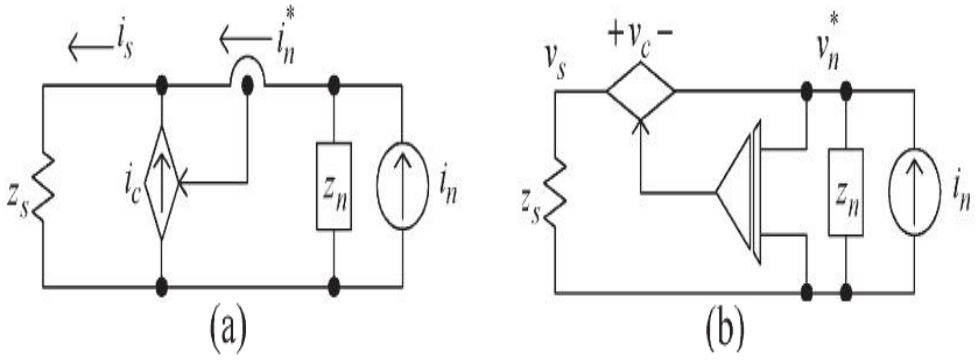


Figure 31: Feed-forward Active EMI Filters.(a) Current-sense current compensation (b) Voltage-sense voltage compensation (Nasiri 2005)

Feedback AEF can be configured into four topologies as shown in figure 30, depending on the basis of how the noise is detected and compensated. The noise can be sensed either by voltage or current across the inductor, similarly the compensation through the injection of either a shunt current or series voltage (LaWhite and Schlecht 1986; Poon et al. 2000). According to this compensation method, the AEF can be classified into two types such as series-voltage compensation and shunt-current compensation. The series path effective impedance is increased by series-voltage compensation while the shunt path effective impedance is decreased by shunt-current compensation. Feed-forward AEF can be configured into two topologies as shown in figure 30 dependent on the basis of compensation and noise sensed. In general, feedback and feed-forward AEFs can be applied for mitigation of both CM and DM conducted EMI noise.

Integration of both feedback and feed-forward AEF techniques have been presented in order to achieve the desired noise attenuation and to lessen the total dimension of the filter compared to passive EMI filter(Chow and Perreault 2003;Nasiri 2005). Hamill (1996) has also proposed the arrangement of both feed-back and feed-forward active EMI filter to mitigate the noise to the desired level, easily. He has also explained the details of the components used to design for the active EMI filter.

Hybrid EMI filtering is formed by the combination of passive and active EMI filters (Biela 2009). It can also improve the overall performance of noise reduction. In a hybrid EMI filter, the noise level is first reduced by a passive filter to the level that can be handled by the active EMI filter. Moreover, Ali et al. (2014) have proposed hybrid EMI filtering with the help of integrated PCB active filtering and passive EMI filtering.

It have been proved experimentally that EMI noise is reduce significantly at low and high frequency and also overall size has been reduced.

3.5 Summary

Electromagnetic Interference (EMI) can easily couple into the audio power amplifier supply rail and is manifest as harmonic distortion in the audio output thereby reducing reproduction fidelity. The principle approach to reducing noise is to incorporate active or passive (external) EMI filters. Also the other technique known as internal EMI filter is used to mitigate the noise internally and effectively reduce the size of filter. Ultra-low noise SMPS designs are possible for audio system as dynamic signal transient are not an issue in this case. To cope with these requirements, the principal aim of this research project is to develop and characterise novel low noise switch mode power supplies for audio power output products. However, the internal EMI filters is investigated to mitigate the EMI noise internally in SMPS. Further investigate the novel technique of internal EMI filter to cope with the converter to mitigate noise internally. Also external EMI filter is incorporate in order to compliance with EMI regulatory requirements.

4 CHAPTER 4 NOVEL SMPS DESIGN AND CHARACTERIZATION

4.1 Introduction

In this chapter, a novel balancing technique for PFC boost, flyback and full-bridge converter has been proposed in order to mitigate CM noise internally. In addition, different prototypes of SMPS have been discussed and evaluated. Moreover, the experimental setup used to analyse SMPS for audio amplifier has been presented.

4.2 PFC Boost Converter

In Switched Mode Power Supplies (SMPS), Power Factor Correction (PFC) Boost converters are often used to achieve an improved power factor rating. The main cause of Common mode (CM) noise generation of a boost converter is discussed in the following section. To analyse and develop a reliable CM noise model of a converter it is necessary to obtain a detailed understanding of the noise generation mechanism.

4.2.1 CM noise generation and coupling path

Normally heat sinks are attached to switching devices to protect these devices from thermal runway. These heat sinks are mostly connected to earth through insulating material for safety reasons. As a result, a small parasitic capacitance is typically introduced between the heat-sink and case of the MOSFET. Futhermore, dielectric behaviour is added into the circuit due to the insulating material used for electrical isolation between the heat-sink and ground. Although the parasitic capacitances are usually in the pico-farad range the high voltage transition (dv/dt) due to switching action causes substantial current flow through these capacitances increasing the CM noise. Therefore, these parasitic capacitances cannot simply ignore with in a converter. The parasitic capacitance between MOSFET drain and ground is denoted by Cq. While the parasitic capacitance between diode cathode and ground is represented by Cd.

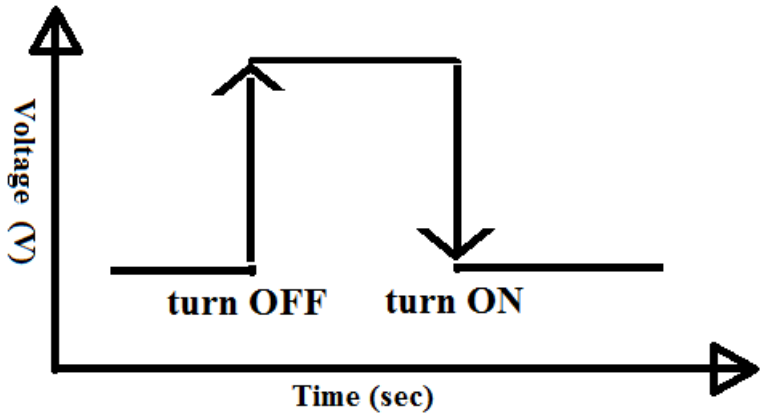


Figure 32: Switching transition of MOSFET

In figure 32, during switching transition from turn ON to OFF, the potential at node Q (as shown in figure 33) changes from low to high. As a result, the parasitic capacitance is charging due to current flowing through it. Similarly, during switching transition from turn OFF to ON, the potential at node Q changes from high to low. That results in a discharging current flow out of the parasitic capacitance. Therefore, the above mentioned current of parasitic capacitance follows the path through these capacitances to ground and returns back via live and neutral lines.

4.2.2 CM noise model of a converter

Consider a boost PFC converter as shown in figure 33. The equivalent circuit of Line impedance stabalization network (LISN) is also indicated with a coloured solid line. It is normally used to stabilize input impedance for measurement of conducted EMI noise.

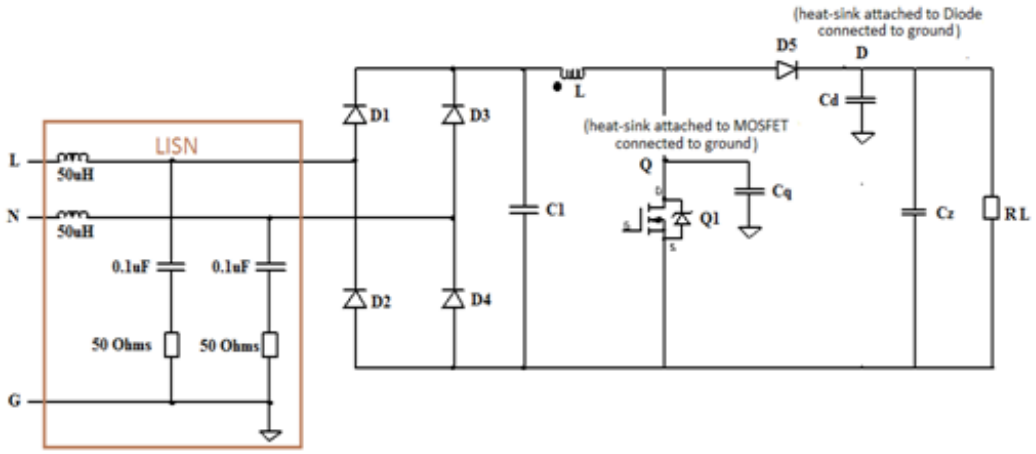


Figure 33: PFC Boost Converter

The parasitic model of high frequency components within a boost converter that affect voltage and current in a circuit is shown in figure 34. In a CM noise model of a boost converter, LISN inductors and capacitors are ignored and resistors of 50 Ohm are denoted with R1 and R2. Moreover, for simplicity of the model, full-bridge diodes are replaced by a short circuit. However, a high frequency inductor model is indicated by EPC (equivalent parallel capacitance) and EPR (equivalent parallel resistance). EPC denotes the capacitance of winding occurring within a boost inductor and EPR represents the winding losses in the inductor. The input and output capacitors include ESR (equivalent series resistance) and ESL (equivalent series inductance). ESR and ESL indicate the existence of resistance and inductance in capacitor plates and leads. The output diode includes the junction capacitance parallel to diode represented with Cj. The node Q and D represent the parasitic capacitance of MOSFET and diode respectively.

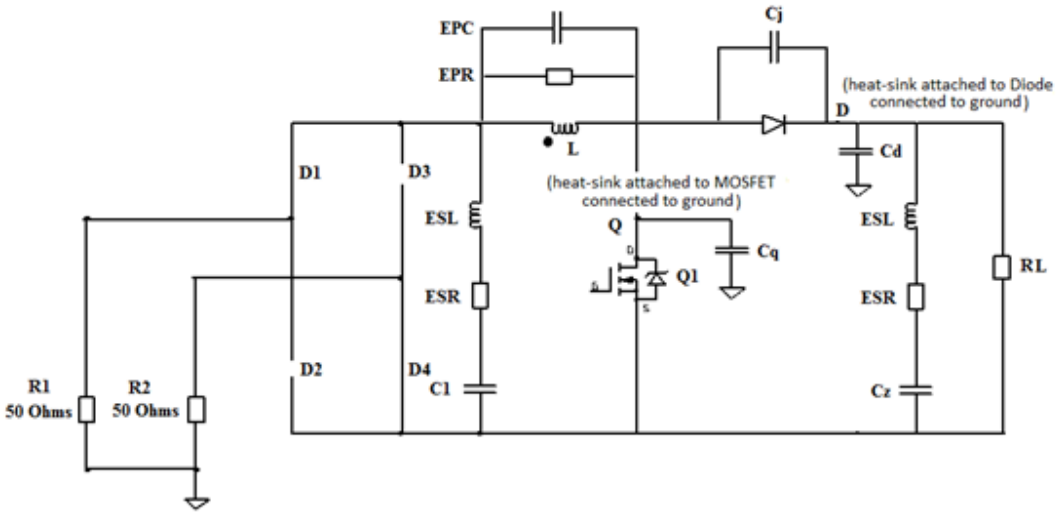


Figure 34: CM noise model of PFC Boost Converter

4.2.3 CM noise flow in PFC boost converter

During MOSFET turn ON

Consider the case, when bridge diodes D1 and D4 are conducting in a boost converter (figure 35). The voltage at point Q reaches to zero and D5 become reverse biased during the MOSFET turn ON period. The parasitic capacitance of MOSFET Cq discharge through D1 and D4 to LISN resistors R1 and R2 respectively. However, the parasitic capacitance of diode Cd also follows the same path by passing through load

capacitor. Moreover, the CM noise propagation path during MOSFET turn ON is shown in figure 35.

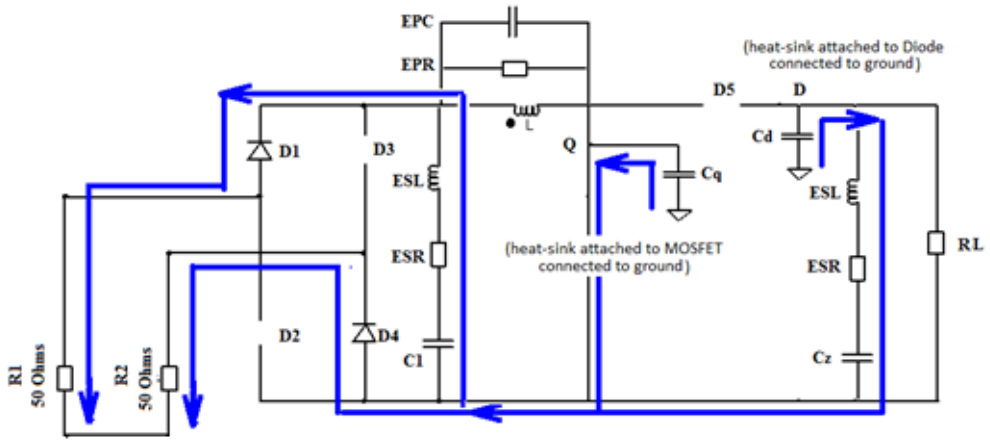


Figure 35: CM noise flow during MOSFET turn ON

During MOSFET turn OFF

The CM noise propagation path during MOSFET turn OFF is shown in figure 36. The voltage at point Q reaches to Vo and D5 becomes conducting during the switch off period. Therefore, the parasitic capacitance of MOSFET Cq charges up and CM noise flows to ground returning through LISN resistors R1 and R2. However, the parasitic capacitance of diode Cd also charges up and CM noise flows to ground and returns through LISN.

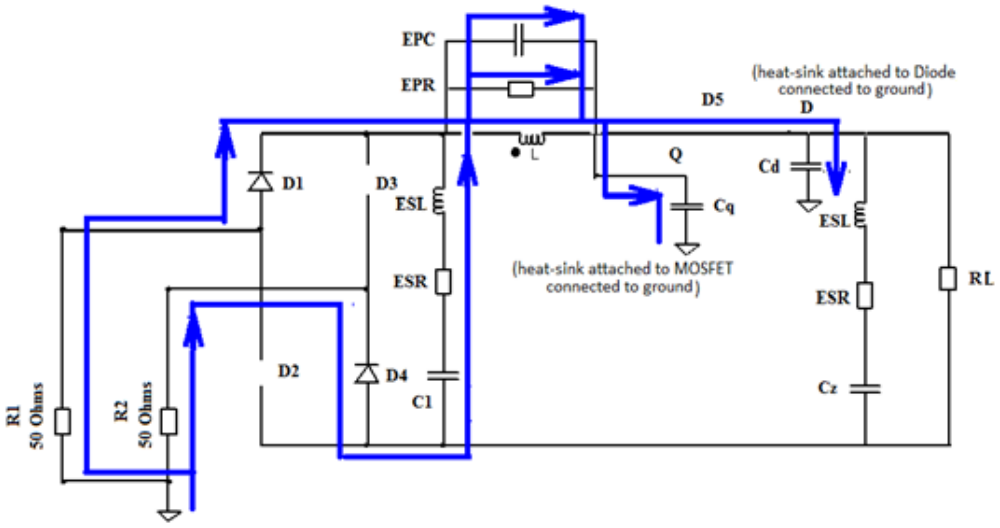


Figure 36: CM noise flow during MOSFET turn OFF

In a boost converter, the switching MOSFET and diode are the dominant components contributing to CM noise. Therefore, a simplified CM noise model that focuses on these components can be used to evaluate converter noise generation. Moreover, the input MOSFET can be change by an equivalent source of voltage that has exactly equal magnitude of voltage as compared to the voltage across the MOSFET as shown in figure 37.

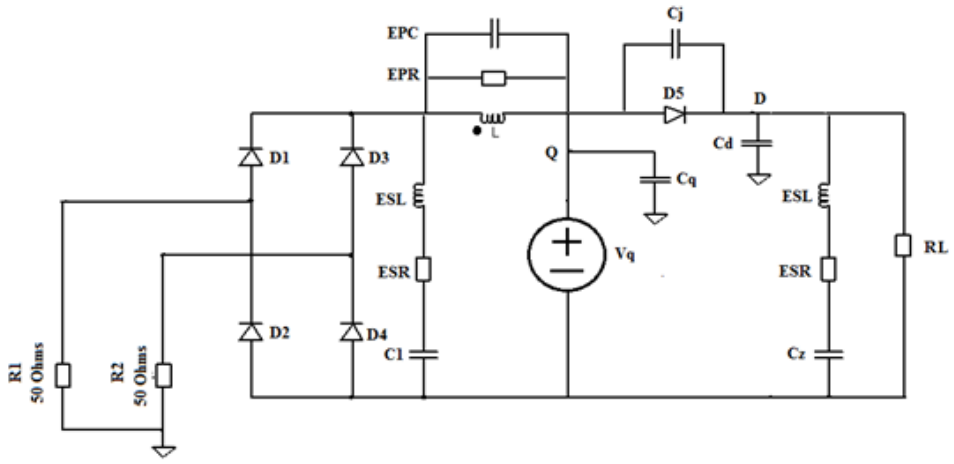


Figure 37: Modified CM noise model of PFC Boost Converter

4.2.4 Simplified CM noise flow in PFC boost converter

During MOSFET turn ON

Simplified model of PFC boost converter is shown in figure 38. The conducting bridge diodes are representing with short circuit in high frequency simplified model. The impedance of capacitor Xc=1/(ωL) is very low at high frequency and acts as a short circuit for high frequency current. Therefore, input and output capacitors can be replaced by a short circuit. The CM noise current can discharge parasitic capacitance of the MOSFET/diode pair through LISN resistors and return back through ground.

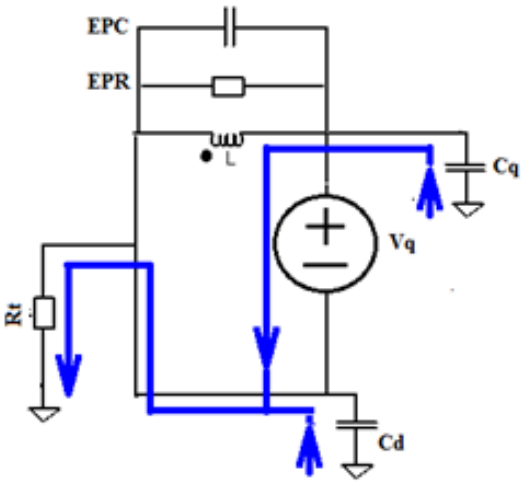


Figure 38: Simplified CM noise flow during MOSFET turn ON

During MOSFET turn OFF

The simplified model of PFC boost converter is shown in figure 39. Similarly, the input and output capacitors act as a short circuit for high frequency model on noise. CM noise current can flow to ground through parasitic capacitance of MOSFET/diode and return through LISN resistors.

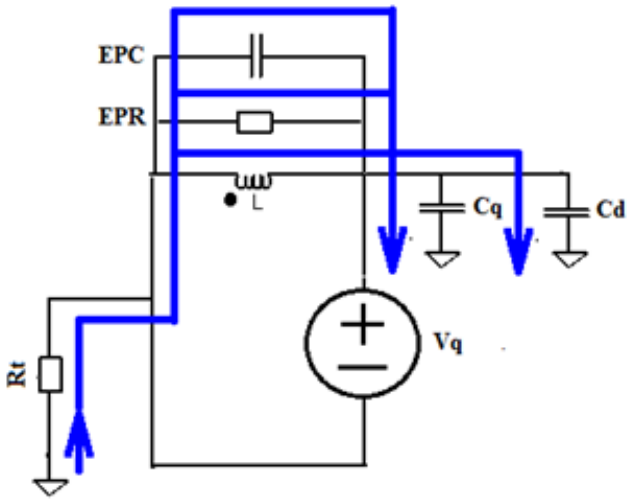


Figure 39: Simplified CM noise flow during MOSFET turn OFF

4.2.5 Proposed Balance Technique

CM noise is predominantly generated due to an imbalance of source and load impedances within a converter. It mainly arises as a result of switching transition of the MOSFET and parasitic capacitances Cq and Cd present in a circuit. Therefore, CM

noise generation is due to the switching action of MOSFET turn ON and OFF. In order to mitigate CM noise, a novel technique is proposed to balance the noise source and load impedance. The concept is to introduce an anti-noise source which has same magnitude and is 180° with the original noise source. This is achieved through addition of a coupled inductor with compensating winding Nc and compensating capacitor Cq' which are added to generate a complimentary voltage at node Q'. The voltage at Q' is 180° out of phase as compared to the voltage at Q producing a current in the opposite direction to cancel out the noise current of Cq. Furthermore, in a conventional boost converter, the heat-sink of the rectification diode is attached to ground as illustrated in figure 33. However, in the proposed converter, the heat-sink of the rectification diode is attached to the neutral line as shown in figure 40.

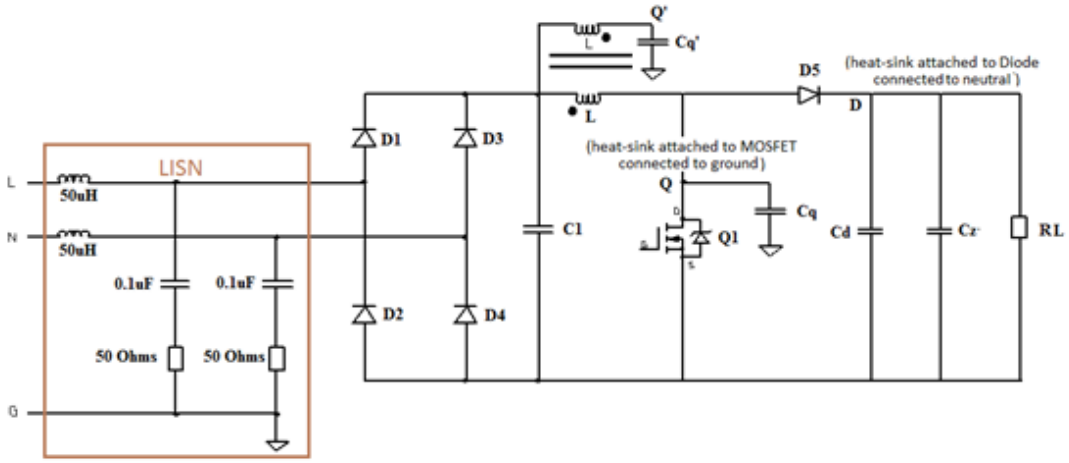


Figure 40: Balanced PFC Boost Converter

Similarly, the parasitic model of high frequency components within balance the PFC boost converter that effect voltage and current in a circuit is shown in figure 41. The node Q and Q' represent the parasitic capacitance of MOSFET and compensation capacitor respectively.

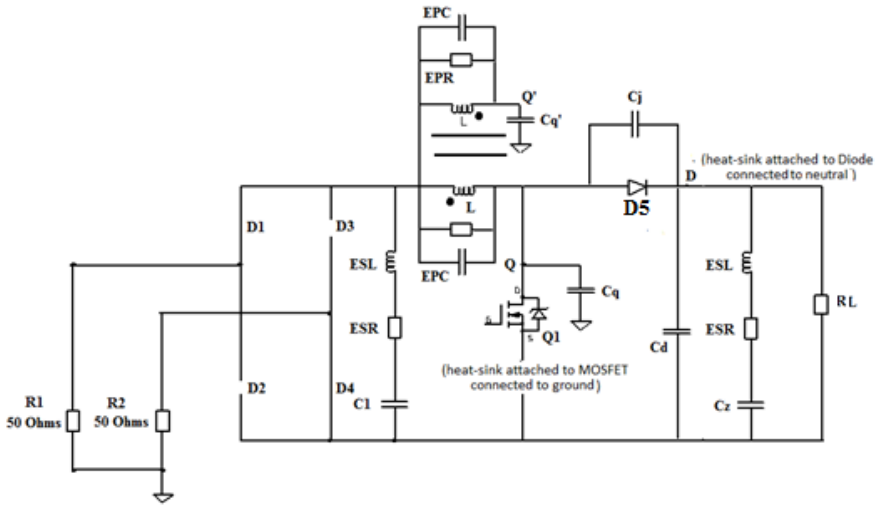


Figure 41: CM noise model of Balanced PFC Boost Converter

4.2.6 CM noise flow in Proposed Balance Technique

During MOSFET turn ON

Consider the case, when bridge diodes D1 and D4 are conducting in a boost converter (figure 40). The voltage at point Q and Q' are anti-voltage to each other due to dot position of coupled inductor. Therefore, voltage at node Q and Q' are low and high respectively. The parasitic capacitance of MOSFET Cq discharges through coupled inductor and Cq' (compensation capacitor) charges up through coupled inductor. As a result, CM noise of a converter can flow with in a converter and overall CM noise can compensated internally. CM noise flow path during MOSFET turn ON is shown in figure 42.

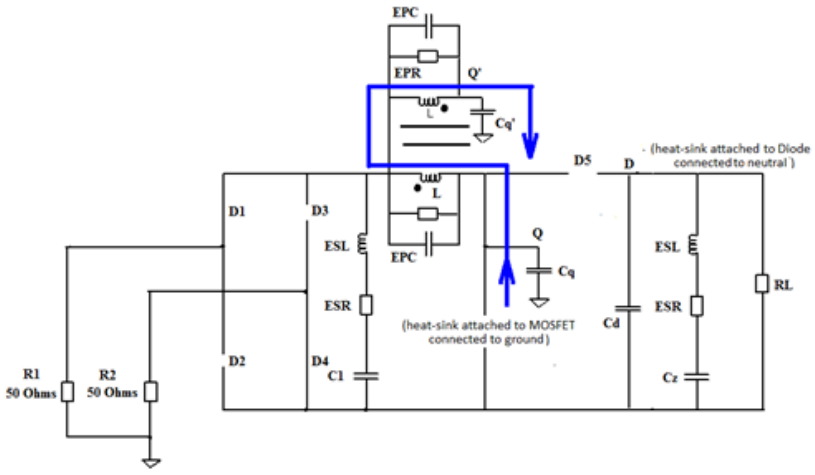


Figure 42: CM noise flow during MOSFET turn ON

During MOSFET turn OFF

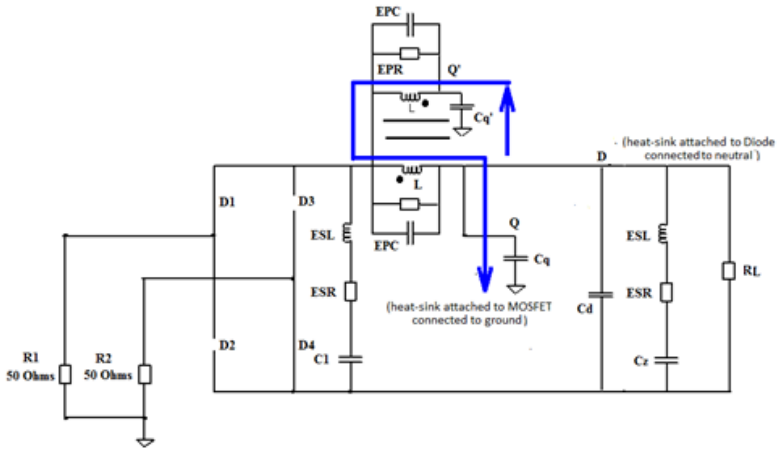


Figure 43: CM noise flow during MOSFET turn OFF

During MOSFET turn OFF, the voltage at point Q and Q' are in anti-phase to each other due to the dot position of the coupled inductor. Consequently, the voltage at node Q and Q' are high and low respectively. The parasitic capacitance of MOSFET Cq charges through coupled inductor and Cq' (compensation capacitor) discharges through coupled inductor. As a result, CM noise of a converter can flow with in a converter and overall CM noise can balance internally. CM noise flow path during MOSFET turn OFF is shown in figure 43.

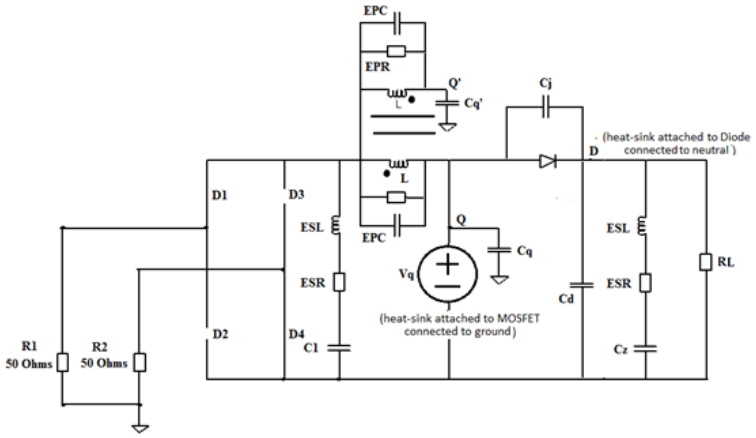


Figure 44: Modified parasitic model of Balanced PFC Boost Converter

The modified parasitic model of Balanced PFC boost converter is shown in figure 44. Similarly, the input MOSFET is replaced by an equivalent source of voltage that has an exactly equal magnitude of voltage as the voltage across the MOSFET.

4.2.7 Simplified CM noise model of balanced boost converter

During MOSFET turn ON

The conducting bridge diodes are represented with a short circuit in the high frequency simplified model. Similarly, input and output capacitors are replaced by a short circuit in a high frequency CM noise model. The CM noise current can discharge parasitic capacitance of MOSFET/diode through LISN resistors and return back through ground. However, CM noise current can charge through Cq' and return back through LISN resistors. Therefore, overall CM noises through LISN resistors are cancelled out due to direction of CM noise flow in reverse direction due to coupled inductor and compensating capacitor. CM noise due to MOSFET turn ON is shown in figure 45.

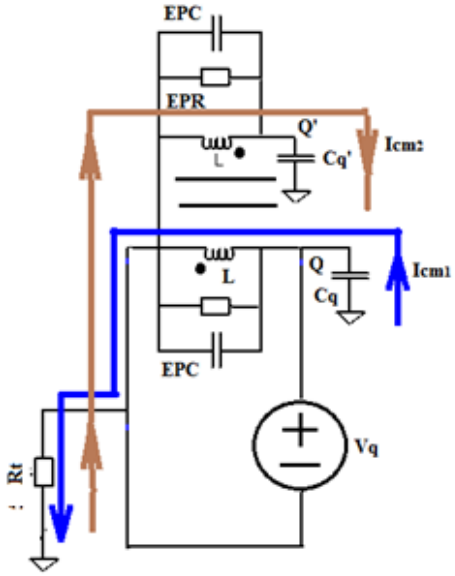


Figure 45: Simplified CM noise flow during MOSFET turn ON

During MOSFET turn OFF

The CM noise current can charge the parasitic capacitance of MOSFET/diode through LISN resistors and return back through ground. However, CM noise current can discharge through Cq' and return back through LISN resistors. Therefore, overall CM noises through LISN resistors are cancelled out due to direction of CM noise flow in reverse direction due to coupled inductor and compensating capacitor. Simplified CM noise due to MOSFET turn OFF is shown in figure 46.

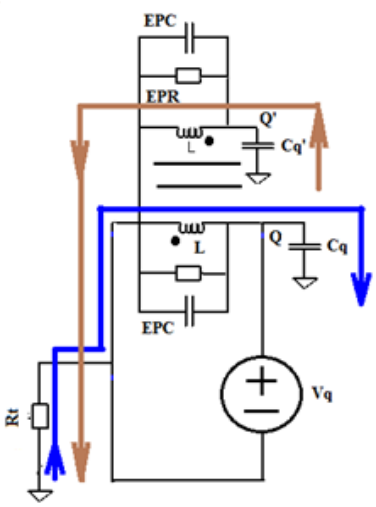


Figure 46: Simplified CM noise flow during MOSFET turn OFF

4.3 Fly-back Converter

4.3.1 CM noise generation and coupling path

In this section, CM noise generation and coupling paths are considered in detail. Understanding of CM noise generation would allow detailed analysis and provide a basis for mitigating CM noise through understanding of its coupling mechanism. Consider a flyback converter as shown in figure 47. At the front end of a converter, normally LISN is used to stabilize the impedance for conducted EMI measurement.

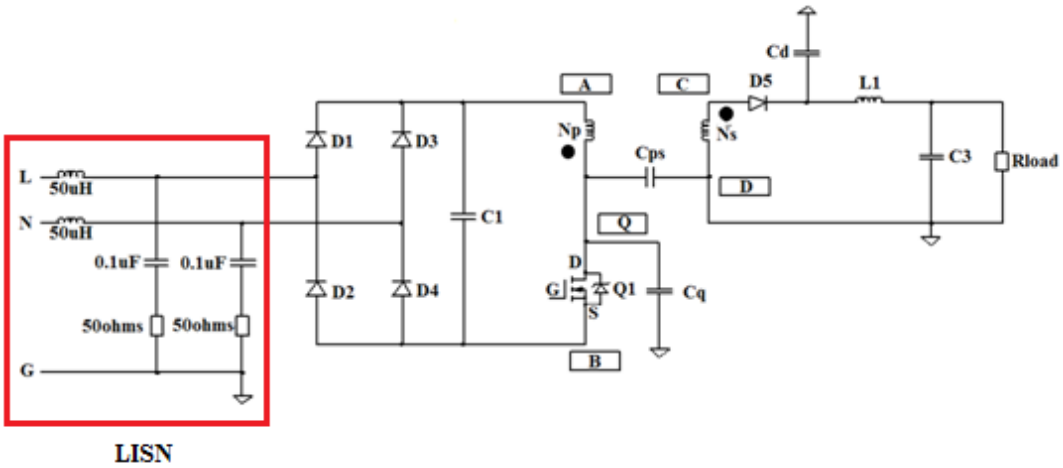


Figure 47: Flyback converter with its parasitic capacitances

Common mode (CM) Electromagnetic interference (EMI) noise in an isolated converter is typically caused by high switching transition (dv/dt) across switches. In the flyback converter, the sources of high dv/dt are MOSFET and diode. In figure 47, the parasitic capacitance between MOSFET drain and ground is denoted with Cq and the parasitic capacitance between Diode cathode and ground is represented with Cd.

A transformer model is necessary to understand the coupling path of CM noise. Therefore, an equivalent model of a real transformer is shown in figure 48. It represents the parasitic element related to transformer windings. In a transformer model, Np and Ns denotes the number of windings for primary and secondary, Rp1 and Rs1 denotes the resistance of copper losses, Lp1 and Ls1 represent leakage inductances, Lm indicates inductance of magnetization for hysteresis losses, Rp2 figure out the resistance of eddy current losses, Cp and Cs indicates the parasitic capacitances of primary and secondary windings respectively and Cp1 to Cp4 represent capacitances of transformer windings between primary to secondary windings. On the other hand, parasitic capacitance between core and windings are represented with Ccw1 and Ccw2 and the parasitic capacitance between core and ground is indicated with Ccg. In a CM noise model of transformer, not all of the parasitic capacitances Cp1-Cp4, Cp and Cs are contributing to CM noise. While there are some parasitic capacitances which can provide a path for CM noise to flow from primary to secondary side and affect the behavior of a converter operating at high frequency. The CM noise can flow through transformer windings to ground and return back to LISN. Therefore, it is necessary to develop a simplified transformer model including parasitic capacitances that contribute to CM noise.

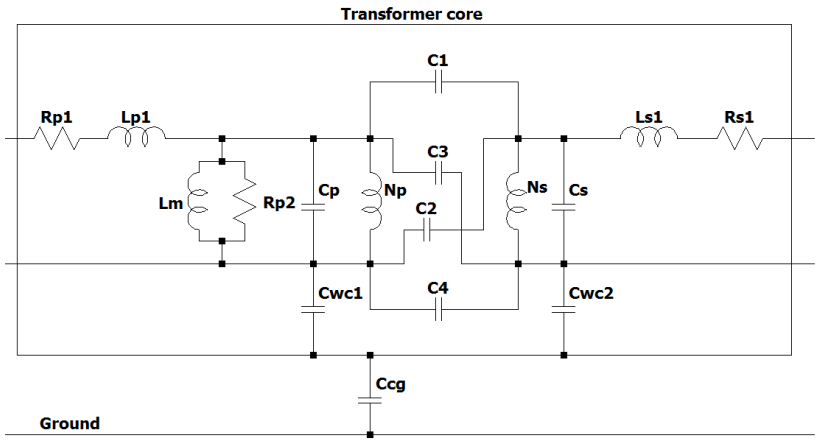


Figure 48: Equivalent model of transformer

In a simplified model, all resistances and inductors are neglected because they are not contributing to the CM noise flow path from the primary to secondary side of transformer. On the other hand, the capacitors (Cp) on primary and (Cs) on secondary side are also neglected. While the capacitors (Cp1-Cp4) between primary and secondary winding play an important role in CM noise path flow. Therefore, these capacitors (Cp1-Cp4) can be summed up and represent with inter-winding capacitance (Cps) as shown in figure 49. However, the parasitic capacitance between core and windings and between core and ground are negligible as compared to inter-winding capacitance Cps. Consequently, these capacitances Ccw1, Ccw2 and Ccg can be neglected in a simplified model.

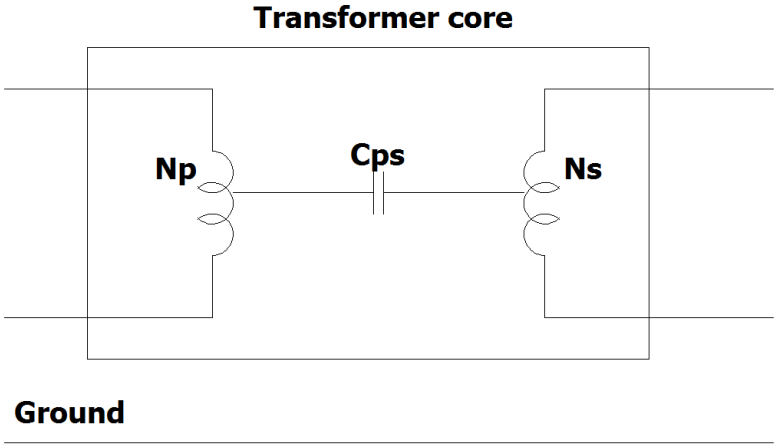


Figure 49: Simplified equivalent model of transformer

CM noise normally flows through parasitic capacitance occurring within the SMPS (Switch-mode Power Supply). It follows the path through the ground wire and returns back via phase and neutral lines. There major paths for CM noise current flow in a flyback converter are inter-winding capacitance and the parasitic capacitance of MOSFETs and Diodes as shown in figure 50. The transformer inter-winding capacitance is denoted with Cps as shown in simplified transformer model. The parasitic capacitance of MOSFET and diode are denoted with Cq and Cd respectively. The noise source due to the MOSFET has two propagation paths such as through parasitic capacitance of MOSFET to ground and through inter-winding capacitance between transformer windings (primary and secondary windings) to ground. Both of types of CM noise current flow to ground and return back to LISN. Conversely, the noise source due to the Diode has propagates through the parasitic capacitance of the diode to ground and returns back to LISN. The noise path due to MOSFET and diode

has shown in figure 50 respectively. Figure 50 also indicates that there are three current loops associated with the switching node.

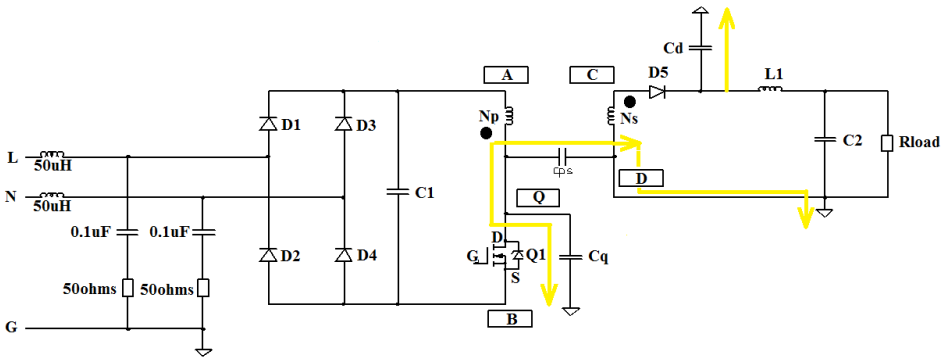


Figure 50: Flyback converter with its CM noise flow path

4.3.2 CM noise model of a flyback converter

To derive a model of CM noise, some assumptions are considered in a circuit comprising of a flyback converter and a LISN. In the LISN circuit, the inductor (50uH) and capacitor (0.1uF) can be representing with a short circuit and two resistors which act in parallel in the CM noise model. In addition, the input bridge diode and input capacitor can also be replaced by a short circuit. The replacement of the input capacitor by a short circuit is justified as at the frequency range used for EMI noise measurement the capacitor impedance is negligible. Furthermore, its ripple voltage can also be disregarded in comparison to the transition voltage of the MOSFET/Diode due to the fast switching rate. The primary side MOSFET and secondary side diode can be replaced with voltage source Vq and voltage source Vd respectively. For similar reasons the output capacitor C2 can also be replaced with a short circuit. With these simplifications applied the simpliofied CM noise model of the flyback converter is as shown in figure 51.

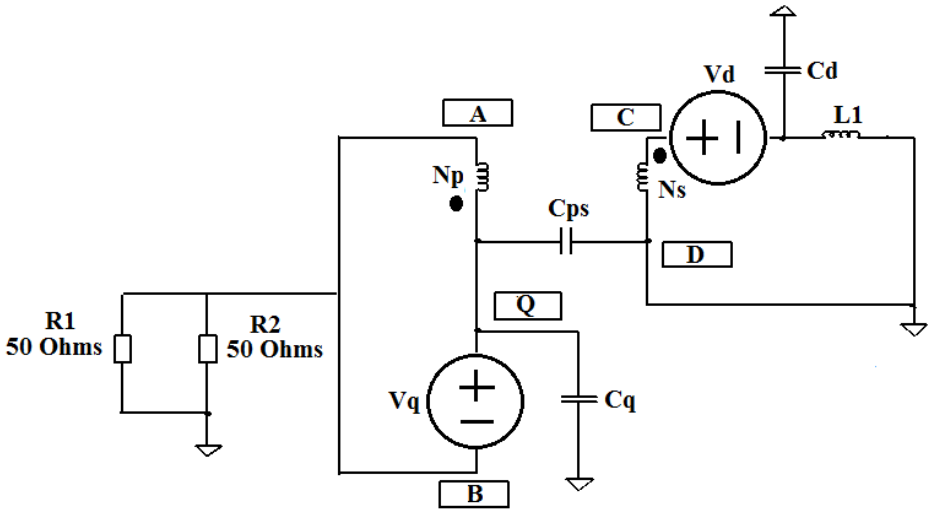


Figure 51: CM noise model of flyback converter

4.3.3 Proposed Balance Technique

The concept of the proposed balance technique is based on cancellation of CM noise sources in a converter. As discussed earlier in the literature review, CM noise can be mitigated through two techniques (i) the cancellation of noise sources and (ii) elimination of the noise propagation path. For the present study the focus was to nullify noise at its origin by introducing an anti-noise source equal in magnitude but opposite in direction. In an isolated converter, extra transformer windings can be used to produce anti-noise sources in a circuit. The design conditions needed for generation of anti-noise are:

- Primary auxiliary and primary windings having an equal number of turns and opposite direction
- Secondary auxiliary and secondary windings are equal number of turns and opposite in direction

Np = Npa

Ns = Nsa

Np = Number of primary turns

Npa = Number of primary auxiliary turns

Ns = Number of secondary turns

Nsa= Number of secondary auxiliary turns

In CM noise model of flyback converter, there are two major sources of noise generation as shown in figure 51 denoted with Vq and Vd. The noise paths due to Vq are through parasitic capacitance of the MOSFET and inter-winding capacitance of the transformer. On the other hand, the noise due to Vd is passed by the parasitic capacitance of diode. To balance the effect of these noise sources Vq and Vd, two anti-noise sources were introduced these are denoted by Vq' and Vd' as shown in figure 52a. One end of the anti-noise winding Vq' can be connected with two silent nodes on the primary side denoted with A and B as shown in figure 52b. While on the other end of the anti-noise source, a compensating capacitor is introduced that has a value equal to that of the MOSFET's parasitic capacitance. The direction of anti-noise windings is in the opposite direction as compared to the primary winding. Moreover, the orientation of windings can be placed in three positions X,Y AND Z as shown in figure 52b. However, anti-noise source Vd' can be connected with two silent nodes C and D in reverse direction as compared to secondary windings as shown in figure 52b. The compensation capacitor is attached on the other end of the anti-noise windings. The value of compensation capacitor is equal to the diode's parasitic capacitance. Again, anti-noise winding Vd' can also be placed in three positions X,Y and Z. Furthermore, the positive end of rectification diode D5 is connected to dotted end of secondary windings in conventional fly-back converter. In the proposed solution the negative end of rectification diode D5 is connected to the non-dotted end of secondary windings in proposed methodology as shown in figure 52b.

The value of compensation capacitors are as follows:

Ccomp1=Cq, Ccomp2=Cd

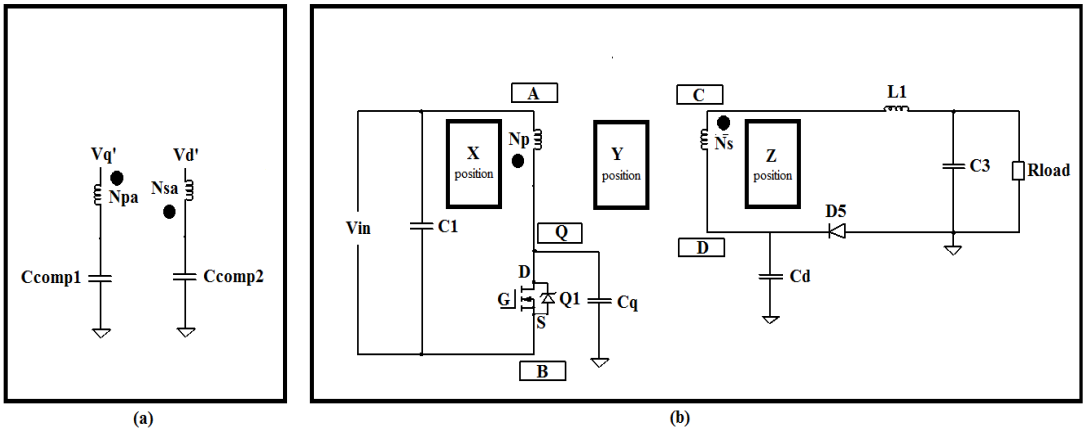


Figure 52: (a) Two anti-noise sources denoted as Vq′ and Vd′ (b) Proposed flyback converter

There are two major concerns in relation to producing an anti-noise source in a transformer winding is the right point of connection and orientation of windings.

Point of connection:

- Anti-noise winding Vq’ can be connected to node A and B respectively.
- Anti-noise winding Vd’ can be connected to node C and D respectively.

Orientation of winding:

- Anti-noise winding Vq’ can be placed at position X, Y and Z.
- Anti-noise winding Vd’ can be placed at position X, Y and Z.

The two main issues such as point of connection and orientation have a major effect on producing anti-noise sources. The wrong point of connection and orientation cannot mitigate CM noise effectively. Therefore the effect of every point of connection and orientation should be necessary to evaluate in detail.

There are four cases to be considered according to point of connection.

Case 1: Anti-noise winding Vq’ is connected with node A

The voltage at node A remains constant during MOSFET turn ON and OFF. Therefore, the primary and primary auxiliary windings have same voltage at one end of windings that is equal to Vin during complete switching transition as shown in figure 53

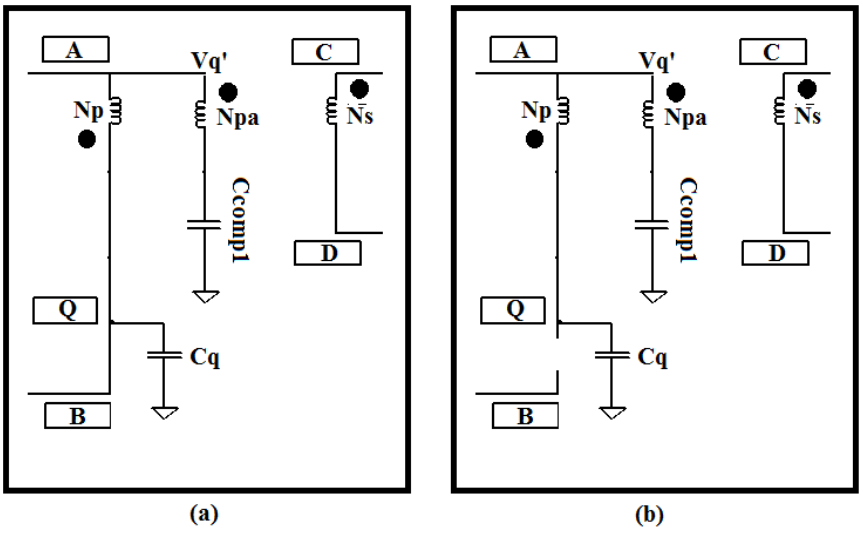


Figure 53: Anti-noise winding Vq′ is connected with node A

Case 2: Anti-noise winding Vq' is connected with node B

The voltage at node B remains constant during MOSFET turn ON and OFF. While the primary and primary auxiliary windings have not same voltage during switching turn OFF period. On the other hand, primary auxiliary winding is not connected to primary winding during MOSFET turn OFF as shown in figure 54.

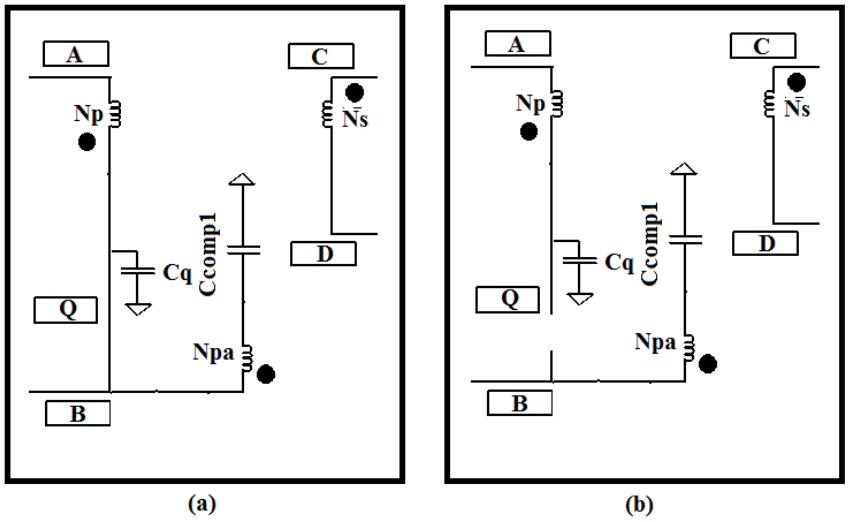


Figure 54: Anti-noise winding Vq′ is connected with node B

Case 3: Anti-noise winding Vd' is connected with node C

The voltage at point C is constant throughout the switching period of MOSFET. Therefore, secondary and secondary auxiliary winding has same potential at one node C. while on the other end of auxiliary secondary winding; anti-noise is generated to cancel out the noise due to Cd at node D.

Case 4: Anti-noise winding Vd' is connected with node D

In this case, the node D is not quite due to diode connected at this point as shown in figure 55b. Therefore, the anti-noise winding can couple with noise at node D and not contribute to mitigate CM noise.

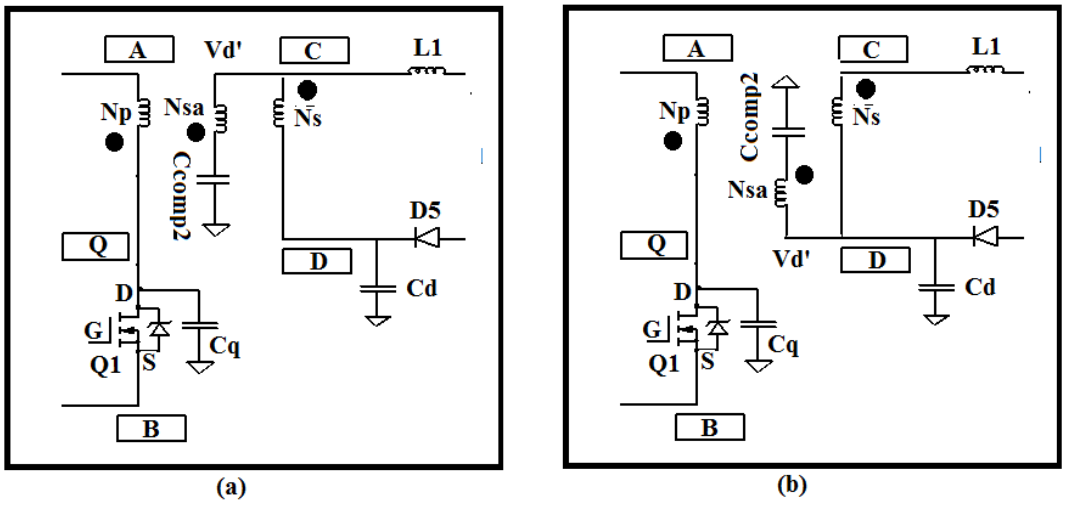


Figure 55: (a) Anti-noise winding Vd' is connected with node C (b) Anti-noise winding Vd' is connected with node D

From above discussion, it is clear that anti-phase winding Vq' and Vd' should be connected to silent node A and C respectively. These two nodes A and C remain constant during throughout switching cycle of MOSFET.

There are three cases to be considered according to orientation of primary auxiliary windings and secondary auxiliary windings.

Case 1a:

In first case, anti-noise winding Vq' is connected to node A and it is placed at position X as shown in figure 56(a). In this configuration, primary windings act as a shielding between primary auxiliary and secondary windings. Therefore, auxiliary windings have no effect to cancel out CM noise through secondary windings. On the other hand, the noise at point Q due to Cq is canceled out with Cq'. However, the effect of Cps has not canceled out with auxiliary windings. CM noise due to Cq can flow through Cps to secondary windings and return to LISN.

Case 1b:

Anti-noise windings Vd' is connected to node C and it is placed at position X as shown in figure 56(b). In this arrangement, secondary auxiliary and secondary windings have an effect on the primary winding to cancel out CM noise. The noise generated due to

node D can be cancelled out with noise generated due to D'. Moreover, parasitic capacitance between secondary auxiliary and primary winding denoted with Cas is equal to parasitic capacitance between primary and secondary winding Cps. Therefore, CM noise path due to node D is through Cd and Cps is cancel out with anti-noise generated due to D' which pass through Ccomp2 and Cas.

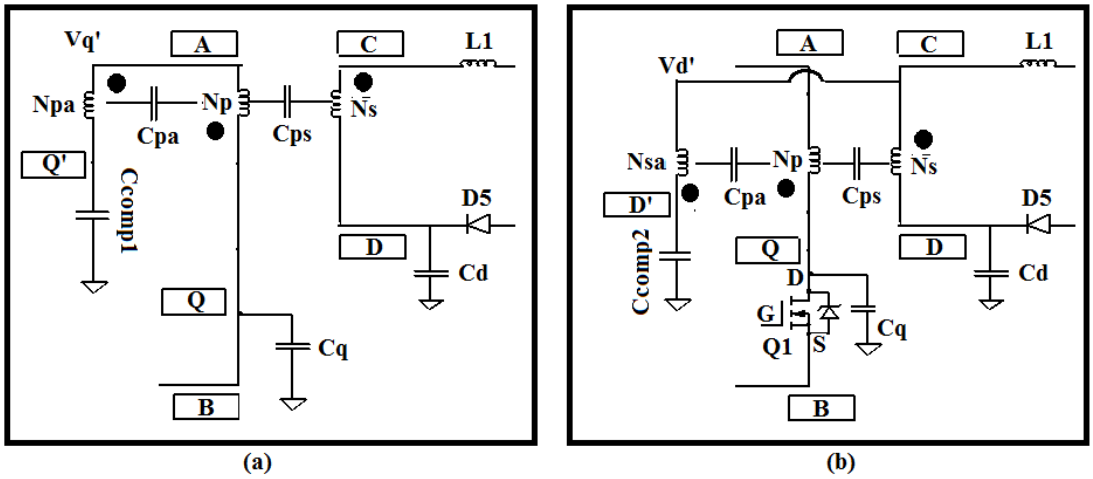


Figure 56: (a) Primary auxiliary windings at position X (b) Secondary auxiliary windings at position X

Case 2a:

Now consider the case when anti-noise winding Vq' is connected to node A and orientation of winding is at position Y as shown in figure 57(a). In this winding arrangement, primary auxiliary winding act as a shielding winding between primary and secondary winding. CM noise due to Q node can be shielded due to primary auxiliary winding. However, CM noise due to Q' can pass through Cas to secondary side and return back to LISN.

Case 2b:

In this arrangement, anti-noise winding Vd' is connected to node C and orientation of winding is at position Y as shown in figure 57(b). Therefore, auxiliary windings act as a shielding winding between primary and secondary windings. Hence, CM noise generated by node Q can pass through Cpa and Ccomp2 to ground and return to LISN.

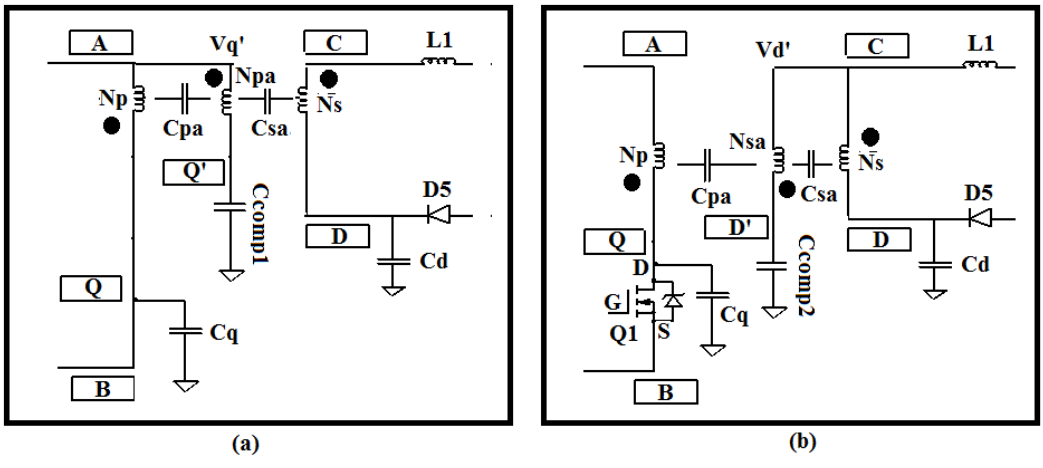


Figure 57:(a)Primary auxiliary windings at position Y(b) Secondary auxiliary windings at position Y

Case 3a:

In this case, anti-noise winding Vq' is connected to node A and orientation of winding is at position Z as shown in figure 58(a). In this pattern, primary and primary auxiliary windings have effect on secondary winding to cancel out CM noise. The noise generated due to node Q can be cancelled out with noise generated due to Q'. The parasitic capacitance between primary and secondary winding denoted with Cps is equal to parasitic capacitance between secondary and primary auxiliary winding Cas. Therefore, CM noise due to node Q is pass through Cq and Cps is cancel out with anti-noise generated due to Q' which pass through Ccomp1 and Cas.

Case 3b:

In this arrangement, anti-noise winding Vd' is connected to node C and orientation of winding is at position Z as shown in figure 58(b). In this arrangement, the secondary winding act as a shielding between primary and secondary auxiliary winding. Therefore, CM noise can flow from primary to secondary ground and return to LISN.

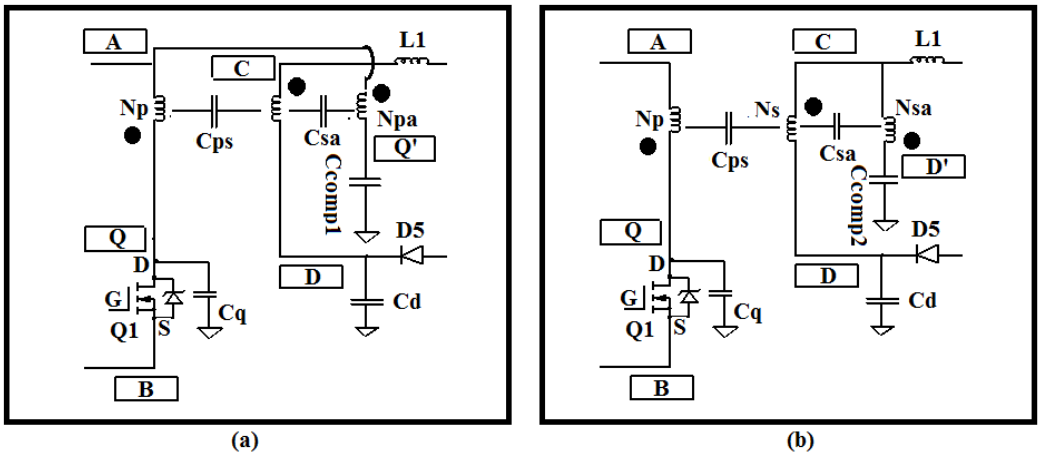


Figure 58: Primary auxiliary windings at position Z (b) Secondary auxiliary windings at position Z

From the above discussion, it is clear that anti-noise winding Vq' should be connected to node A and placed at position Z is the effective way to balance and cancel out CM noise on secondary windings. Similarly, anti-noise windings Vd' should be connected to node C and placed at position X is effective way to balance and cancel out CM noise on primary windings. Therefore, the proposed balance circuit for flyback converter is shown in figure 59.

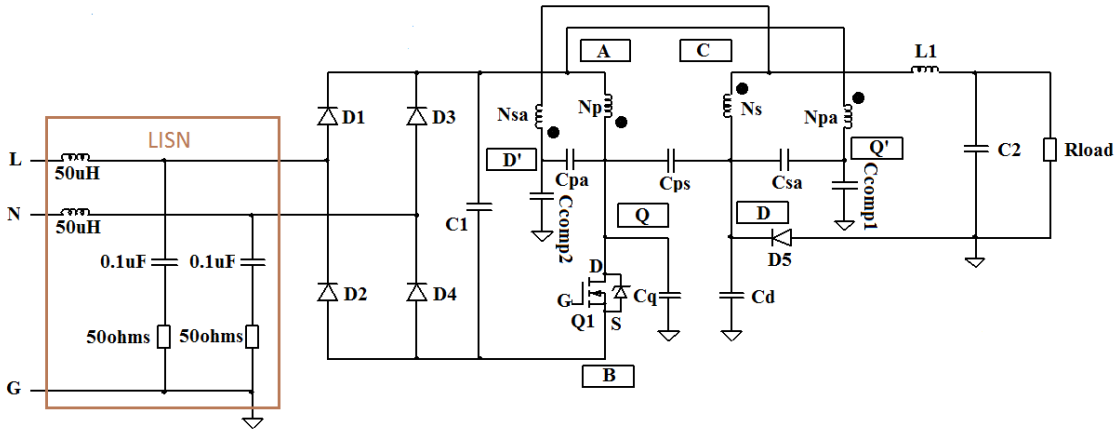


Figure 59: CM noise balanced flyback converter

4.3.4 CM noise sources and coupling path in balance converter

The primary and secondary, primary and secondary auxiliary, secondary and primary auxiliary transformer inter-winding capacitances are denoted with Cps, Cpa and Csa respectively. However, the noise due to MOSFET has two propagation paths such as

through parasitic capacitance of MOSFET (Cq) to ground and through inter-winding capacitance between transformer windings (primary and secondary windings Cps).These noise sources can be balanced out due to anti-noise voltage produce at Q' on primary auxiliary windings Npa. Therefore, overall CM noise due to node Q and Q' can flow internally with in a converter as shown in figure 60 with yellow line. Similarly, overall CM noise due to node D and D' can flow internally with in a converter as shown with blue lines in figure 60.

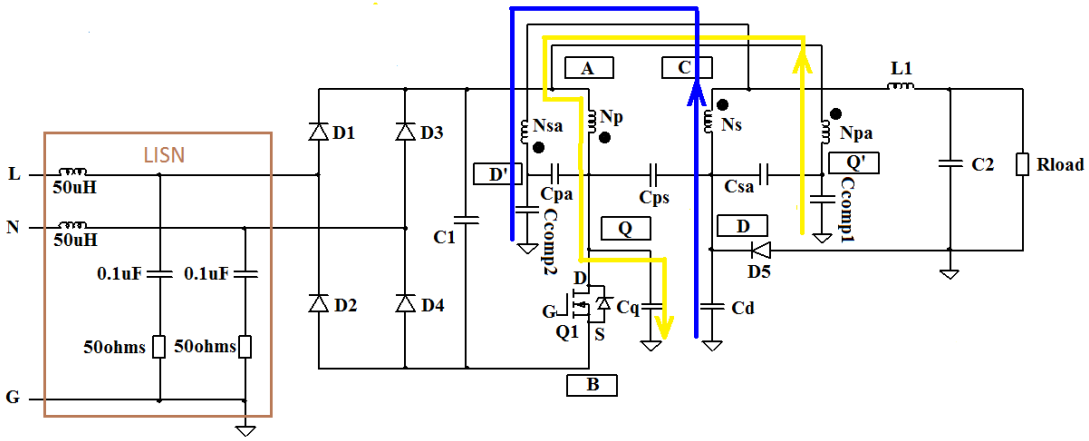


Figure 60: Balanced flyback converter with its CM noise path flow

4.3.5 CM noise model of balanced fly-back converter

In proposed balance flyback converter, the nodes Q' and D' act as anti-noise sources due to anti-phase windings Npa and Nsa respectively. Moreover, the value of Ccomp1 and Ccomp2 capacitors are equal to Cq and Cd respectively. In order to derive a CM noise model, similar assumptions are considered in circuit. In LISN circuit, the inductor (50uH) and capacitor (0.1uF) can be represented by a short circuit and two resistor acting in a parallel arrangement in the CM noise model. Moreover, the input bridge diode can also be considered as a short circuit. On the other hand, the input capacitor and output capacitor are also replaced with short circuits. Therefore, it can be ignored in the CM noise model. The primary side MOSFET and secondary side diode can be replaced with voltage source Vq and voltage source Vd respectively. With the help of above assumption, the final CM noise model of flyback converter is shown in figure 61. It represents simplified CM noise model of balanced flyback converter.

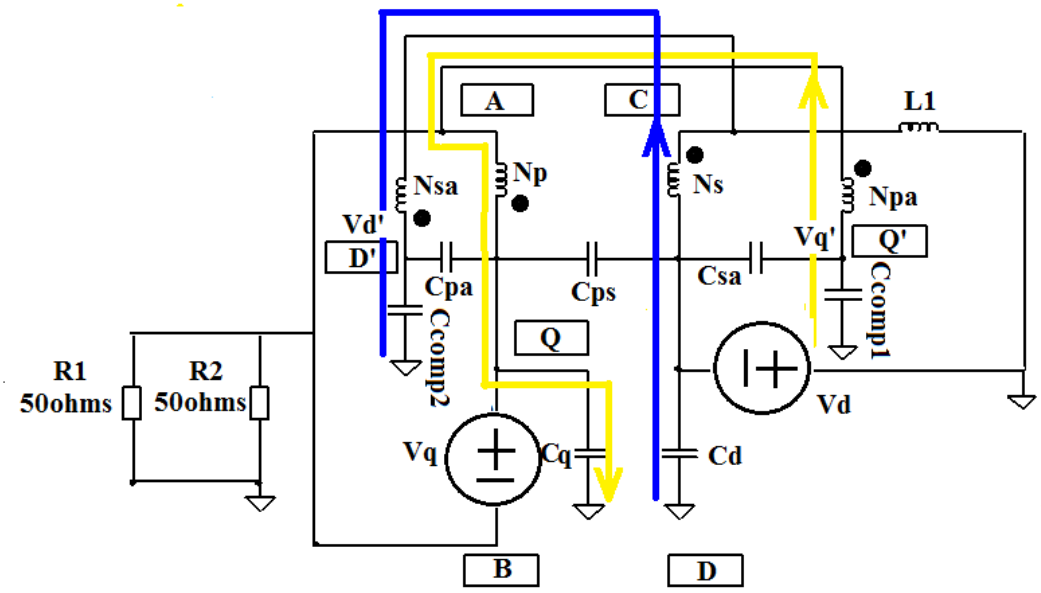


Figure 61: CM noise model of balanced flyback converter

To fulfil the condition of CM noise to nullify overall in balance converter, the following conditions of voltage and current should be met as given in equation (1), (2) and (3)

$$Vq' = -c\,Vq \quad \text{where c is constant} \qquad (1)$$

$$Vd' = -c\,Vd \quad \text{where c is constant} \qquad (2)$$

$$Ip + Ipa + Is + Isa = 0 \qquad (3)$$

Where Ip = Cm noise through primary windings

Ipa = Cm noise through primary auxiliary windings

Is = Cm noise through secondary windings

Isa = Cm noise through secondary auxiliary windings

4.3.6 Transformer Winding Construction

The design of the transformer winding for a conventional converter is shown in figure 62. Np and Ns stand for the total number of primary and secondary windings respectively. Cps represents the inter-winding capacitance between primary and secondary coils. On the other hand, the proposed transformer construction is shown in figure 63, which includes Npa and Nsa compensating windings. Npa and Nsa characterize the total number of primary auxiliary and secondary auxiliary windings

respectively. Cpa and Csa are the inter-winding capacitances between primary and auxiliary windings and secondary and auxiliary windings respectively.

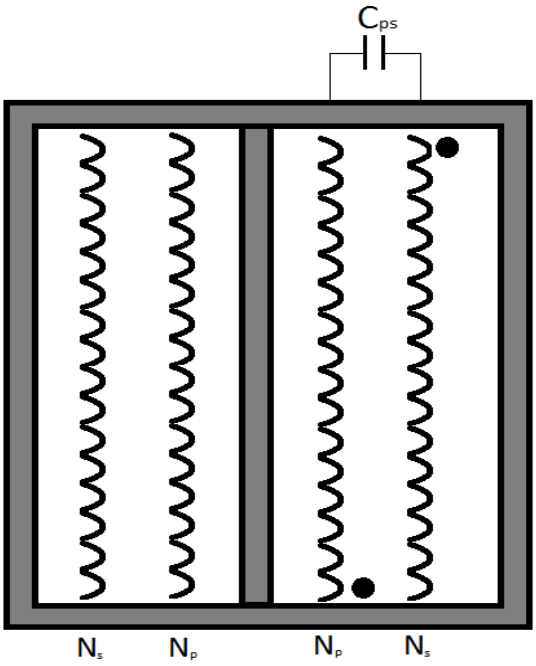


Figure 62: Conventional Transformer winding construction

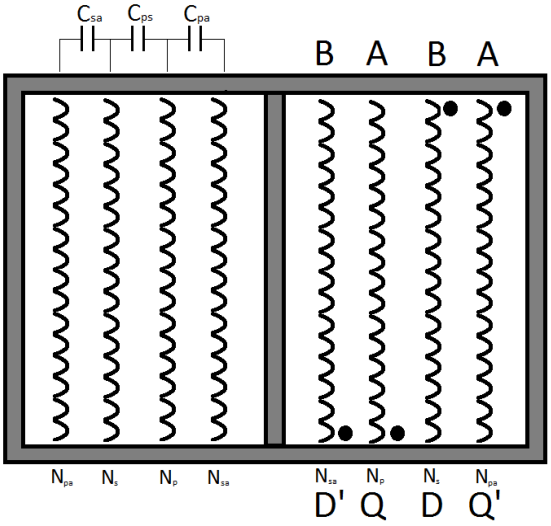


Figure 63: Transformer winding construction with balancing technique

4.3.7 Voltage noise distribution across transformer windings

During MOSFET turn ON

The voltage noise distribution across primary winding, Np, and primary auxilary winding, Npa, are shown in figure 64a. The voltage at nodes Q and Q' are 0V and 2Vin

respectively. While the voltage at point A is constant at Vin (input voltage of converter). In figure 64b, the voltage noise distribution across secondary winding Ns is shown and it is clear from the figure that the voltage noise distribution across secondry winding is constant and equal to Vin.

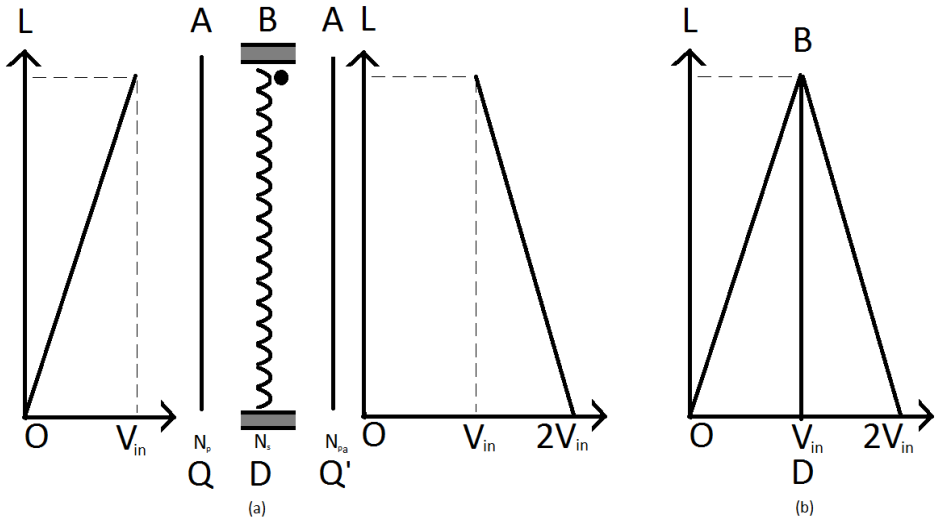


Figure 64: Voltage noise distribution during MOSFET turn ON (a) across primary and auxilary primary windings. (b) across secondry windings

In figure 65a, the voltage at point D is {Vo + (Vin/N)} and the voltage at point D' is {Vo – (Vin/N)}. While the voltage at point B is constant at Vo (output voltage of converter). In figure 65b, the voltage noise distribution across primary winding Np is shown and it is clear from the figure that the voltage noise distribution across primary winding is constant and equal to Vo.

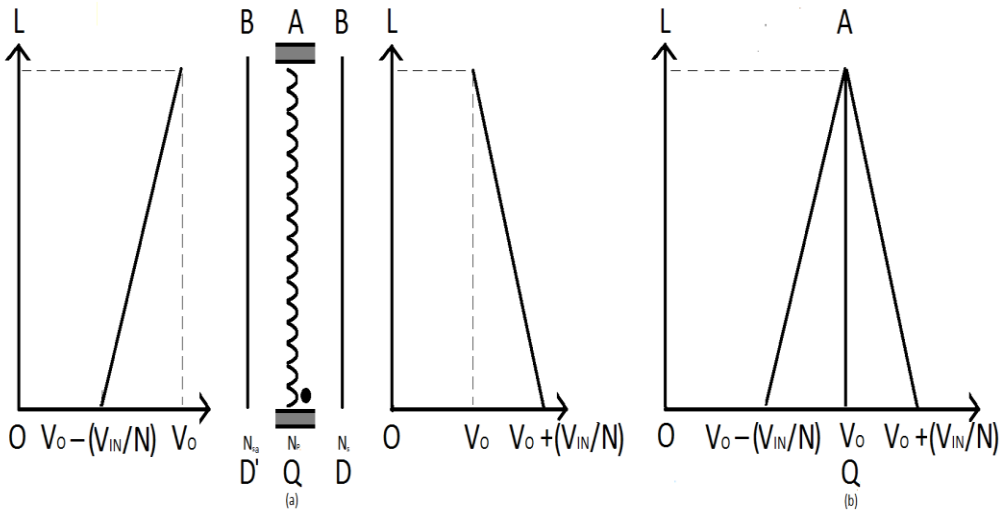


Figure 65: Voltage noise distribution during MOSFET turn ON (a) across secondary and auxilary secondary windings. (b) across primary windings

During MOSFET turn OFF

The voltage noise distribution across primary winding Np and primary auxilary winding Npa are shown in figure 66a. The voltage at point Q is {Vin + (V_O*N)} and the voltage at point Q' is {Vin - (V_O*N)}. While the voltage at point A is constant at Vin (input voltage of converter). In figure 66b, the voltage noise distribution across secondary winding Ns is shown and it is clear from this figure that the voltage noise distribution across the secondry winding is constant and equal to Vin.

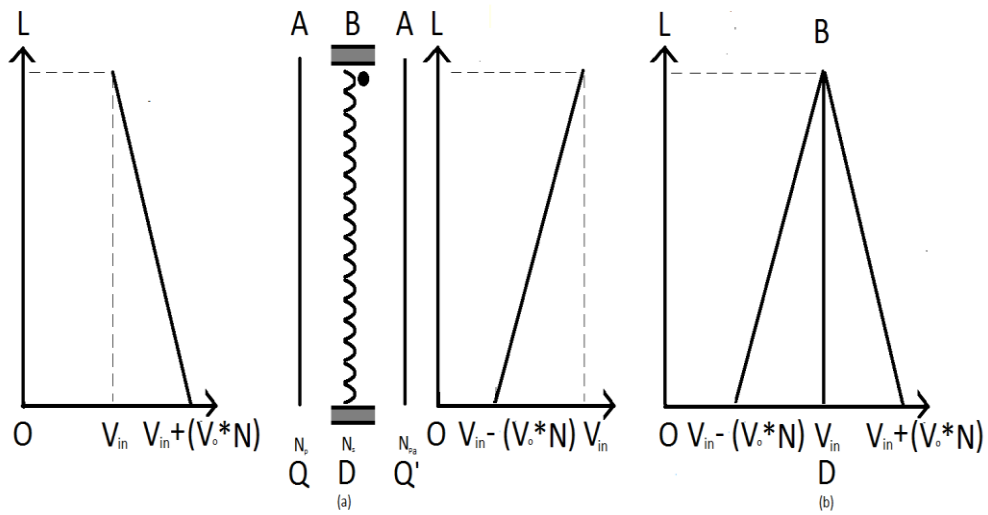


Figure 66: Voltage noise distribution during MOSFET turn OFF (a) across primary and auxilary primary windings. (b) across secondry windings

In figure 67a, the voltage at point D is 0 and the voltage at point D' is 2Vo. While the voltage at point B is constant at Vo (output voltage of converter). In figure 67b, the voltage noise distribution across primary winding Np is shown and it is evident that the voltage noise distribution across the primary winding is constant and equal to Vo.

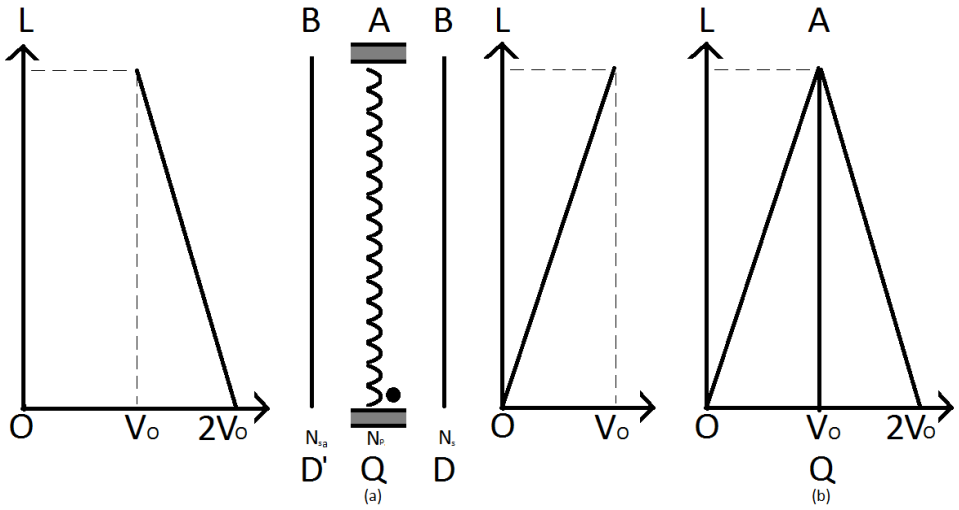


Figure 67: Voltage noise distribution during MOSFET turn OFF (a) across secondary and auxilary secondary windings. (b) across primary windings

From the above discussion, it is clear that the voltage noise distribution across primary and secondary windings are constant throughout the switching period of the converter. Therefore, the common mode noise across both windings should be reduced due to the compensating windings.

4.4 Full-bridge Converter

The basic CM noise model is important to identify and understand the noise generation and coupling mechanism. On the basis of noise model, a novel balancing scheme has been investigated to balance CM noise internally which reduces the overall CM noise of converter.

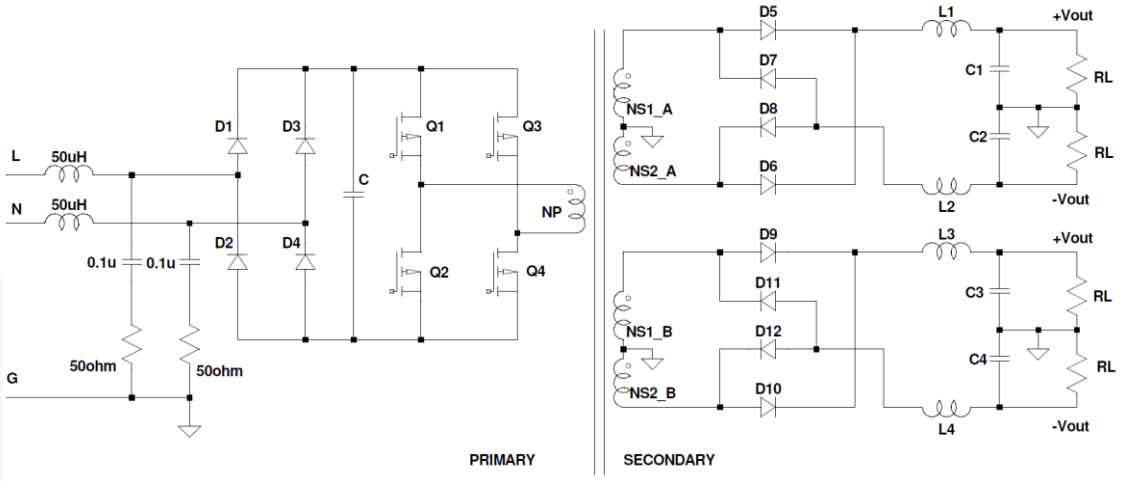


Figure 68: Off-line full-bridge converter showing LISN

A full-bridge converter is shown in figure 68. The switches Q1 Q4 form one leg of the bridge and switches Q3 Q2 formed the other leg. The common leg of both transistors Q1 Q4 is connected to transformer's primary dot end and Q3 Q4 is connected to the other end. As a result, applied voltage across primary is pulsating AC voltage. The transformer function is to provide the isolation between input and output voltages as well as step down the pulsating voltage up to the required output level.

4.4.1 CM noise generation mechanism

Ideally, Q1 Q4 are simultaneously ON and OFF respectively as shown in figure 69. However, a driving signal for diagonal power devices has to pass through different circuits before being received at the switches. These control circuits are normally composed of comparators, opto-coupler, different logic gates and driver circuit. Hence, they introduce a different transmission delay between each driving signal of diagonal switches as shown in fig. Consequently, the synchronicities of diagonal switches disturb and introduce a CM noise at these switching nodes. Moreover, PCB tracks for each driving signal have different path length and also disturb synchronization of driving signal.

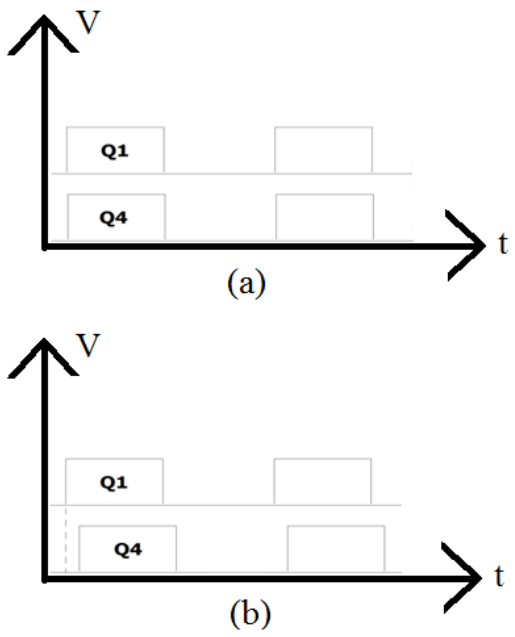


Figure 69: (a) Ideal switching period of Q1 and Q4 (b) Real switching period of Q1 and Q2

The full-bridge converter circuit diagram is shown in figure 70. The operation of circuit for both outputs on secondary side of converter is always remains the same and constant. For simplicity only one output circuit of secondary side is considered here. The parasitic capacitances of conventional full bridge converter are shown in figure 70. Cp1-Cp4, Cp5-Cp7 and C9-C12 are parasitic capacitance of MOSFET switches and Diodes. On the other hand, Cps1 and Cps2 are coupling capacitances of transformer windings. Cp1 and Cp3 are connected to a quiet node so they are not contributing in CM noise. Cp2 and Cp4 are subject to CM noise due to different switching delays between the switches. Cps1 and Cps2 are also contributing in CM noise flow between primary and secondary windings. Cp6 and Cp7 are balancing each other's CM noise. Additionally, extra CM noise is added due to Cp5 in the circuit. Similarly, the parasitic capacitances of other output secondary circuit are shown in figure 70.

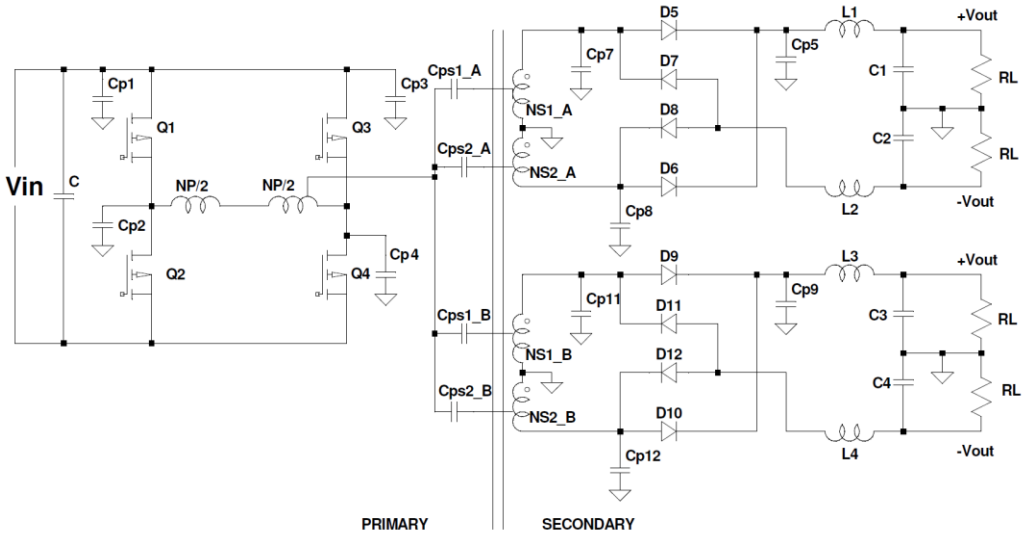


Figure 70: Full-bridge converter with its parasitic capacitances

4.4.2 Transformer Construction

- Wire-wound transformer
- Planar Transformer

4.4.3 Wire-wound transformer

4.4.4 Transformer winding structures

Next, I consider two different transforming winding structures such as conventional, and interleaving as shown in figure 71. Primary windings represent with yellow colour while secondary windings represent with blue colour. In conventional method, usually primary winding is wounded on bobbin first then secondary winding is adjacent to primary winding. On the other hand, interleaved technique windings are placed alternatively primary and secondary windings adjacent to each other.

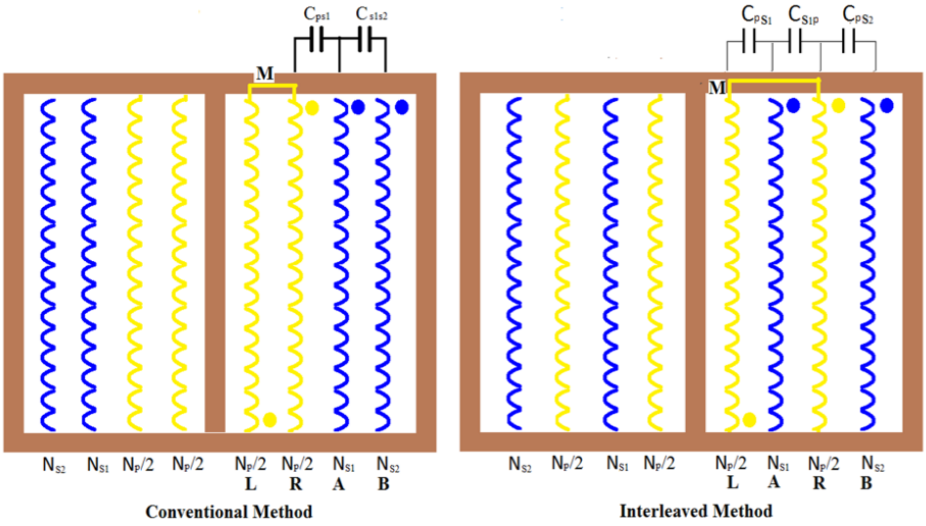


Figure 71: Different types of transformer construction

4.4.5 Proposed Balancing Technique

In this novel scheme, the basic idea is to introduce counter noise in the circuit using extra compensation windings and capacitors. The voltage introduced due to compensation windings and capacitors is anti-phase to nullify the noise current due to switching node. There are different compensation winding arrangements for different types of transformer configurations.

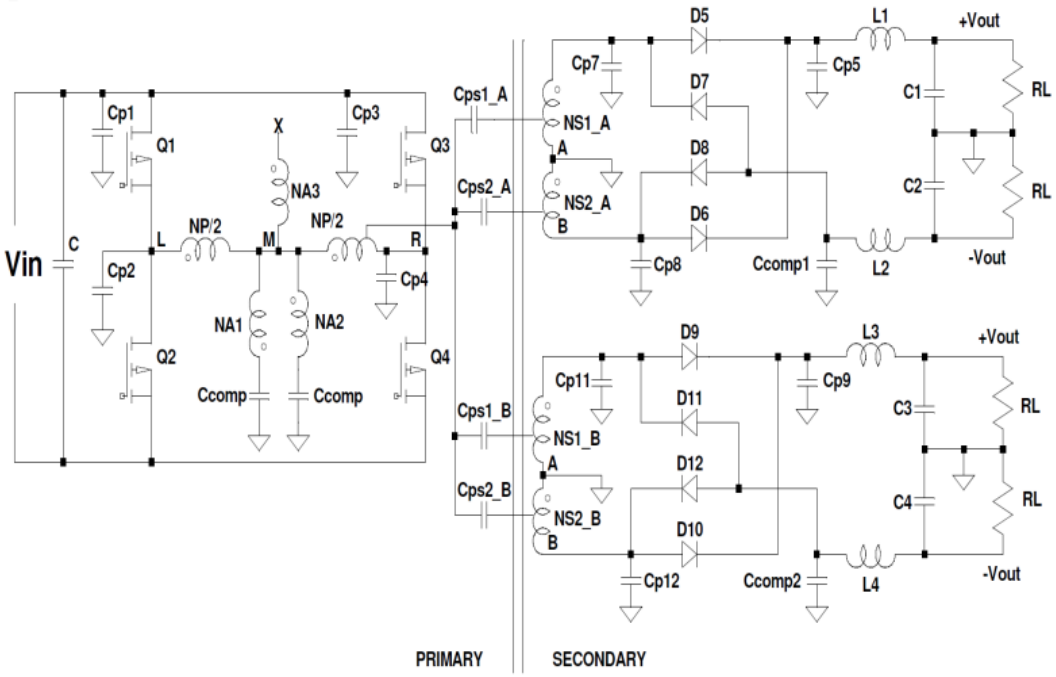


Figure 72: Proposed full-bridge converter for conventional transformer winding structure

In conventional transformer winding structure, primary and secondary windings are denoted with Np and Ns respectively. The coupling capacitors between primary and secondary windings are represented with Cps. On the other hand, the proposed full-bridge converter for conventional transformer windings is shown in figure 72, which comprises of three additional windings and capacitors known as Na1, Na2, Na3 and Ccomp. These extra windings and capacitors have two advantages such as to balance the noise distribution across secondary windings and also generate the anti-phase noise to cancel out noise produced across primary winding parasitic capacitance of MOSFETs. Moreover, Ccomp is added on secondary side of converter in proposed scheme. The secondary side Ccomp at anode of diodes D8 and D7 produce anti-noise voltage to balance out of noise due to Cp5 parasitic capacitance of diode D5 and D6. Similarly, the proposed full-bridge converter for interleaved transformer windings is shown in figure 73, which comprises of two additional windings and capacitors known as Na1, Na2 and Ccomp.

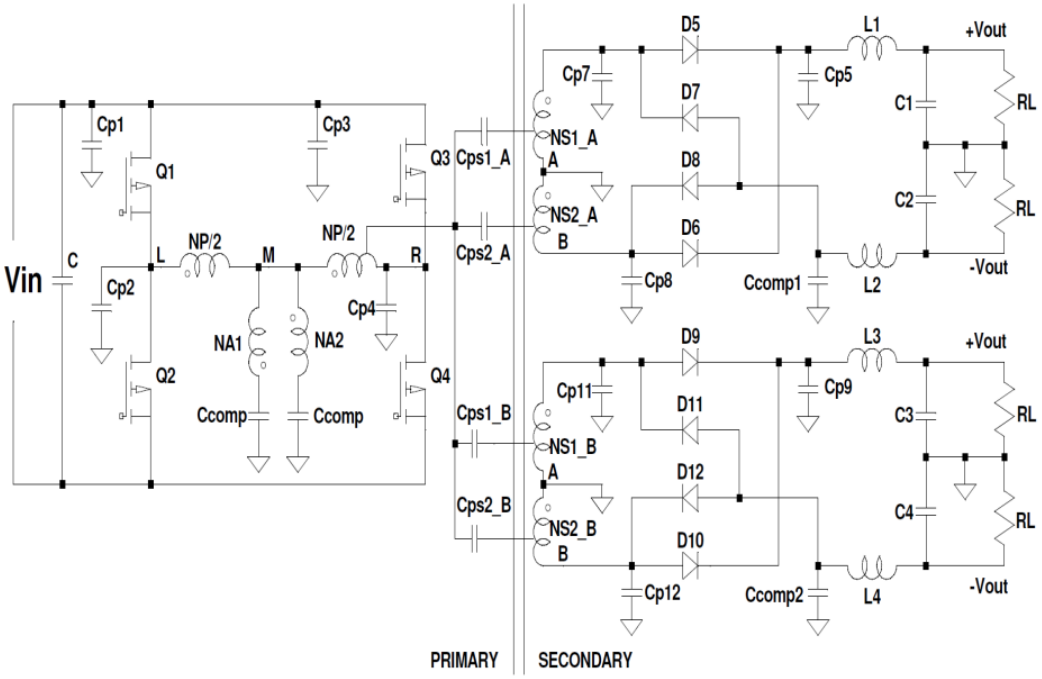


Figure 73: Proposed full-bridge converter for interleaved transformer winding structure

In next section, the detail of voltage noise distribution of transformer windings have been discussed with graphical representation of each case of diagonal switches turn ON and OFF.

4.4.6 Voltage noise distribution across balance transformer windings

In multi-layer transformer windings, the layers which are not adjacent to each other have fundamentally shielding effect between each other. In figure 74 (a), the windings L and R is tied together with quiet node such as $V_{IN}/2$. If any noise is generated across winding L, it cannot be influenced any noise on A due to R acting as a shielding between L and A windings. The windings R and A has effect on each other due to switching noise on R winding. Therefore, in order to achieve the balance condition in transformer windings, the voltage noise across winding should remain constant on middle winding.

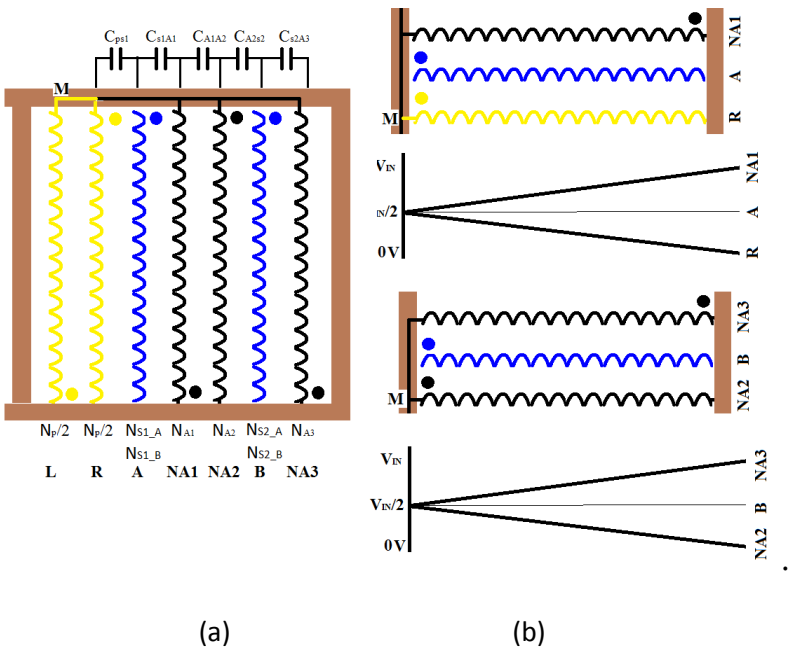
4.4.7 Conventional transformer Construction

In a conventional transformer, the arrangements of windings for proposed balance technique are shown in figure 74a. The additional compensation windings NA1, NA2 and NA3 can be placed in order to generate the anti-noise across secondary windings.

These compensation windings are attached to quite noise node M. The NA1 and NA2 are placed in middle of secondary windings NS1 and NS2. The third compensation windingNA3 are placed on top of NS2 with wound in reverse direction. The voltage noise on R and NA1 are anti-phase to each other in every condition of switching action. Similarly voltage noise on NA2 and NA3 are out of phase to each other during every cycle of switching transition. The voltage noise across two secondary winding NS1 and NS2 are always equal to zero.

Case 1: Q1 and Q4 turn ON

Consider a first case in which two diagonal switches Q1 and Q4 turn ON to transfer power from primary to secondary windings. The voltage at dot end of primary winding is equal to V_{IN} and voltage at non-dot end is equal to zero. Therefore, the voltage at node M is equal to $V_{IN}/2$ and voltage at dot end of auxiliary winding NA1 is equal to V_{IN}. In figure 74 (b), the voltage noise distribution across secondary winding NS1 is equal to $V_{IN}/2$. The compensating capacitor of NA1 is producing anti-noise voltage to compensate the noise of node R due to parasitic capacitor Cp4. The arrangement of windings NA2, B and NA3 also have same effect to cancel out noise on secondary winding NS2



(a) (b)

Figure 74: (a) Balance conventional transformer winding structure, (b) Voltage noise distribution during MOSFETs Q1 and Q4 turn ON

Case 2: Q2 and Q3 turn ON

The voltage noise distribution across secondary windings Ns1 and Ns2, are shown in fig 75(b). The voltage at nodes NA1 and R are 0V and V_{IN} respectively. While the voltage at point A is constant at $V_{IN}/2$. Therefore, the voltage noise distribution across secondary winding Ns1 is shown and it is clear from the figure that the voltage noise distribution across secondry winding is constant. Similarly the winding arrangements of NA2, Ns2 and NA3 are creating the voltage at node NA3 and NA2 are equal to 0V and V_{IN} respectively. Therefore, the voltage noise distribution across secondary winding Ns2 is constant.

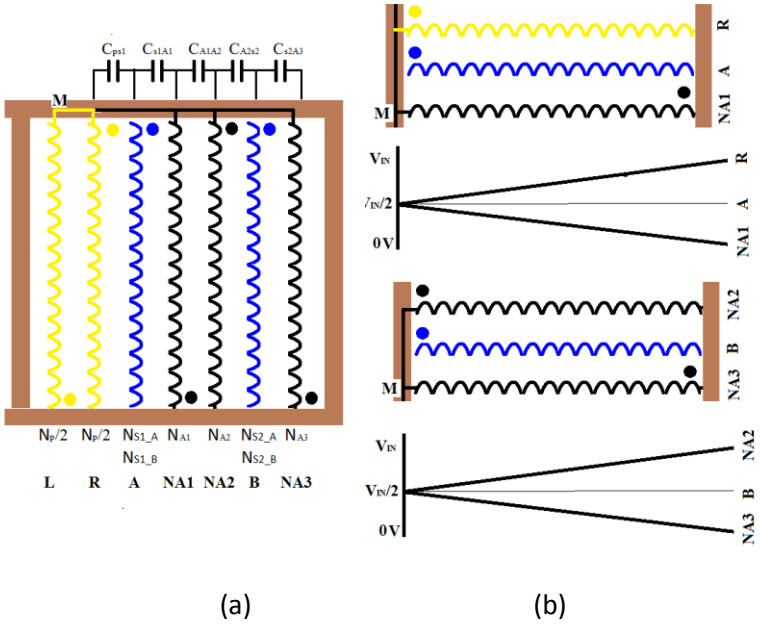


Figure 75: (a) Balance conventional transformer winding structure, (b) Voltage noise distribution during MOSFETs Q2 and Q3 turn ON

Case 3: Q1, Q2, Q3 and Q4 OFF

During dead time interval, the voltage at dot and non dot end of primary winding is equal to $V_{IN}/2$. Also the voltage on all auxiliary winding NA1, NA2 and NA3 are equal to to $V_{IN}/2$. Therfore, the voltage noise distribution across NS1 and NS2 are constant.

4.4.8 Interleaved Transformer Construction

The interleaving winding arrangement of balanced transformer includes two auxiliary windings NA1 and NA2 on top of second secondary windings to generate anti-noise

across NS2. The dot represents direction of windings in a clockwise direction start from here. In figure 76 (a), the windings L and R across secondary winding NS1 produce the noise voltage in opposite to each other. Therefore, the noise across secondary winding NS1 is zero due to anti-noise effect. Similarly, noise across secondary NS2 is nullified due to compensation winding NA1 and primary winding.

Case 1: Q1 and Q4 turn ON

During this time of interval, the power is transferred from primary to secondary windings. The half turns of primary winding placed across bobbin has voltage equal to V_{IN} at dot end and $V_{IN}/2$ at node M as shown in In figure 76 (b),. On the other hand, the voltage at non-dot end of other half primary winding is equal to zero. Therefore, the voltage noise distribution across secondary winding NS1 is equal to constant. The compensating winding NA1 and capacitor is placed across secondary winding to produce anti-noise voltage to balance the noise generated due to parasitic capacitance of MOSFETs. The voltage at dot end of auxiliary winding NA1 is equal to V_{IN} and voltage at non dot end of primary winding is equal to zero. Overall, the voltage noise distribution across winding NS2 is equal to constant. In a nutshell, the arrangement of winding L,A,R and R,B,NA1 are creating the constant voltage noise distribution across windings NS1 and NS2.

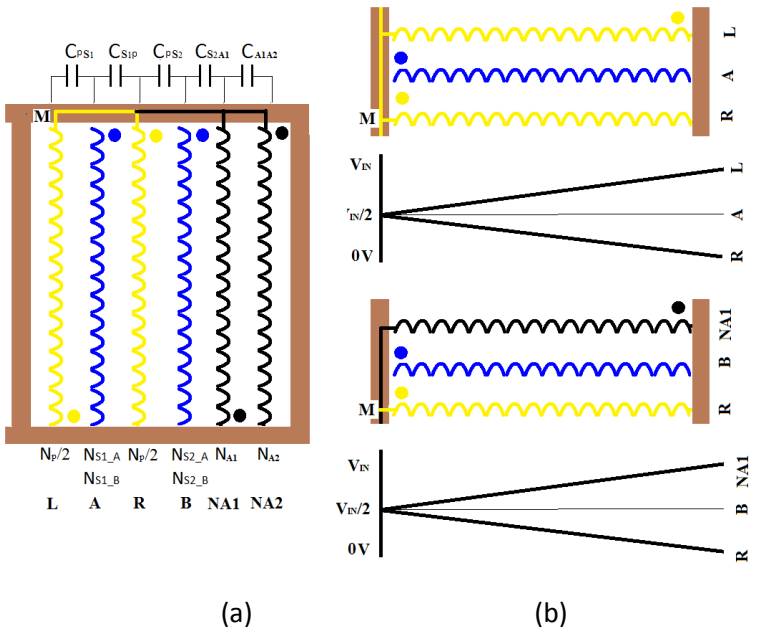
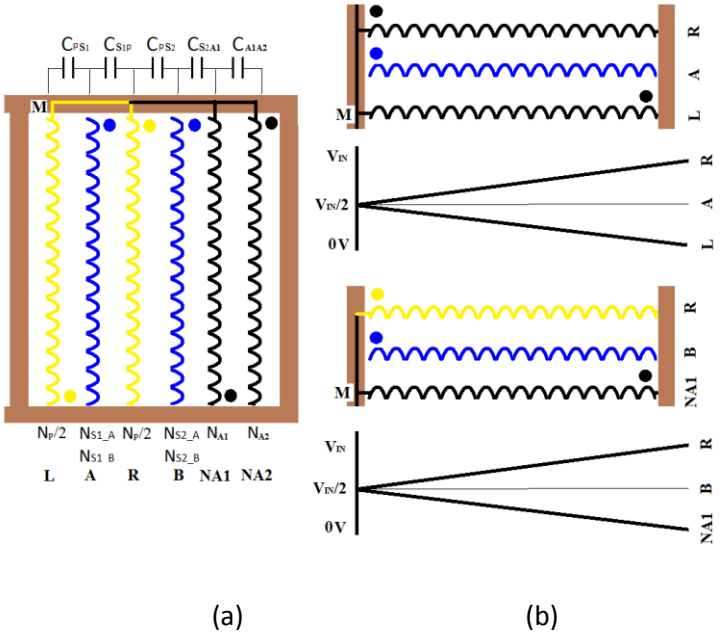


Figure 76: (a) Balance Interleaved transformer winding structure, (b) Voltage noise distribution during MOSFETs Q1 and Q4 turn ON

Case 2: Q2 and Q3 turn ON

During this time interval, the dot end of primary attached to zero voltage while the non dot end of primary has voltage Vin. The arrangement of windings L, A and R producing the constant voltage noise distribution across seconday winding NS1. On the other hand, the dot end of auxiliary winding NA1 has zero voltage and other end is attached to $V_{IN}/2$. The noise voltage distribution across winding NS2 is equal to constant due to R, B and NA1 arrangement of winding as shown in figure 77(b).



(a) (b)

Figure 77: (a) Balance Interleaved transformer winding structure, (b) Voltage noise distribution during MOSFETs Q1 and Q4 turn ON

Case 3: Q1, Q2, Q3 and Q4 OFF

During this time interval, the voltage at dot and non dot end of primary winding is equal to $V_{IN}/2$. Also the voltage on all auxiliary windings NA1 and NA2 are equal to $V_{IN}/2$. Therfore, the voltage noise distribution across NS1 and NS2 are equal to constant.

Based on the above discussion, it is clear that the voltage noise distribution across NS1 and NS2 are always equal and remain constant throughout the switching period of the converter. The voltage noise distribution of secondary windings is unaffected due to different switching transition periods. Therefore, the proposed winding arrangement for different transformer construction produces the anti-noise voltage across the secondary windings which, cancels out the noise produced in the primary windings. Thus the

secondary windings are sandwiched between two windings of opposite noise polarity and consequently the noise on secondary windings are cancelled.

4.4.9 Planar Transformer

Planar transformers have attracted significant attention in recent years due to their several inherent advantages, such as, the low profile achieved using spiral windings etched directly on to a printed circuit board (PCB), greatly simplifying construction. Moreover, these transformers can be manufactured with high precision, consistency and reliability. Typically these are constructed as a multi-layered structure. In this section, the commonly used planar transformers in SMPS are considered. The previously discussed balancing technique approach for wire wound transformer can be applied also to planar transformer topologies.

4.4.10 Planar Transformer winding structures

In figure 78 two different transforming winding structures commonly used are shown and these are referred to as conventional and interleaving topologies.

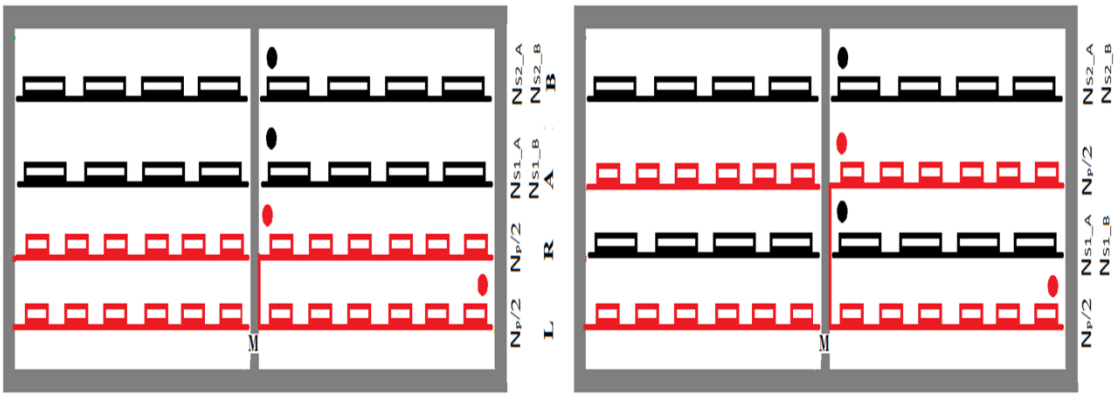


Figure 78: Different types of transformer construction

4.4.11 Proposed Balancing Technique

There are different compensation winding arrangements for different types of planar transformer configurations. The voltage noise distributions of transformer windings for each case are discussed in the following section.

4.4.12 Voltage noise distribution across balance transformer windings

In multi-layer transformer windings, the PCB layers which are not adjacent to each other provide a shielding effect. In figure 79 (a), the PCB windings layer L and R are tied together with a quiet node such as $V_{IN}/2$. The noise generated across winding L has no influence on A due to R acting as a shielding between the L and A windings layer. Conversely, the windings R and A has an effect on each other due to the switching noise the R winding. Therefore, in order to achieve the balanced condition in the transformer windings, the voltage noise across the middle winding should remain constant.

4.4.13 Conventional Transformer Construction

For a conventional transformer approach, the arrangements of windings for the proposed balance technique are as shown in figure 79a. The additional compensation PCB windings NA1, NA2 and NA3 can be placed in order to generate anti-noise across the secondary windings. Overall, the voltage noise across two secondary winding Ns1 and Ns2 are always equal and constant.

Case 1: Q1 and Q4 turn ON

The voltage noise distribution across secondary windings Ns1 and Ns2, are shown in figure 79(b). The voltage at node NA1 and R are Vin and 0V respectively. Hence the voltage across NS1 is equal and constant to Vin/2. In a nutshell, the arrangement of windings R, A and NA1 has produced a constant voltage across secondary winding NS1. Similarly, the arrangement of windings NA2, B and NA3 produce a constant voltage across secondary winding NS2 as also shown in the figure. Therefore, the overall effect on secondary windings NS1 and NS2 are equal and constant during this switching cycle.

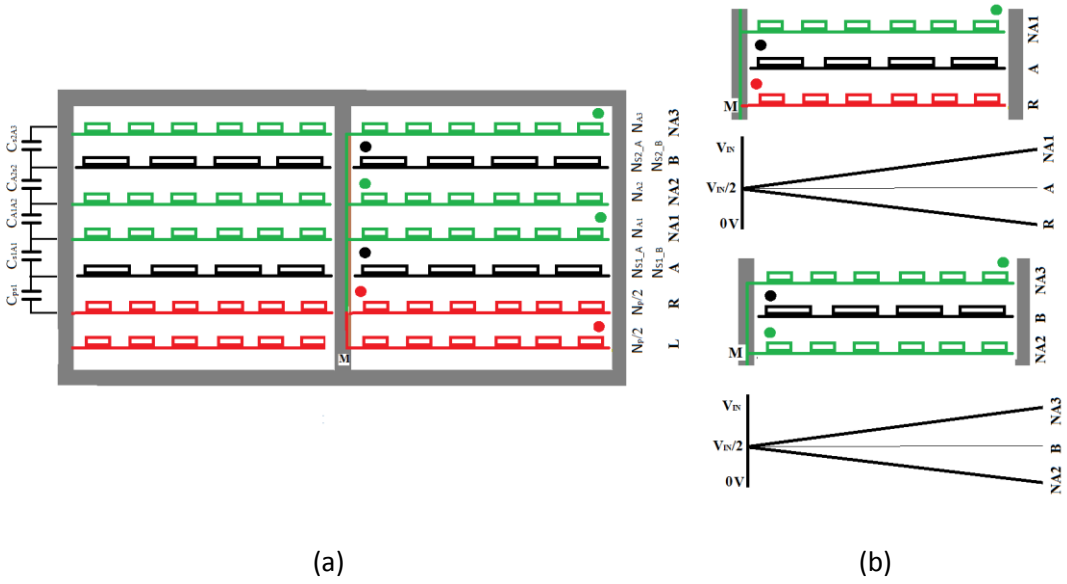


Figure 79: (a) Balance conventional transformer winding structure, (b) Voltage noise distribution during MOSFETs Q1 and Q4 turn ON

Case 2: Q2 and Q3 turn ON

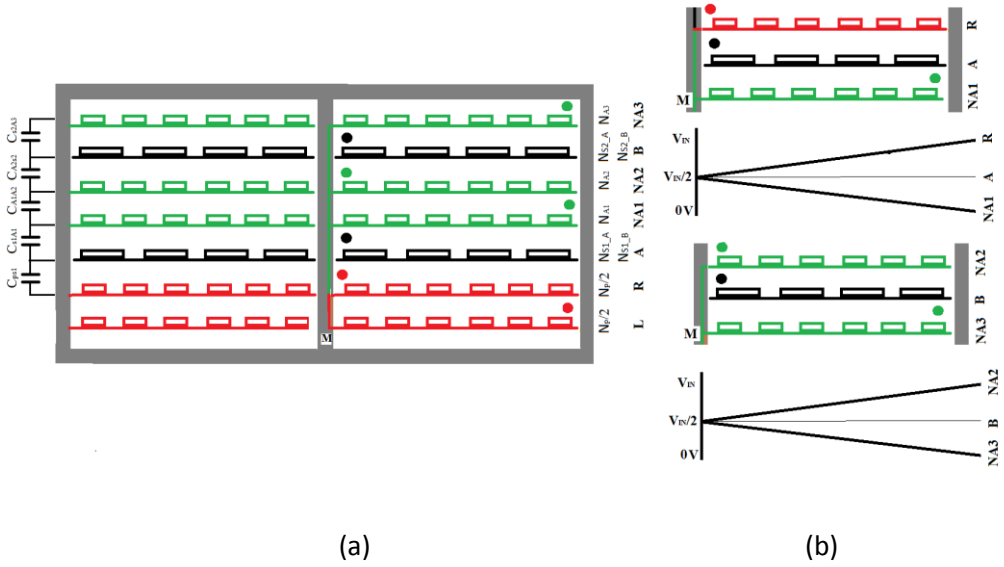


Figure 80: (a) Balance conventional transformer winding structure, (b) Voltage noise distribution during MOSFETs Q2 and Q3 turn ON

The voltage noise distribution across secondary windings Ns1 and Ns2, are shown in figure 80(b). The voltage at node NA1 and R are 0V and Vin respectively. Therefore, the voltage across NS1 is equal and constant to Vin/2. Similarly, the voltage at node NA3 and NA2 are 0V and Vin respectively. Consequently, the overall effect on secondary windings NS1 and NS2 are equal and constant during this switching cycle.

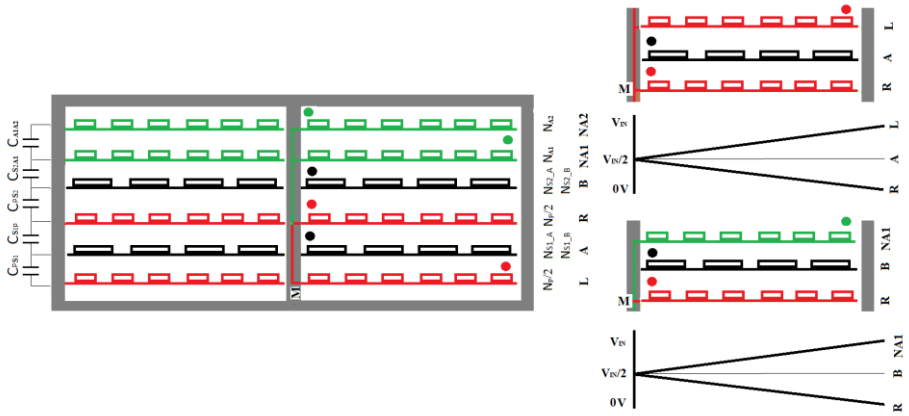
Case 3: Q1, Q2, Q3 and Q4 OFF

During this period, the voltage across primary winding is equal to $V_{IN}/2$. Moreover, the voltage across PCB winding NA1, NA2 and NA3 are also equal to $V_{IN}/2$. Therfore, the voltage across secondary windings NS1 and NS2 are constant through out this switching period.

4.4.14 Interleaved Transformer Construction

The interleaving winding arrangement for the balanced transformer includes two auxiliary windings NA1 and NA2 on top of second secondary windings to generate anti-noise across NS2. The dot represents direction of windings in a clockwise direction. The voltage noise distribution during the switching cycle is discussed below.

Case 1: Q1 and Q4 turn ON



(a) (b)

Figure 81: (a) Balance Interleaved transformer winding structure, (b) Voltage noise distribution during MOSFETs Q1 and Q4 turn ON

The voltage noise distribution across secondary windings Ns1 and Ns2, are shown in figure 81(b). The voltage at node L and R are Vin and 0V respectively. Hence the voltage across NS1 is equal and constant to Vin/2. Thus the arrangement of windings R, A and L has produced a constant voltage across secondary winding NS1. Similarly, the arrangement of windings R, B and NA1 has produced a constant voltage across

secondary winding NS2. Therefore, the overall effect on secondary windings NS1 and NS2 are equal and constant during this switching cycle.

Case 2: Q2 and Q3 turn ON

The voltage noise distribution across secondary windings Ns1 and Ns2, are shown in figure 82(b). The voltage at node L and R are 0V and Vin respectively. Therefore, the voltage across NS1 is equal and constant to Vin/2. Similarly, the voltage at node NA1 and R are 0V and Vin respectively. Consequently, the overall effect on secondary windings NS1 and NS2 are equal and constant during this switching cycle.

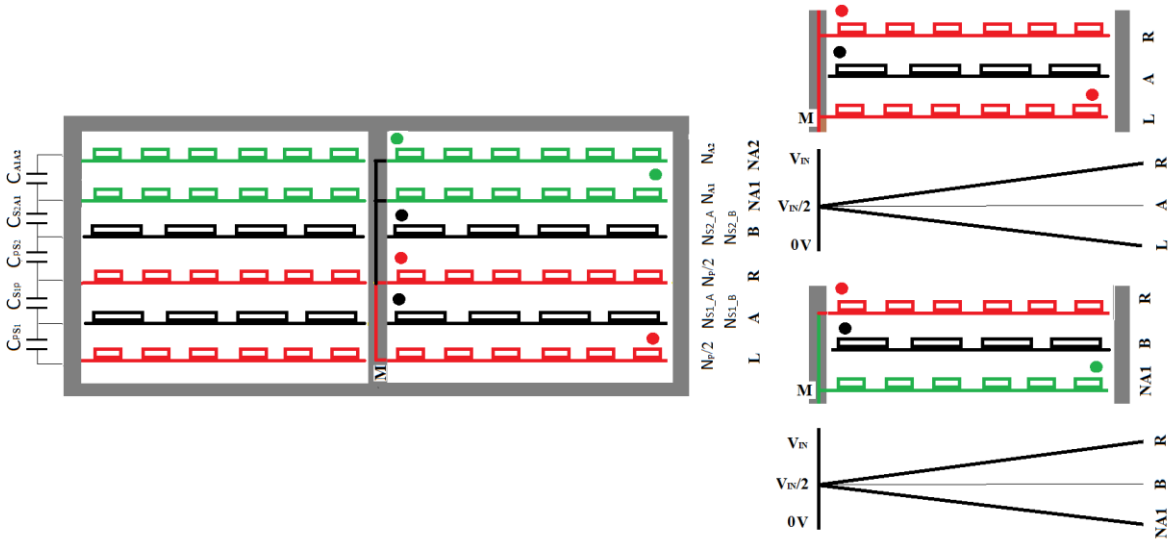


Figure 82: (a) Balance Interleaved transformer winding structure, (b) Voltage noise distribution during MOSFETs Q2 and Q3 turn ON

Case 3: Q1, Q2, Q3 and Q4 OFF

During this period, the voltage across primary winding is equal to $V_{IN}/2$. Moreover, the voltage across PCB winding NA1 and NA2 are also equal to $V_{IN}/2$. Therfore, the voltage across secondary windings NS1 and NS2 are constant through out this switching period.

From above discussion, it is clear that the voltage noise distribution across NS1 and NS2 are always equal and remain constant throughout the switching period of converter. Therefore, the proposed winding arrangements for different transformer

construction produces the anti-noise voltage across secondary windings to cancel out noise generated due to original windings. In other words, I can say that the secondary windings are sandwiched between two windings of opposite noises. Therefore, the overall noises on secondary windings are cancelled out.

4.5 ZVS full-bridge converter

Full-bridge converters are commonly used for medium-to-high power applications due to its simple circuit configuration based on hard and soft switching techniques. Hard switching converters are normally turned on and off switches diagonally at same time. Due to overlap between voltage and current in switches causes losses and reduced efficiency of converter. To improve efficiency of converter, soft switching techniques are normally used. The soft-switching technique can be classified into two types such as ZVS (zero voltage switching) and zero-voltage and zero current switching (ZVZCS). ZVS is most popular technique due to fixed switching frequency and simplicity. In conventional ZVS method, the switches are turned on when voltage across these are nearly equal to zero. To achieve ZVS, the parasitic capacitors of the switches and leakage inductance of transformer are normally utilized to meet the condition of soft switching. This technique improved efficiency of converter and minimizing EMI noise. While on the other hand, there are some limitations of this technique such as narrow range of load handling capability to achieve zero voltage switching. In light load condition, they lose their ability to achieve zero voltage switching due to less energy stored in leakage inductance.

The range of ZVS can be extended by increasing stored energy of inductance using high leakage inductance of transformer or adding series inductance. The effective duty cycle is comprised due to increasing inductance of transformer. The loss of effective duty cycle can be minimized by using saturable inductor in series to achieve ZVS. These methods of increasing the inductance for stored energy can significantly increases current through switches and conduction losses. A full range of ZVS can be achieved by help of passive auxiliary pole circuit that results in fixed circulating current and higher conduction losses. In a nutshell, conduction losses are higher in these types of ZVS techniques of increasing inductance of transformer through different ways such as series inductance, saturable inductor and passive auxiliary pole circuit.

In this section, a novel technique is proposed to extend the range of ZVS over entire range of load. Moreover, the conduction losses also reduced significantly and the

stored energy in auxiliary circuit is dependent on load. The minimum energy is stored under full load condition and it gradually increases as load decreases. The proposed technique not only increases the range of ZVS but also improves efficiency of full-bridge converter by reducing conduction losses. The experimental results obtained from proposed converter are also presented to confirm the proposed idea.

4.5.1 Novel ZVS Full-bridge Converter

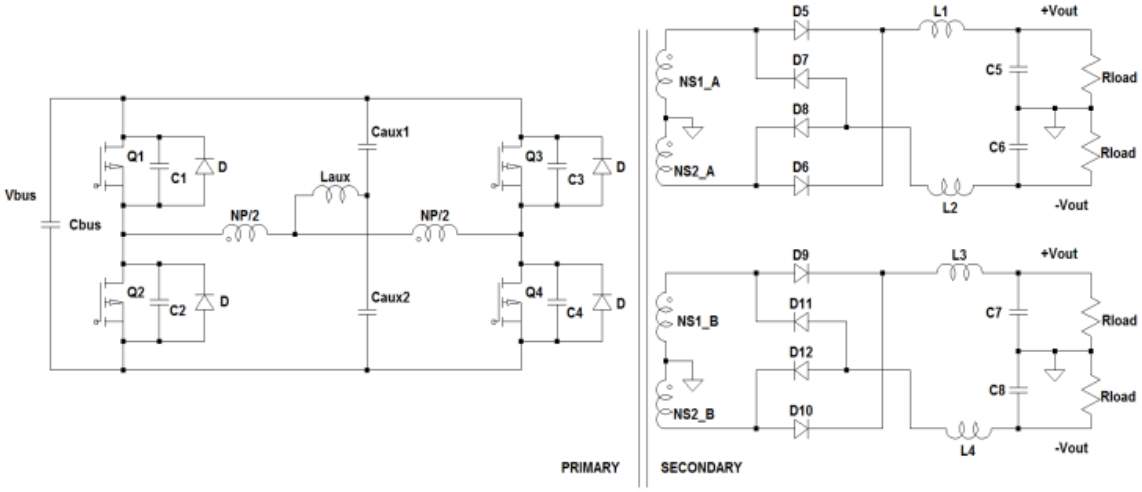


Figure 83: Schematic of novel proposed ZVS full-bridge Converter

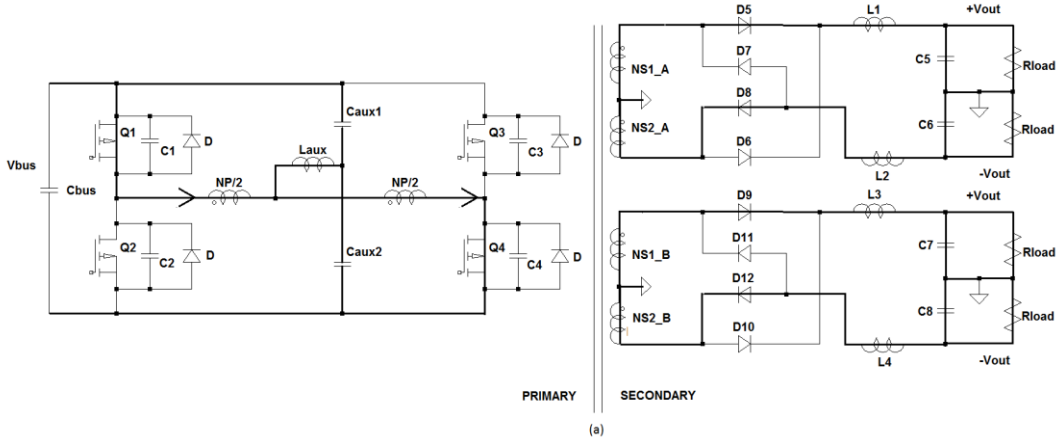
The circuit diagram of proposed ZVS full-bridge converter is shown in figure 83. In proposed circuit, there are four main switches Q1 Q2 Q3 Q4 (also the parasitic capacitances and body diodes are including as well), Np/2 and Np/2 are primary windings of equal turns, Ns1_A, Ns2_A, Ns1_B and Ns2_B are secondary windings, D1-D8 are output rectifier diode, L1-L4 are output filter inductor, C5-C8 are output filter capacitors. Laux is an auxiliary inductor, Caux1 and Caux2 are voltage divider capacitors. The passive energy storage circuit consists of Laux, Caux1 and Caux2. The operation of circuit for both outputs on secondary side of converter is always remains same and constant. In discussion, I can consider only one output circuit of secondary side for simplicity.

4.5.2 Operation Principle of Novel ZVS Full-bridge Converter

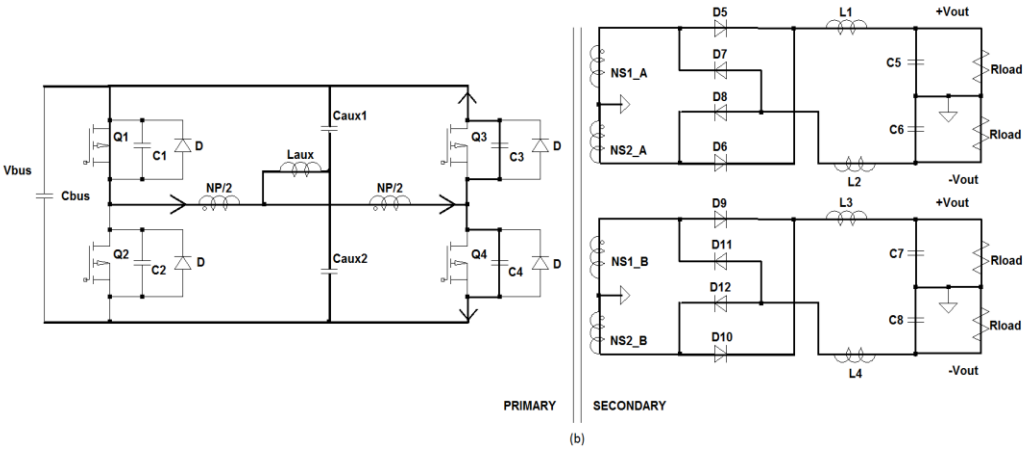
The converter has several operating cycles to perform ZVS over entire range of cycle. The related equivalent circuits under different operating cycles are shown in Figure 84.

For analysis of circuit, several assumptions are made to simplify the analysis such as

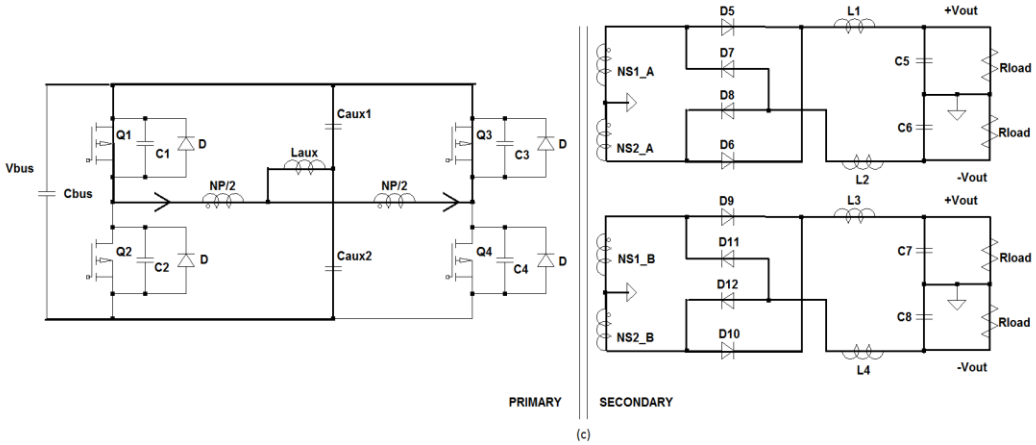
- Ideal components are considered and assume Vbus = Vin.
- Inductor of output filter is large enough that it can be considered as a constant current source.
- Caux 1 and Caux2 can act as a constant voltage source, (Vcaux1=Vcaux2=Vbus/2).



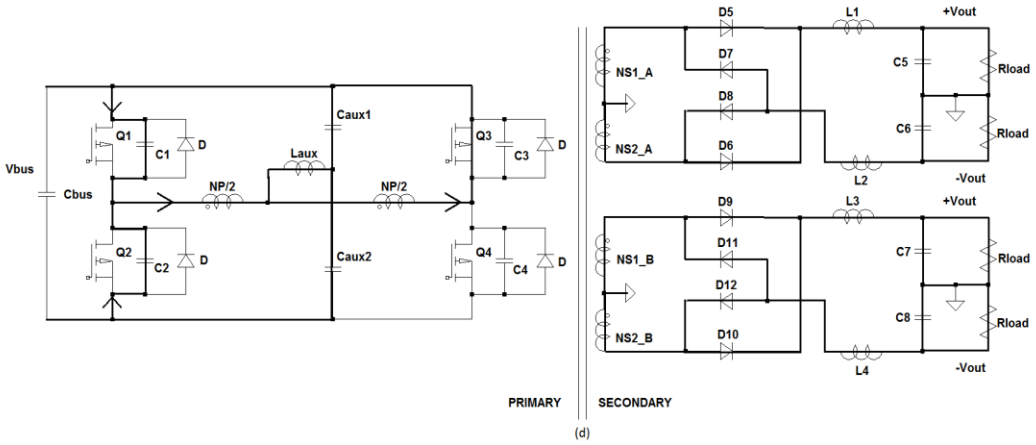
(a)



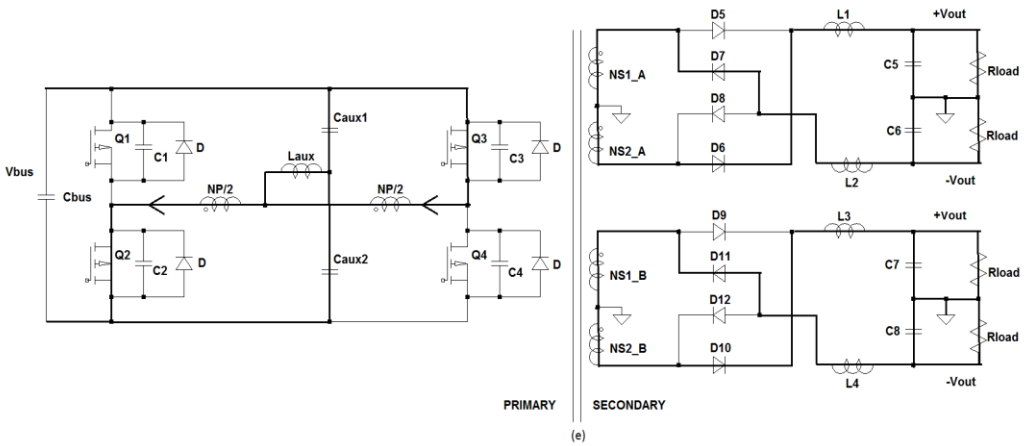
(b)


Vbus
Cbus
Q1
C1
D
Q2
C2
Q3
C3
Q4
C4
Laux
Caux1
Caux2
NP/2
NP/2
D5
L1
+Vout
D7
NS1_A
D8
NS2_A
D6
C5
Rload
C6
Rload
L2
-Vout
D9
L3
+Vout
D11
NS1_B
D12
NS2_B
D10
C7
Rload
C8
Rload
L4
-Vout
PRIMARY
SECONDARY

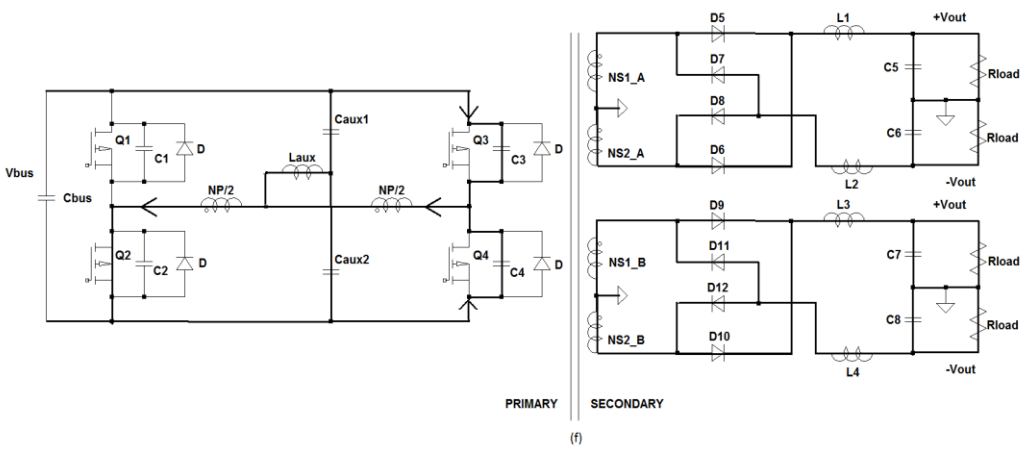
(c)


Vbus
Cbus
Q1
C1
D
Q2
C2
Q3
C3
Q4
C4
Laux
Caux1
Caux2
NP/2
NP/2
D5
L1
+Vout
D7
NS1_A
D8
NS2_A
D6
C5
Rload
C6
Rload
L2
-Vout
D9
L3
+Vout
D11
NS1_B
D12
NS2_B
D10
C7
Rload
C8
Rload
L4
-Vout
PRIMARY
SECONDARY

(d)


Vbus
Cbus
Q1
C1
D
Q2
C2
Q3
C3
Q4
C4
Laux
Caux1
Caux2
NP/2
NP/2
D5
L1
+Vout
D7
NS1_A
D8
NS2_A
D6
C5
Rload
C6
Rload
L2
-Vout
D9
L3
+Vout
D11
NS1_B
D12
NS2_B
D10
C7
Rload
C8
Rload
L4
-Vout
PRIMARY
SECONDARY

(e)


Vbus
Cbus
Q1
C1
D
Q2
C2
Q3
C3
Q4
C4
Laux
Caux1
Caux2
NP/2
NP/2
D5
L1
+Vout
D7
NS1_A
D8
NS2_A
D6
C5
Rload
C6
Rload
L2
-Vout
D9
L3
+Vout
D11
NS1_B
D12
NS2_B
D10
C7
Rload
C8
Rload
L4
-Vout
PRIMARY
SECONDARY

(f)

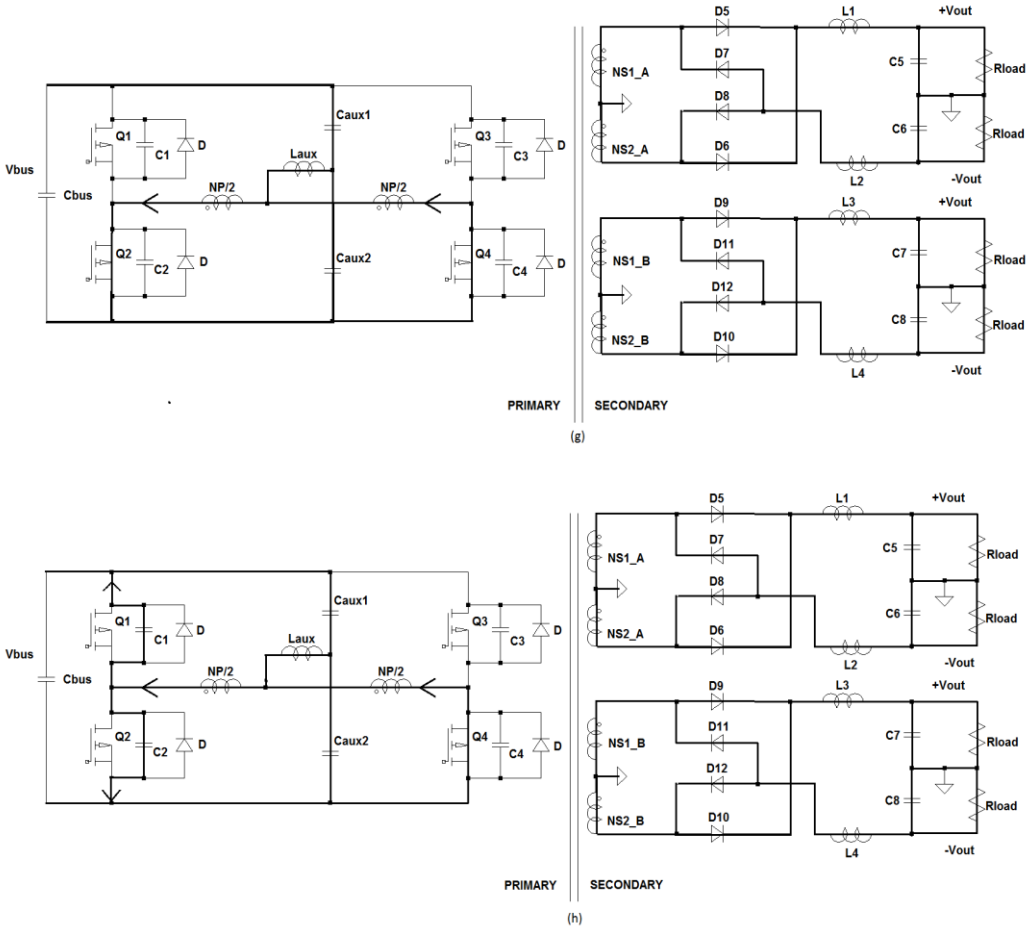


Figure 84: (a) Active circuit of mode A. (b) Active circuit of mode B. (c) Active circuit of mode C. (d) Active circuit of mode D (e) Active circuit of mode E. (f) Active circuit of mode F. (g) Active circuit of mode G. (h) Active circuit of mode H.

Mode A

Before time t0, the power is transferred from input source Vin to the load. The MOSFET Q1 and Q4 are conducting to build the primary voltage across transformer. On the secondary side, the D5, D8, D9 and D12 are conducting to deliver the power to load. The voltage across auxiliary winding is equal to zero V_{Laux} =0. Therefore, the current in auxiliary inductor freewheels and remains unchanged.

Mode B

At to, Q4 is turned OFF and Q1 still turn ON. The auxiliary circuit is providing current to charge up capacitor C4 and discharge up capacitor C3. On the secondary side, the diodes become reverse bias and are not conducting. Moreover, the rising voltage across C4 due to current providing by auxiliary circuit builds up to voltage equal to $V_{IN.}$ At the

end of this mode, the voltage across C4 charges up to input voltage V_{IN} and the capacitor C3 discharges completely.

Mode C

This mode starts when C4 charges up to V_{IN} and C3 completely discharges to zero voltage. Also Q1 remains turn ON in this mode and MOSFET Q3 turns ON at zero voltage across it. Therefore, the free wheel mode builds the constant voltage of V_{IN} across primary windings of transformer and the auxiliary inductor is charging due to voltage across it. Moreover, the secondary diodes clamp the secondary voltage to output voltage.

Mode D

MOSFET Q3 still conducts in this mode as shown in figure 84(d). However, MOSFET Q1 turns OFF in this mode. The capacitor C2 is discharging from V_{IN} and C1 is charging up to $V_{IN.}$ The auxiliary inductor draws a current during this mode which provides energy for discharging C2 and charging C1. The capacitor C1 charges up and C2 discharges fully at the end of this mode.

Mode E

In this mode, Q3 still conducts and Q2 turns ON at zero voltage across it. The primary current starts to flow in opposite direction to previous power transfer mode. The power is transferred from primary to secondary side load through Q3 and Q2. The output diodes D6, D7, D10 and D11 start conducts to deliver power to the load.

Mode F

In this mode, Q3 is turned OFF and Q2 still turn ON. The capacitor C3 is charging to V_{IN} and capacitor C4 is discharging from V_{IN}. The auxiliary circuit is drawing current to discharge C4 and charge up C3. On the secondary side, the diodes become reverse bias and are not conducting. Moreover, the voltage across C4 drops to zero due to current drawn by auxiliary circuit and C3 voltage builds up to $V_{IN.}$ At the end of this mode, the

voltage across C3 charges up to input voltage V_{IN} and the capacitor C4 discharges completely.

Mode G

This mode starts when C4 discharges up to zero voltage and C3 charges up to V_{IN} voltage. Also Q2 remains turn ON in this mode and MOSFET Q4 turns ON at zero voltage across it. Therefore, the free wheel mode builds the zero voltage across primary windings of transformer and the auxiliary inductor (V_{Laux}) has negative voltage across it. The current in auxiliary winding flows in opposite direction as shown in figure 84(g). Moreover, the secondary diodes clamp the secondary voltage to output voltage.

Mode H

MOSFET Q4 still conducts in this mode as shown in figure 84(h). However, MOSFET Q2 turns OFF in this mode. The capacitor C1 is discharging from V_{IN} and C2 is charging up to $V_{IN.}$ The auxiliary inductor provides energy for discharging C1 and charging C2 in this mode. The capacitor C1 discharges and C2 charges fully at the end of this mode.

4.6 Several Prototypes of Proposed Power Supply

Several prototypes of SMPS have been designed and analysed in lab. The proposed CM noise balance scheme of flyback, PFC boost and full-bridge converter have also been implemented in prototypes of SMPS. The following prototypes of SMPS have been built in lab for audio amplifier.

4.6.1 First Prototype of SMPS

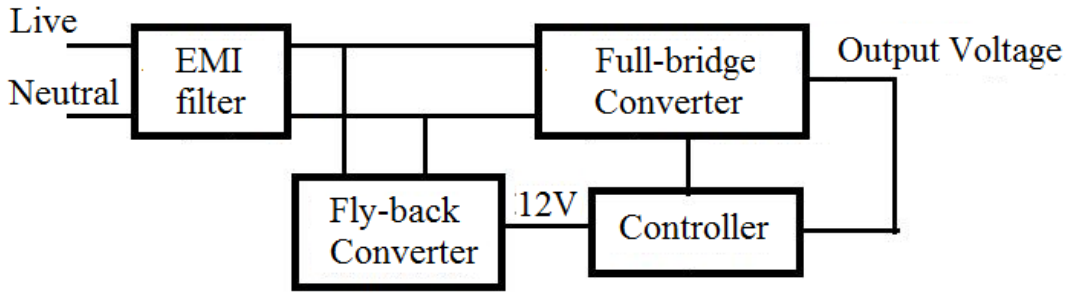


Figure 85: Block diagram of First Prototype of SMPS

First prototype of SMPS has been built in lab. The flyback converter is designed to power PWM controller for full-bridge converter. The hard-switched full-bridge converter is designed for power transfer stage from input to output of converter. Moreover, passive EMI filter is also designed for mitigation of conducted EMI noise in SMPS.

4.6.2 Second Prototype of SMPS

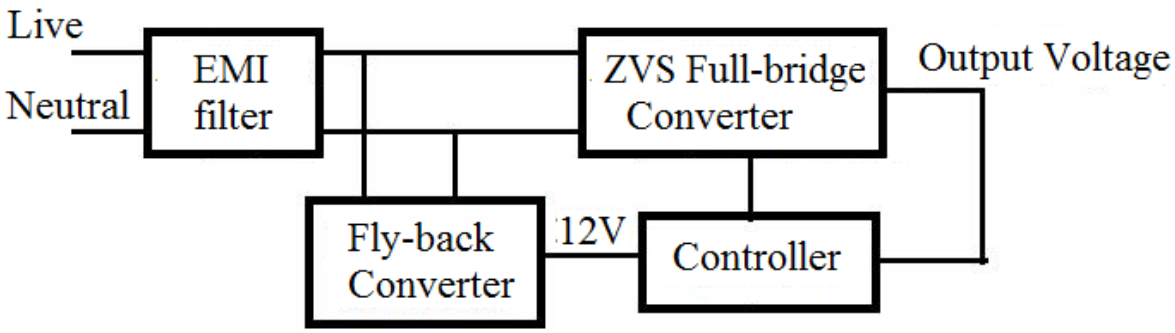


Figure 86: Block diagram of Second Prototype of SMPS

Second prototype of SMPS has been built in lab. ZVS full-bridge converter topology has chosen to fulfil the power requirement of audio amplifier. However, flyback converter is designed to power PWM controller for ZVS-full-bridge converter. Moreover, novel ZVS full-bridge converter has been proposed and fabricated in lab. Conventional and novel ZVS full-bridge converter has been implemented in this prototype. Furthermore, passive EMI filter is also designed for mitigation of conducted EMI noise in SMPS.

Modified Version of Second Prototype of SMPS

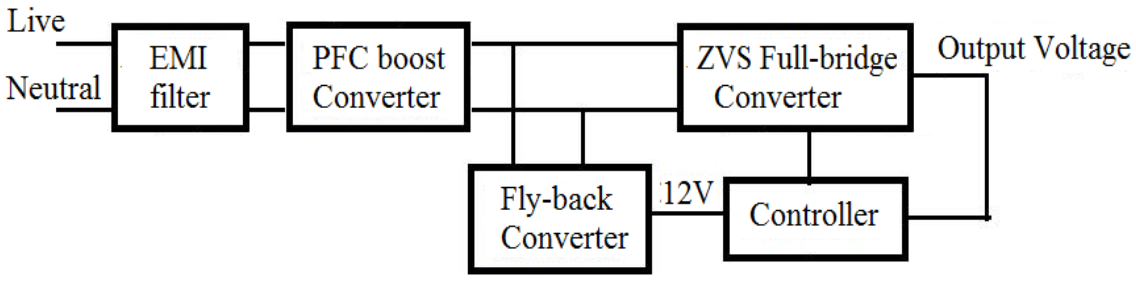


Figure 87: Block diagram of modified Second Prototype of SMPS

To improve the power factor of converter, PFC boost converter has been added in second prototype of SMPS. PFC boost converter topology has chosen to increase power factor of converter. However, flyback converter is designed to power PWM controller for ZVS-full-bridge converter.

4.6.3 Third Prototype of SMPS

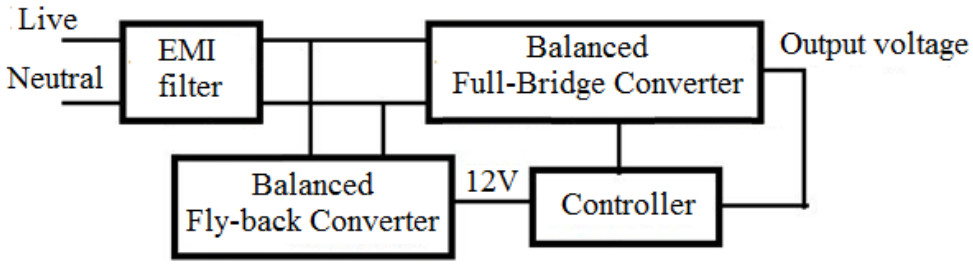


Figure 88: Block diagram of Third Prototype of SMPS

Third prototype of SMPS has been built in lab. In this prototype, balanced flyback and full-bridge converter have been implemented. Wire wound and planar transformer has been constructed for balanced full-bridge converter. The passive EMI filter and internal balancing proposed scheme have been employed to cope with EMI standard requirement. The size of EMI filter is considerably reduced due to novel balancing technique.

Modified Version of Third Prototype of SMPS

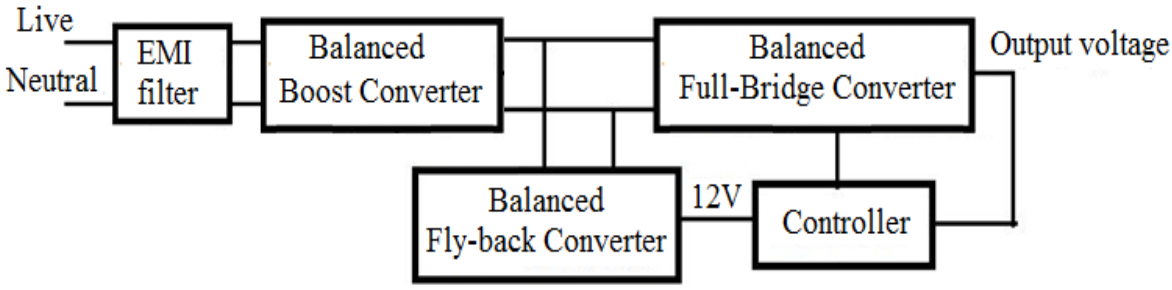


Figure 89: Block diagram of modified Third Prototype of SMPS

To improve the power factor of converter, PFC boost converter has been added in third prototype of SMPS. PFC boost converter topology has chosen to increase power factor

of converter. Moreover, novel balancing technique for PFC boost converter has been proposed and fabricated in lab.

4.7 Evaluate the Performance of Power Supply

To verify the proposed methodology, experiments are performed in lab to validate the effectiveness of novel balancing technique. Several experiments are accomplished on prototype of built SMPS. Here is the list of several experimental setup used to analyse SMPS for audio amplifier.

- Conducted EMI noise measurement
- Output noise measurement
- Audio power amplifier performance evaluation

4.7.1 Conducted EMI noise measurement

The mains power lines have an impedance varies extensively. The impedance varies according to different places like a remote and industrial area effect on impedance of system. The conducted EMI noise measurement of power supply varies widely due to not constant impedance of power supply. Therefore, standard impedance is required to measure noise of power supply. As a result, LISN ("Line Impedance Stabilizer Network") is used to stable the impedance for measurement. The noise current from power supply generates noise voltages across resistors of LISN. These noise voltages can be fed to spectrum analyser. The analyser measures the harmonic content of frequencies present with in noise voltages of SMPS. The standardized setup for measuring conducted EMI noise is shown in figure 90.

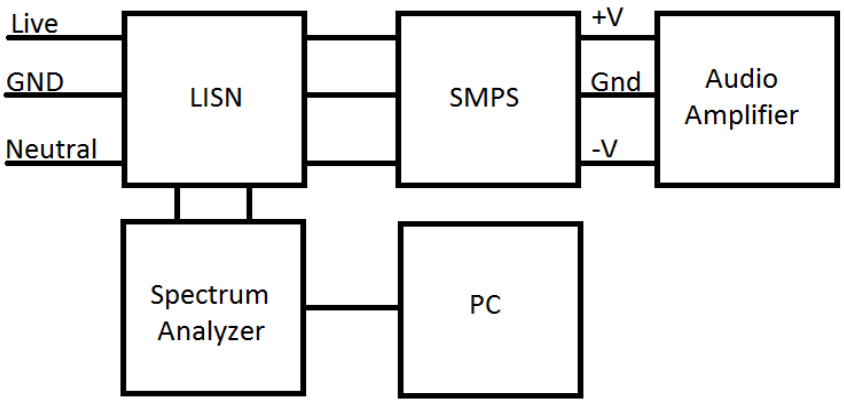


Figure 90: Measurement setup for Conducted EMI noise

4.7.2 Output noise measurement

The measurement setup for output noise for SMPS is shown in figure 91. The oscilloscope is used to measure the noise of SMPS. The ac coupling of oscilloscope is chose to measure the noise from power supply. Both channels are used to measure noise of SMPS.

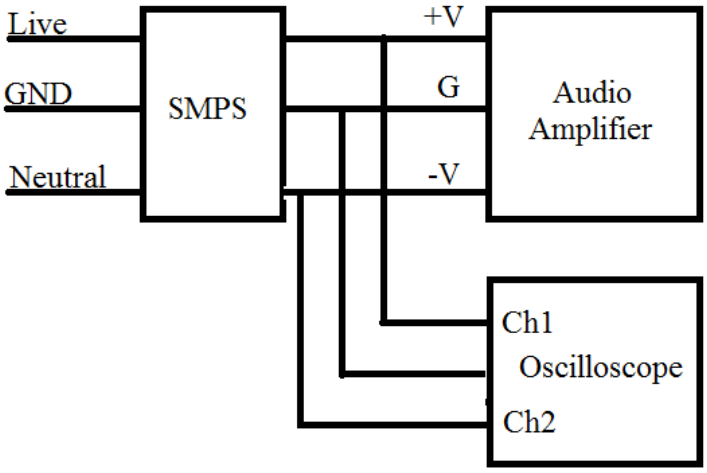


Figure 91: Measurement setup for Output noise

4.7.3 Audio power amplifier performance evaluation

The performance of proposed novel low noise SMPS is evaluated on the basis of subjective and objective tests performed on the power amplifier. The subjective tests involved the blind audio listening tests. In a blind listening test, the listener was unaware of the power supply used to power the audio amplifier. Therefore, the

psychological influence was not affected the judgment of listener related to brand product. On the basis of subjective test, the decision has been made that SMPS solution is as good as or better than the linear solution. Also the performance of SMPS is analyzed on the basis of objective test such as THD+N, frequency response and audio dynamic range. The audio precision equipment is used to measure the above tests and compare these results with LPS. Dynamic range of audio amplifier is to be measured from the response of device with the audio variation. It is useful test to provide the performance of audio product under the wide variation in audio dynamic range.

4.7.3.1 Subjective tests

Blind audio listening test

The blind audio listening test set up is shown in figure 92. SMPS and linear power supply are used to power the audio amplifier and load the speaker. The listeners do not have knowledge about the power supply running at a time. The listener provides the rating depend on sound quality of audio amplifier with different power supplies.

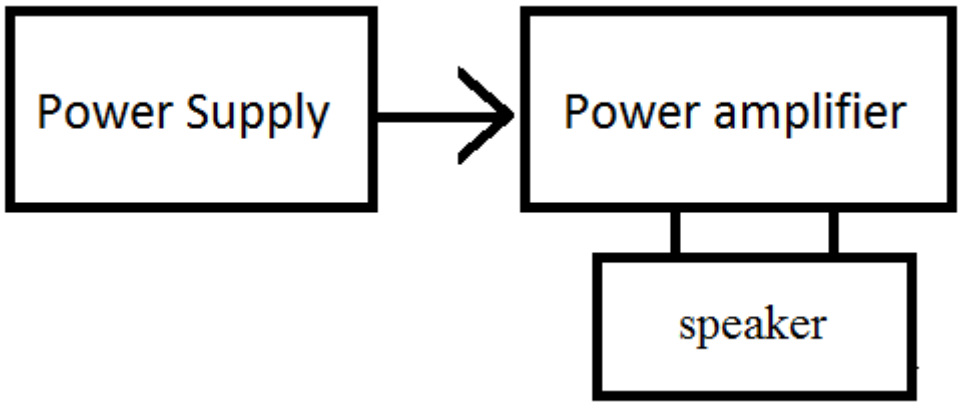


Figure 92: Measurement setup for blind tests

4.7.3.2 Objective tests

- THD+N Vs Frequency
- THD+N Vs Level
- FFT Distortion Spectrum

THD+N Vs Frequency

THD+N measure total harmonic distortion plus noise in a system. It includes all noise and other unwanted signal such as buzz, hum and harmonics of fundamental frequencies. It represents the value of THD+N at range of frequencies from 20Hz to 20KHz.

THD+N Vs Level

It sweeps the level of input voltage and measures THD+N at different level of input voltage.

FFT Distortion Spectrum

This test is to see how clean the output is on an amp based on harmonics generated form a fundamental tone.

Audio amplifier measurement setup for objective tests

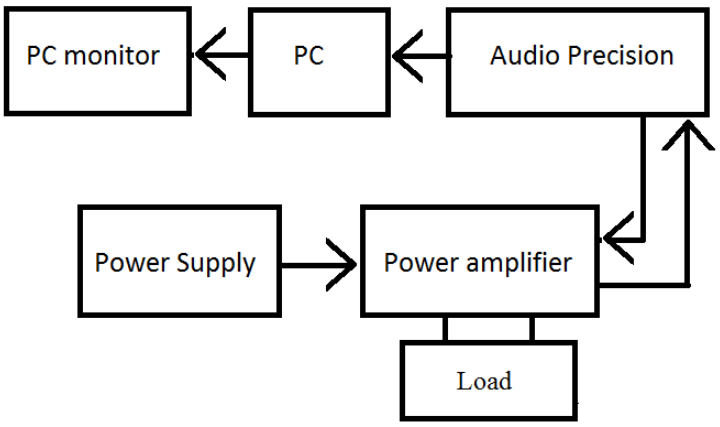


Figure 93: Measurement setup for objective tests

The measurement setup for objective test of audio amplifier is shown in figure 93. The audio precision equipment is used for the evaluation of performance of an audio amplifier.

4.8 Summary

In this chapter, a novel balancing technique is proposed to reduce the overall CM noise of PFC boost converter, fly-back converter and full-bridge converter. In this scheme, I introduced the anti-phase noise source with compensating winding and compensating capacitor to generate a complimentary voltage. The voltage produced due to additional winding and capacitor is 180° out of phase as compared to the original noise voltage. Therefore, the overall noise is cancelled out with the help of novel technique. In addition, a novel ZVS full-bridge converter is proposed to improve the range of zero voltage switching over the entire range of load.

5 CHAPTER 5 EXPERIMENTAL RESULTS AND DISCUSSION

5.1 Introduction

In this chapter, experimental results are discussed for proposed PFC boost converter, flyback converter and full-bridge converter. The performance of audio amplifier is analyzed using designed SMPS to compare with existing linear power supply. In the end, conclusion has been made to finalize the best prototype of SMPS which are comparable to linear power supply in accordance to audio performance of audio amplifier.

5.2 PFC boost converter

The experiments are carried out to validate the proposed methodology of PFC boost converter. In experiments, the PFC boost converter is supplied with input voltage of 230Vac, input frequency of 50 Hz and switching frequency of 125KHz.

5.2.1 Conducted EMI noise

The conventional and balanced PFC boost circuit is designed and built in lab. The heat-sinks of MOSFET and Diode are attached to ground in conventional method. On the other hand, coupled inductor and compensation capacitor are added in balanced converter and heat-sink of diode is attached to neutral line. Then, the conducted EMI scan has been performed on these converters (conventional and balanced).

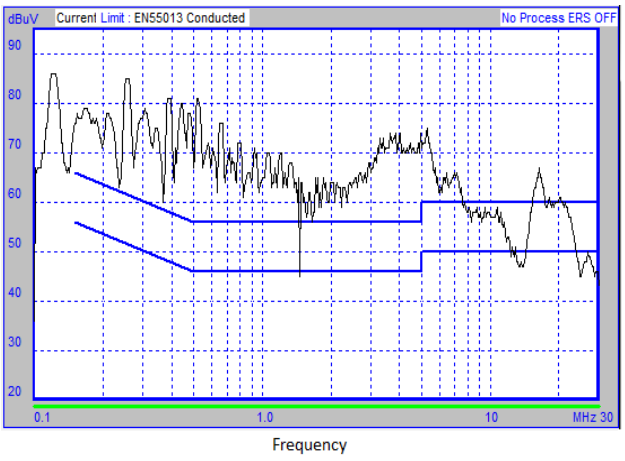


Figure 94: Conducted EMI noise measurement of conventional PFC boost converter

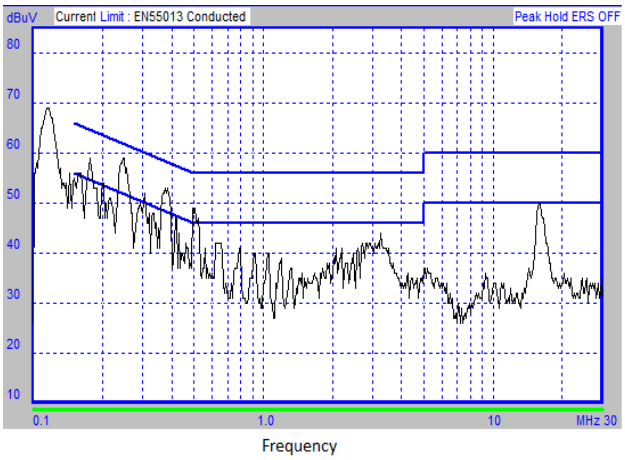


Figure 95: Conducted EMI noise measurement of balanced PFC boost converter

The EMI scans for conventional and balanced PFC boost converters are shown in figure 94 and figure 95 respectively. It is clear from the results that the first, second, third peak of EMI noise are at 125KHz of 83dBuV, 250KHz of 82dBuV and 400KHz of 81dBuV, respectively for conventional method. On the other hand, in balanced converter the respective same frequency peaks appear for 69dBuV, 60 dBuV and 54 dBuV, respectively. So I can say that EMI noise is improved by almost 14dB by applying proposed balancing technique in boost converter.

5.3 Flyback Converter

To validate the proposed novel balancing technique, a flyback converter of 132 kHz switching frequency is built and tested. The input and output specifications of this converter are shown in table 1 below

Table 1: Specification of Flyback converter

	Specification	***Value***
1.	Input Voltage	230V
2.	Input frequency	50Hz
3.	Output Voltage	12V
4.	Output Current	1A
5.	Output power	12W

5.3.1 Conducted EMI noise

The results of conducted EMI noise measurements for the Flyback converter using the conventional transformer and new modified balanced transformer winding structure are shown in figure 96 and figure 97. It is predicted that the conducted EMI noise for balanced transformer winding is improved by almost 10 dB.

The proposed technique used the extra windings in a transformer which not only reduce the EMI noise but also increase the performface of power supply. This would provide the benefits of improved EMI reduction in practical designs compatible with EMI specifications.

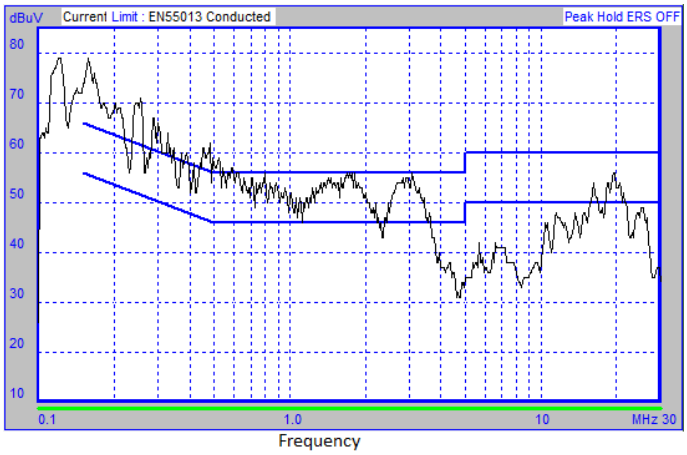


Figure 96: Conducted EMI noise measurement of conventional flyback converter

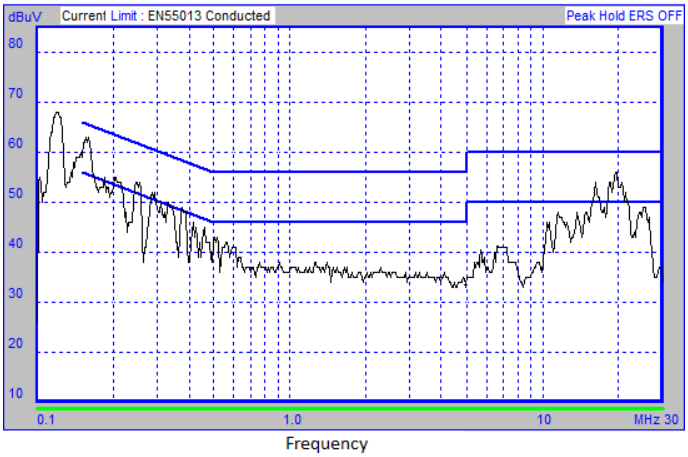


Figure 97: Conducted EMI noise measurement of balanced flyback converter

5.4 First Prototype of SMPS (Hard switching Full-bridge Converter)

The switching frequency of full-bridge converter is 110 KHz with input and output specifications provided in Table 2.

Table 2: Specification of First prototype of SMPS

	Specification	***Value***
1.	Input Voltage	230V
2.	Input frequency	50Hz
3.	Output Voltage	+/-48V
4.	Output Current	6A
5.	Output power	1152W

5.4.1 Conducted EMI noise

A conducted EMI test scan from 150kHz to 30MHz is performed on a converter. The EMI scan for first prototype of SMPS (hard-switching converter) is shown in figure 98.

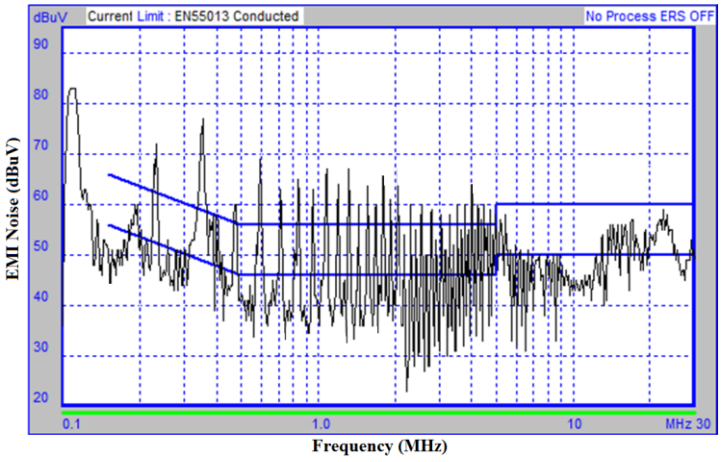


Figure 98: Conducted EMI noise measurement of first prototype (Hard switching Full-bridge Converter)

It is evident from the above result that the first peak of EMI noise is at 110kHz of 82dBuV. and second and third peak of EMI noises appear at 220KHz and 330KHz of 71dBuV and 76dBuV respectively. The conducted EMI noise of SMPS is above the

limit in the range of frequency from 200 kHz to 5 MHz. Therefore it crosses the limit set by international EMI standard (CISPR-22) and fails the EMI test.

5.4.2 Output Noise

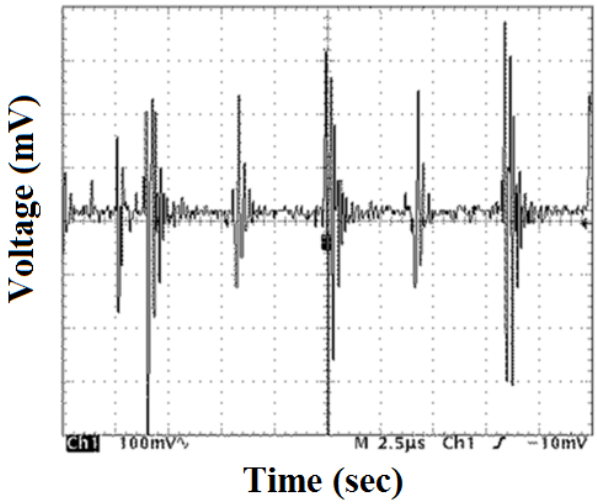


Figure 99: Output noise of first prototype (Hard switching full-bridge converter)

The output noise of first prototype of SMPS (hard-switching converter) is shown in figure 99. The maximum peak to peak level of output noise is 730mVp-p.

5.5 Second Prototype of SMPS (ZVS Full-bridge Converter)

The switching frequency of ZVS full-bridge converter is 100 KHz with input and output specifications given in Table 3.

Table 3: Specification of Second prototype of SMPS

	Specification	***Value***
1.	Input Voltage	230V
2.	Input frequency	50Hz
3.	Output Voltage	+/-48V
4.	Output Current	6A
5.	Output power	1152W

5.5.1 Conducted EMI noise

The EMI scan for second prototype of SMPS (ZVS converter) is shown in figure 100.

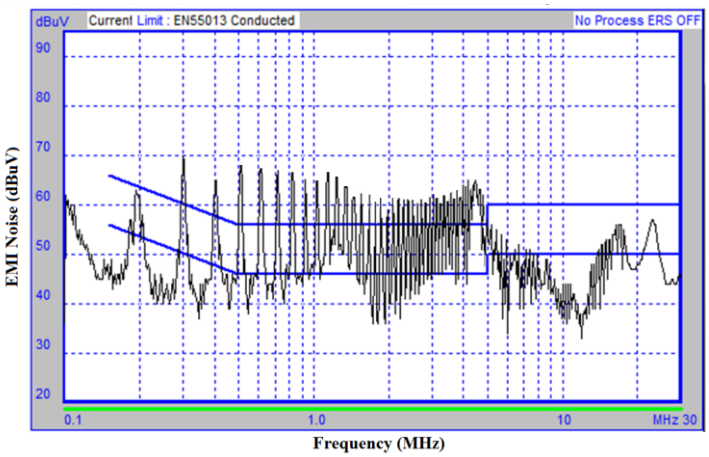


Figure 100: Conducted EMI noise measurement of Second prototype (ZVS full-bridge Converter)

It is clear from the result that the first peak of EMI noise is at 100KHz of 62dBuV. Moreover, the second and third peak of EMI noises are at 200KHz and 300KHz of 64dBuV and 70dBuV respectively. Also, the conducted EMI noise of SMPS is above the limit in the range of frequency from 300 kHz to 5 MHz. Therefore it crosses the limit set by international EMI standard (CISPR-22) and fails the EMI test.

5.5.2 Output Noise

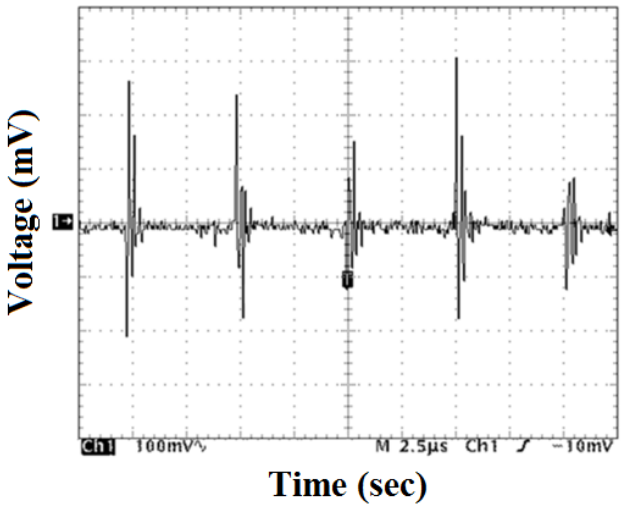


Figure 101: Output noise of ZVS Second prototype (ZVS full-bridge converter)

The output noise of second prototype of SMPS (ZVS converter) is shown in figure 101. The maximum peak to peak level of output noise is 480mVp-p.

5.6 Third Prototype of SMPS (Balanced Full-bridge Converter)

5.6.1 Wire Wound Transformer

In order to validate the theory of balancing technique, full-bridge converter has been investigated by performing experimental tests on two different types of transformer construction. As discussed earlier about transformer with different winding arrangements known as conventional and interleaving are built and tested. The proposed balancing technique has been applied on these transformers constructions. The switching frequency of full-bridge converter is considered 110 KHz with input and output specifications are presented in Table 4.

Table 4: Specification of Third prototype of SMPS with wire-wound Transformer

	Specification	***Value***
1.	Input Voltage	230V
2.	Input frequency	50Hz
3.	Output Voltage	+/-48V
4.	Output Current	6A
5.	Output power	1152W

5.6.2 Conventional Transformer Winding

5.6.2.1 Conducted EMI noise

First EMI scan test is performed on conventional transformer winding structure and the second EMI scan is performed on corresponding proposed balanced transformer structure.

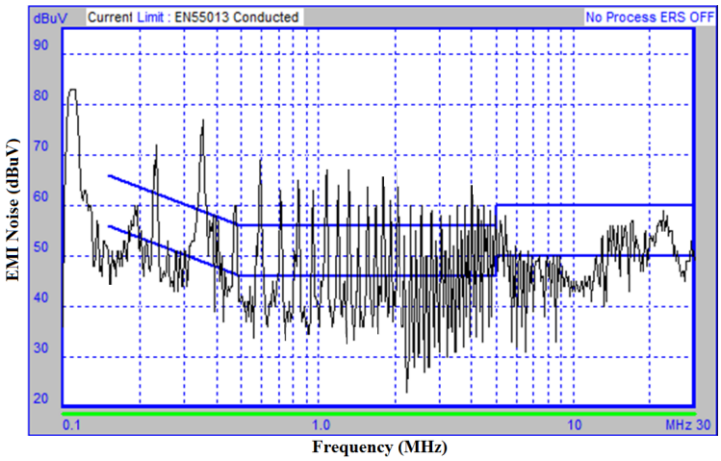


Figure 102: Conducted EMI noise measurement of full-bridge converter with conventional transformer

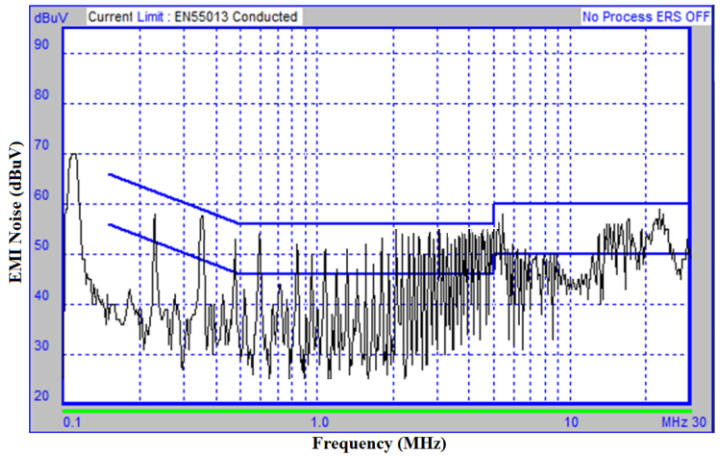


Figure 103: Conducted EMI noise measurement of full-bridge converter with balanced conventional transformer

In figure 102, the first peak of EMI noise is at 110KHz of 82dBuV. Moreover, the second and third peak of EMI noises are at 220KHz and 330KHz of 71dBuV and 76dBuV respectively. On the other hand, the first peak of EMI noise in balanced conventional transformer winding is at 110KHz of 70dBuV shown in figure 103. Moreover, the second and third peak of EMI noises are at 220KHz and 330KHz of 57dBuV and 56dBuV respectively. Overall, the EMI noise has improved by 12dB with incorporating balanced technique in conventional transformer.

5.6.2.2 Output Noise

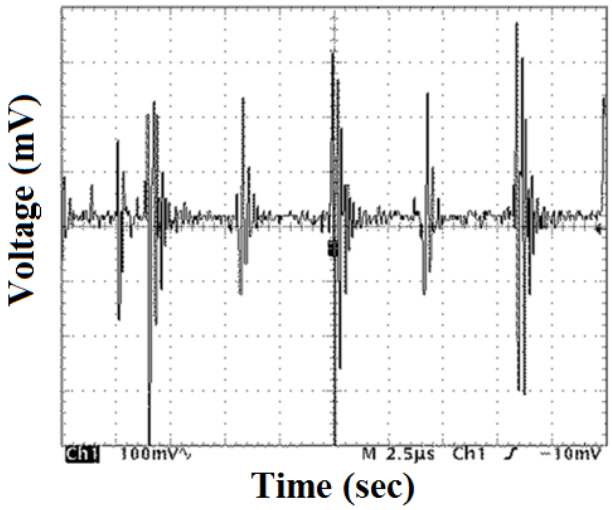


Figure 104: Output noise of full-bridge converter with conventional transformer

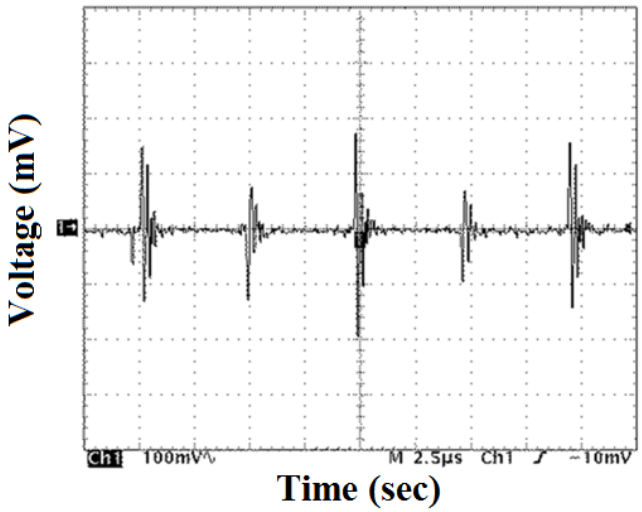


Figure 105: Output noise of full-bridge converter with balanced conventional transformer

The output noise of full-bridge converter with conventional transformer and balanced conventional transformer are shown in figure 104 and figure 105 respectively. The maximum peak to peak level of output noise with conventional transformer is 730mVp-p. However, the maximum peak to peak level of output noise with balanced conventional transformer is 370mVp-p. Overall, the output noise has reduced significantly due to novel balancing technique.

5.6.3 Interleaved Transformer Winding

5.6.3.1 Conducted EMI noise

The EMI scan is performed on interleaved transformer winding and results of unbalanced and balanced winding arrangements are compared for interleaved transformer.

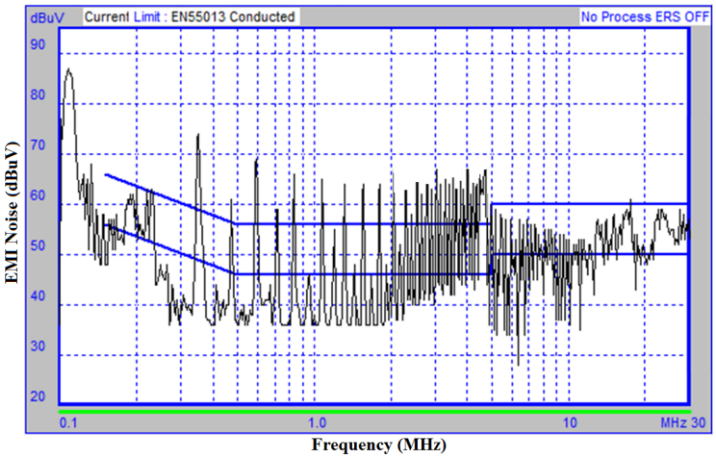


Figure 106: Conducted EMI noise measurement of full-bridge converter with interleaved transformer

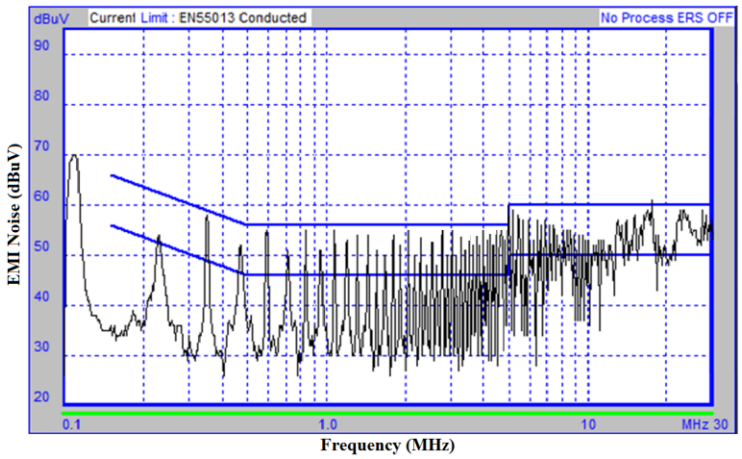


Figure 107: Conducted EMI noise measurement of full-bridge converter with balanced interleaved transformer

In figure 106, the first peak of EMI noise is at 110KHz of 84dBuV. Moreover, the second and third peak of EMI noises are at 220KHz and 330KHz of 63dBuV and 73dBuV respectively. On the other hand, the first peak of EMI noise in balanced interleaved transformer winding is at 110KHz of 70dBuV is shown in figure 107. Moreover, the second and third peak of EMI noises are at 220KHz and 330KHz of

53dBuV and 58dBuV respectively. Overall, the EMI noise has improved by 10dB with incorporating balanced technique in interleaved transformer.

5.6.3.2 Output Noise

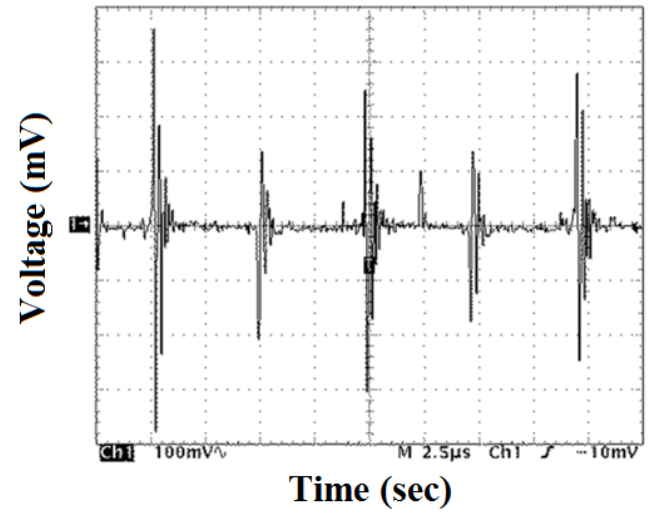


Figure 108: Output noise of full-bridge converter with interleaved transformer

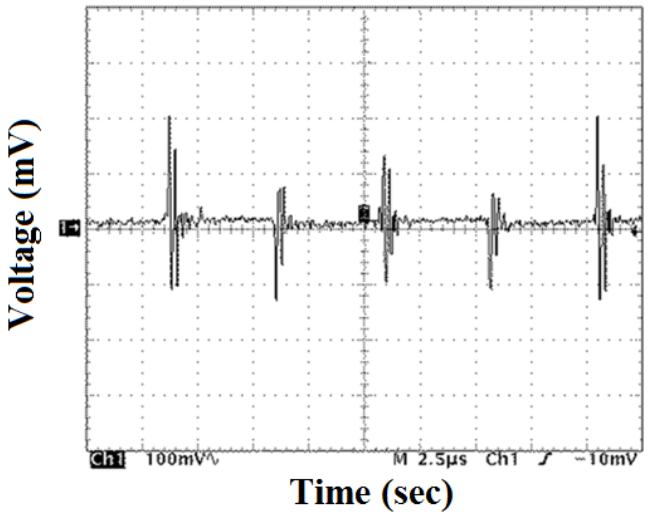


Figure 109: Output noise of full-bridge converter with balanced interleaved transformer

The output noise of full-bridge converter with interleaved transformer and balanced interleaved transformer are shown in figure 108 and figure 109 respectively. The maximum peak to peak level of output noise with interleaved transformer is 750mVp-p. However, the maximum peak to peak level of output noise with balanced interleaved transformer is 300mVp-p. Overall, the output noise has reduced significantly due to novel balancing technique.

5.6.4 Planar Transformer

In order to validate the theory of balancing technique, full-bridge converter has been investigated by performing experimental tests on two different types of planar transformer construction. The switching frequency of full-bridge converter is 110 KHz with input and output specifications given in Table 5.

Table 5: Specification of Third prototype of SMPS with Planar Transformer

	Specification	***Value***
1.	Input Voltage	230V
2.	Input frequency	50Hz
3.	Output Voltage	+/-48V
4.	Output Current	6A
5.	Output power	1152W

5.6.5 Conventional planar Transformer Winding

5.6.5.1 Conducted EMI noise

The conducted EMI test scan is performed with conventional planar transformer windings and the corresponding balanced planar transformer windings structure.

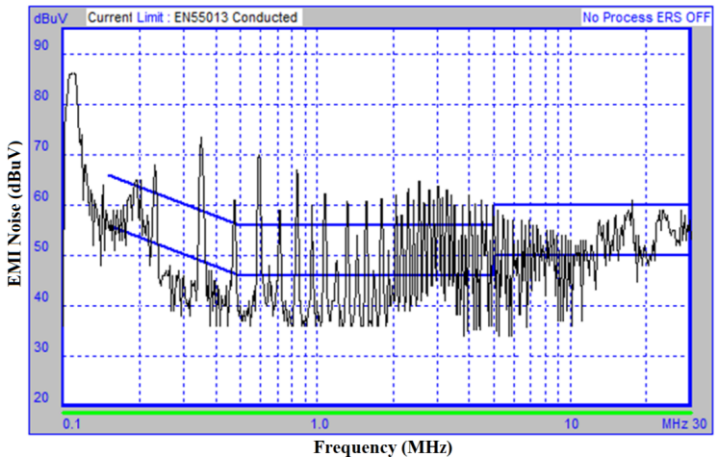


Figure 110: Conducted EMI noise measurement of full-bridge converter with conventional planar transformer

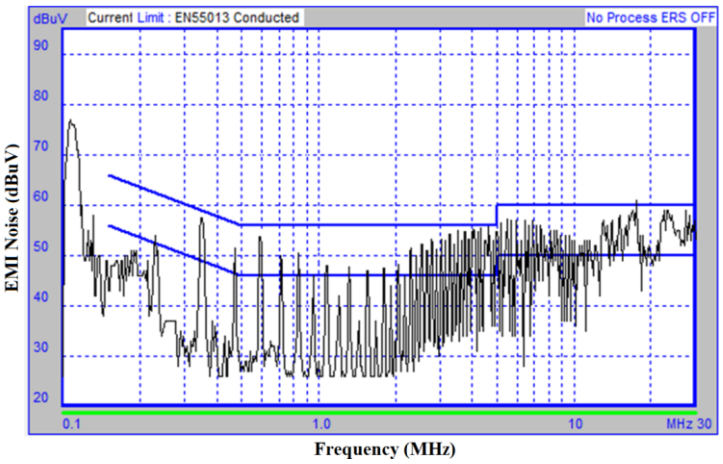


Figure 111: Conducted EMI noise measurement of full-bridge converter with balanced conventional planar transformer

In figure 110, the first peak of EMI noise is at 110KHz of 83dBuV. Moreover, the second and third peak of EMI noises are at 220KHz and 330KHz of 68dBuV and 73dBuV respectively. On the other hand, the first peak of EMI noise in balanced conventional planar transformer is at 110KHz of 77dBuV as shown in figure 111. Moreover, the second and third peak of EMI noises are at 220KHz and 330KHz of 55dBuV and 57dBuV respectively. Overall, the EMI noise has improved by 13dB with incorporating balanced technique in conventional planar transformer.

5.6.5.2 Output Noise

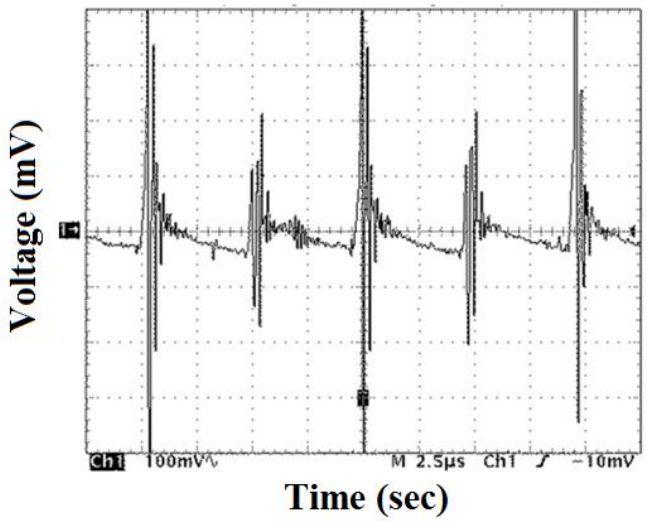


Figure 112: Output noise of full-bridge converter with conventional planar transformer

The output noise of full-bridge converter with conventional planar transformer is shown in figure 112. The maximum peak to peak level of output noise is 800mVp-p.

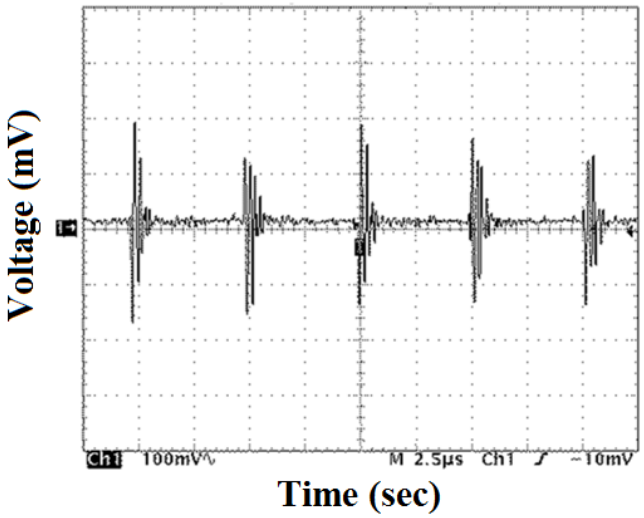


Figure 113: Output noise of full-bridge converter with balanced conventional planar transformer

The output noise of full-bridge converter with balanced conventional planar transformer is shown in figure 113. The maximum peak to peak level of output noise is 310mVp-p. Overall, the output noise has reduced considerably due to balanced conventional planar transformer.

5.6.6 Interleaved planar Transformer Winding

5.6.6.1 Conducted EMI noise

The EMI scan is performed on interleaved transformer windings and the corresponding balanced interleaved transformer windings. Moreover, the results of unbalanced and balanced winding arrangements for interleaved transformer structure are compared.

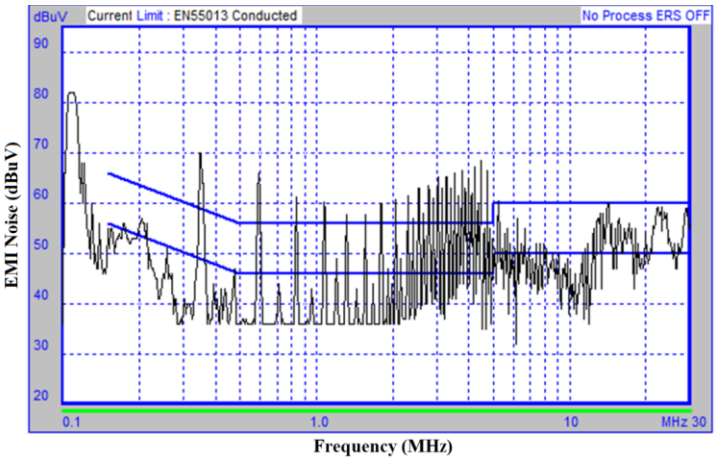


Figure 114: Conducted EMI noise measurement of full-bridge converter with interleaved transformer

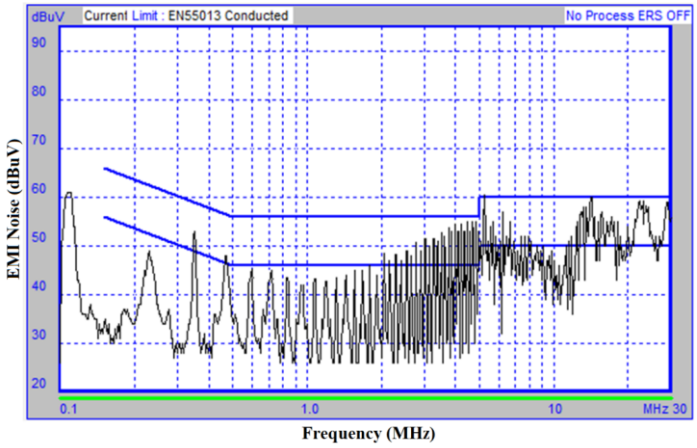


Figure 115: Conducted EMI noise measurement of full-bridge converter with balanced interleaved planar transformer

In figure 114, the first peak of EMI noise is at 110KHz of 81dBuV. Moreover, the second and third peak of EMI noises are at 220KHz and 330KHz of 58dBuV and 70dBuV respectively. On the other hand, the first peak of EMI noise in balanced interleaved planar transformer is at 110KHz of 61dBuV as shown in fig 115. Moreover, the second and third peak of EMI noises are at 220KHz and 330KHz of 49dBuV and 54dBuV respectively. Overall, the EMI noise has improved by 9dB with incorporating balanced technique in interleaved planar transformer.

5.6.6.2 Output Noise

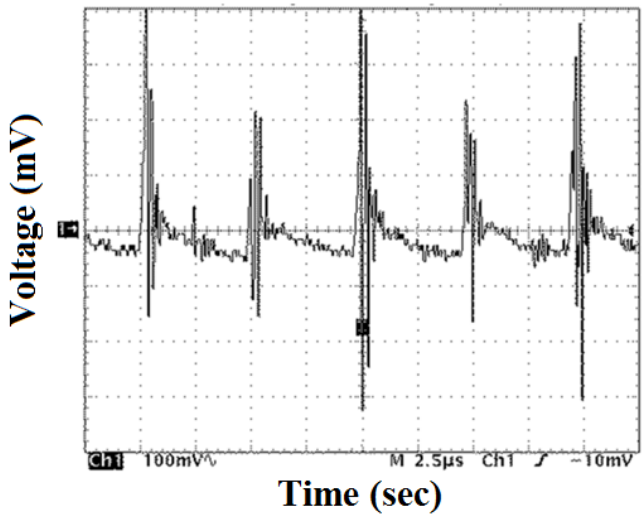


Figure 116: Output noise of full-bridge converter with interleaved planar transformer

The output noise of full-bridge converter with interleaved planar transformer is shown in figure 116. The maximum peak to peak level of output noise is 720mVp-p.

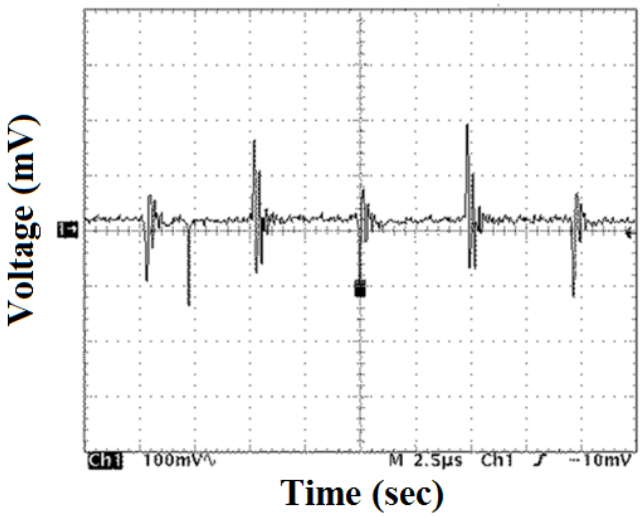


Figure 117:Output noise of full-bridge converter with balanced interleaved planar transformer

The output noise of full-bridge converter with balanced interleaved planar transformer is shown in figure 117. The maximum peak to peak level of output noise is 270mVp-p.

5.7 Existing Linear Power supply

5.7.1 Conducted EMI noise

The EMI scan is performed on existing Linear power supply by collaborating company (Naim Audio)

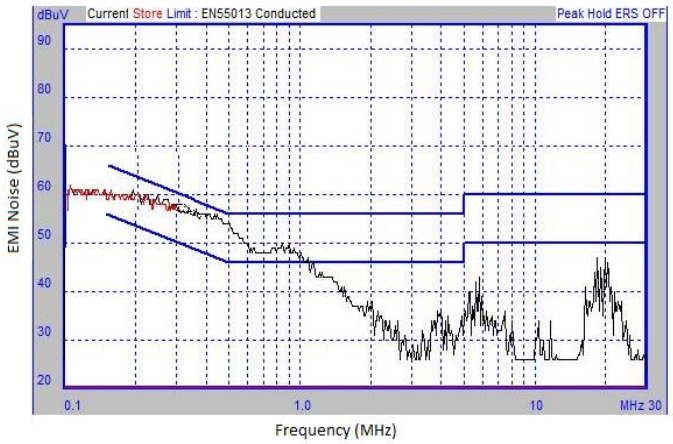


Figure 118: Conducted EMI noise of linear power supply

The results indicate that the conducted EMI noise of linear power supply is below the limit set by international EMI standard (CISPR-22) as shown in Figure 118.

5.8 Evaluate the audio Performance of audio amplifier

5.8.1 Objective Test

The performance of SMPS is analyzed on the basis of objective tests such as THD+N Vs Freq, THD+N Vs Level and FFT. The audio precision equipment is used in the lab to measure the objective tests of an audio amplifier by providing power with two different power supplies.

5.8.1.1 First prototype of SMPS from other Supplier

- Existing LPS (Linear Power Supply) used for an audio amplifier by collaborating company.
- First prototype of SMPS (Switch-mode Power Supply) from other supplier (Connexelectronix).

THD+N Vs Frequency

Plot the THD+N versus frequency of an audio amplifier. Sweep the frequency from 20Hz to 20kHz.

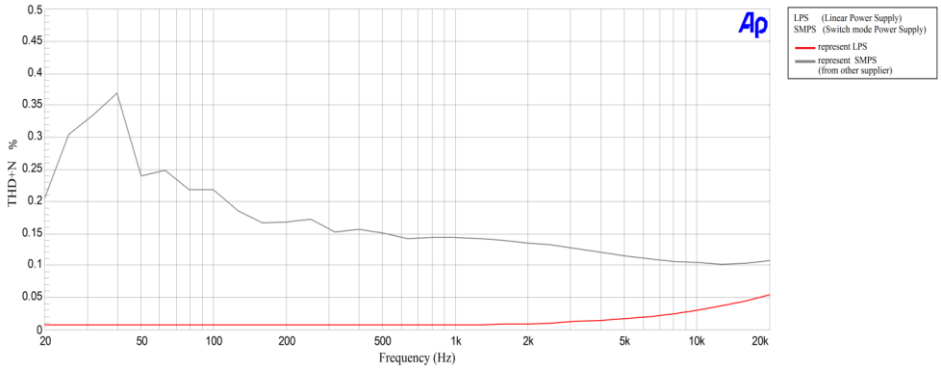


Figure 119: Variation of total harmonic distortion plus noise with frequency

In the above plots, the THD+N for an audio amplifier are measured when it is powered with two different power supplies.

- The red line represents THD+N of an audio amplifier for LPS(Linear Power Supply)
- The gray line represents THD+N of an audio amplifier for SMPS (Switch-mode Power Supply)

Summary

I conclude from the experimental results that THD+N are higher in an audio amplifier when running with the SMPS as compared to LPS.

THD+N Vs Level

Plot THD+N versus level at 20Hz, 1kHz and 20kHz of an audio amplifier.

THD+N versus level at 20Hz

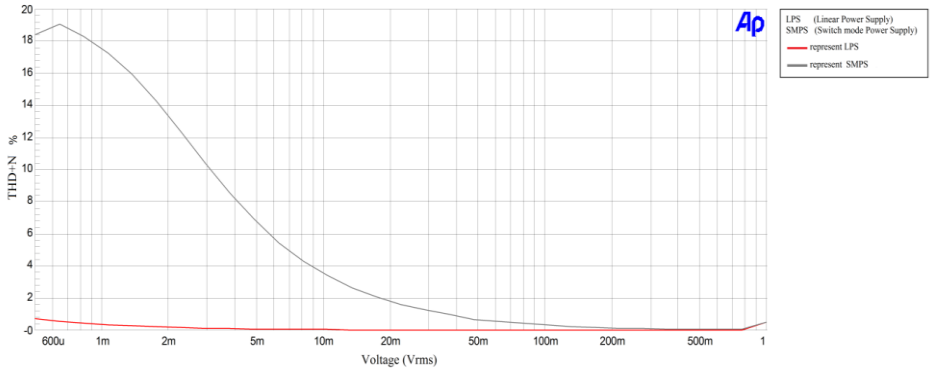


Figure 120: Variation of total harmonic distortion plus noise with level

THD+N versus level at 1 kHz

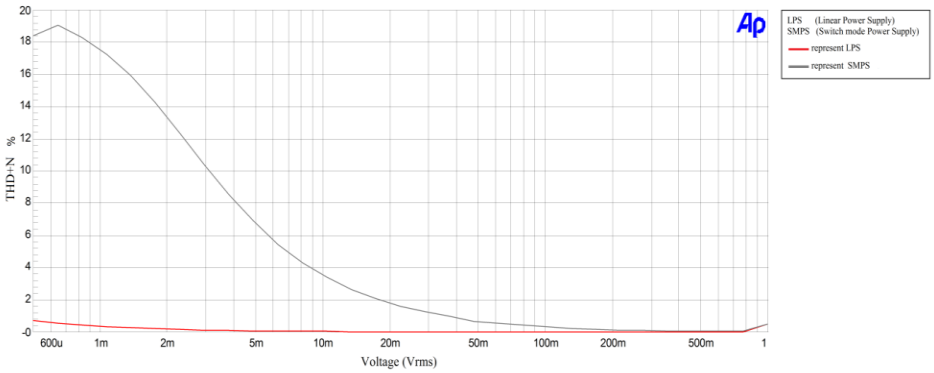


Figure 121: Variation of total harmonic distortion plus noise with level

THD+N versus level at 20 kHz

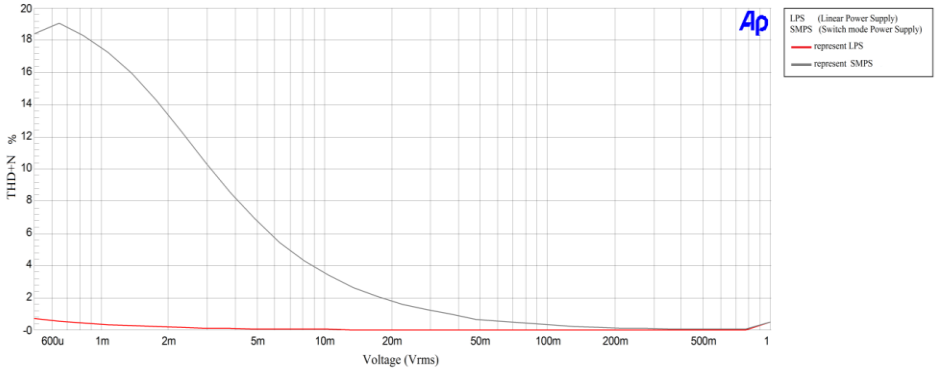


Figure 122: Variation of total harmonic distortion plus noise with level

In the above plots, the THD+N for an audio amplifier are measured using two different power supplies.

- The red line represents THD+N of an audio amplifier for LPS(Linear Power Supply)
- The gray line represents THD+N of an audio amplifier for SMPS (Switch-mode Power Supply)

Summary

From the above plots, it is concluded that the THD+N are higher in an audio amplifier when running with the SMPS as compared to LPS.

FFT

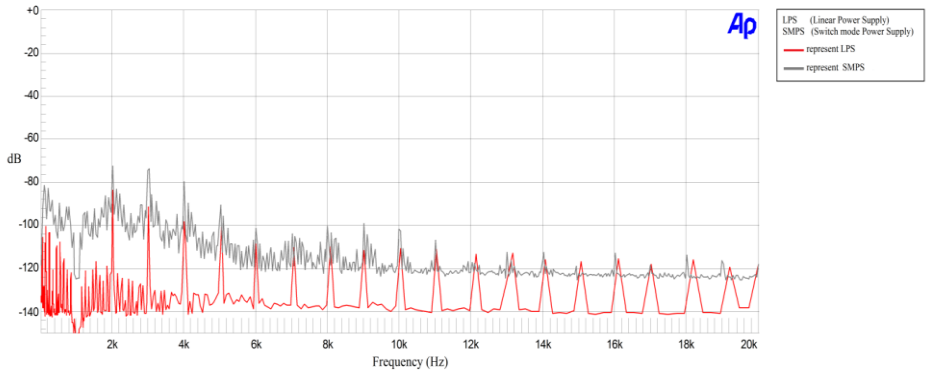


Figure 123: Level Vs Frequency

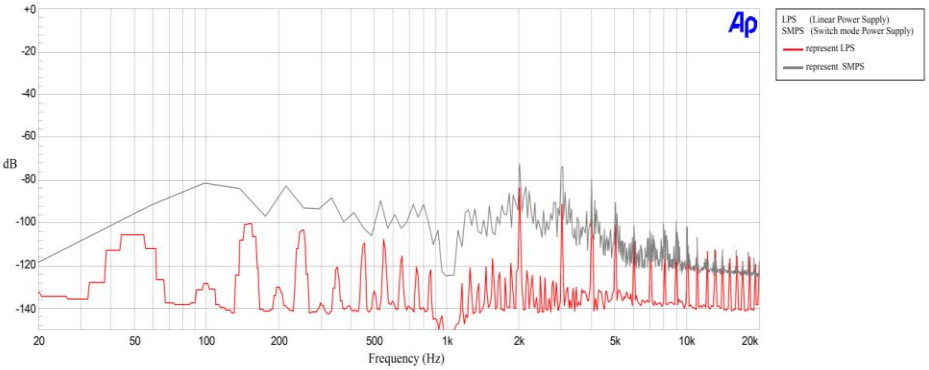


Figure 124: Level Vs Frequency

In the above plots, the FFT for an audio amplifier are measured by providing powered with two different power supplies.

- The red line represents FFT of an audio amplifier for LPS(Linear Power Supply)
- The gray line represents FFT of an audio amplifier for SMPS (Switch-mode Power Supply)

Summary

From the above plots, it is concluded that noise level are higher in an audio amplifier when running with the SMPS as compared to LPS.

5.8.1.2 Second prototype of SMPS from other Supplier

- Existing LPS (Linear Power Supply) used for an audio amplifier by collaborating company.
- Second prototype of SMPS (Switch-mode Power Supply) from other supplier (A and T labs).

THD+N Vs Frequency

Plot the THD+N versus frequency of an audio amplifier. Sweep the frequency from 20Hz to 20kHz.

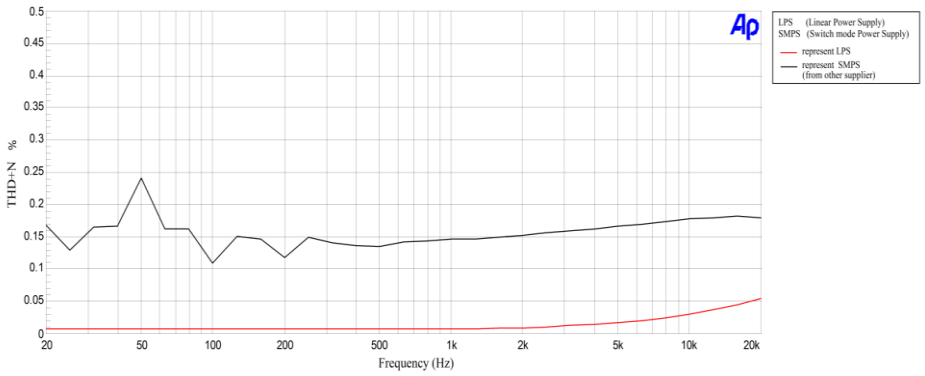


Figure 125: Variation of total harmonic distortion plus noise with frequency

In the above plots, the THD+N for an audio amplifier are measured with two different power supplies.

- The red line represents THD+N of an audio amplifier for LPS(Linear Power Supply)
- The black line represents THD+N of an audio amplifier for SMPS (Switch-mode Power Supply)

Summary

From the above plots, it is concluded that the THD+N are higher in an audio amplifier when running with the SMPS as compared to LPS.

THD+N Vs Level

Plot THD+N versus level at 20Hz, 1kHz and 20kHz of an audio amplifier.

THD+N versus level at 20Hz

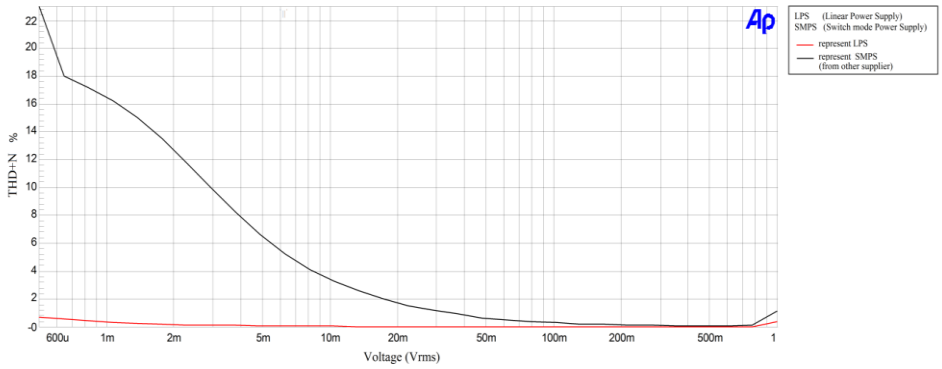


Figure 126: Variation of total harmonic distortion plus noise with level

THD+N versus level at 1 kHz

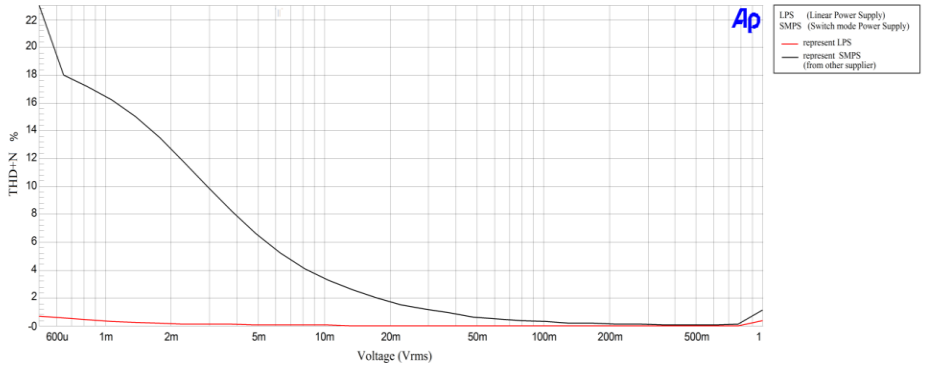


Figure 127: Variation of total harmonic distortion plus noise with level

THD+N versus level at 20 kHz

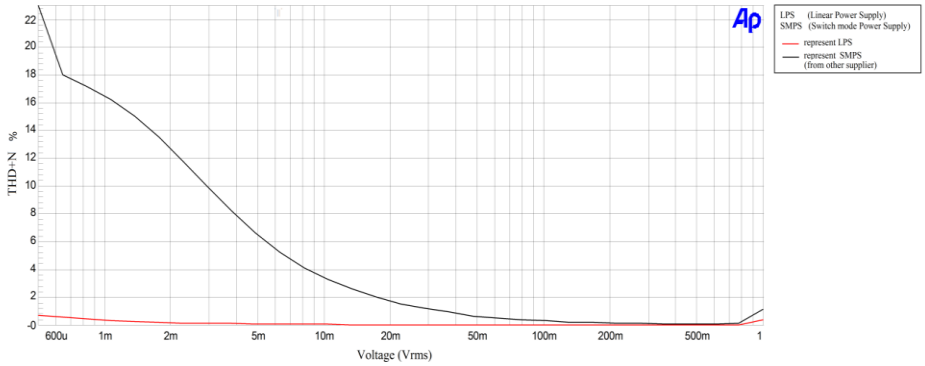


Figure 128: Variation of total harmonic distortion plus noise with level

In the above plots, the THD+N for an audio amplifier are measured with two different power supplies.

- The red line represents THD+N of an audio amplifier for LPS(Linear Power Supply)
- The black line represents THD+N of an audio amplifier for SMPS (Switch-mode Power Supply)

Summary

From the above plots, it is concluded that the THD+N are higher in an audio amplifier when running with the SMPS as compared to LPS.

FFT

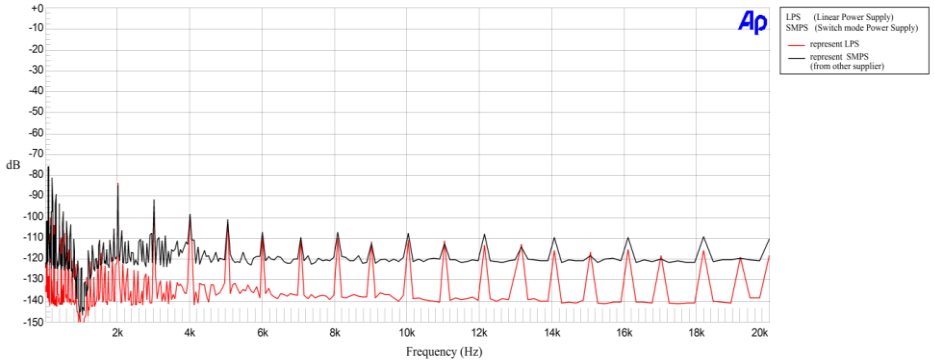


Figure 129: Level Vs Frequency

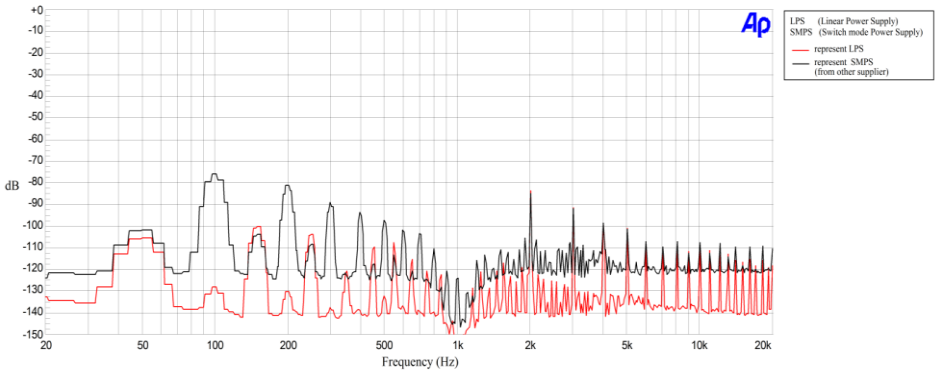


Figure 130: Level Vs Frequency

In the above plots, the THD+N for an audio amplifier are measured with two different power supplies.

- The red line represents FFT of an audio amplifier for LPS(Linear Power Supply)

- The black line represents FFT of an audio amplifier for SMPS (Switch-mode Power Supply)

Summary

From the above plots, it is concluded that noise level are higher in an audio amplifier when running with the SMPS as compared to LPS.

5.8.1.3 Proposed Prototypes of SMPS

- Existing LPS (Linear Power Supply) used for an audio amplifier by collaborating company (Naim audio).
- First prototype of SMPS (Hard-switching Converter)
- Second prototype of SMPS (ZVS-switching Converter)
- Third prototype of SMPS (Balanced Converter)

THD+N Vs Frequency

Plot the THD+N versus frequency of an audio amplifier. Sweep the frequency from 20Hz to 20kHz.

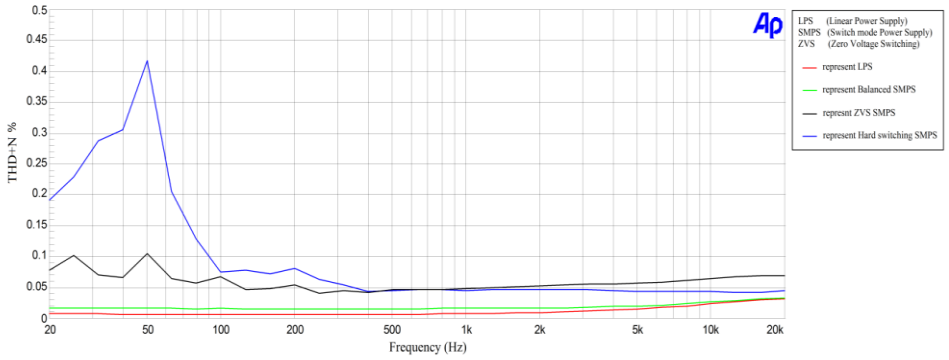


Figure 131: Variation of total harmonic distortion plus noise with frequency

In the above plots, the THD+N for an audio amplifier are measured with four different power supplies.

- The red line represents THD+N of an audio amplifier for LPS(Linear Power Supply)
- The blue line represents THD+N of an audio amplifier for hard switching SMPS.
- The black line represents THD+N of an audio amplifier for ZVS-SMPS.

- The green line represents THD+N of an audio amplifier for Balanced SMPS.

Summary

From the above plots, it is concluded that the THD+N of an audio amplifier when running with the balanced converter are comparable to THD+N with LPS. However, the THD+N are higher in an audio amplifier when running with the hard switching and ZVS SMPS as compared to LPS.

THD+N Vs Level

Plot THD+N versus level at 20Hz, 1kHz and 20kHz of an audio amplifier.

THD+N versus level at 20Hz

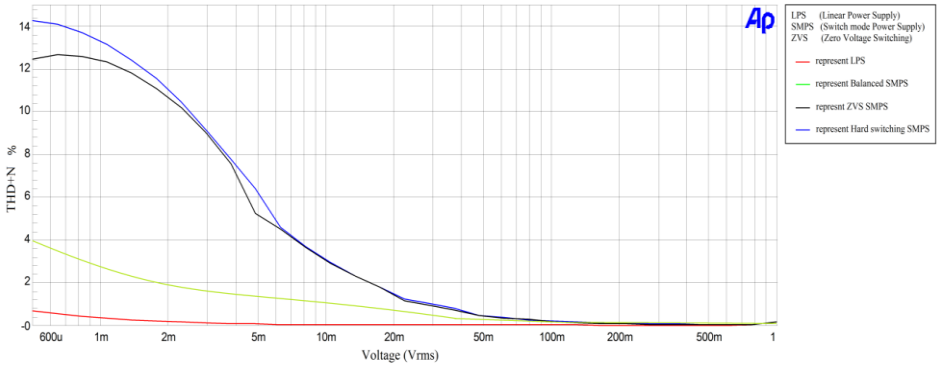


Figure 132: Variation of total harmonic distortion plus noise with level

THD+N versus level at 1 kHz

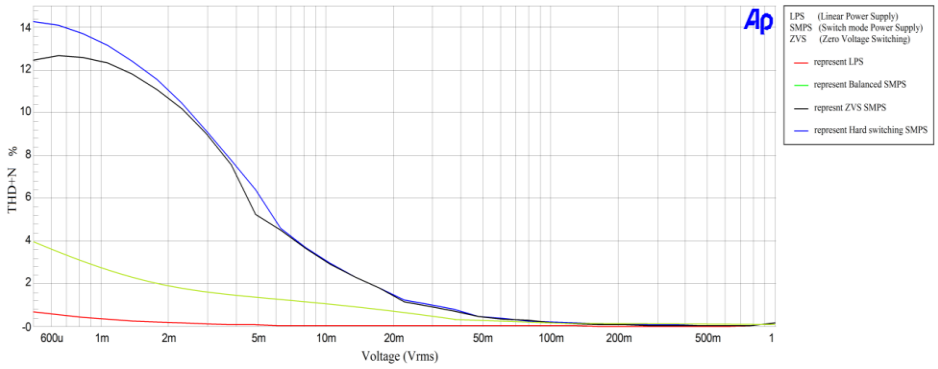


Figure 133: Variation of total harmonic distortion plus noise with level

THD+N versus level at 20 kHz

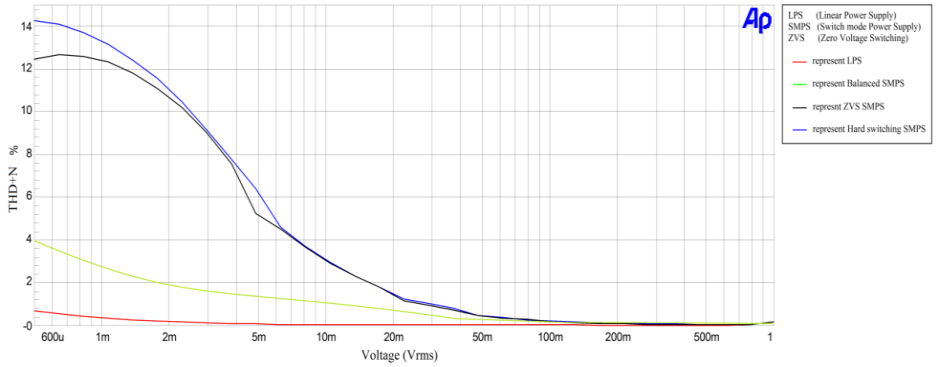


Figure 134: Variation of total harmonic distortion plus noise with level

In the above plots, the THD+N for an audio amplifier are measured with four different power supplies.

- The red line represents THD+N of an audio amplifier for LPS(Linear Power Supply)
- The blue line represents THD+N of an audio amplifier for hard switching SMPS.
- The black line represents THD+N of an audio amplifier for ZVS-SMPS.
- The green line represents THD+N of an audio amplifier for Balanced SMPS.

Summary

From the above plots, it is concluded that the THD+N of an audio amplifier when running with the balanced converter are comparable to THD+N with LPS. However, the THD+N are higher in an audio amplifier when running with the hard switching and ZVS SMPS as compared to LPS.

FFT

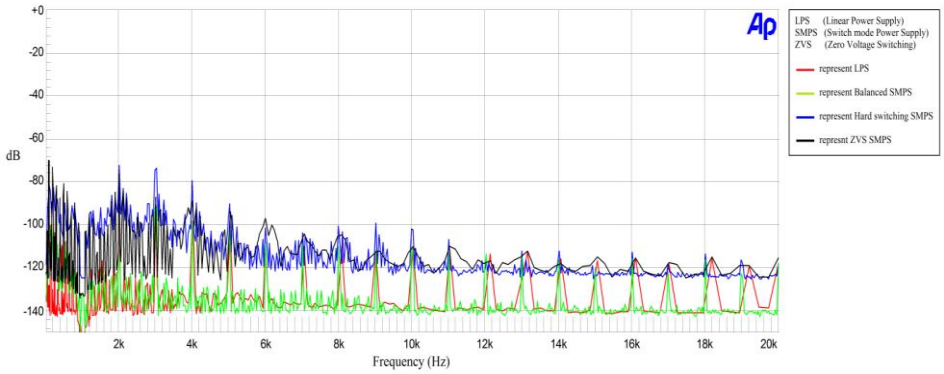


Figure 135: Level Vs Frequency

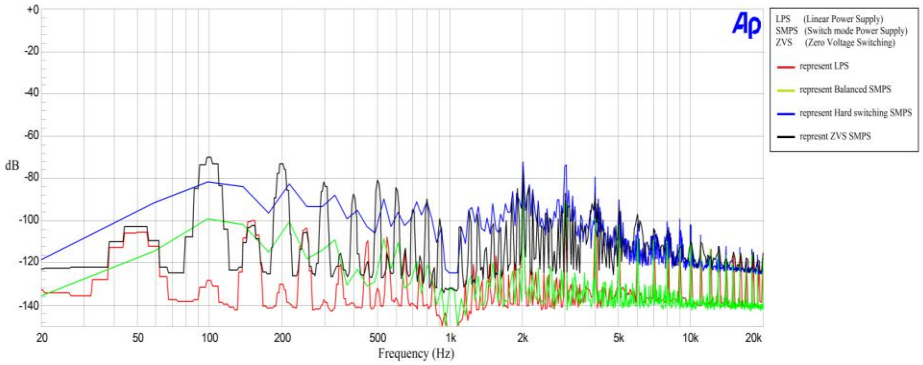


Figure 136: Level Vs Frequency

In the above plots, the THD+N for an audio amplifier are measured with two different power supplies.

- The red line represents THD+N of an audio amplifier for LPS(Linear Power Supply)
- The blue line represents THD+N of an audio amplifier for hard switching SMPS.
- The black line represents THD+N of an audio amplifier for ZVS-SMPS.
- The green line represents THD+N of an audio amplifier for Balanced SMPS.

Summary

I conclude from the results that the THD+N of an audio amplifier when running with the balanced converter are comparable to THD+N with LPS. However, the THD+N are

higher in an audio amplifier when running with the hard switching and ZVS SMPS as compared to LPS.

5.8.2 Subjective test

The performance of proposed novel low noise SMPS is evaluated on the basis of subjective tests performed on the power amplifier. The subjective tests involved the blind audio listening tests. In a blind listening test, the listener was unaware of the power supply used to power the audio amplifier. Therefore, the psychological influence was not affected the judgment of listener related to brand product. On the basis of subjective test, the decision is made that balanced SMPS solution is comparable to linear solution.

5.9 Summary

In this chapter, a proposed balanced technique for flyback, boost and full-bridge converter have been evaluated. The proposed schemes effectively reduce the conducted EMI noise in balanced converter as compared to conventional method. In addition, the novel design of low noise switch mode power supply satisfies the EMI standard set by International bodies (CISPR-22).

6 CHAPTER 6 CONCLUSIONS

6.1 Introduction

The development of a novel low noise switch power supply for audio amplifiers is quite fascinating but a challenging task. Recently, a lot of efforts have been already dedicated in this direction to overcome the underlying problems of electromagnetic interference in such devices but still there is need to find and develop an alternative solution that reduces the noise in SMPS to a substantial level to meet EMI standard of International bodies. In this thesis, I proposed different solutions based on balancing mechanism with experimental implementation to mitigate the noise of SMPS in different topologies. I thoroughly explore and understand the different mechanisms that contribute to generation of CM noise. In particularly, I investigate PFC boost converter, fly-back converter and full-bridge converters, as a basic topologies, to verify proposed idea and finally show that the proposed technique reduces the noise significantly in SMPS to meet EMI standard of International bodies (CISPR-22). The development and characterization of a novel SMPS for audio amplifiers is successfully completed with expected results in this thesis. The proposed scheme based on balancing technique is quite effective and easily implementable in SMPS for audio amplifiers. The substantial reduction of noise in SMPS naturally enters research to next phase, which is commercialization of the product for audio applications. These findings are not important only for technological point of view but also it give deep insights to scientific community working in this research field.

In this chapter, I summarized the proposed methodology of balancing technique and their overall effect on the performance of SMPS. The performance of proposed novel low noise SMPS is also evaluated on the basis of subjective and objective tests performed on the power amplifier. Moreover, the suggestions for future work are also presented.

6.2 Summary

6.2.1 Proposed Balance Technique for PFC boost converter

A novel balancing technique is proposed to reduce overall CM noise of PFC boost converter. In this scheme, I introduced the anti-phase noise source by adding a coupled

inductor with compensating winding and compensating capacitor to generate a complimentary voltage. The voltage produced due to additional winding and capacitor is 180° out of phase as compared to the original noise voltage. Therefore, the overall noise is cancelled out with the help of novel technique. Furthermore, experimental measurements demonstrate that this technique mitigates the CM noise effectively through parasitic capacitance of MOSFET/Diode. It is also confirmed experimentally that the proposed method reduces the noise by nearly 14 dB for the case of a PFC boost converter when compared to the conventional technique.

6.2.2 Proposed Balance Technique for Flyback converter

A novel balancing technique is proposed to reduce the overall CM noise for fly-back converter. This technique mitigates the CM noise not only through parasitic capacitance of MOSFET/Diode but also through inter-winding capacitance by balancing the transformer winding. It is confirmed experimentally that the proposed method works efficiently to overcome the problem of EMI noise in isolated converters and reduces the noise by nearly 10 dB for the case of a flyback converter when compared to conventional technique. I intend to further refine the technique and investigate its application in a range of converter topologies.

6.2.3 Proposed Balance Technique for Full-bridge converter

A novel balancing technique for full-bridge converter is proposed to mitigate CM noise by using balanced transformer construction method. The proposed technique is employed not only on conventional transformer method but also applied to interleaved transformer construction. This technique mitigates CM noise by producing anti-noise voltage which is out of phase as compared to original noise in a converter. This technique mitigates CM noise through both propagation paths such as parasitic capacitance of MOSFETs/Diodes and transformer inter-winding capacitance. The experimental results predicts that proposed scheme is universal and can be applied to any transformer construction effectively to achieve the better performance of EMI noise and reduces the noise by nearly 12dB.

Furthermore, the balancing techniques for full-bridge converter are applied to different transformer construction such as wire-wound and planar transformer. Moreover, the proposed scheme for wire wound and planar transformer have been investigated for full-bridge converter. Also, different types of transformer such as conventional and interleaved transformer construction have been considered for proposed balanced technique. It effectively reduces conducted EMI noise and output noise in balanced transformer construction for wire wound and planar transformer. In addition, the novel design of low noise switch mode power supply satisfies the EMI standard set by International bodies (CISPR-22).

6.2.4 Novel ZVS full-bridge Converter

A novel ZVS full-bridge converter is proposed to improve the range of zero voltage switching over the entire range of load. The experimental results prove that ZVS can be achieved for both legs switching devices (leading and lagging MOSFET). It is also evident from proposed circuit that it is a simple and cost effective solution. It also improves the overall efficiency of converter over entire range of load.

The performance of proposed novel low noise SMPS is evaluated on the basis of subjective and objective tests performed on the power amplifier. The subjective tests involved the blind audio listening tests. In a blind listening test, the listener was unaware of the power supply used to power the audio amplifier. Therefore, the psychological influence was not affected the judgment of listener related to brand product. Also the performance of SMPS is analyzed on the basis of objective test such as THD+N, frequency response and audio dynamic range. The audio precision equipment is used to measure the above tests and compare these results with LPS. On the basis of subjective and objective tests, the decision has been made that SMPS solution is as good as or better than the linear solution.

6.3 Future Work

Apart from successful development of SMPS for audio amplifiers in this thesis, my proposed technique is generic in nature and provide rich possibilities to further implement this technique to other SMPS topologies. Some of possible future research directions to extend this work are given below

6.3.1 Balancing technique for other hard switching topologies

I have proposed balancing technique for PFC boost, fly-back and full-bridge converter. However, the other topologies such as buck, forward, half-bridge and push-pull converter will also need to be considered due to universality of balancing technique in future. Therefore, it helps to mitigate the noise of these converters and enhance the performance of power supply.

6.3.2 Balancing technique for soft-switching topologies

The balancing technique for different types of resonant converter can be useful for mitigation of EMI noise from these converters. These resonant converter types such as series resonant converter (SRC), parallel resonant converter (PRC) and series parallel resonant converter (SPRC). Furthermore Zero voltage switching (ZVS), zero current switching (ZCS) and zero voltage zero current switching (ZVZCS) topologies should also be considered for balancing technique.

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8 APPENDICES

Appendix A. List of Publications

Appendix B. Circuit Schematic for SMPS

Appendix C. PCB Layout for SMPS

Appendix A

List of Publications

International Conferences

1. Nasir and Cobb, J., 2016. CM Noise Reduction of Isolated Converter by Balancing Technique. Power and Energy Conference, Illinois, U.S.A, 2016

2. Nasir and Cobb, J., 2016. Mitigation of Common mode Noise for PFC Boost Converter by Balancing Technique. The 8th IET International Conference on Power Electronics, Machines and Drives., Glasgow, Scotland, UK, 2016

3. Nasir and Cobb, J., 2016. A Novel ZVS Full-Bridge Converter. 16 IEEE International Conference on Environment and Electrical Engineering Florence, Italy, 2016

Poster Conferences

1) Nasir and Cobb, J., 2015. Novel low noise Switch-mode power supply design, 8th Annual PGR Poster Conference January 2015, Bournemouth University.

2) Nasir and Cobb, J., 2014. CM noise mitigation by balancing technique for SMPS, 7th Annual PGR Poster Conference 12th May 2014, School of Design Engineering and Computing Bournemouth University.

3) Nasir and Cobb, J., 2013. Conducted EMI noise mitigation techniques for switch-mode power supply. 6th Annual PGR Poster Conference 23rd May 2013, School of Design Engineering and Computing Bournemouth University.

Appendix B

Circuit Schematic for SMPS

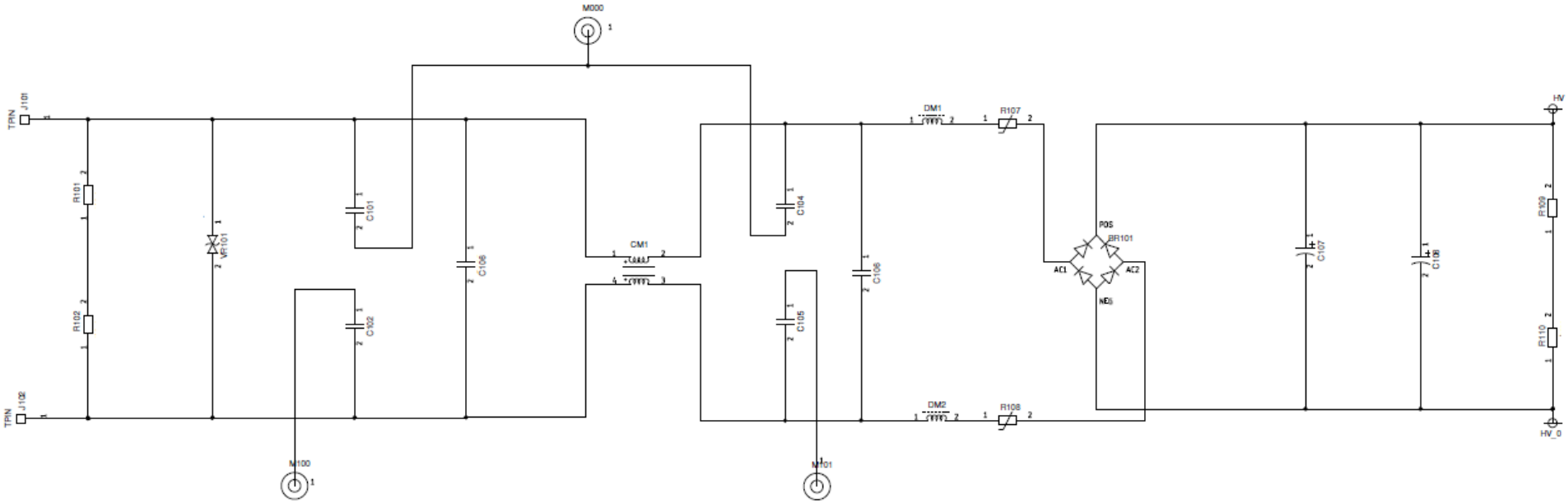

Figure 1 (a): Circuit Schematic for First prototype of SMPS

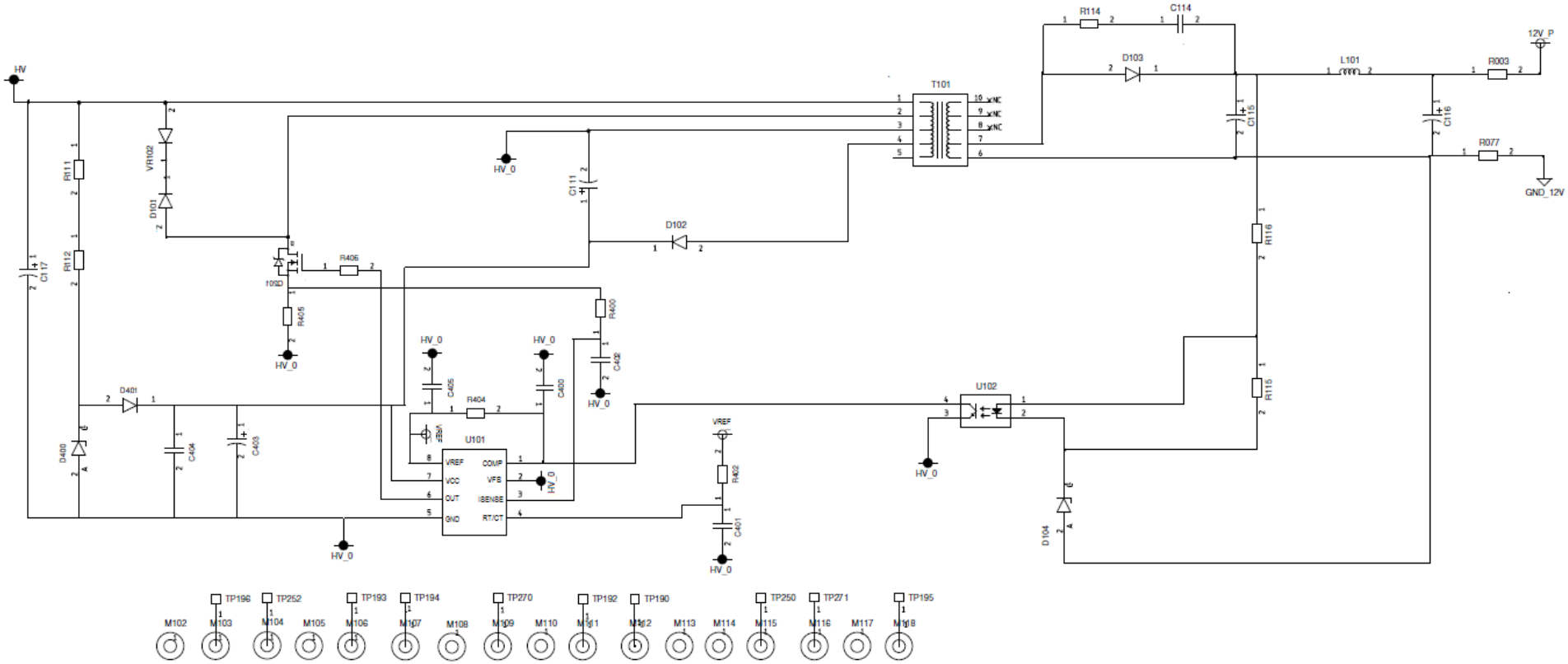

Figure 1 (b): Circuit Schematic for First prototype of SMPS

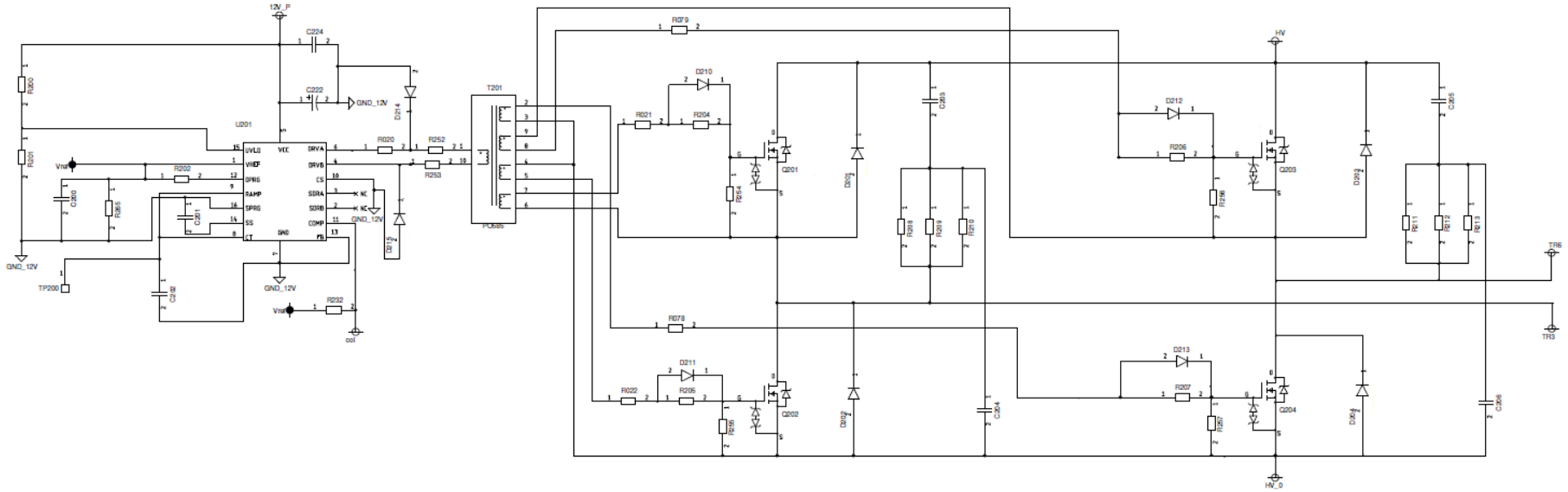

Figure 1 (c): Circuit Schematic for First prototype of SMPS

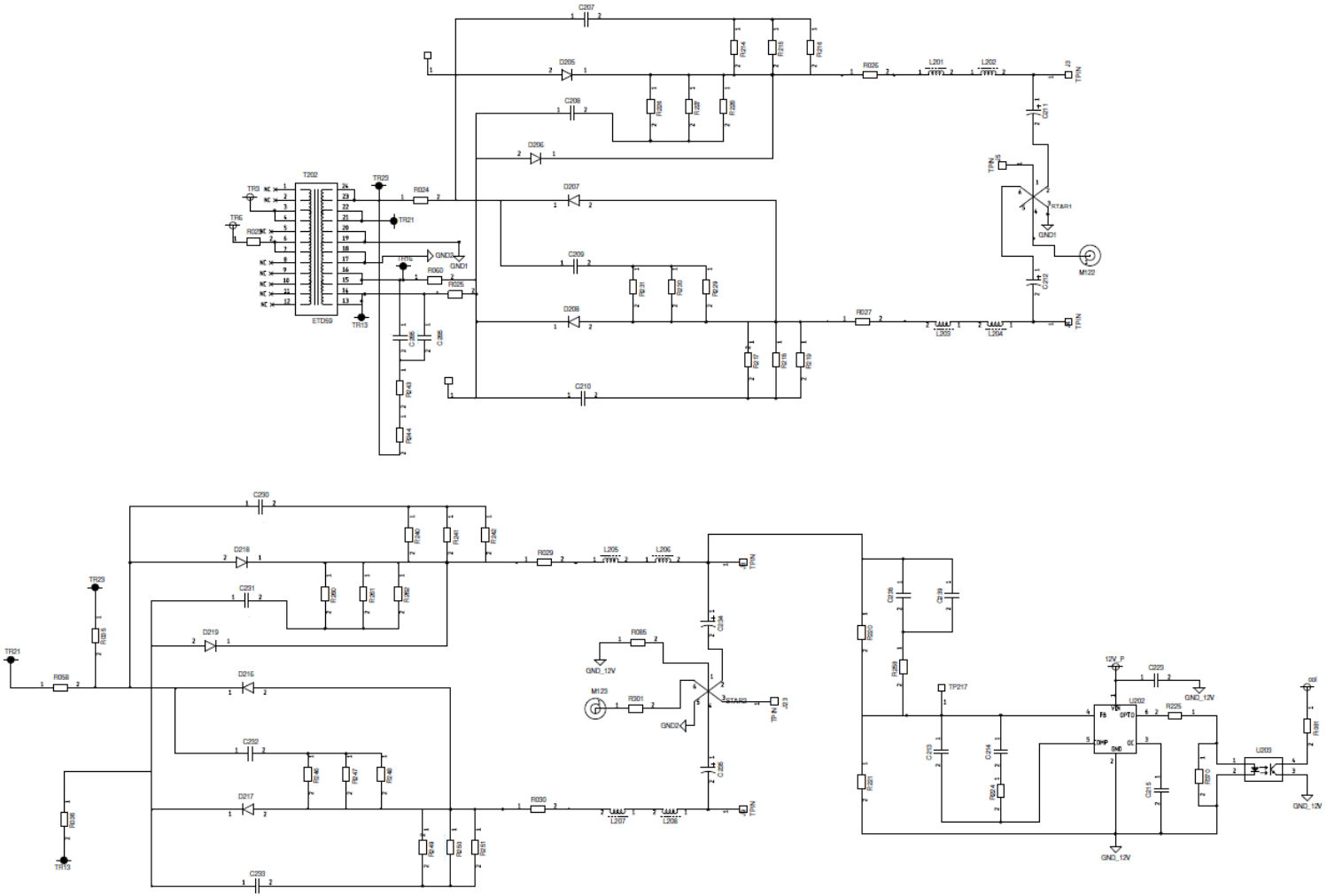

Figure 1 (d): Circuit Schematic for First prototype of SMPS

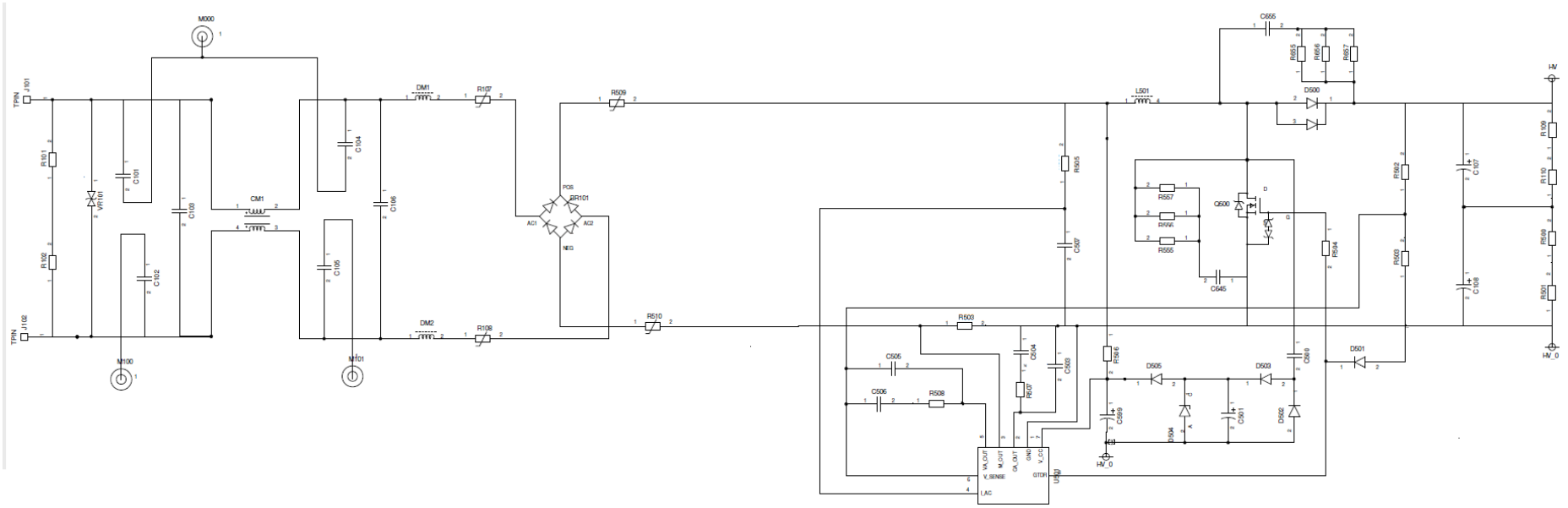

Figure 2(a): Circuit Schematic for Second prototype of SMPS

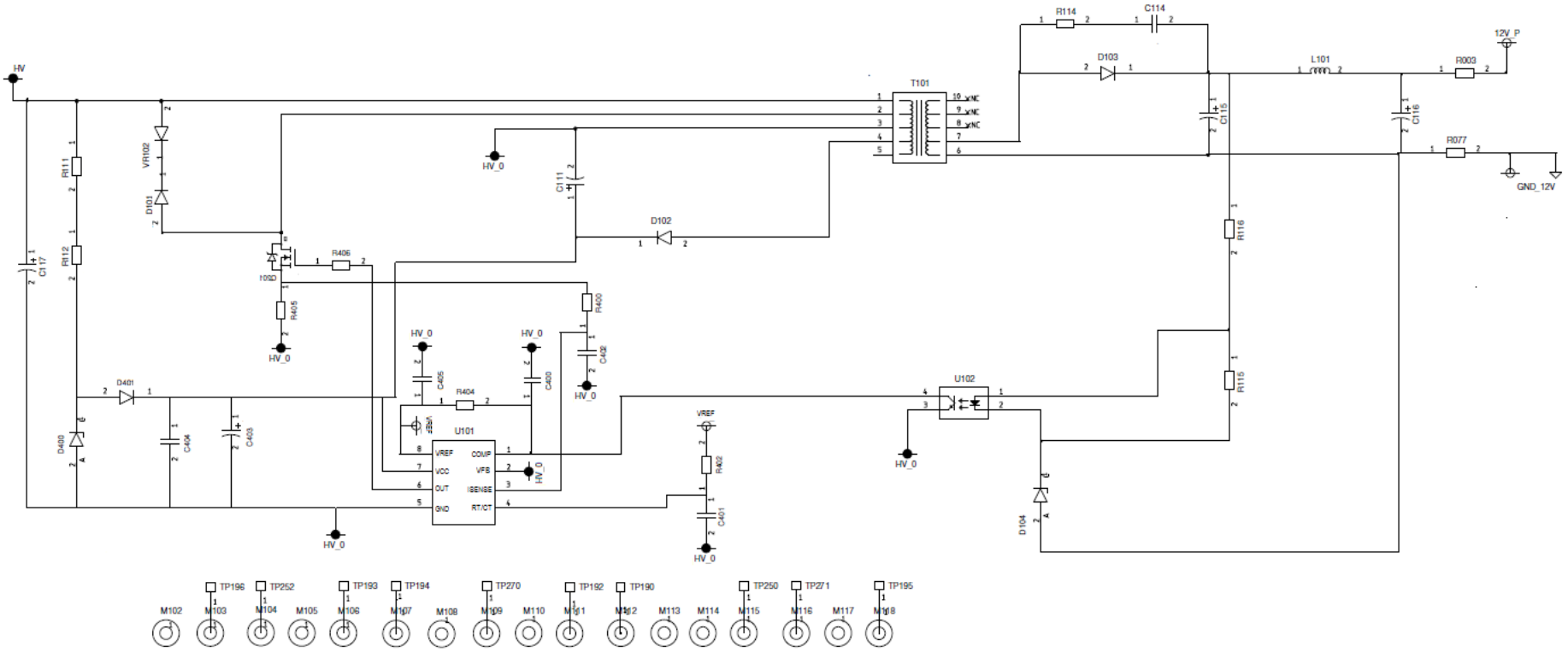

Figure 2(b): Circuit Schematic for Second prototype of SMPS

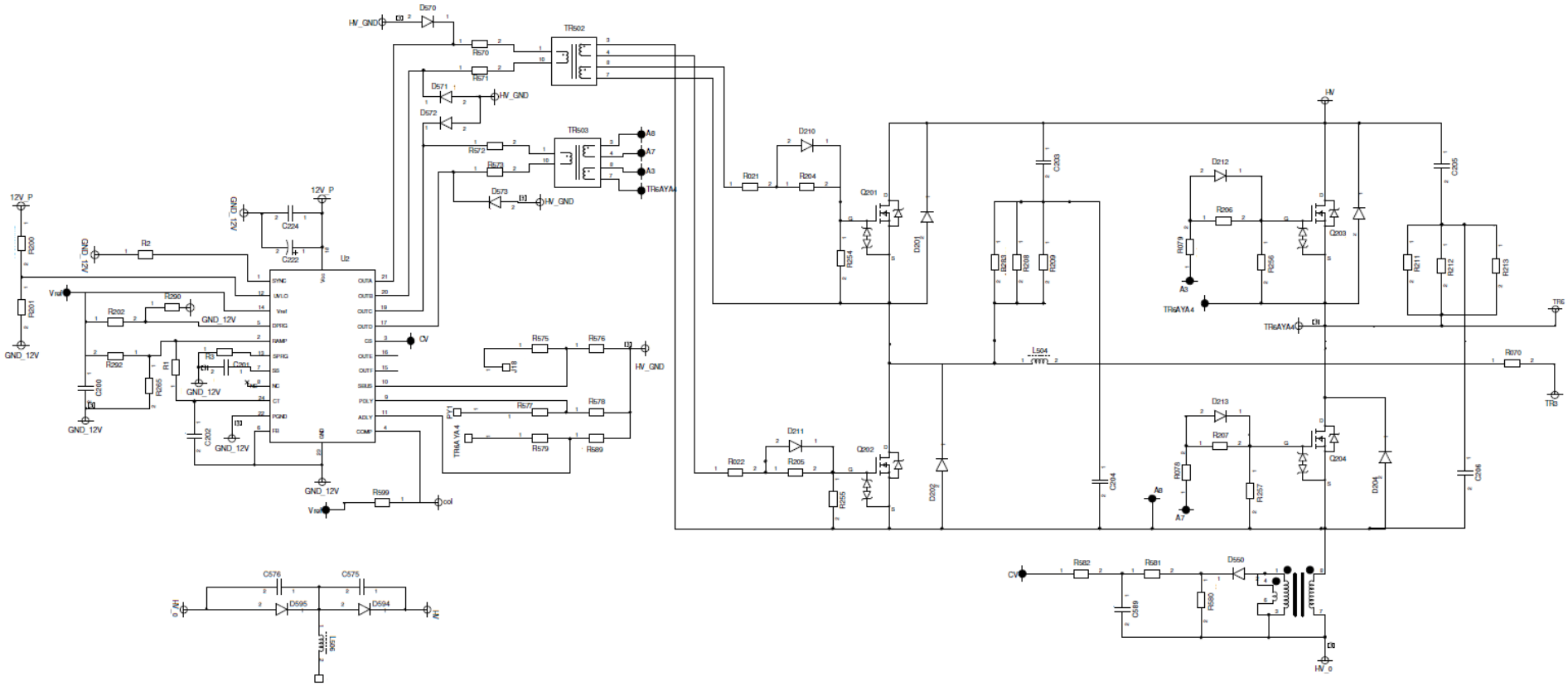

Figure 2(c): Circuit Schematic for Second prototype of SMPS

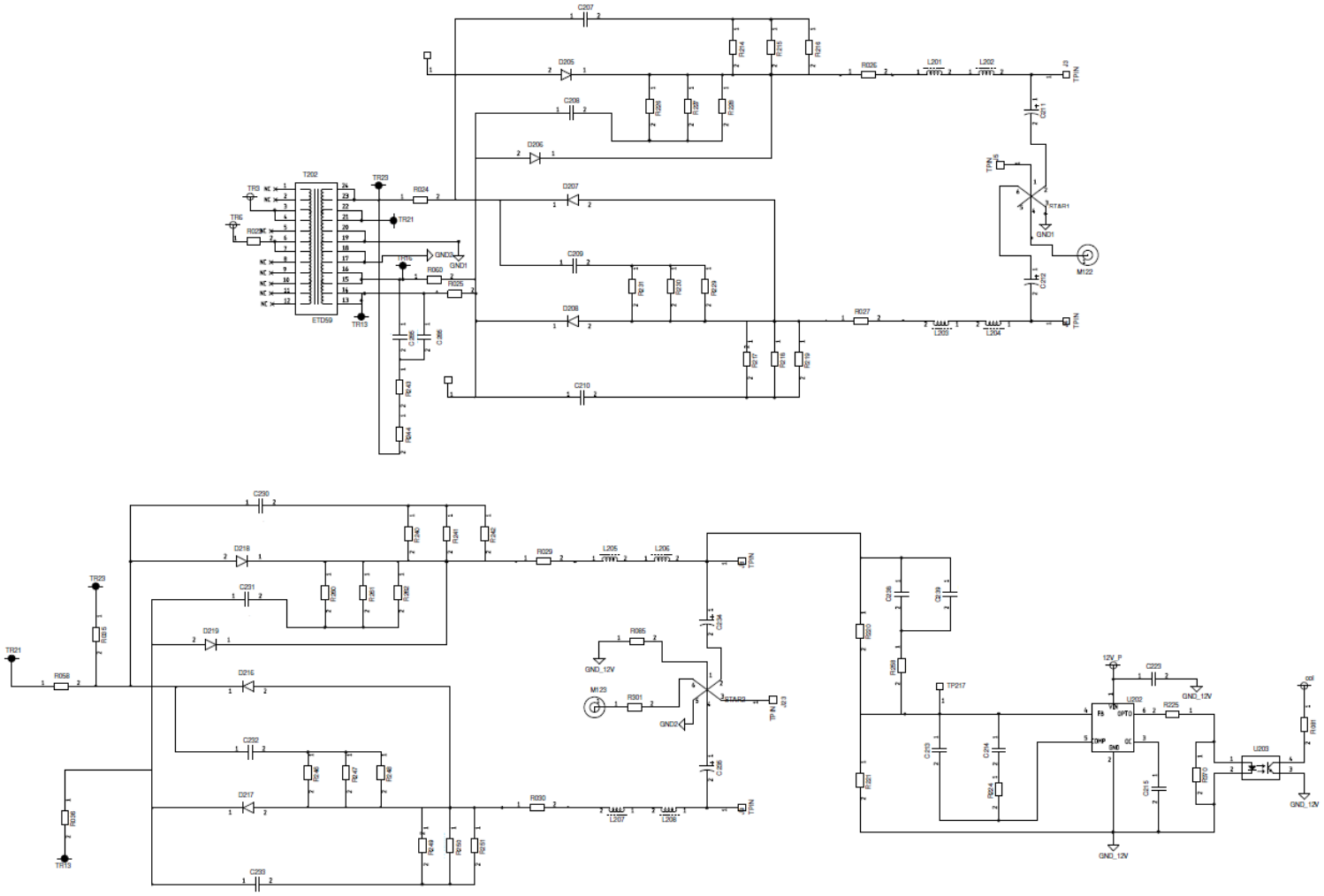

Figure 2(d): Circuit Schematic for Second prototype of SMPS

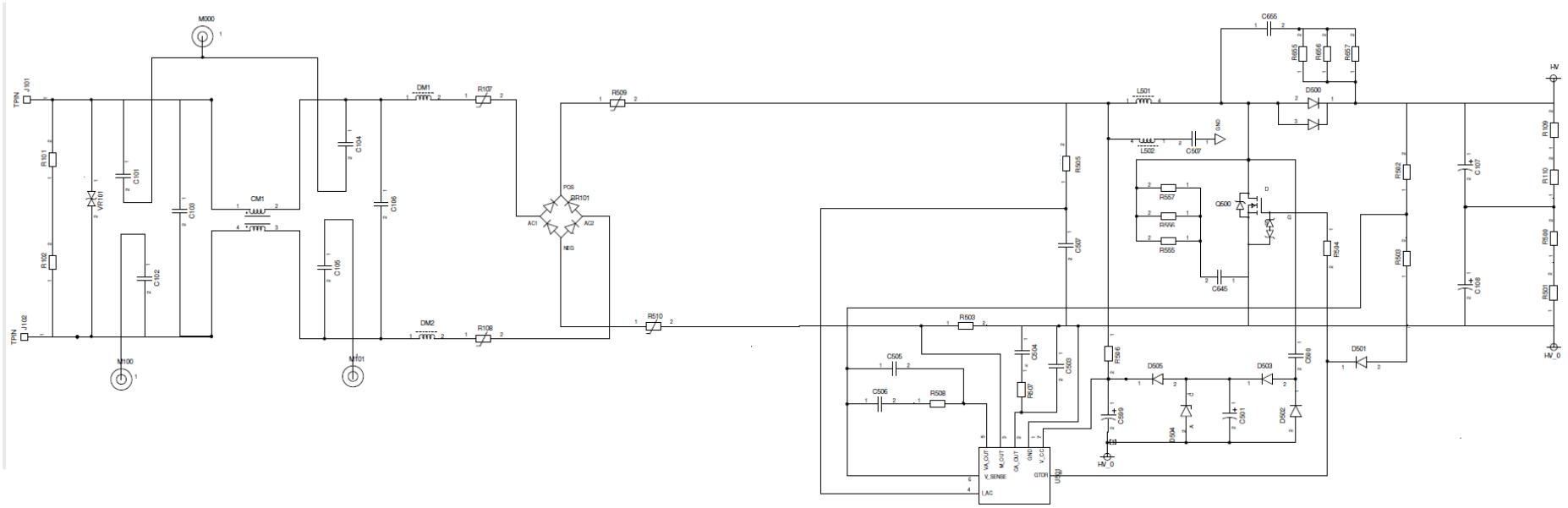

Figure 3(a): Circuit Schematic for Third prototype of SMPS

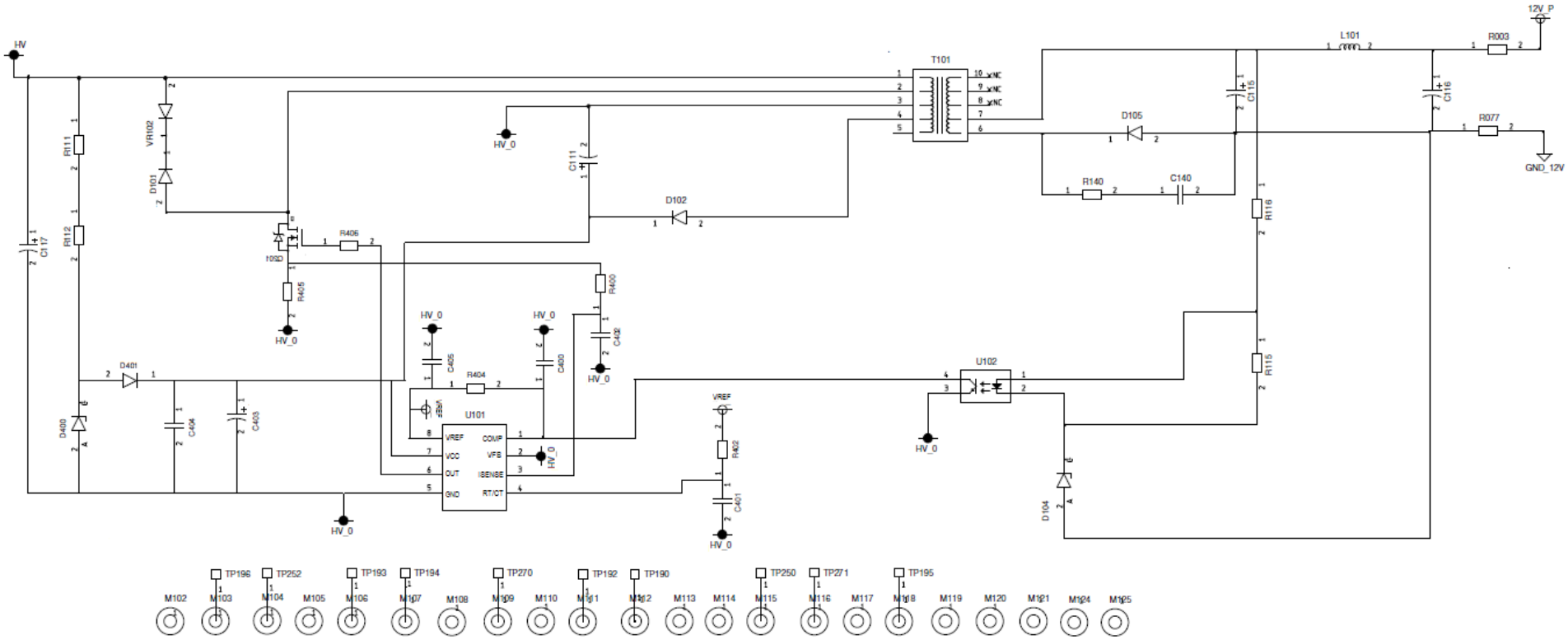

Figure 3(b): Circuit Schematic for Third prototype of SMPS

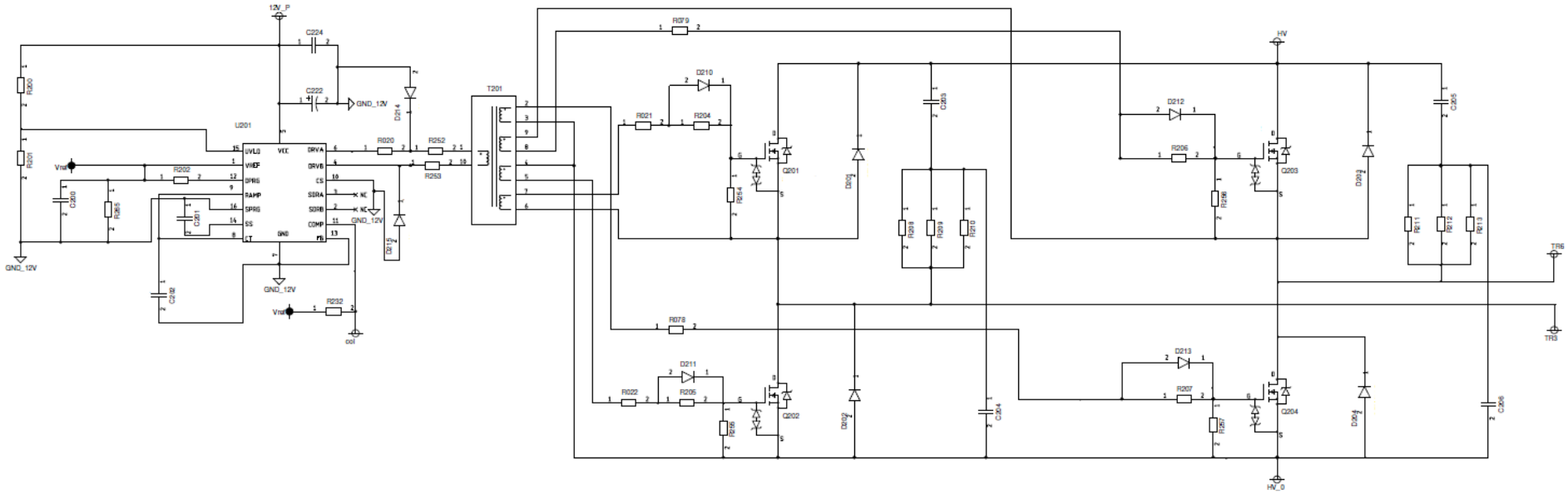

Figure 3(c): Circuit Schematic for Third prototype of SMPS

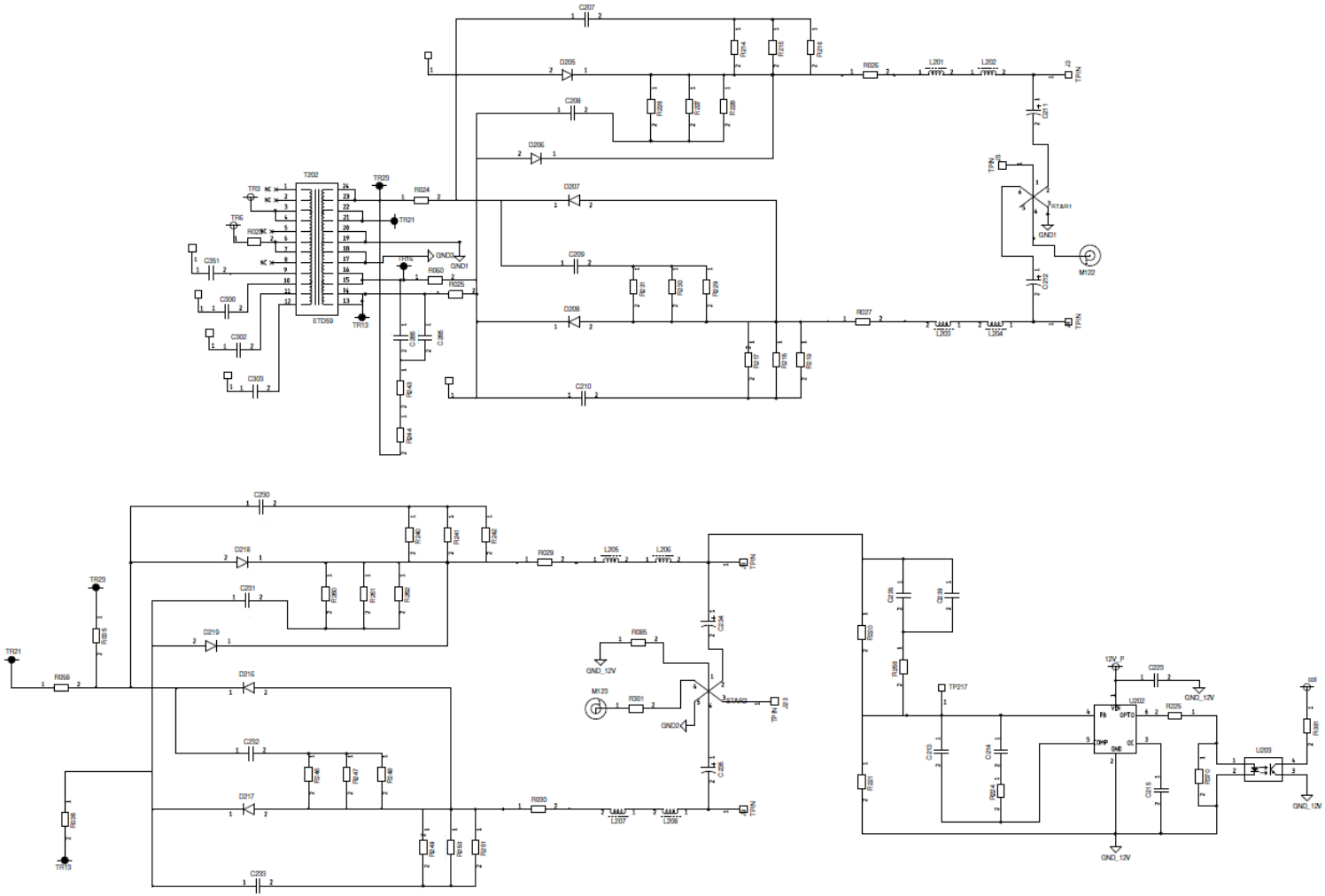

Figure 3(d): Circuit Schematic for Third prototype of SMPS

Appendix C

PCB Layout for SMPS

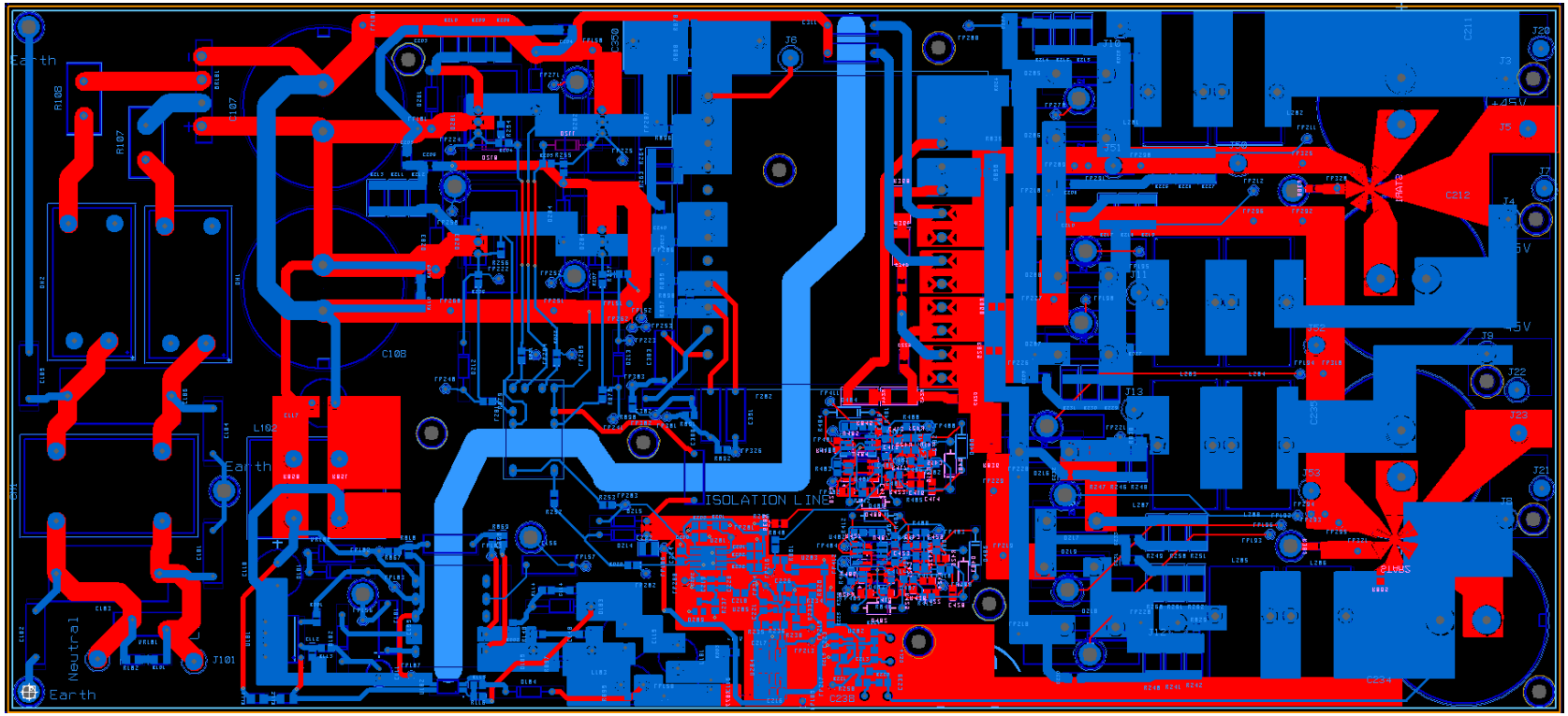

Figure 4: PCB Layout for First prototype of SMPS

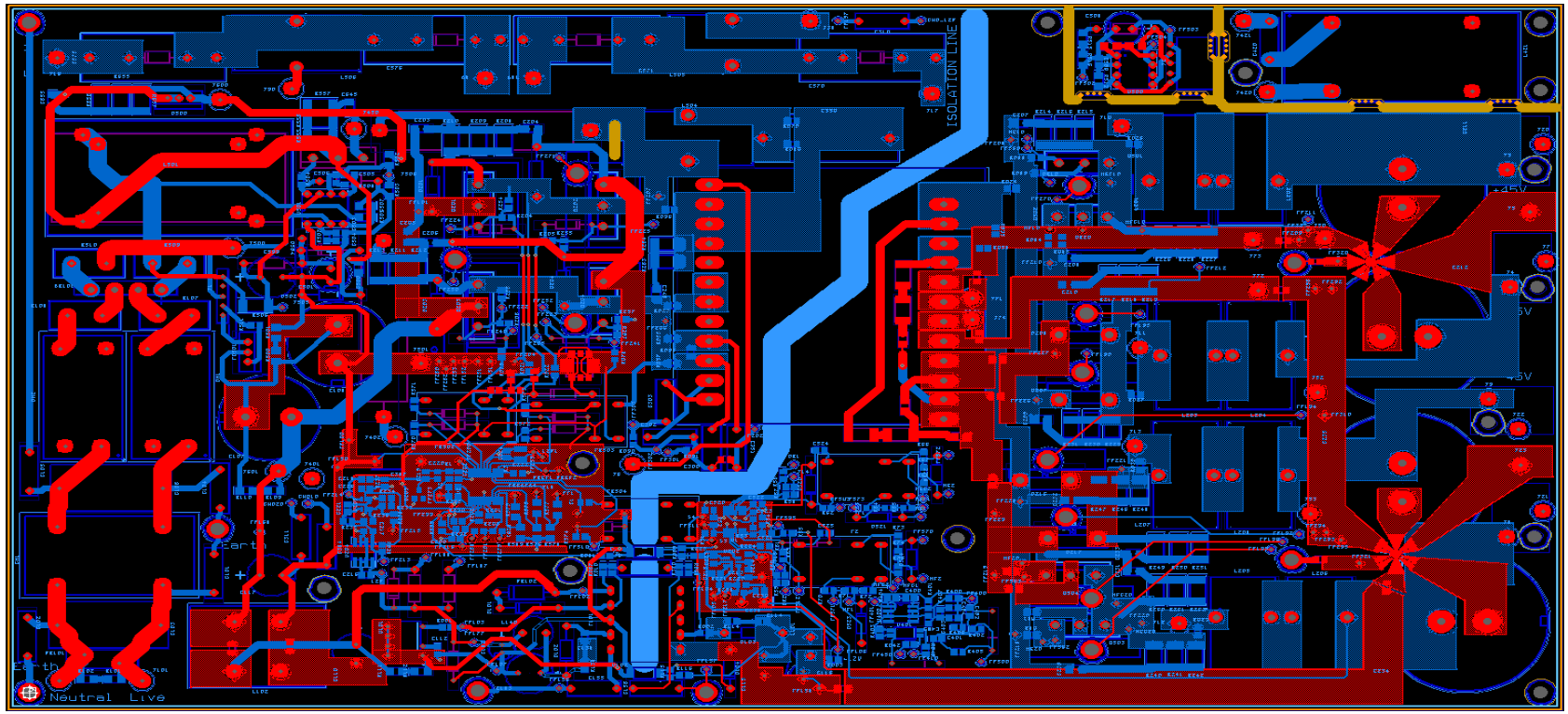

Figure 5: PCB Layout for Second prototype of SMPS

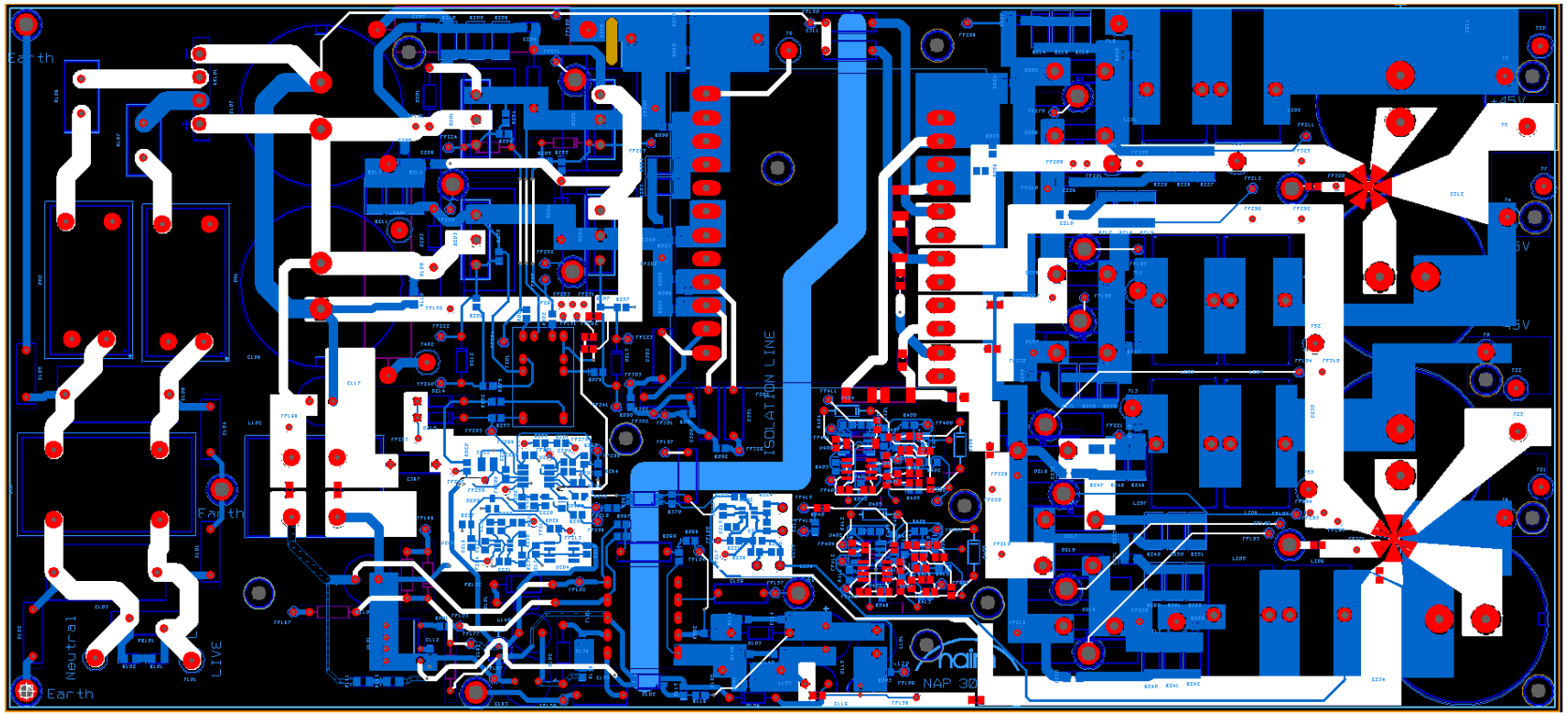

Figure 6: PCB Layout for Third prototype of SMPS

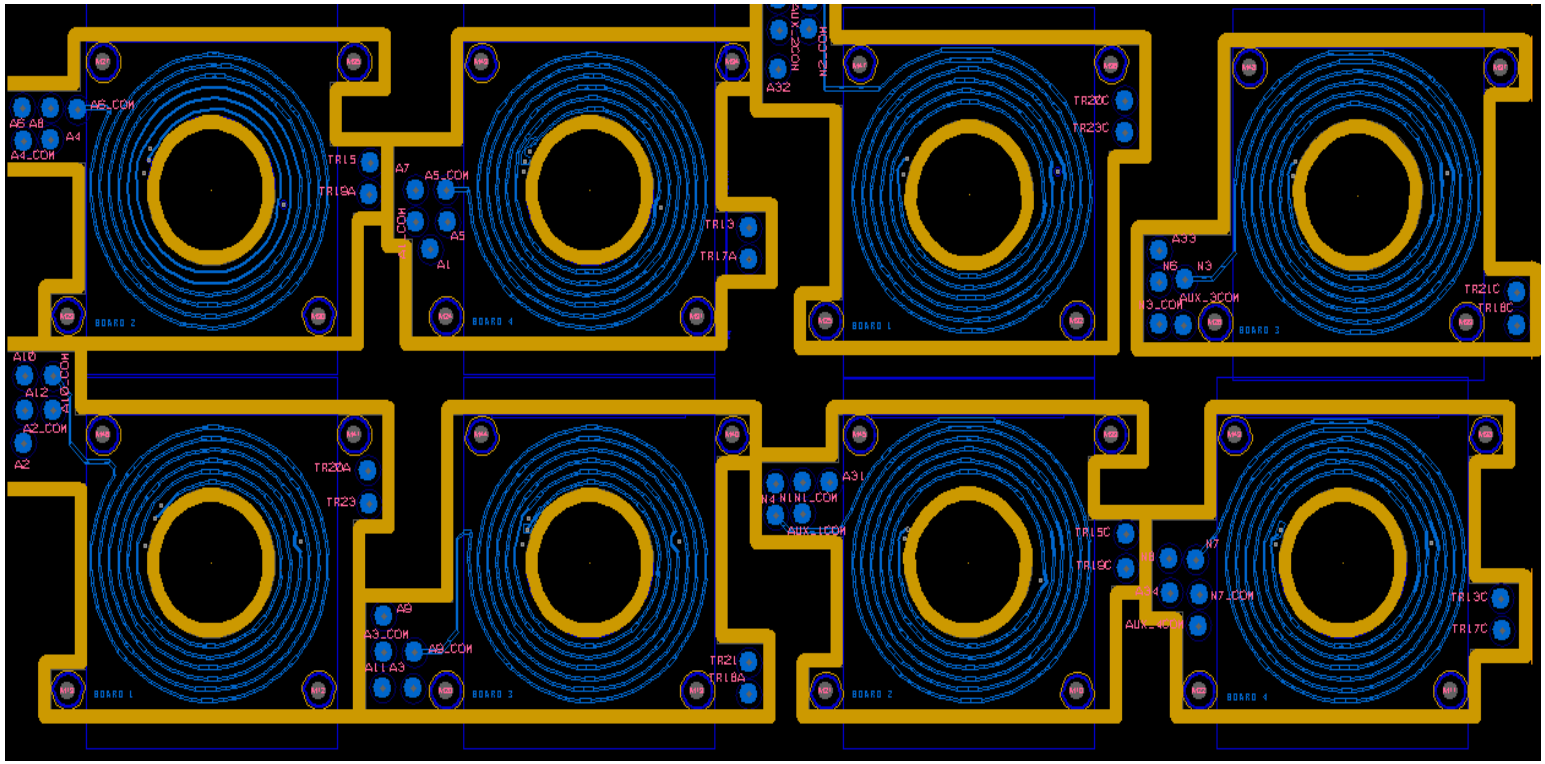

Figure 7: PCB Layout for Planar Transformer