Analysis of GaN HEMTs Switching Transients Using Compact Model

Soroush Faramehr and Petar Igić, *Senior Member, IEEE*

***Abstract*— This paper presents a methodology to model GaN power HEMT switching transients. Thus, a compact model to predict devices' pulse switching characteristics and current collapse reliability issue has been developed. Parasitic RC subcircuits and a standard double-pulse switching tester to model intrinsic parasitic effects and to analyze power dissipation of GaN power HEMT are proposed and presented. Switching transient including gate-lag and drain-lag is predicted for ideal (without trap) and nonideal (with trap) devices. The results are validated by and compared to 2-D finite-element technology computer-aided design simulations. The original aim of this exercise is to develop a fast (near-real-time) model which can predict dynamic behavior of single and multiple power GaN HEMTs used for the switching transients of GaN power devices at circuit level.**

***Index Terms*— Compact model, current collapse (CC), double-pulse switch, drain-lag, GaN HEMTs, gate-lag, switching transients, technology computer-aided design (TCAD).**

I. Introduction

INCREASING efficiency and power density are important requirements for power applications. Semiconductor devices with various material types are being developed for power electronics applications. The demand for reduction in size and increase in switching frequency leads to more power losses and efficiency reduction. To allow for higher power density [1], devices with lower switching losses are required.

GaN-based devices have become more attractive for commercialization after emerging power switching GaN-on-silicon [2] and CMOS GaN-on-sapphire [3] technologies.

Nonnegligible carrier trapping is observed during GaN device operations affecting their power efficiency when in circuit operation, i.e., under the electrical stress, device characteristics become different from steady-state ones for a period of time due to long trap capture and emission rates [4]. This behavior is referred to as the current collapse (CC). The complete elimination of the CC is a long-term task requiring radical improvements.

It is important to analyze the influence of trap parasitic effects on efficiency of fast switching GaN HEMTs. Due to high switching frequencies of GaN HEMTs, a small parasitic effect can significantly influence efficiency and switching performance. The higher the operating frequency is, the less efficient the device may become [5]. Recently, a hybrid GaN converter with 97% efficiency was reported in [6] at $f = 250$ KHz.

In an experimental test of fast switching devices, the switching transients are strongly dependent on the measurement systems. Therefore, trap dynamics including recovery time and energy level cannot be accurately extracted from the measurement systems. The simulations enable any change to circuit parameters to study the effects on switching transients. To predict the power dissipation at circuit level, compact models are employed.

Various approaches have been reported for the compact modeling such as the surface potential physical-based [7], [8] and charge-based [9], [10] models. However, developing and run-time of these models can be time consuming and may lead to convergence issues. It is possible to extend existing fast (near-real-time) empirical models to capture nuances of GaN HEMTs. Empirical nature of these models including a number of fitting parameters increases model accuracy and speed.

Since trapping effects are not included in commercial circuit tools, it is important to develop a methodology to predict this behavior. A physical compact model to distinguish different types of traps and to model gate-lag and drain-lag effects has been demonstrated recently [11].

There are two approaches in modeling of current dispersion: 1) analytical and 2) subcircuit. In analytical approach, the dispersion effects are incorporated into the output current equation whereas in subcircuit approach the equivalent circuit is extended with resistors and capacitors (RCs) in series connections to model the dispersion effects.

We focus on modeling of switching transients in presence of bulk traps (BTs) and surface traps (STs) using *RC* subcircuits. To reach this goal, the method described in [12] and [13] is extended and the results are validated by the experimental dc sweep data, I–V pulsed measurements, and technology computer-aided design (TCAD) simulation results of authors' previous work [14].

Using the existing Angelov model, the original contributions of this work are: 1) to introduce an approach to evaluate the

Manuscript received February 7, 2017; revised April 18, 2017 and May 5, 2017; accepted May 5, 2017. Date of publication May 18, 2017; date of current version June 19, 2017. This work was supported in part by FLEXIS the European Regional Development Fund (ERDF) through the Welsh Government and in part by the EPSRC RC UK under grant RGS 122292/118084. The review of this paper was arranged by E. M. Darwish. *(Corresponding author: Soroush Faramehr.)*

The authors are with the Electronic Systems Design Center, College of Engineering, Swansea University Bay Campus, Swansea SA1 8EN, U. K. (e-mail: soroush.faramehr@swansea.ac.uk; p.igic@swansea.ac.uk).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TED.2017.2703103

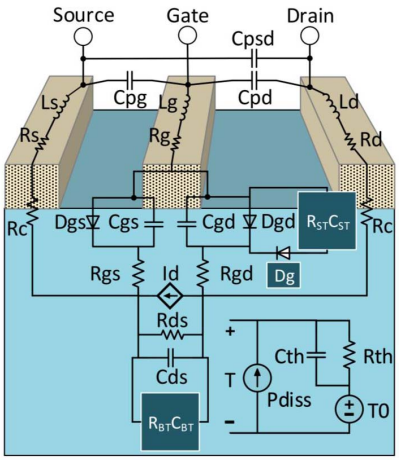

Fig. 1. Equivalent circuit of a GaN HEMT with extrinsic elements including R_s, R_g, R_d, L_s, L_g, L_d, C_{pg}, C_{pd}, and C_{psd}, intrinsic elements consisting of RC(s), RC(d), D_{gs}, D_{gd}, C_{gs}, C_{gd}, C_{ds}, R_{gs}, R_{gd}, and R_{ds}, and controlled current source Id. $R_{ST}C_{ST}$ and $R_{BT}C_{BT}$ are dispersion subcircuits both including a resistance and a capacitor in series connections. Diode D_g is a part of $R_{ST}C_{ST}$ subcircuit ensuring correct direction of current. Rth and Cth are a part of self-heating subcircuit. T_0 and T are ambinet and device operating temperatures, respectively.

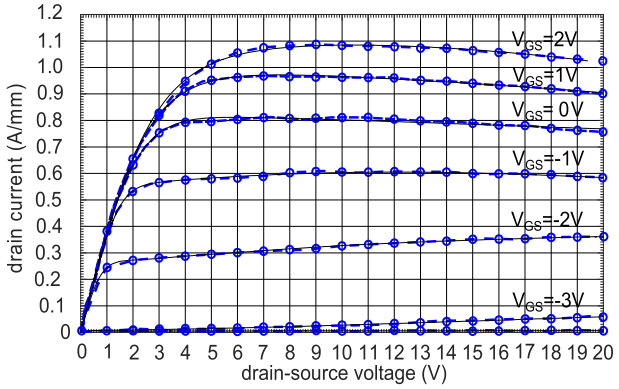

Fig. 2. Compact model (black lines) and measured (blue circles) output dc sweep of a quarter micrometer GaN HEMT at off ($V_{GS} = -4$ V) to on ($V_{GS} = 2$ V) in steps of $V_{STEP} = 1$ V using fitting parameters of Table I obtained from error minimizing function.

performance of GaN power HEMTs on the system level; 2) to develop a near-real-time empirical compact model for a power GaN HEMT including instabilities with no convergence issues; 3) to use simulink integrated with MATLAB as wide used platform for compact modeling; 4) to validate the GaN HEMT instabilities by pulse measurements; and 5) to investigate double-pulse switch transients with *RC* subcircuits.

II. Compact Model Development

The GaN HEMT equivalent circuit consists of connected linear and nonlinear electrical elements corresponding to real device elements (see Fig. 1). This well-known topology is after Kondoh [15].

The current source [12] in this model is the core of nonlinearity, self-heating, and transient behavior and is described by the following equations [12]:

$$I_d = I_{\text{pkt}}[1 + \tanh(\psi)] \times \tanh\left(\alpha_T V_{\text{ds}} + k_T V_{\text{ds}}^3\right)[1 + \lambda V_{\text{ds}}] \tag{1}$$

where

$$\psi = \sinh[P_{1t}(V_{\text{gs}} - V_{\text{pkt}}) + P_{2t}(V_{\text{gs}} - V_{\text{pkt}})^2 + P_{3t}(V_{\text{gs}} - V_{\text{pkt}})^3] \tag{2}$$

$$\alpha_T = \alpha_R + \alpha_S[1 + \tanh(\psi)] \tag{3}$$

$$x_{\text{pkt}} = x_{\text{pk0}} + (x_{\text{pk}} - x_{\text{pk0}}) \times \tanh(\alpha_R V_{\text{ds}}) \tag{4}$$

$$P_{\text{it}} = P_{i0} + (P_i - P_{i0}) \times \tanh(\alpha_R V_{\text{ds}}). \tag{5}$$

The equation parameters I_{pkt} and I_{pk0} define the height of transconductance, ψ is the power series centered at V_{gs} and V_{pkt}, λ controls the slope for transconductance, α_R determines the slope of linear region in transconductance, α_S defines the variation of slope, and P_i (P_{it}) determines the shape of transconductance defined in [13]. The tanh term in (1) is to ensure that current equation has infinite derivatives.

Drain-induced barrier lowering and short-channel effects can also be captured by this model.

The simulation results are obtained by employing data fitting function starting from a set of initial parameters. The parameters given in Table I are calculated through iterations by minimizing the error of the modeled currents to the experimental data until the convergence criteria are met in MATLAB.

The GaN HEMT equivalent circuits ideally possess intrinsic variable capacitors in a range of femto-(10^{-15}) [16] to pico-(10^{-12}) farads [17] making them potentially operate at very high frequencies with negligible parasitic effect and power loss.

A dynamic behavior of the device is partially defined by intrinsic parameters seen in Fig. 1. The effect of the intrinsic capacitors on dynamic behavior has been measured in [16] showing a negligible change in the gate-to-drain (C_{gd}) and gate-to-source (C_{gs}) capacitances with respect to frequency operation in a range of a few femto Farads.

A comparison between the compact model and experimental dc sweep data is presented in Fig. 2 using the parameter values given in Table I incorporated into Fig. 1. The values of variable resistor [12] and variable capacitors of GaN HEMT equivalent circuit and *RC* subcircuits changing with respect to voltage were extracted from [16].

Fig. 3 is the logarithmic transfer characteristic of the quarter micrometer GaN device showing the accuracy of the compact model at the OFF and ON states for $V_{DS} = 1$ V and $V_{DS} = 5$ V using the fitting parameters of Table I incorporated into the equivalent circuit of GaN HEMT.

III. Compact Model Validation

The compact model validation was done against TCAD results obtained from Silvaco commercial simulation software. A TCAD model for a GaN capped AlGaN/GaN HEMT with a quarter micrometer gate length was developed. The device simulations were carried out in geometrical structure editor of Silvaco called Deckbuild.

The input file was optimized using mesh refining and model selections for the optimum computational accuracy

TABLE I
COMPACT MODEL PARAMETER VALUES CALCULATED BY ERROR MINIMIZING FUNCTION TO EXPERIMENTAL OUTPUT DC SWEEP OF THE QUARTER MICROMETER GaN DEVICE

Parameter values	T=25 °C
λ	0.0447
k_T	-0.0006
α_S	0.1723
α_R	0.0300
P_3	0.1045
P_{30}	0.0829
P_2	0.1872
P_{20}	0.1445
P_1	0.3511
P_{10}	0.2665
I_{pk}	0.0071
I_{pk0}	0.0520
V_{pk}	-1.9404
V_{pk0}	-1.4393

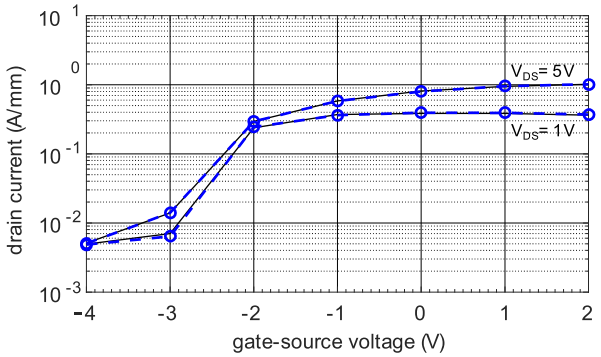

Fig. 3. Compact model (black lines) and measured (blue circles and dashes) transfer dc sweep data of quarter micrometer GaN HEMT at $V_{DS} = 1$ V and $V_{DS} = 5$ V using fitting parameters of Table I obtained from error minimizing function.

and speed. The modeled GaN HEMT consists of a 300-μm 4H-SiC substrate followed by a 1.9-μm GaN buffer, 18-nm $Al_{0.28}Ga_{0.72}N$ barrier, and a 3-nm GaN cap [14]. The GaN HEMT is a two-finger device with a total gate width of 100 μm.

Ideally, the output current is a function of voltage. However, experimental results suggest that the drain current of GaN HEMTs is also a function of time. This is due to the existence of trap locations in the III-V structures. Therefore, including parasitic traps becomes a necessity in advance modeling of GaN HEMTs [18].

In TCAD, donor traps with an energy of 0.1 eV with respect to the valence band and a capture cross section of 10^{-19} cm^2 were considered for AlGaN barrier surface. Acceptor traps with energy of 1.8 eV with respect to the conduction band and a capture cross section of 10^{-15} cm^2 were considered for GaN bulk buffer layer [14]. The donor traps were uniformly distributed at the surface with the density of 5.75×10^{21} cm^{-3}. The acceptor traps were uniformly distributed in GaN buffer layer with the density of 2.5×10^{16} cm^{-3}. The dynamic of traps was modeled using Shockley–Read–Hall recombination model which is added to the continuity equation [14]. The calibration parameters for this device such as polarization strength, trap density, and mobility and their values have been reported in [14].

The transient functions in GaN HEMTs are affected by the trap capture and emission rates. To include trapping parasitic in compact modeling, *RC* subcircuits are introduced. The emission and capture rates are given by

$$t_{ST} = R_{ST} \times C_{ST} \quad (6)$$

$$t_{BT} = R_{BT} \times C_{BT} \quad (7)$$

where t_{ST} is the emission and capture rate from the STs through R_{ST} and C_{ST} for the gate-lag, slow transient response of the drain current when gate–source voltage is pulsed, and t_{BT} is the capture and emission rate from the BTs through R_{BT} and C_{BT} for the drain-lag, the slow transient response of the drain output current when drain–source voltage is pulsed.

The subcircuits shown in Fig. 1 consisting of RCs connected in series are added to the equivalent GaN HEMT circuit to model the gate-lag and drain-lag.

The gate-lag is assigned to generation of virtual gate at the device surface and drain side of the gate, inducing a delay in switching transients and creating knee-walkout effect [19]. The subcircuit ($R_{ST}C_{ST}$) followed by the diode (Dg) is placed in parallel with the gate-to-drain (C_{gd}) capacitor to model this behavior (see Fig. 1).

To model gate-lag, the drain voltage is kept constant at $V_{DS} = 12$ V and the gate voltage is ramped up from OFF ($V_{GS} = -4$ V) to ON ($V_{GS} = 0$ V). Before the system is disturbed by electrical stress at the gate, the capacitor (C_{ST}) of the subcircuit in Fig. 1 is at steady state and charged through gate resistor (R_G). When the input voltage changes from OFF to ON, the capacitor C_{ST} is discharged through R_{gd}, and the resistor R_{ST} adding capacitor current component to the current source [12], [13] of the device. The subcircuit emission rate mimicking the long process [4] of traps releasing charges is controlled by R_{ST} and C_{ST} values. The Dg diode in Fig. 1 is placed to ensure that subcircuit is not charged through R_{gd} but R_G.

Fig. 4 represents predicted gate-lag transient response of the quarter micrometer GaN HEMT using compact model with and without the *RC* subcircuits compared with TCAD results. Three scenarios are presented here: 1) a compact model with no subcircuit showing no pronounced CC (black dashes); 2) a compact model with the subcircuit and a variable capacitor of $C_{ST} = 2.5 \times 10^{-8}$ F (black line) at $V_{GS} = -4$ V and $V_{DS} = 12$ V showing the closest transient response to TCAD results (blue circles); and 3) a compact model with the subcircuit and a variable capacitor of $C_{ST} = 9 \times 10^{-9}$ F (green line) at $V_{GS} = -4$ V and $V_{DS} = 12$ V. The maximum resistance of the subcircuit (R_{ST}) was set at 35 Ω. Increasing the emission rate (t_{ST}) worsens the CC phenomenon by extending the steady-state time of the device.

The drain-lag is assigned to the BTs inducing a delay in switching transients of the GaN devices. A subcircuit ($R_{BT}C_{BT}$) is placed in parallel with the drain-to-source

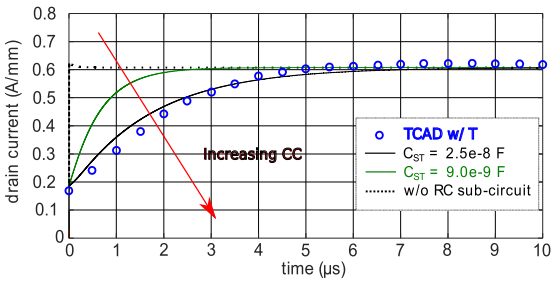

Fig. 4. Comparison of predicted gate-lag transient response of the quarter micrometer GaN HEMT using variable R_{ST} and C_{ST} values incorporated in compact model with TCAD results. The resistor of subcircuit has the maximum value of $R_{ST} = 35\ \Omega$, and the variable capacitors have the values of $C_{ST} = 2.5\times10^{-8}$ F and $C_{ST} = 9\times10^{-9}$ F at $V_{GS} = -4$ V and $V_{DS} = 12$ V. The pulse ramp-up time is 1 ns for compact and TCAD models. The dashes are predicted gate-lag without additional RC subcircuit.

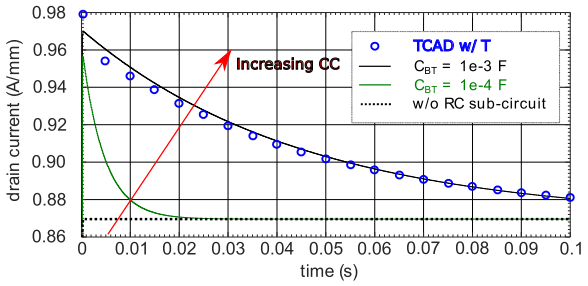

Fig. 5. Comparison of predicted drain-lag transient response of the quarter micrometer GaN HEMT using compact model with TCAD results. The resistor of subcircuit is calculated via (8), and the variable capacitors have the values of $C_{BT} = 10^{-3}$ F and $C_{BT} = 10^{-4}$ F at $V_{GS} = V_{DS} = 0$ V. The pulse ramp-up time is 1 μs for compact and TCAD models. The dashes are predicted drain-lag without additional RC subcircuit.

capacitor (C_{ds}) to model this behavior. Similar methodologies to model the drain-lag using RC subcircuits were presented in the previous works [12], [18].

To model drain-lag, the gate voltage is kept constant at $V_{GS} = 0$ V and the drain voltage is ramped up from $V_{DS} = 0$ V to $V_{DS} = 12$ V. The capacitor (C_{BT}) of the subcircuit in Fig. 1 is charged through resistor (R_{BT}). The output current of the GaN device follows the current behavior of the capacitor C_{BT}.

Fig. 5 represents a comparison of predicted drain-lag transient response of the quarter micrometer GaN HEMT using compact model with and without the RC subcircuits. Three scenarios are presented in Fig. 5: 1) a compact model without RC subcircuit showing no pronounced current dispersion effect (black dashes); 2) a compact model with the RC subcircuit and a variable capacitor with a value of $C_{BT} = 10^{-3}$ F (black line) at $V_{GS} = V_{DS} = 0$ V showing the closest transient response to TCAD results (blue circles); and 3) a compact model with the subcircuit and a variable capacitor with a value of $C_{BT} = 10^{-4}$ F (green line) at $V_{GS} = V_{DS} = 0$ V. The variable resistance of the $R_{BT}C_{BT}$ subcircuit was set at $R = 50\ \Omega$ at $V_{GS} = 0$ V and $V_{DS} = 12$ V using the following equation [12]:

$$R_{BT} = R_0 + [R_1/1 + \tanh(\varphi)] \quad (8)$$

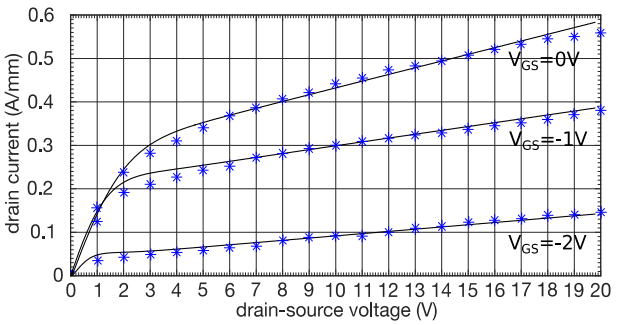

Fig. 6. Compact model (black lines) and pulsed I–V measurements (blue stars) at quiescent bias points of $V_{GS} = -3.39$ V and $V_{DS} = 60$ V for a quarter micrometer GaN HEMT. The pulselength is 1 μs and pulse separation is 1 ms. The RC subcircuits consist of variable capacitors with the values of $C_{ST} = 25$ pF and $C_{BT} = 125$ pF at $V_{GS} = V_{DS} = 0$ V and the variable resistors with the maximum of $R_{ST} = 35\ \Omega$ and minimum of $R_{BT} = 50\ \Omega$.

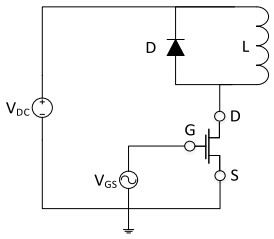

Fig. 7. Power circuit used for double-pulse switching test with an inductive load of $L = 0.4$ mH.

where R_0 and R_1 are the user definable values for R_{BT}. The parameter φ is the power series function calculated through (2).

The gate-lag and drain-lag transients predicted by the compact model are in a good quantitative agreement with authors' previous TCAD results [14]. Similar behaviors for gate-lag and drain-lag were reported in the past in the literature from other authors [20], [21].

Since one cannot distinguish between polarization and interface trapped charge, some uncertainty may remain for physical parameter extractions using TCAD results. In addition, the values used in TCAD simulations were extracted from the literature to only emphasize the large scales of current dispersion and may vary for different devices. The TCAD transient results are highly dependent on the carrier transport model employed.

IV. Compact Model Investigation of Current Collapse

Pulse measurement is a conventional technique to test the reliability of transistors. When the voltage within the pulse is lower (higher) than positive quiescent bias point, the traps release (capture) charges. On the other hand, when the voltage within the pulse is lower (higher) than negative quiescent bias point, the traps capture (release) charges.

Fig. 6 is the pulsed experimental data at quiescent points of $V_{GS} = -3.39$ V and $V_{DS} = 60$ V compared to the compact model using the parameters of Table I incorporated into Fig. 1. The pulselength is 1 μs and pulse separation is 1 ms to

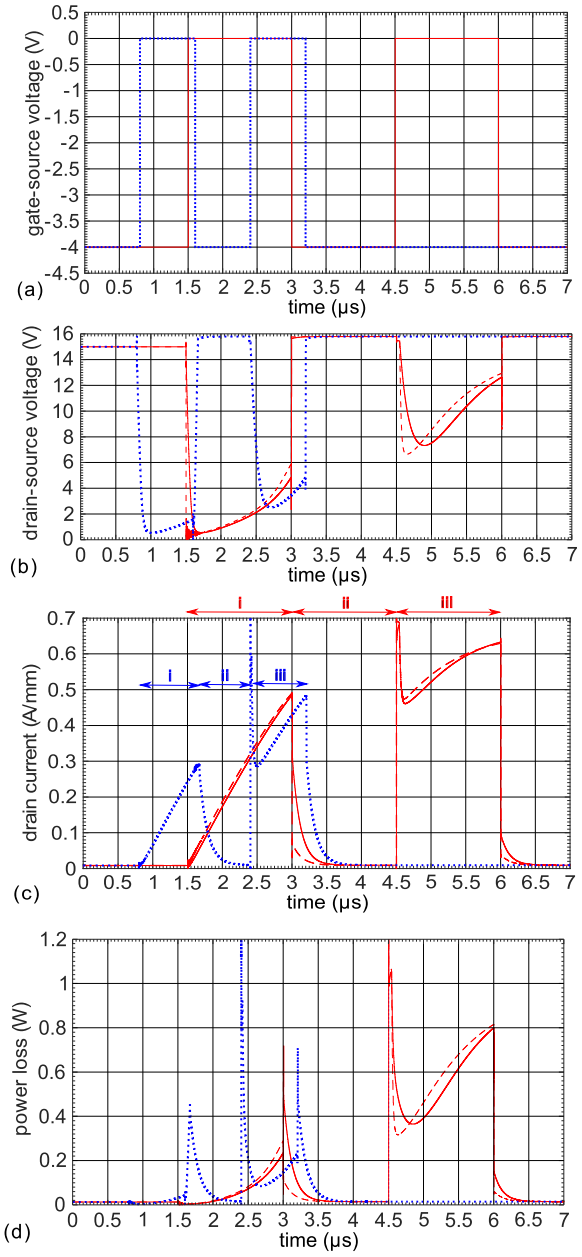

Fig. 8. Predicted transients of (a) gate input voltage switching between off (−4 V) and on (0 V) at $f_1 = 0.3$ MHz (red line) and $f_2 = 0.6$ MHz (blue dot), (b) drain voltage with RC subcircuits (red line and blue dots) and without RC subcircuits (red dashes), (c) output current, and (d) power loss switching at f_1 and f_2. The RC subcircuits consist of variable capacitors with the values of $C_{ST} = 25$ pF and $C_{BT} = 125$ pF at $V_{GS} = V_{DS} = 0$ V and the variable resistors with the maximum of $R_{ST} = 35\ \Omega$ and minimum of $R_{BT} = 50\ \Omega$.

avoid thermal effects on the output current. The pulselength during experiments (1 μs) is fast enough to enhance the visualization of CC since this process is typically large in order of seconds [22].

Comparing Figs. 2–6, one can observe the knee-walkout phenomenon. The STs are believed to affect the current at the knee region [19] resulting from the trapped charge at the vicinity of the gate and reducing the number of electrons, while BTs play a major role in shaping the device characteristics in large time scales [14].

V. Double-Pulse Switching Test

The standard double-pulse switching test was employed to measure the switching features and to predict the power dissipation using the test circuit presented in Fig. 7. The load inductor value of $L = 0.4$ mH was chosen to obtain the desired current value during double-pulse testing at the low applied frequencies of $f_1 = 0.3$ MHz and $f_2 = 0.6$ MHz in this paper. At higher frequencies, the inductor values can be reduced to $L = 0.4$ nH giving a maximum efficiency of 90% for GaN power transistor outperforming silicon MOSFET with maximum efficiency of 86% for the inductor value of $L = 2.9$ nH [23]. However, to drive the frequency higher in hard-switching converters, power devices needs to have low-dynamic losses. The diode of the double-pulse tester has a junction capacitor of 0.1 pF and reverse recovery time of 60 ns, respectively.

Since GaN HEMTs degrade under the high-frequency operations [5], the gate signal switches at $f_1 = 0.3$ MHz (red line) and $f_2 = 0.6$ MHz (blue dots) between the OFF and the ON states are shown in Fig. 8(a).

Fig. 8(b) shows the output voltage for f_1 and f_2 with the RC subcircuits (line and dots) and without subcircuits (dashes). Fig. 8(c) represents the predicted drain current using the double-pulse tester. The spike of the drain current is due to the reverse recovery of the diode. One can distinguish three regions in Fig. 8(c).

In region (i), device is at the ON-state and the inductor is linearly charged and diode is OFF. In region (ii), the HEMT is switched OFF, the diode is forced to switch ON and the stored energy of the inductor dissipates through the freewheeling diode. In region (iii), the HEMT is switched back to ON, the diode is forced to shut down and the inductor is linearly charged.

Comparing the maximum currents at the end of region (iii)'s for f_1 and f_2, one can predict a 16% output current reduction at $f_2 = 0.6$ MHz. Finally, Fig. 8(d) shows the typical instant power dissipation across the GaN switch predicted by the compact model.

VI. Conclusion

A methodology to model transient switching of power GaN HEMTs has been developed using an existing fast (near-real-time) empirical compact model to explore the trapping effects on device behavior. The compact models were validated by TCAD results [14] and calibrated to experimental data obtained from the output dc sweeps and pulsed I–V measurements.

The capture and emission of carriers under gate-lag and drain-lag were modeled using RC subcircuits. To account for the gate-lag, the subcircuit $R_{ST}C_{ST}$ was added in parallel with the gate-to-drain capacitor (C_{gd}) and the predicted transient response was validated using the TCAD results. To model the drain-lag, the subcircuit $R_{BT}C_{BT}$ was added in parallel with the drain-to-source capacitor (C_{ds}) and the predicted transient response was validated using the transient results obtained from TCAD.

The power GaN has been tested by a standard double-pulse switching tester using the compact model for the two frequencies of $f_1 = 0.3$ MHz and $f_2 = 0.6$ MHz. The reduction of the output current by 16% was predicted for device operation at the higher frequency.

The methodology presented in this paper is a platform for integration of single or multiple GaN HEMTs including their instabilities into the system level using widely-used MATLAB program.

ACKNOWLEDGMENT

This work is a part of FLEXIS project. The authors would like to thank M. J. Uren from the University of Bristol for providing them with the experimental data.

REFERENCES

[1] S. Faramehr, K. Kalna, and P. Igić, "Design and simulation of a novel 1400 V–4000 V enhancement mode buried gate GaN HEMT for power applications," *Semicond. Sci. Technol.*, vol. 29, no. 11, pp. 115020–115026, Nov. 2014.

[2] M. Ishida, T. Ueda, T. Tanaka, and D. Ueda, "GaN on Si technologies for power switching devices," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3053–3059, Oct. 2013, doi: 10.1109/TED.2013.2268577.

[3] R. Chu, Y. Cao, M. Chen, R. Li, and D. Zehnder, "An experimental demonstration of GaN CMOS technology," *IEEE Electron Device Lett.*, vol. 37, no. 3, pp. 269–271, Mar. 2016.

[4] J. Joh and J. A. del Alamo, "A current-transient methodology for trap analysis for GaN high electron mobility transistors," *IEEE Trans. Electron Devices*, vol. 58, no. 1, pp. 132–140, Jan. 2011.

[5] Y. Wu, M. Jacob-Mitos, M. L. Moore, and S. Heikman, "A 97.8% efficient GaN HEMT boost converter with 300-W output power at 1 MHz," *IEEE Electron Device Lett.*, vol. 29, no. 8, pp. 824–826, Aug. 2008.

[6] Y. Lei, Z. Ye, and R. C. N. Pilawa-Podgurski, "A GaN-based 97% efficient hybrid switched-capacitor converter with lossless regulation capability," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Oct. 2015, pp. 4264–4270.

[7] S. Ghosh, A. Dasgupta, S. Khandelwal, S. Agnihotri, and Y. S. Chauhan, "Surface-potential-based compact modeling of gate current in AlGaN/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 62, no. 2, pp. 443–448, Feb. 2015.

[8] W. Deng, J. Huang, X. Ma, and J. J. Liou, "An explicit surface potential calculation and compact current model for AlGaN/GaN HEMTs," *IEEE Electron Device Lett.*, vol. 36, no. 2, pp. 108–110, Feb. 2015.

[9] U. Radhakrishna, D. Piedra, Y. Zhang, T. Palacios, and D. Antoniadis, "High voltage GaN HEMT compact model: Experimental verification, field plate optimization and charge trapping," in *IEDM Tech. Dig.*, Dec. 2013, pp. 32.7.1–32.7.4.

[10] N. Karumuri, G. Dutta, N. DasGupta, and A. DasGupta, "A compact model of drain current for GaN HEMTs based on 2-DEG charge linearization," *IEEE Trans. Electron Devices*, vol. 63, no. 11, pp. 4226–4232, Nov. 2016.

[11] B. Syamal, X. Zhou, S. B. Chiah, A. M. Jesudas, S. Arulkumaran, and G. I. Ng, "A comprehensive compact model for GaN HEMTs, including quasi-steady-state and transient trap-charge effects," *IEEE Trans. Electron Devices*, vol. 63, no. 4, pp. 1478–1485, Apr. 2016.

[12] I. Angelov, L. Bengtsson, and M. Garcia, "Extensions of the Chalmers nonlinear HEMT and MESFET model," *IEEE Trans. Microw. Theory Techn.*, vol. 44, no. 10, pp. 1664–1674, Oct. 1996.

[13] S. Stoffels *et al.*, "High temperature calibration of a compact model for GaN-on-Si power switches," in *Proc. 17th Int. Workshop Thermal Invest. ICs Syst. (THERMINIC)*, Sep. 2011, pp. 1–5.

[14] S. Faramehr, K. Kalna, and P. Igić, "Drift-diffusion and hydrodynamic modeling of current collapse in GaN HEMTs for RF power application," *Semicond. Sci. Technol.*, vol. 29, no. 2, pp. 25007–25017, Feb. 2014.

[15] H. Kondoh, "An accurate FET modelling from measured S-parameters," in *IEEE MTT-S Int. Microw. Symp. Dig.*, vol. 86. Jun. 1986, pp. 377–380.

[16] A. Jarndal and G. Kompa, "A new small-signal modeling approach applied to GaN devices," *IEEE Trans. Microw. Theory Techn.*, vol. 53, no. 11, pp. 3440–3448, Nov. 2005.

[17] P. M. Cabral, J. C. Pedro, and N. B. Carvalho, "Nonlinear device model of microwave power GaN HEMTs for high power-amplifier design," *IEEE Trans. Microw. Theory Techn.*, vol. 52, no. 11, pp. 2585–2592, Nov. 2004.

[18] O. Jardel *et al.*, "An electrothermal model for AlGaN/GaN power HEMTs including trapping effects to improve large-signal simulation results on high VSWR," *IEEE Trans. Microw. Theory Techn.*, vol. 55, no. 12, pp. 2660–2669, Dec. 2007.

[19] C. Roff *et al.*, "Analysis of DC–RF dispersion in AlGaN/GaN HFETs using RF waveform engineering," *IEEE Trans. Electron Devices*, vol. 56, no. 1, pp. 13–19, Jan. 2009.

[20] J. M. Tirado, J. L. Sanchez-Rojas, and J. I. Izpura, "Simulation of surface state effects in the transient response of AlGaN/GaN HEMT and GaN MESFET devices," *Semicond. Sci. Technol.*, vol. 21, no. 8, pp. 1150–1159, Aug. 2006.

[21] W. D. Hu, X. S. Chen, F. Yin, J. B. Zhang, and W. Lu, "Two-dimensional transient simulations of drain lag and current collapse in GaN-based high-electron-mobility transistors," *J. Appl. Phys.*, vol. 105, no. 8, p. 84502, Apr. 2009.

[22] O. Jardel, F. De Groote, C. Charbonniaud, T. Reveyrand, J. P. Teyssier, R. Quere, and D. Floriot, "A drain-lag model for AlGaN/GaN power HEMTs," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2007, pp. 601–604, doi: 10.1109/MWSYM.2007.379972.

[23] A. Lidow, J. Strydom, M. de Rooij, and D. Reusch, *GaN Transistors for Efficient Power Conversion*. California, CA, USA: Wiley, 2015.

Soroush Faramehr received the M.Sc. and Ph.D. degrees in electrical engineering from Swansea University, Swansea, U.K., in 2010 and 2015, respectively.

He is currently a Post-Doctoral Researcher with the Electronic Systems Design Center, Swansea University. His current research interests include power GaN compact models and novel III-Vs lateral and vertical power FETs.

Petar Igić (SM'15) received the Dipl.-Eng. and Mag.Sc. degrees from the University of Nis, Nis, Serbia, in 1993 and 1997, respectively, and the Ph.D. degree from Swansea University, Swansea, U.K., in 2000.

He is currently a Reader with the College of Engineering, Swansea University, where he is the Director of the Electronic Systems Design Center.